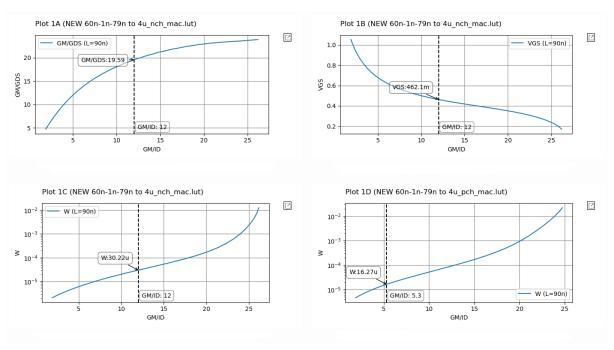
Design a single ended amplifier shown in the fig to achieve the following specs

Spec.		T VDD
DC Gain	6 dB	
BW	≥ 10 GHz	V _{out}
Power Consumption	≤ 1.5 mW	V _{in} ⊶
Cap Load	50 fF	Ţ

$$\begin{split} P_{cons} &= V_{DD} \; I_D \leq 1.5 \; \text{mW} \rightarrow I_D \leq 1.25 \; \text{mA} \\ GBW &= \frac{g_{m1}}{2\pi C_{out}} \geq 2 * 10 \; \text{GHz} \rightarrow g_{m1} \geq 6.28 \; \text{mS} \\ g_{m1} &= 15 \; \text{mS} \rightarrow \left(\frac{g_m}{I_D}\right)_1 = 12 \\ A_v &= g_{m1} R_{out} = 2 \rightarrow R_{out} = 134 \; \Omega \\ \frac{1}{g_{m2}} &= 150 \; \Omega \rightarrow g_{m2} = 6.7 \; \text{mS} \rightarrow \left(\frac{g_m}{I_D}\right)_2 = 5.3 \\ R_{out} &= \frac{R_{D1}. \, r_{o1}}{R_{D1} + r_{o1}} = 134 \rightarrow r_{o1} \geq 1257 \; \Omega \rightarrow \left(\frac{g_m}{g_{ds}}\right)_1 \geq 19 \end{split}$$

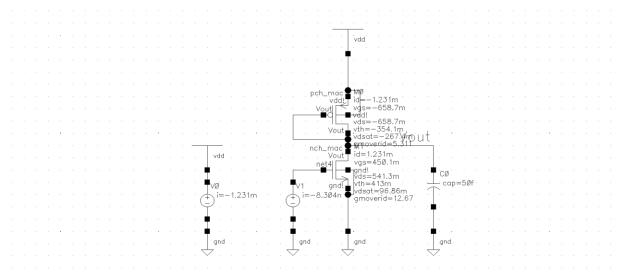




$$L = 90 \text{ nm}, V_{GS1} = 462.1 \text{ mV}, W_1 = 30.22 \text{ um}, W_2 = 16.27 \text{ um}$$

Apply Results to Cadence

DC - OP



AC Analysis

