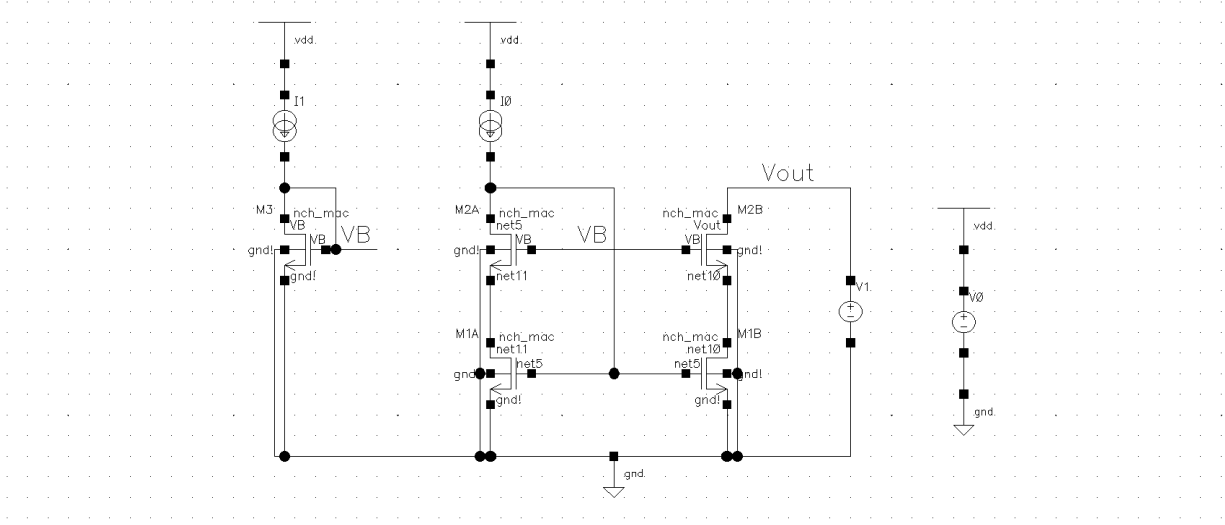


*Design a low-voltage cascode current mirror with a 1:2.5 input current to output current ratio. The low frequency output impedance should be greater than 200 k $\Omega$ . Assume a 25  $\mu$ A input current and V<sub>out</sub> is 400 mV.*



1. Design (Using gmoverid charts)

As large Rout is required  $\rightarrow$  Assume  $L_1 = 180$  nm and bias it in SI  $\left(\frac{g_m}{I_D} = 10\right)$

$$W_1 = 2.142 \mu\text{m} \rightarrow r_{o1} = 19.08 \text{ k}\Omega$$

$$R_{out} = g_{m2}r_{o2}r_{o1} = 200 \text{ k}\Omega$$

$$g_{m2}r_{o2} = \frac{200 \text{ k}\Omega}{19.08 \text{ k}\Omega} = 10.5$$

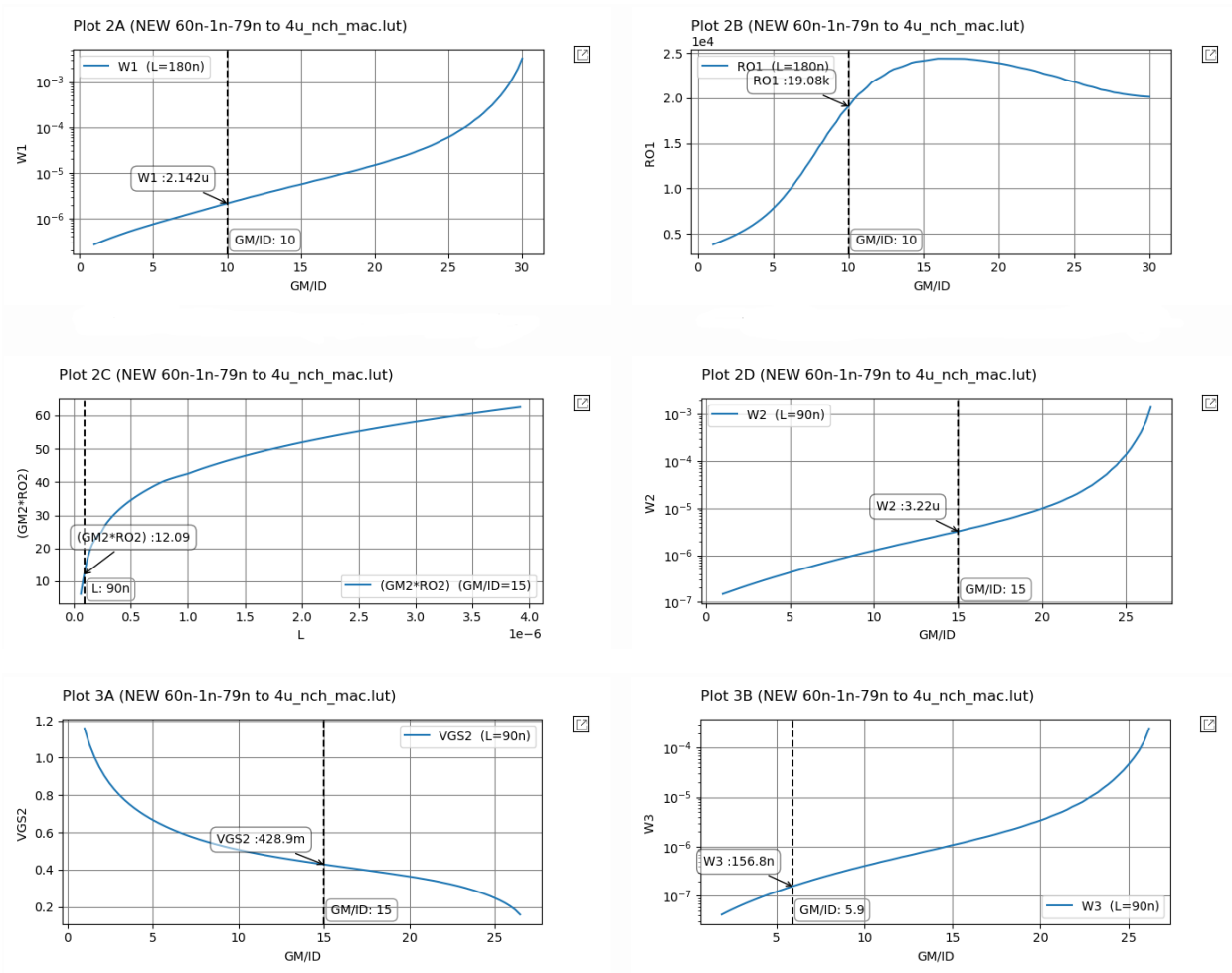
For cascode transistor bias it in MI  $\left(\frac{g_m}{I_D} = 15\right)$

$$L_2 \geq 90 \text{ nm} \rightarrow W_2 = 3.22 \mu\text{m}$$

For the VB device M3 :  $V_{GS3} \geq V_{GS2} + V_1^*$

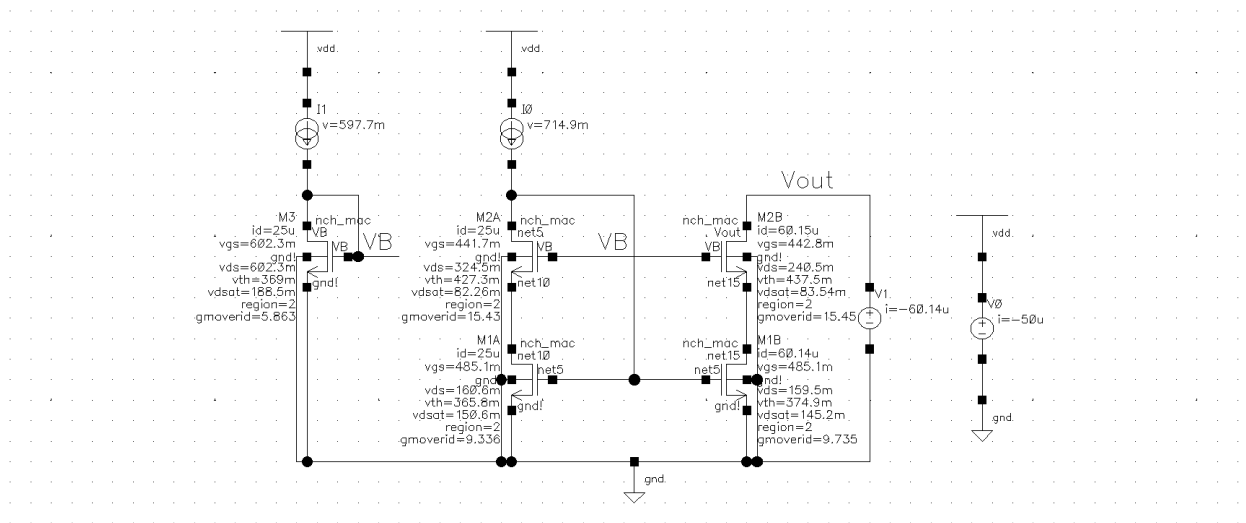
$$V_{GS3} \geq 628.9 \text{ mV} \rightarrow \left(\frac{g_m}{I_D}\right)_3 = 5.9$$

$$L_3 = L_2 \rightarrow W_3 = 156 \text{ nm}$$



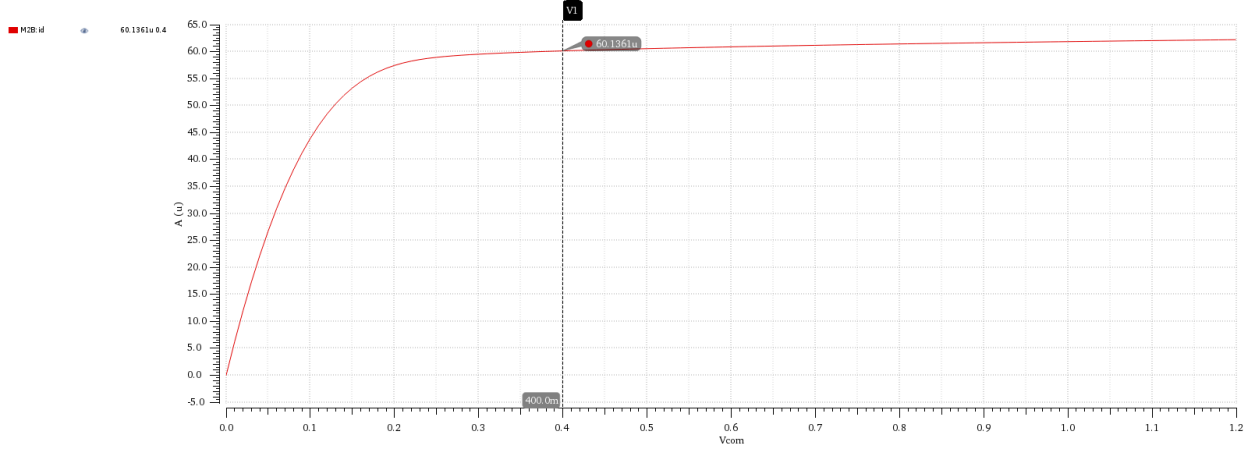
## 2. Simulations

### - DC OP



DC Analysis 'dc': Vcom = (0 -> 1.2)

1



## - AC Output Impedance

VR('Vout')/IR('V1/PLUS')

1

