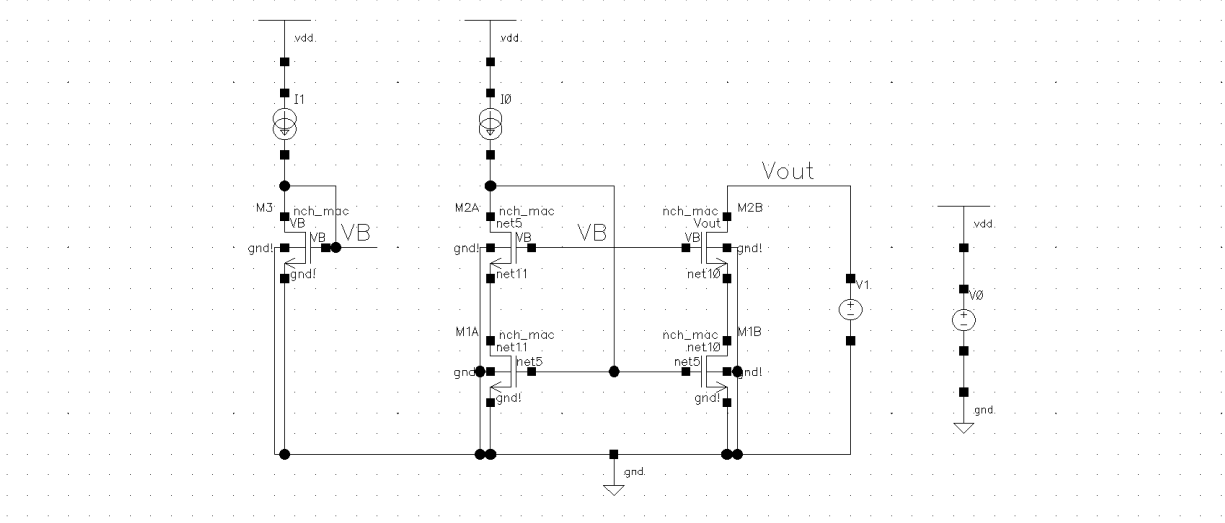


*Design a low-voltage cascode current mirror with a 1:2 input current to output current ratio. The low frequency output impedance should be greater than 2 MΩ. Assume a 50 μA input current and V<sub>out</sub> is 0.5 VDD.*



1. Design (Using gmoverid charts)

As large  $R_{out}$  is required  $\rightarrow$  Assume  $L_1 = 1\mu m$  and bias it in SI  $\left(\frac{g_m}{I_D} = 10\right)$

$$W_1 = 16.6 \mu m \rightarrow r_{o1} = 40.99 k\Omega$$

$$R_{out} = g_{m2}r_{o2}r_{o1} = 2 M\Omega$$

$$g_{m2}r_{o2} = \frac{2 M\Omega}{40.99 k\Omega} = 48.8$$

For cascode transistor bias it in MI  $\left(\frac{g_m}{I_D} = 15\right)$

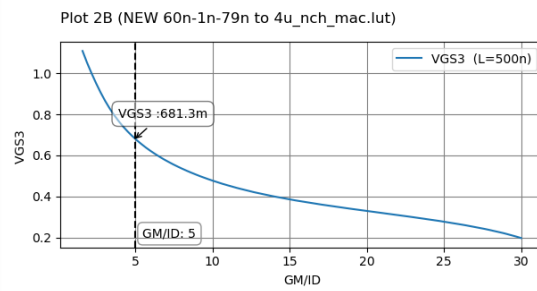
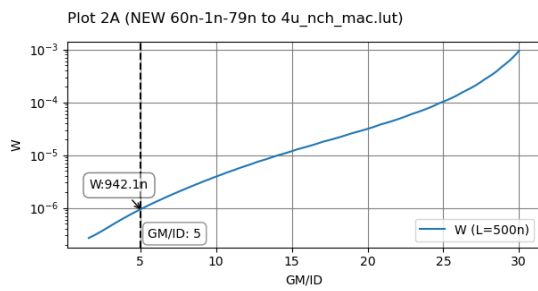
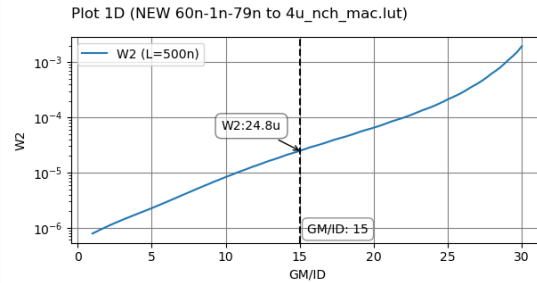
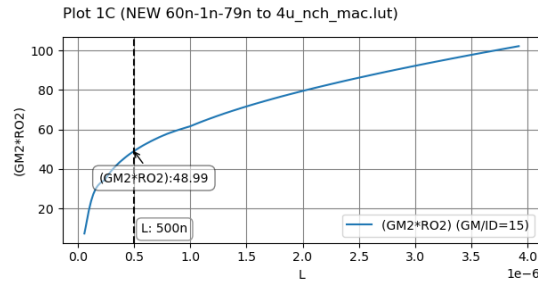
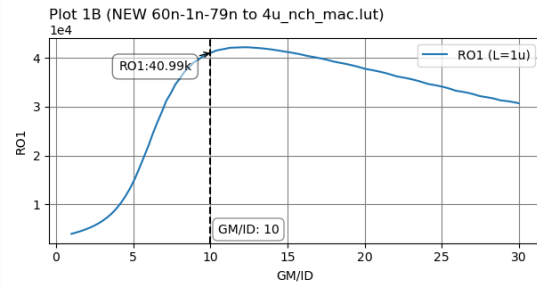
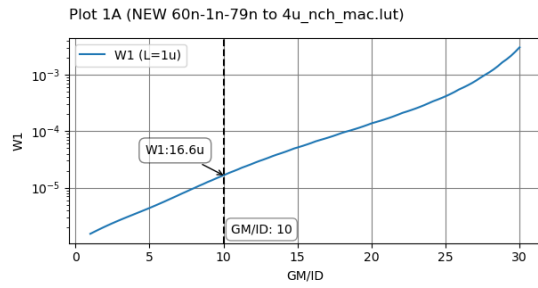
$$L_2 \geq 500 nm \rightarrow W_2 = 24.8 \mu m$$

For the VB device M3 :  $V_{GS3} \geq V_{GS2} + V_1^*$

assume  $V_{th1} = V_{th2}$

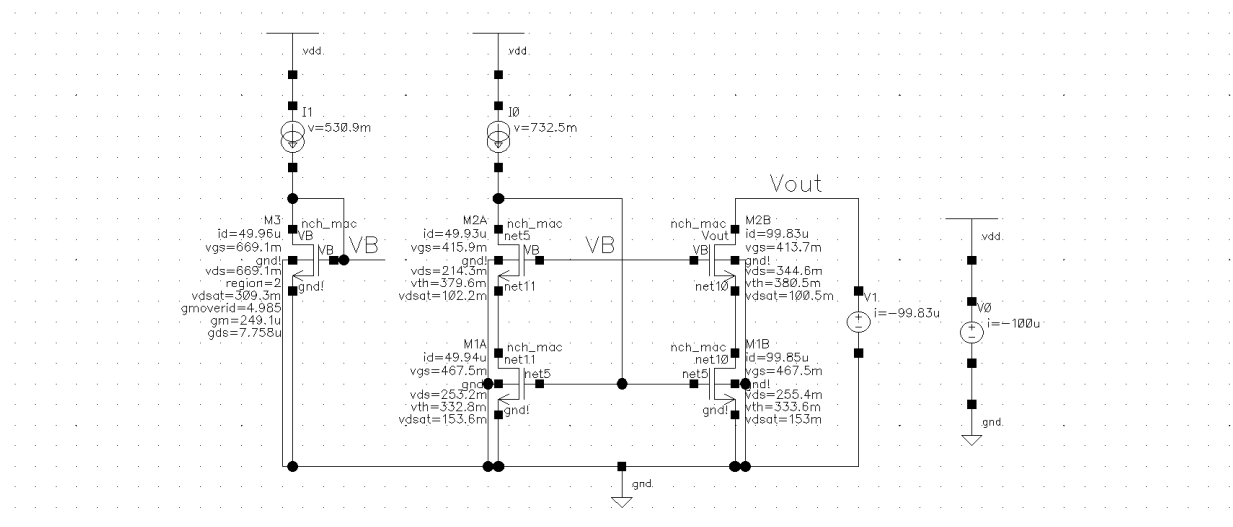
$$V_3^* \geq V_1^* + V_2^* \rightarrow V_3^* \geq 0.334 \rightarrow V_3^* = 0.4 \rightarrow \left(\frac{g_m}{I_D}\right)_3 = 5$$

$$L_3 = L_2 \rightarrow W_3 = 0.95 \mu m$$



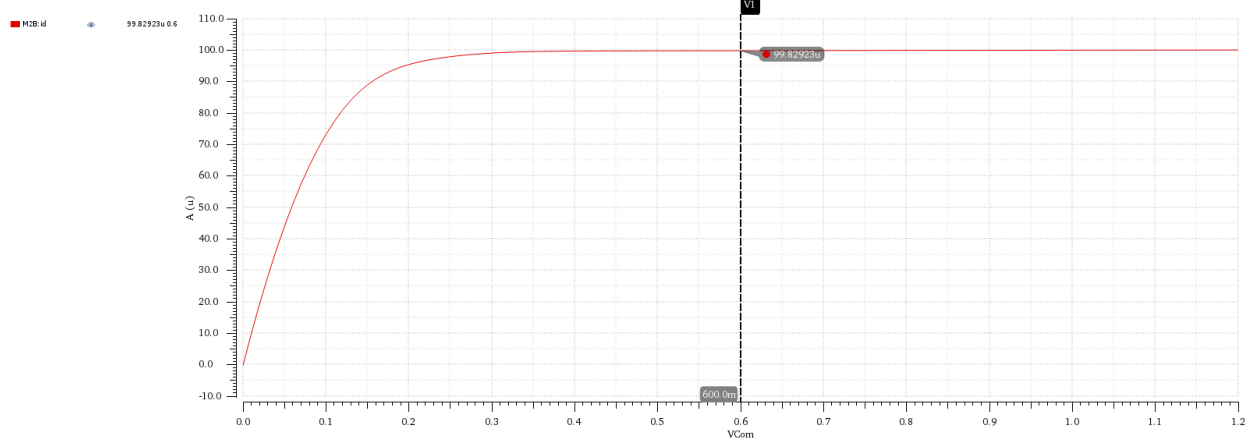
## 2. Simulations

### - DC OP



DC Analysis 'dc': VCom = (0 -> 1.2)

1



## - AC Output Impedance

VR('Vout')/IR('V1/PLUS')

1

