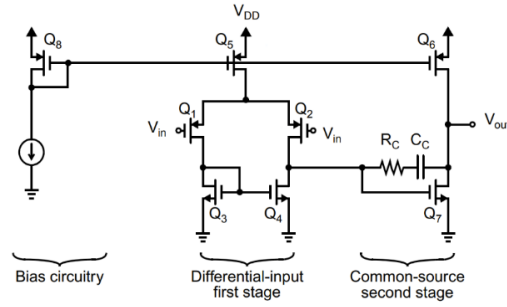


Design a Single Ended Two Stage Miller Compensated OTA meets the Specs (Use IREF = 10u)

Spec.	
DC Gain	≥ 63 dB
Unity Gain Frequency	≥ 10 MHz
Power Consumption	≤ 0.8 mW
Cap Load	2 pF

- Assume $C_C = 0.5 C_L = 1$ pF
- Assume CMIR from 0.2 \rightarrow 0.6 V \rightarrow use PMOS input transistors
- Assign higher gain for the first stage $A_V = A_{V1} \cdot A_{V2} = 45 * 32$



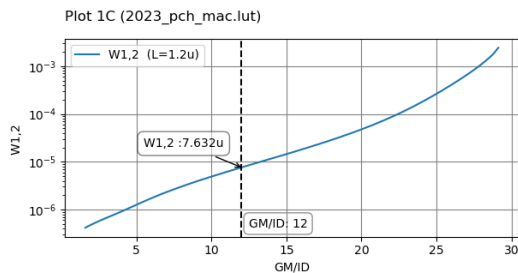
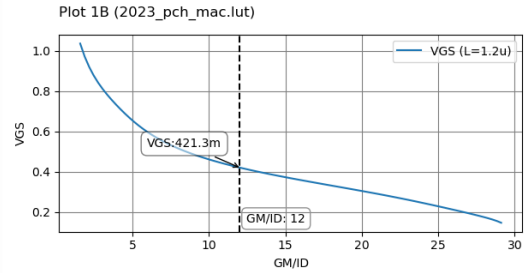
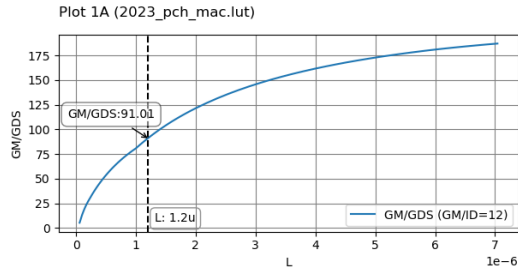
$$I_{\text{Consmax}} = \frac{P_{\text{cons}}}{V_{DD}} \rightarrow I_{D\text{max}} \leq 666 \text{ uA}$$

$$\text{UGF} = \frac{g_{m1,2}}{2\pi C_C} \geq 10 \text{ MHz} \rightarrow g_{m1,2} \geq 63 \text{ uS} \rightarrow g_{m1,2} = 90 \text{ uS}$$

$$\text{Assume } M_{1,2} \text{ in MI } \left(\frac{g_{m1,2}}{I_D} = 12 \right) \rightarrow I_{D1,2} = 7.5 \text{ uA} \rightarrow I_{B1} = 15 \text{ uA}$$

$$A_{V1} = \frac{g_{m1,2} r_{o2,4}}{2} (\text{Assume } r_{o2} = r_{o4}) \geq 45 \rightarrow r_{o2,4} = 1 \text{ M}\Omega \rightarrow (g_m r_o)_{1,2} = 90$$

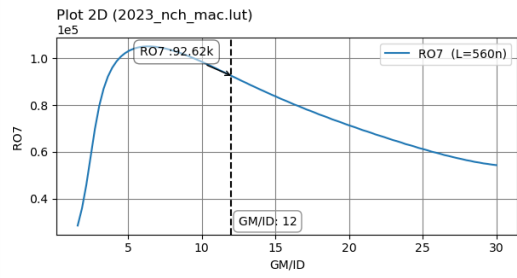
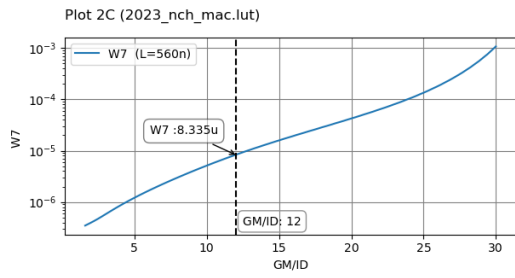
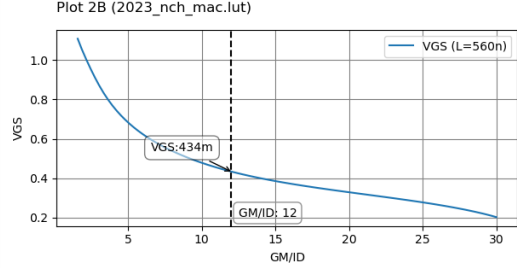
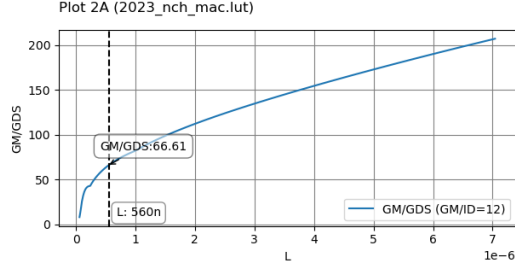
$$L_{1,2} = 1.2 \text{ um}, V_{GS1,2} = 421.3 \text{ mV}, W_{1,2} = 7.632 \text{ um}$$



Choose $\omega_{p2} = 4\omega_u \rightarrow PM > 70^\circ \rightarrow g_{m7} = 8 g_{m1,2} = 720 \mu S \rightarrow I_{B2} = 4I_{B1} = 60 \mu A$

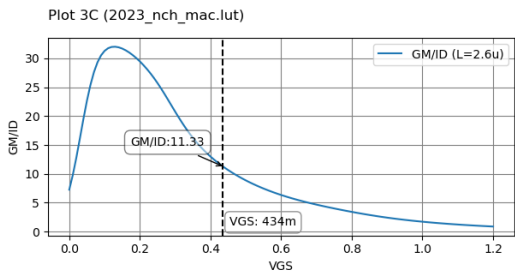
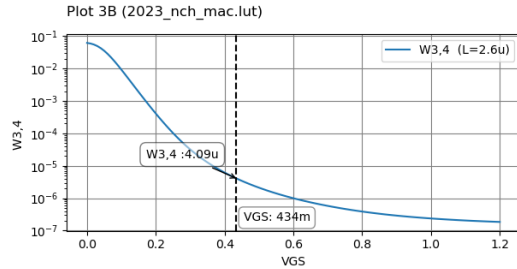
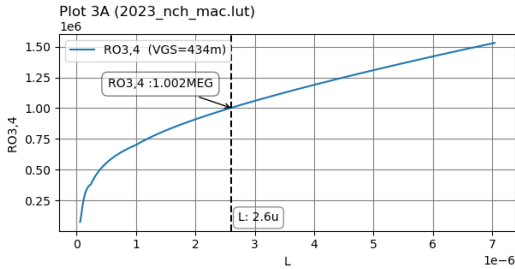
$$A_{V1} = \frac{g_{m7} r_{o6,7}}{2} (\text{Assume } r_{o6} = r_{o7}) \geq 32 \rightarrow r_{o2,4} = 89 \text{ k}\Omega \rightarrow (g_m r_o)_7 = 64$$

$$L_7 = 560 \text{ nm}, V_{GS7} = 434 \text{ mV}, W_7 = 8.335 \mu\text{m}$$



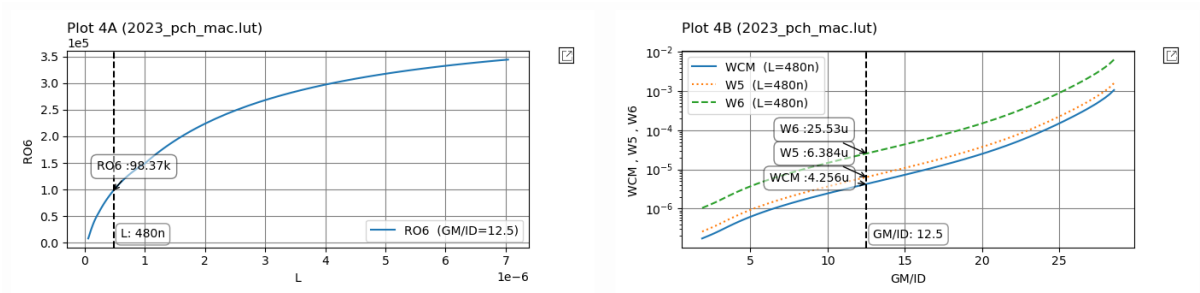
set $V_{GS3,4} = V_{GS7}$ (Cancels offset)

$$L_{3,4} = 2.6 \mu\text{m}, W_{3,4} = 4.09 \mu\text{m}, \left(\frac{g_{m3,4}}{I_D} \right) = 11.33$$



$$CMIR_H = -V_{SG1,2} - V_5^* + V_{DD} = 0.6 \rightarrow V_5^* \leq 0.1787 \text{ V} \rightarrow V_5^* = 0.16 \text{ V} \rightarrow \left(\frac{g_{m5}}{I_D} \right) = 12.5$$

$$L_{CM} = L_5 = L_6 = 480 \mu\text{m}, W_{CM} = 4.256 \mu\text{m}, W_5 = 6.384 \mu\text{m}, W_6 = 25.53 \mu\text{m}$$



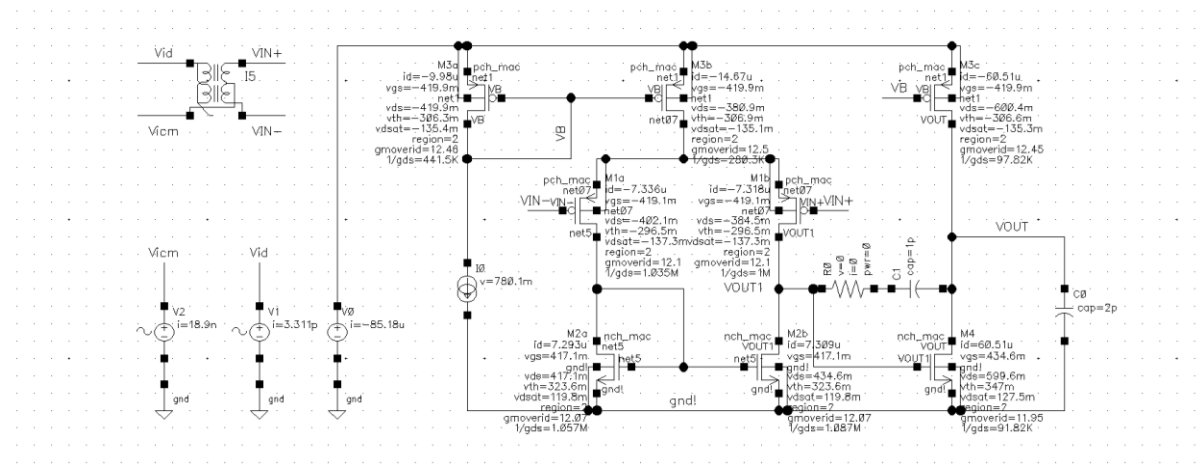
**** After Running DC Analysis W3,4 needed to be increased to 4.82u ****

Sizing Summary

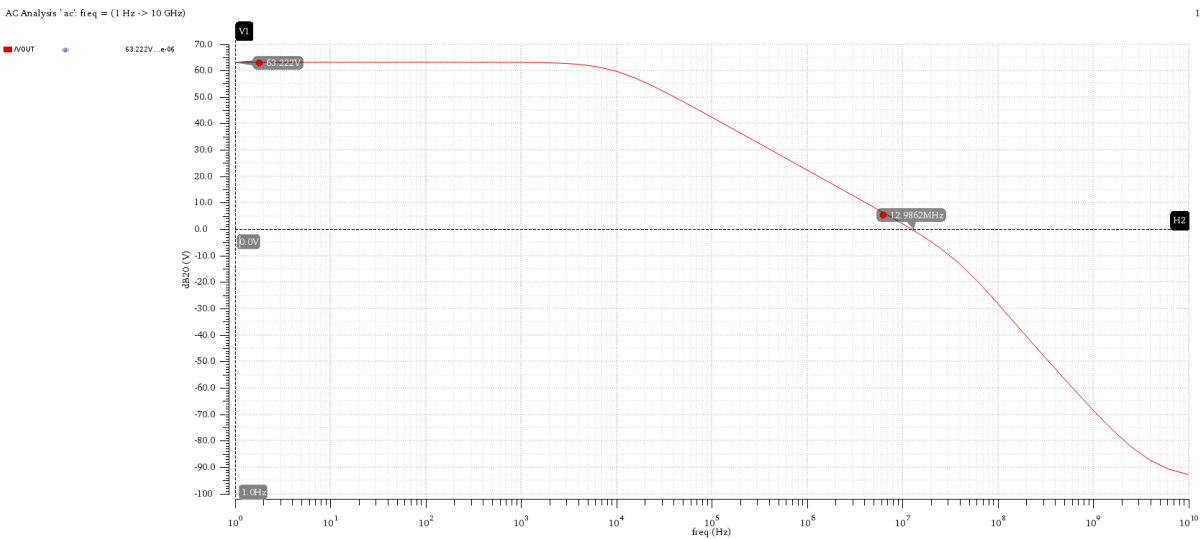
	M1	M2	M3	M4	M5	M6	M7	MCM
L	1.2u	1.2u	2.6u	2.6u	480n	480n	560n	480n
W	7.632u	7.632u	4.82u	4.82u	6.256u	25.53u	8.335u	4.256u

Simulations Results

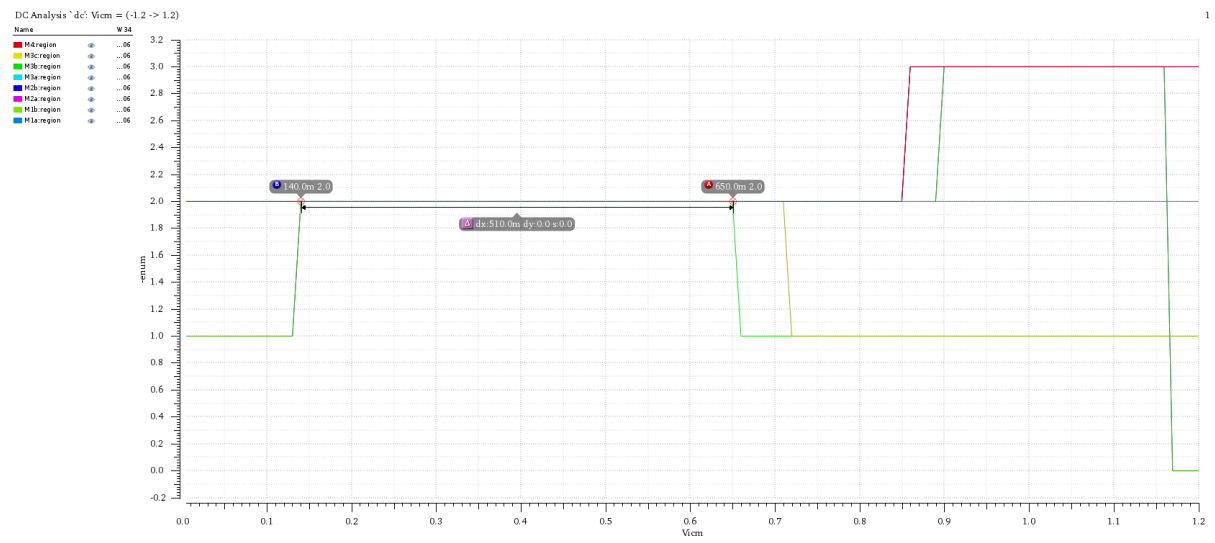
- DC Operating Points



- AC Analysis



- CMIR Results



- STB Analysis

