Use gm/Id methodology to design a differential input, single-ended output two-stage Miller-compensated OTA. The OTA is to be used as a buffer (unity gain feedback configuration) to probe sensitive internal signals in a complex mixed-signal design. The OTA should achieve the specs below. (Using 180 nm Technology)

| Spec | Value |
|---|---|
| Supply Voltage | 1.8 V |
| Static Gain Error | ≤ 0.05% |
| CMRR @ DC | ≥ 74 dB |
| Phase Margin (Avoid Pole-Zero Doublets) | ≥ 70° |
| OTA Current Consumption | ≤ 60 uA |
| CMIR-High | ≥ 1 V |
| CMIR-Low | ≤ 0.2 V |
| Output Swing | 0.2 : 1.6 V |
| Load | 5 pF |
| Buffer Closed Loop Rise Time (10% to 90%) | ≤ 70 ns |
| Slew Rate SR | 5 V/uS |

Table 1. OTA Specs

Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own bias circuit (current mirrors). Create a schematic and an appropriate symbol for the OTA.

## Design Procedures

1. - Since CMIR is 1 : 0.2 closer to GND rail we use a PMOS input pair of first stage
   - The current mirror load of the second stage should be the same as the current tail of the first stage (PMOS) since they are both current mirrors so the second stage input transistor should be NMOS, Also the VGS of the second stage input pair should be the same as VGS of the current mirror load of first stage (NMOS) to cancel the offset.

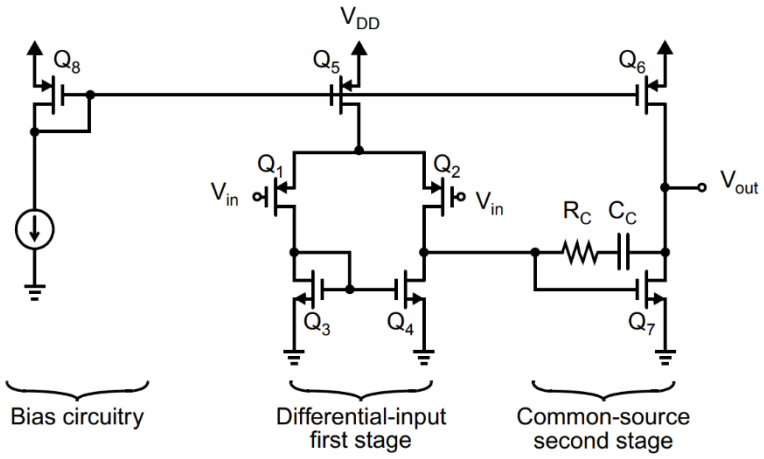


Figure 2. Selected OTA Topology

2.

$$C_C = 0.5 * 5\ pF = 2.5\ pF$$

3.

$$t_{rise} = 2.2\ \tau = 2.2\ RC = \frac{2.2}{2\pi\ BW_{CL}} = 70\ ns \rightarrow BW_{CL} = 5\ MHz$$

$$\therefore BW_{CL} = UGF_{CL} = \frac{g_{m1,2}}{2\pi\ C_C} = 5\ MHz \rightarrow g_{m1,2} = 78.5\ uS$$

4.

$$SR = \frac{I_{B1}}{C_C} = \frac{5}{10^6} \rightarrow I_{B1} = 12.5\ uA$$

$$I_{B2} = I_{total} - I_{B1} = 60\ uA - 12.5\ uA = 47.5\ uA$$

5.

$$I_{D1} = \frac{I_{B1}}{2} = 6.25\ uA$$

$$\therefore \frac{g_{m1,2}}{I_D} = \frac{78.5\ uS}{6.25\ uA} = 12.56\ S/A$$

6.

$$A_{VCL} = \frac{A_{VOL}}{1 + \beta A_{VOL}} = \frac{1}{\frac{1}{A_{VOL}} + 1} = 1 - \frac{1}{A_{VOL}}$$

$$\epsilon_s = \left|\frac{Actual - ideal}{ideal}\right| * 100 \rightarrow \frac{0.05}{100} \geq \left|\frac{1 - \frac{1}{A_{VOL}} - 1}{1}\right| = \frac{1}{A_{VOL}}$$

$$\therefore A_{VOL} \geq 2000 = 66.02\ dB$$

7. We assign higher gain to the first stage as it has lower current so we can get higher gain easier, also we need higher gain to get high CMRR, also to reduce the input referred noise of the second stage. If we want to get higher gain of the second stage, we should use cascaded devices with will limit the output swing.

$$A_{V1} = 36.02\ \text{dB} = 63.24 \ \text{ and } A_{V2} = 30\ \text{dB} = 31.62$$

8.

$$A_{V1} = g_{m1,2} * \frac{r_{o1,2}}{2} = 63.24 \rightarrow \frac{g_{m1,2}}{g_{ds1,2}} = 126.5$$

$$g_{ds1,2} = 620.5\ \text{nS} \rightarrow r_{o1,2} = 1.611\ \text{M}\Omega$$

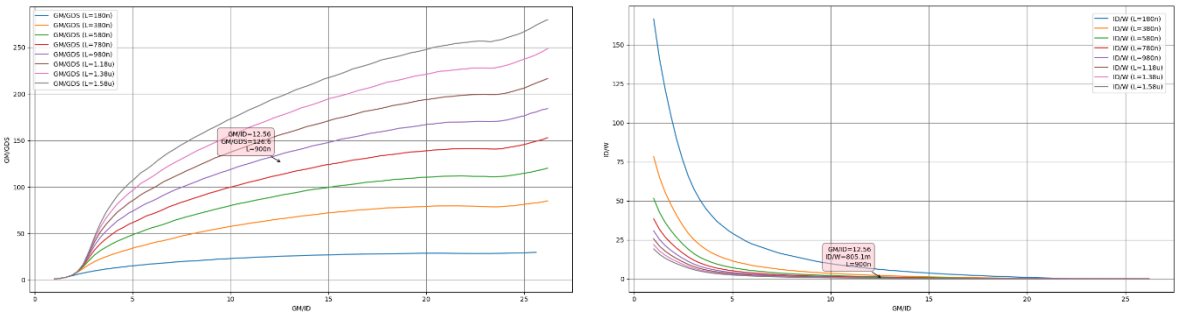

Figure 3. Input Pair GM/GDS Vs GM/ID and ID/W Vs GM/ID

$$L_{1,2} = 900\ \text{nm}$$

$$\frac{I_D}{W_{1,2}} = 805.1\ \text{m} \rightarrow W_{1,2} = 7.76\ \text{um}$$

9.

$$\text{Assume } \frac{g_{m3,4}}{I_D} = 15$$

$$\text{given } I_D = 6.25\ \text{uA and } g_{ds3,4} = 620.5\ \text{nS}$$

$$\therefore \frac{g_{ds3,4}}{I_D} = 0.0992 \rightarrow L_{3,4} = 1.4\ \text{um}$$

10.

$$\text{Assuming } \omega_{p2} = 4\omega_u \rightarrow \frac{G_{m1}}{C_C} = 4 * \frac{G_{m2}}{C_L} \rightarrow G_{m2} = 630\ \text{uS} = g_{m7}$$

$$\frac{g_{m7}}{I_D} = \frac{630\ \text{uS}}{47.5\ \text{uA}} = 13.26\ \text{S/A}$$

$$V_{out} \mid \text{min} = V_7^* = \frac{2}{13.26} = 150\ \text{m}$$

11.

$$\text{CMIR}_{\text{High}} = -V_{SG1} - V_5^* + V_{DD} = 1.8 - 0.567 - V_5^* \geq 1$$

$$V_5^* \leq 0.233\ \text{V} = 0.2\ \text{V} \rightarrow \frac{g_{m5}}{I_D} = 10 \rightarrow g_{m5} = 125\ \text{uS}$$

$$V_{out} \mid \max = V_{DD} - V_6^* = 1.8 - V_6^* = 1.6$$

$$V_6^* = 0.2\ \text{V} \rightarrow \frac{g_{m6}}{I_D} = 10 \rightarrow g_{m6} = 475\ \text{uS}$$

12.

$$\text{CMRR} = 5012 = g_{m1,2} * r_{o2,4} * g_{m3,4} * r_{o5}$$

$$\text{Assume } \frac{g_{m3,4}}{I_D} = 10 \rightarrow g_{m3,4} = 62.5\ \text{uS}$$

13.

$$\therefore r_{o5} = 634.11\ \text{k}\Omega \rightarrow g_{ds5} = 1.577\ \text{uS} \rightarrow \frac{g_{m5}}{g_{ds5}} = 79.26$$

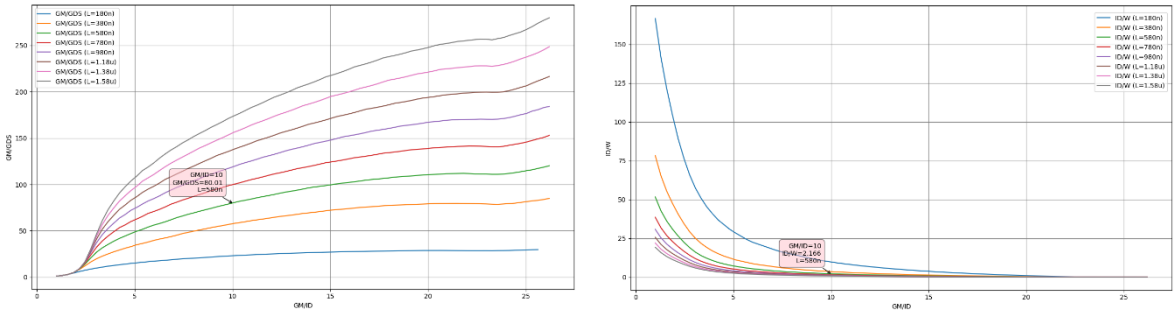

Figure 4. Tail Current Source GM/GDS Vs GM/ID and ID/W Vs GM/ID

$$L_{5,6} = 580\ \text{nm}$$

$$\frac{I_D}{W_5} = 2.166 \rightarrow W_5 = 5.77\ \text{um}$$

$$\frac{I_D}{W_6} = 2.166 \rightarrow W_6 = 21.93\ \text{um} \rightarrow \frac{g_{m6}}{g_{ds6}} = 80 \rightarrow g_{ds6} = 5.937\ \text{uS}$$

14.

$$A_{V2} = 31.62 = g_{m7}\left(\frac{1}{g_{ds7}} \mid\mid \frac{1}{g_{ds6}}\right)$$

$$\frac{g_{m7}}{I_D} = 13.26\ \text{S/A}$$

$$r_{o7} = 71.5\ k\Omega \rightarrow g_{ds7} = 13.98\ uS \rightarrow \frac{g_{m7}}{g_{ds7}} = 45$$

$$L_7 = 220\ nm$$

$$\frac{I_D}{W_7} = 12.52 \rightarrow W_7 = 3.79\ um \rightarrow V_{GS7} = 620.6\ m$$

15.

$$V_{GS3} = V_{GS7} = 620.6\ m$$

$$\frac{g_{ds3,4}}{I_D} = 0.0992 \rightarrow \frac{g_{m3}}{I_D} = 10.33$$

$$L_{3,4} = 740\ nm$$

$$\frac{I_D}{W_{3,4}} = 5.946 \rightarrow W_{3,4} = 1.05\ um$$

16.

$$CMIR_{High} = -V_{SG1} - V_5^* + V_{DD} = 1.8 - 0.567 - 0.2 = 1.033\ V$$

$$CMIR_{Low} = -V_{SG1} + V_{DSAT1} + V_{GS3} = -567\ m + 132.2\ m + 620.6\ m = 185.8\ mV$$

$$V_{out} \mid max = V_{DD} - V_{SG6} = 1.8 - 0.2 = 1.6$$

$$V_{out} \mid min = V_7^* = \frac{2}{13.26} = 150\ m$$

All choices meet the specs

17.

$$R_z = \frac{1}{g_{m7}} = \frac{1}{630\ u} = 1.587\ k\Omega$$

## Sizing Summary

| | M1,2 | M3,4 | M5 | M6 | M7 | M8 |
|---|---|---|---|---|---|---|
| **W** | 7.76 u | 1.05 u | 5.77 u | 21.93 u | 3.79 u | 4.616 u |
| **L** | 900 n | 740 n | 580 n | 580 n | 220 n | 580 n |
| **gm** | 78.5 u | 64.5 u | 125 u | 475 u | 629.8 u | 100 u |
| **gm/ID** | 12.56 | 10.33 | 10 | 10 | 13.26 | 10 |
| **$V_{DSAT}$** | 132.2 m | 153 m | 166.3 m | 166.3 m | 115.4 m | 166.3 m |
| **Vov** | 152 m | 199.8 m | 195.3 m | 195.3 m | 139.6 m | 195.3 m |
| **V*** | 159 m | 193 m | 200 m | 200 m | 150 m | 200 m |
| **Type** | PMOS | NMOS | PMOS | PMOS | NMOS | PMOS |
| **Rule** | 1st Stage In | CM Load | Tail CS | Active Load | 2nd Stage In | Biasing |

## Part 3 : Open-Loop OTA Simulation

Report The Following

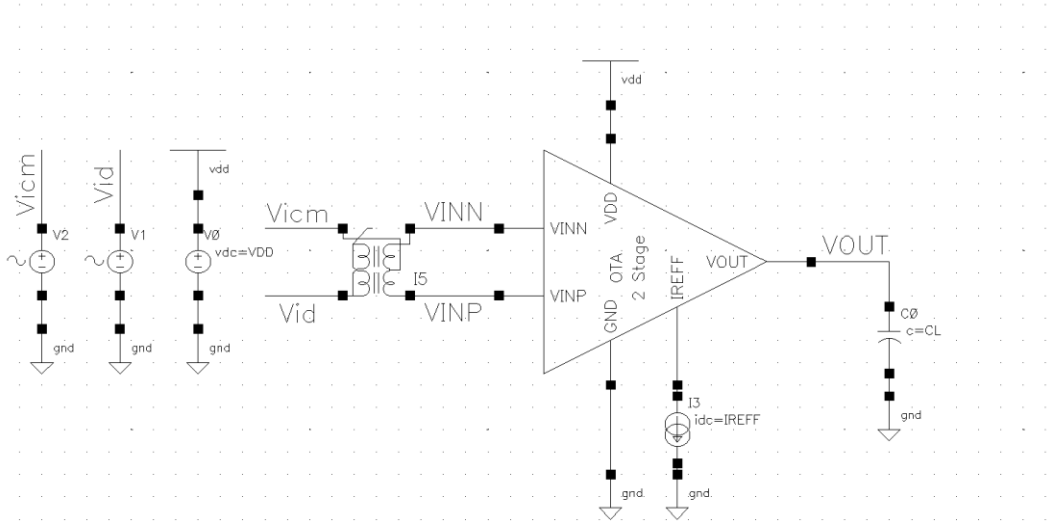


Figure 5. Two Stage OTA Test Bench

- Is the current (and gm) in the input pair exactly equal?

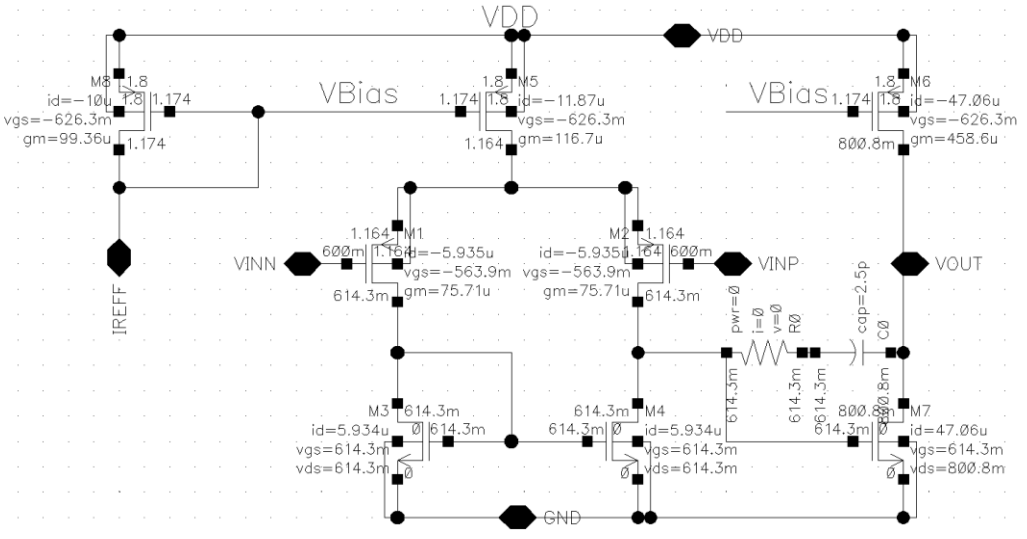


Figure 6. Two Stage OTA Schematic

Yes, As they are designed to be identical

- What is DC voltage at the output of the first stage? Why?

614.3 mV, $V_{out1} = V_F = V_{GS3} = 614.3$ mV

- What is DC voltage at the output of the second stage? Why?

800.8 mV, $V_{out2} = V_{DD} - V_{SD6} = 1.8 - 1 = 800$ mV

1. Diff small signal ccs:

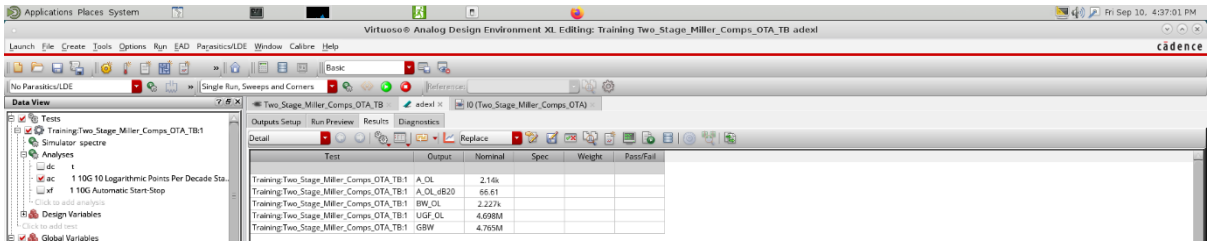


Figure 7. Two Stage OTA AC Results.

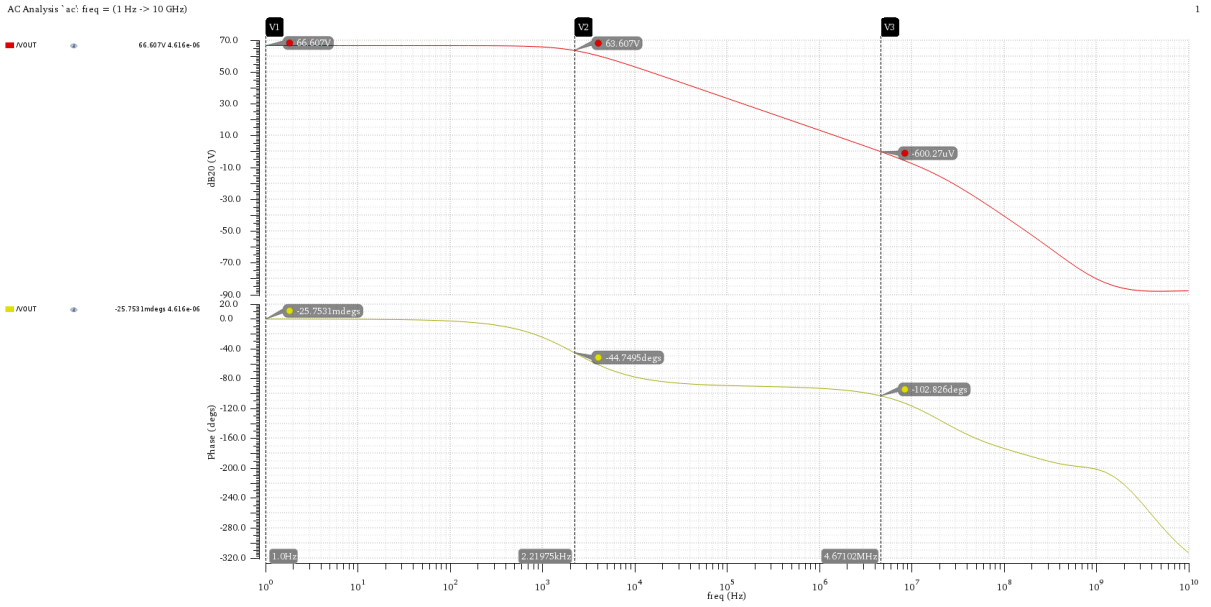


Figure 8. Two Stage OTA Diff Gain Bode Plot

- Compare simulation results with hand calculations in a table.

$$A_{Vd} = A_{V1} * A_{V2} = g_{m1} * R_{out1} * g_{m7} * R_{out2} = 63.23 * 31.63 = 2000 = 66 \text{ dB}$$

$$BW = \frac{1}{2\pi * R_{out1} * (1 + A_{V2}) * C_C} = \frac{1}{2\pi * 805.5\text{ k} * 32.63 * 2.5\text{ p}} = 2.42 \text{ kHz}$$

$$GBW = UGF = A_V * BW = 4.84 \text{ MHz}$$

GBW and BW from simulation is smaller because of the parasitic capacitances.

| | Simulations | Hand Analysis |
|---|---|---|
| Av | 66.6 dB | 66 dB |
| BW | 2.22 kHz | 2.42 kHz |
| GBW | 4.7 MHz | 4.84 MHz |
| UGF | 4.76 MHz | 4.84 MHz |

2. CM small signal ccs:

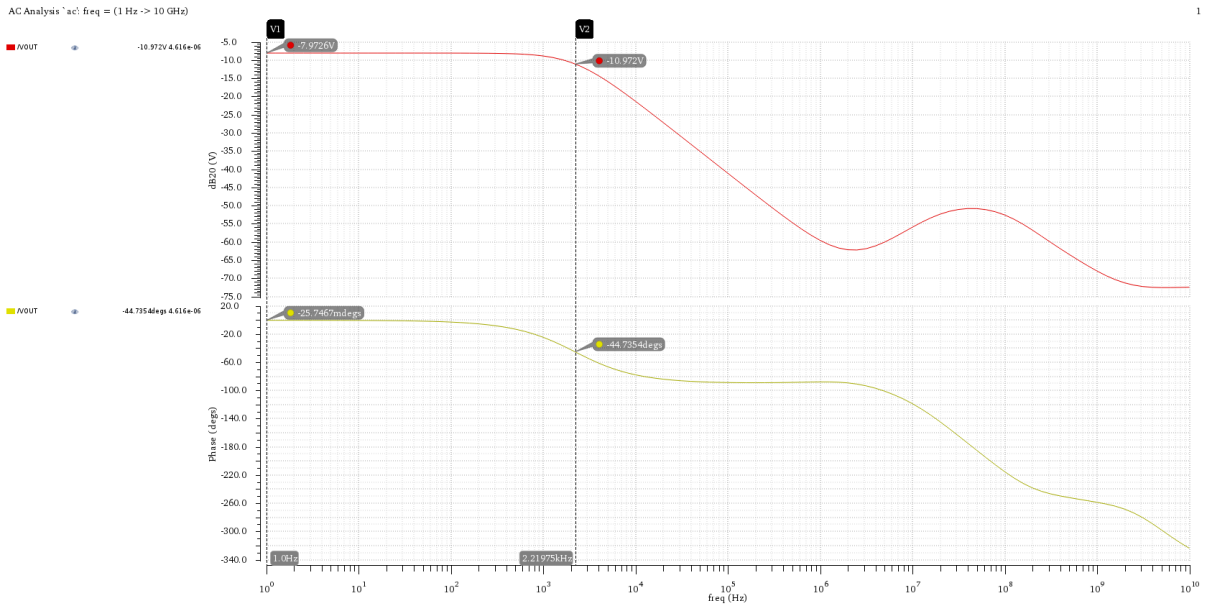


Figure 9. Two Stage OTA CM Gain Bode Plot

- Compare simulation results with hand calculations in a table.

$$A_{Vcm} = \frac{1}{2 * r_{o5} * g_{m3}} * g_{m7}R_{out2} = \frac{31.63}{2 * 634.11\ k * 64.5\ u} = 0.386 = -8.25\ dB$$

$$BW = \frac{1}{2\pi * R_{out1} * (1 + A_{V2}) * C_C} = \frac{1}{2\pi * 805.5\ k * 32.63 * 2.5\ p} = 2.42\ kHz$$

The common mode and differential mode have the same poles as the poles do not depend on the input.

| | Simulations | Hand Analysis |
|---|---|---|
| Av | -7.97 dB | -8.25 dB |
| BW | 2.22 kHz | 2.42 kHz |

## 3. (Optional) CMRR:

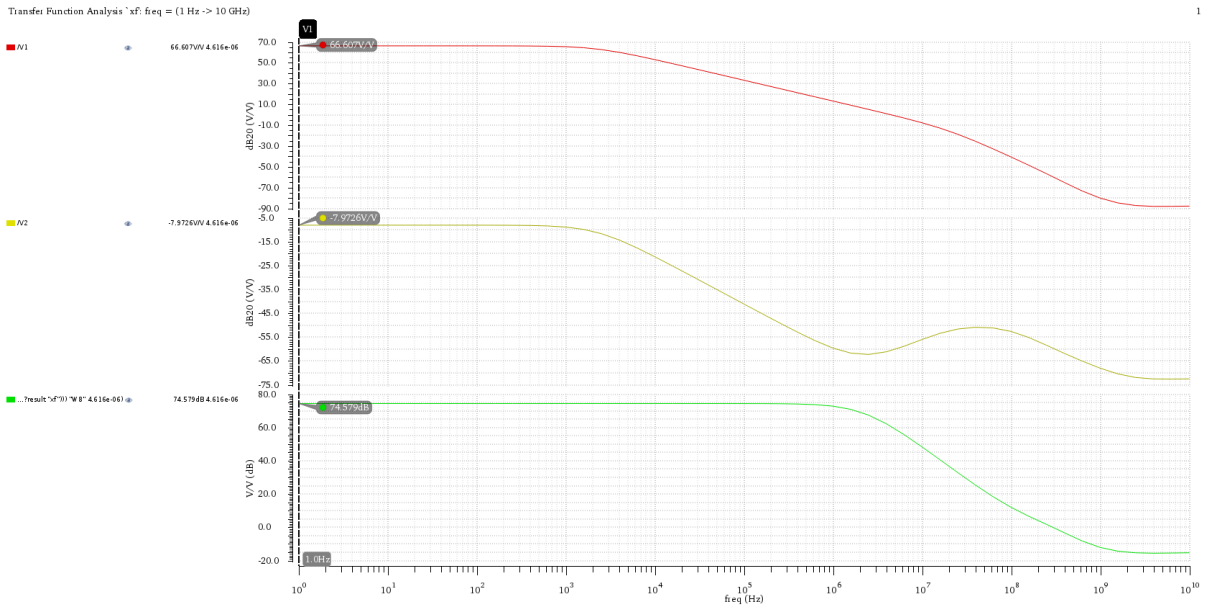


Figure 10. Two Stage OTA CMRR Bode Plot

$$\text{CMRR} = g_{m1} * r_{o2} * g_{m3,4} * r_{o5} = 78.5\ \text{u} * 1.611\ \text{M} * 64.5\ \text{u} * 634.11\ \text{k} = 74.53\ \text{dB}$$

| | Simulations | Hand Analysis |
|---|---|---|
| CMRR | 74.57 dB | 74.53 dB |

## 4. (Optional) Diff large signal ccs:

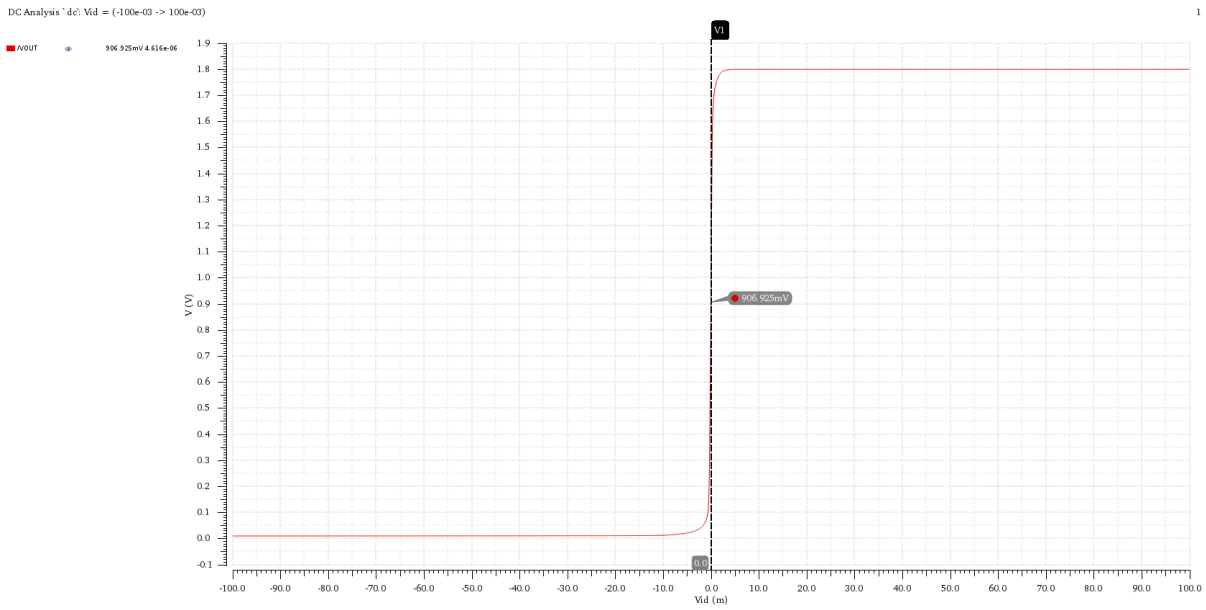


Figure 11. Two Stage OTA Diff Large Signal Analysis.

- What is the value of Vout at VID = 0. Compare it with value obtained in DCOP.

Vout @ VID = 0 is equal to 906.9 mV which is the same value as DC @ VICM = 0.9

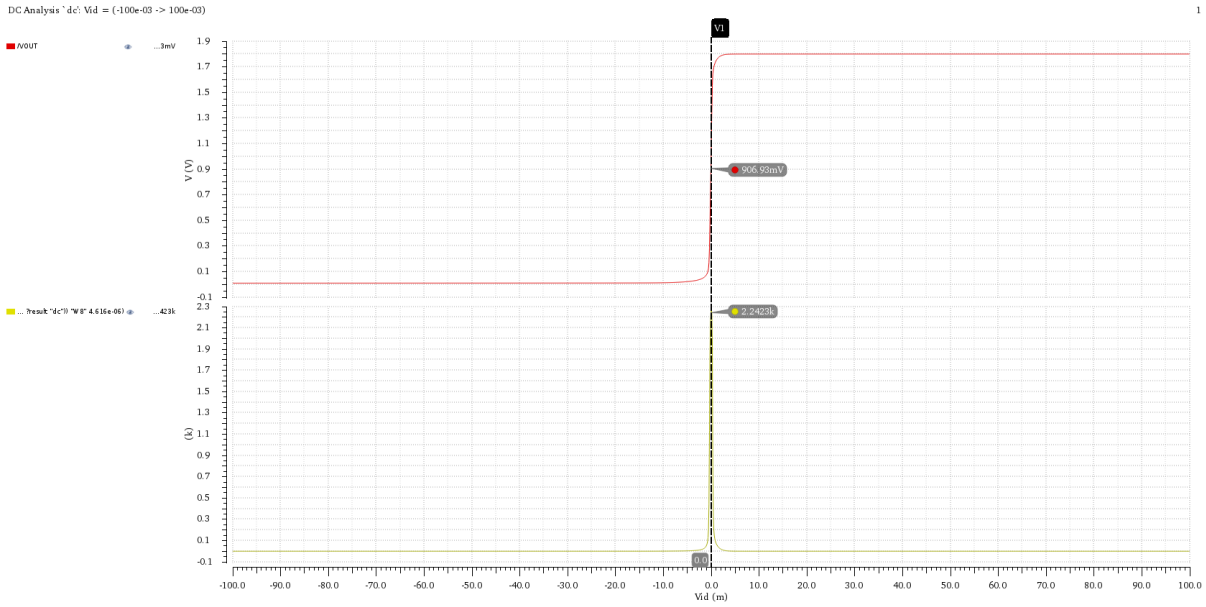


Figure 12. Two Stage OTA Diff Large Signal Analysis with Derivative.

- Compare the peak with Avd from ac analysis. Comment on the result.

The peak value is 2242 which is very close to the Avd @ VICM = 0.9 because the derivative of Vout with Vin is by definition the small signal gain.

5. CM large signal ccs (region vs VICM):

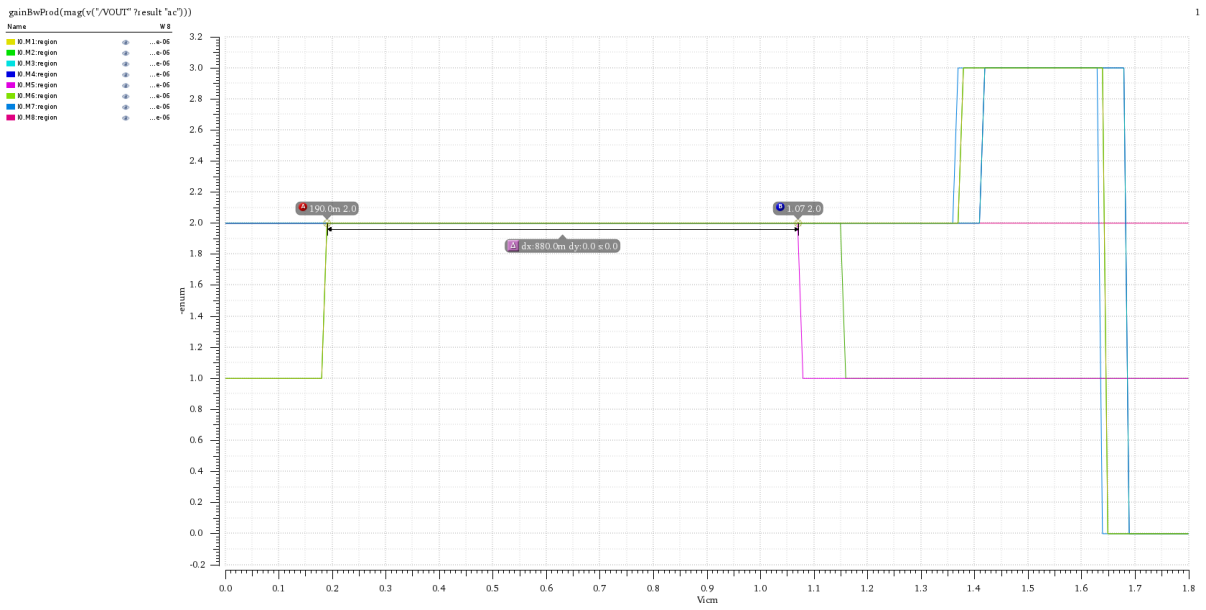


Figure 13. Operating Region Vs VICM

| | Simulations | Hand Analysis |
|---|---|---|
| CMIR | 190 m : 1.07 | 185 m : 1.03 |

6. (Optional) CM large signal ccs (GBW vs VICM):

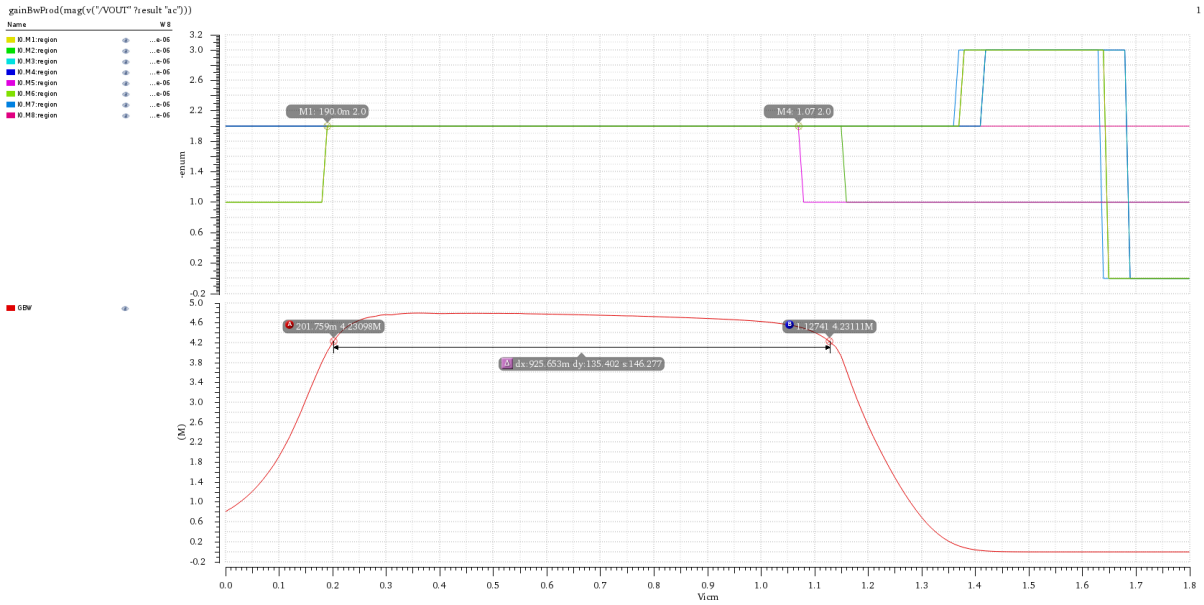


Figure 14. Operating Region Vs VICM and GBW Valid Range.

## Part 4 : Closed-Loop OTA Simulation

1. Schematic of the OTA and the bias circuit with DC OP point clearly annotated in unity gain buffer configuration.

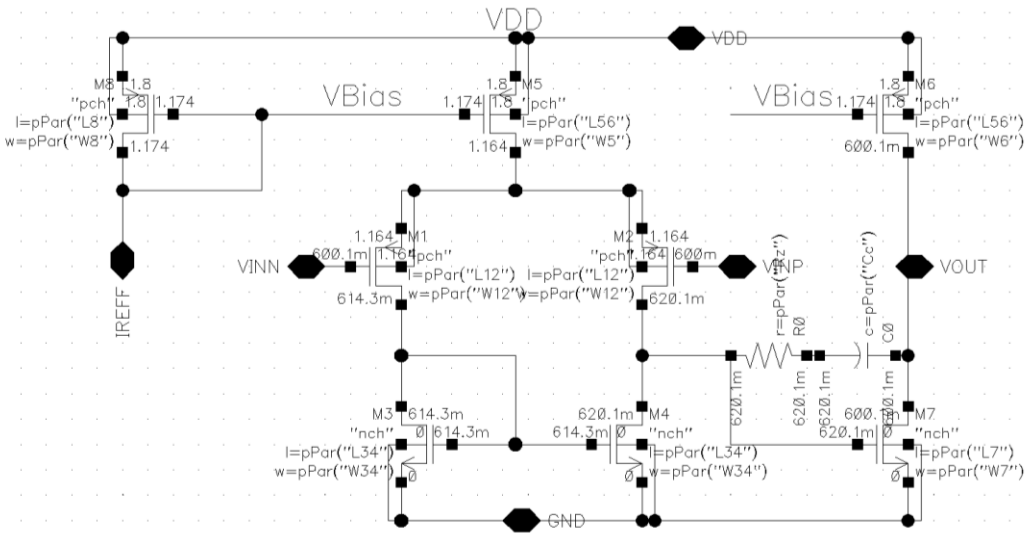


Figure 15. Two Stage OTA Closed Loop DC Voltages

- Are the DC voltages at the input terminals of the op-amp exactly equal? Why?

Yes, The DC input voltages are exactly equal there is only a 0.1 mV difference because of the feedback (unity gain buffer), and the difference is because the amplifier is not infinite gain.

- Is the DC voltage at the output of the first stage exactly equal to the value in the open-loop simulation? Why?

The DC output voltage of the first stage is not exactly equal to the open-loop simulation, because Vout of the second stage has changed from 0.8 V to 0.6 V, so the change in the input of the second stage should be $\Delta Vin2 = (0.8-0.6)/31.6 = 6.3$ mV, so Vout1 increases by 6.3 mV to be 620 mV. Also, because the two inputs are not the same, so the currents are not the same and the VDS is not equal.

- Is the current (and gm) in the input pair exactly equal? Why?

The current and gm are the same, they differ only in the third or fourth digit, because of the feedback which is not infinite.

2. Loop gain:

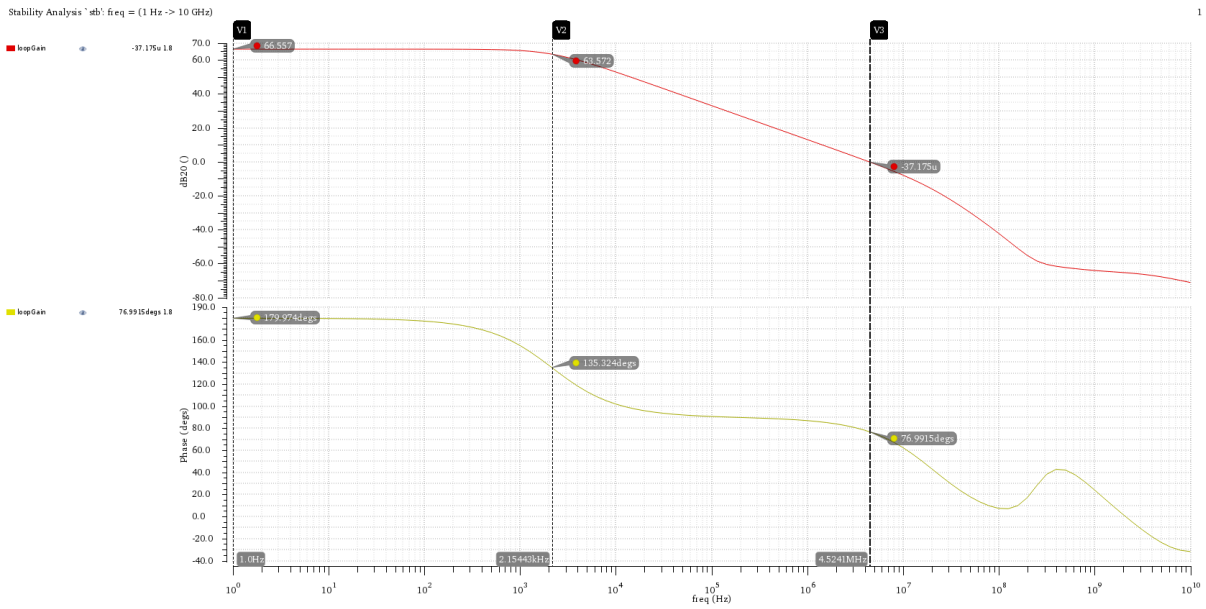


Figure 16. Two Stage OTA Loop Gain.

- Compare DC gain, fu, and GBW with those obtained from open-loop simulation.

The gain has changed because Vout has changed and that will change ro and Rout but The UGF and GBW have decreased because of the loading effect of the input capacitance.

- Report PM. Compare with hand calculations. Comment.

PM = 77° and the hand analysis gives 76°, which is nearly the same.

- Compare simulation results with hand calculations in a table.

| | Simulations | Hand Analysis |
|---|---|---|
| LG | 66.5 dB | 66 dB |
| BW | 2.15 kHz | 2.42 kHz |
| GBW | 4.52 MHz | 4.84 MHz |
| UGF | 4.52 MHz | 4.84 MHz |

3. Slew rate:

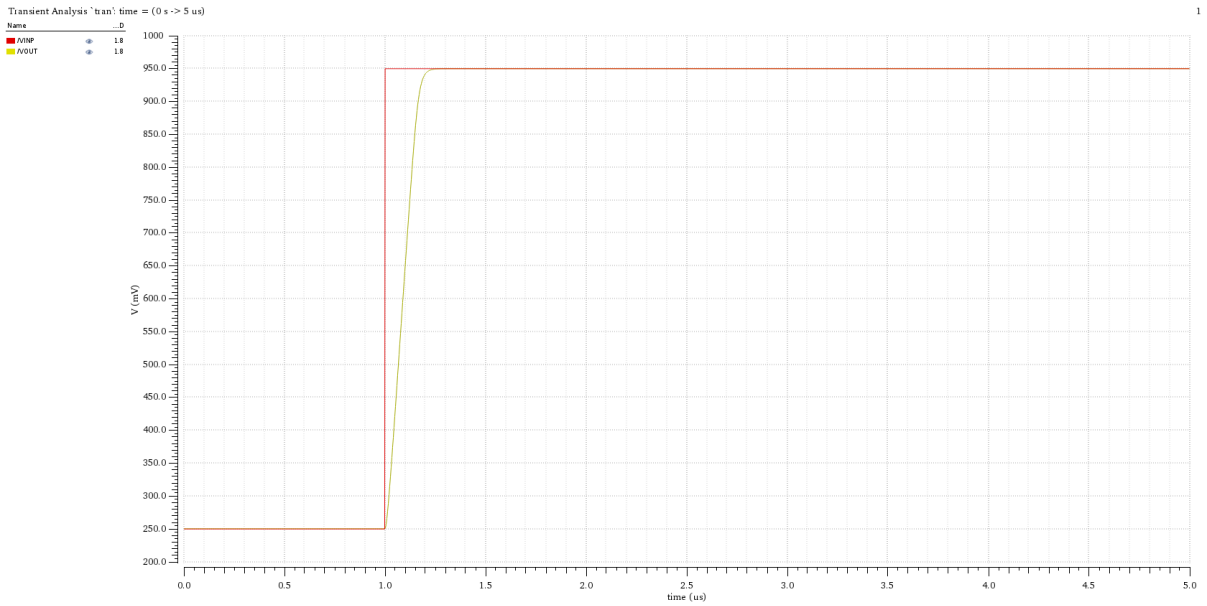


Figure 17. Two Stage OTA Closed Loop Transient SR.

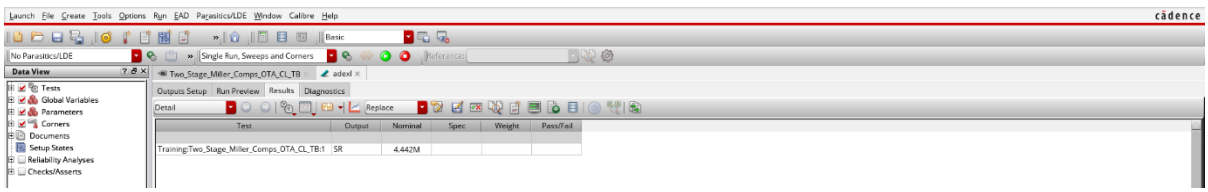


Figure 18. Two Stage OTA Closed Loop SR.

- Compare simulation results with hand calculations in a table.

| | Simulations | Hand Analysis |
|---|---|---|
| SR | 4.442 V/us | 4.748 V/us |

Note: SR does not meet the spec but it accepted, We can improve SR by decreasing Cc although it will affects the current Consumption and Stability.

4. Settling time:

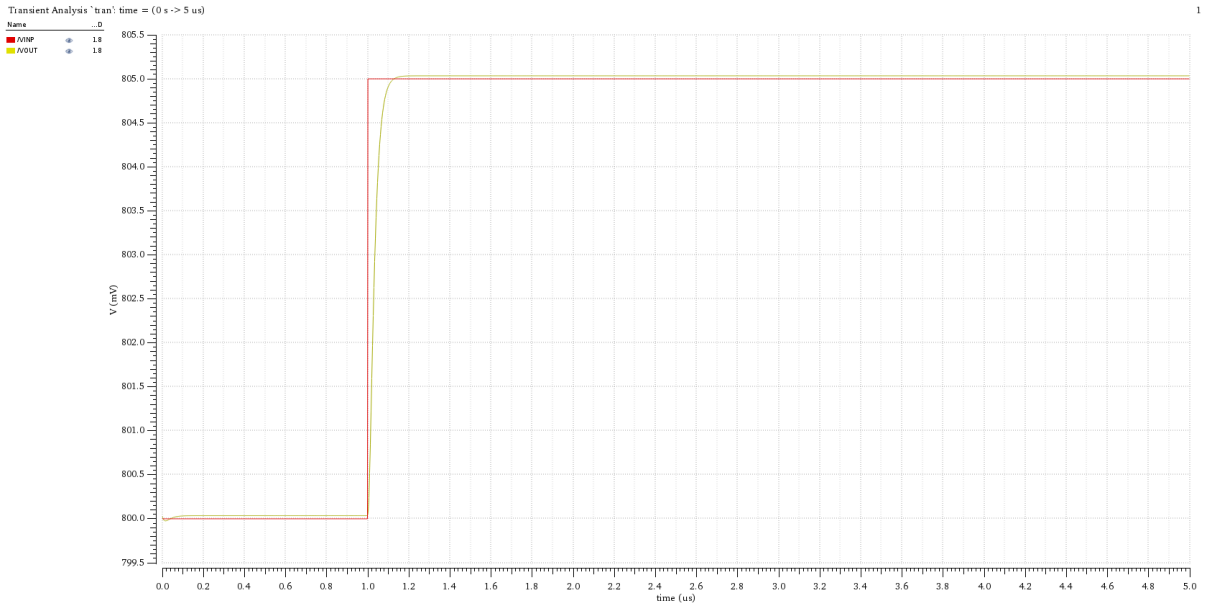


Figure 19. Two Stage OTA Closed Loop Transient Settling Time.

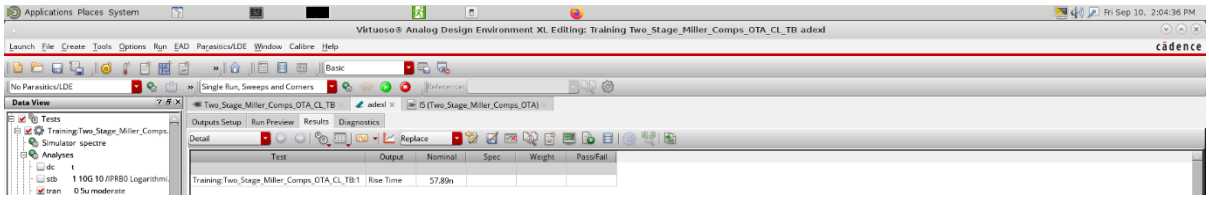


Figure 20. Two Stage OTA Closed Loop Settling Time.

- Compare simulation results with hand calculations in a table

$$\text{Rise Time} = 2.2\tau = \frac{2.2}{2\pi * \text{BW}} = \frac{2.2}{2\pi * \text{GBW}} = 77.46\ \text{ns}$$

| | Simulations | Hand Analysis |
|---|---|---|
| Rise Time | 57.89 ns | 77.46 ns |

$$\text{But for a critical damped system} \rightarrow \text{Rise Time} = 1.7\tau = \frac{1.7}{2\pi * \text{GBW}} = 5.98\ \text{ns}$$

- Do you see any ringing? Why?

No, Since the PM > 76 with small margin, So it is stable and critical damped system

## Part 5 (optional): DC Closed Loop AC Open-Loop OTA Simulation

The switches are used to close the feedback in the dc and to run open loop ac analysis.

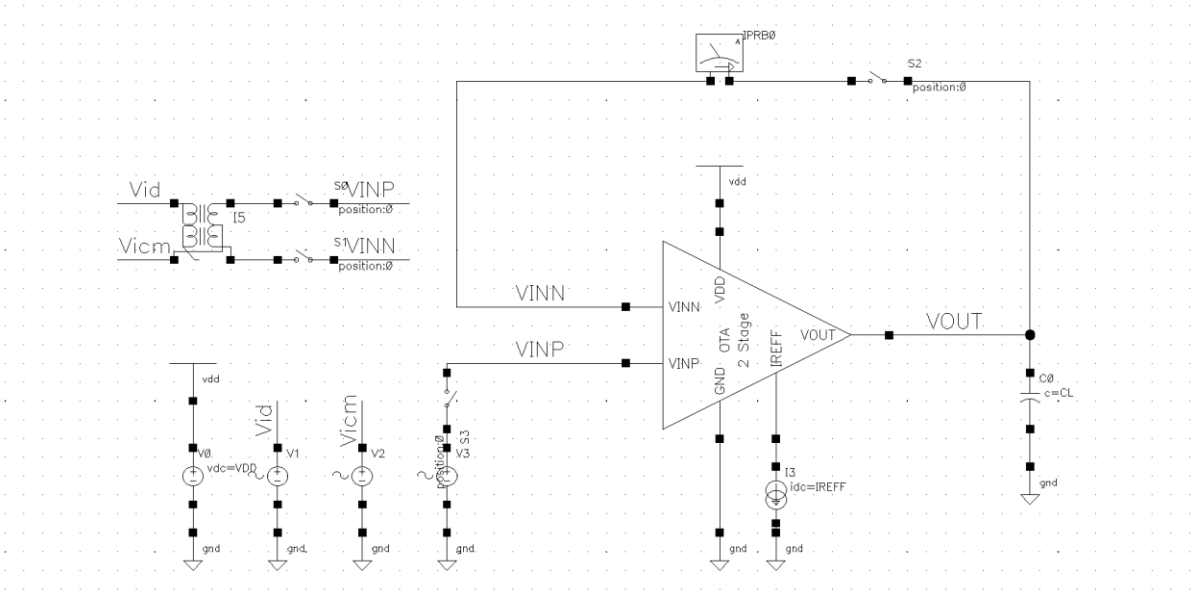


Figure 21. DC Closed Loop AC Open-Loop OTA

# Result Summary

| Spec | Value | Achieved |
|---|---|---|
| Supply Voltage | 1.8 V | 1.8 V |
| Static Gain Error | ≤ 0.05% | 0.046% |
| CMRR @ DC | ≥ 74 dB | 74.58 dB |
| Phase Margin | ≥ 70° | 76.9° |
| OTA Current Consumption | ≤ 60 uA | 58.93 uA |
| CMIR-High | ≥ 1 V | 1.07 V |
| CMIR-Low | ≤ 0.2 V | 0.195 V |
| Output Swing | 0.2 : 1.6 V | 0.15 : 1.6 V |
| Load | 5 pF | 5 pF |

Table 2. Design Results