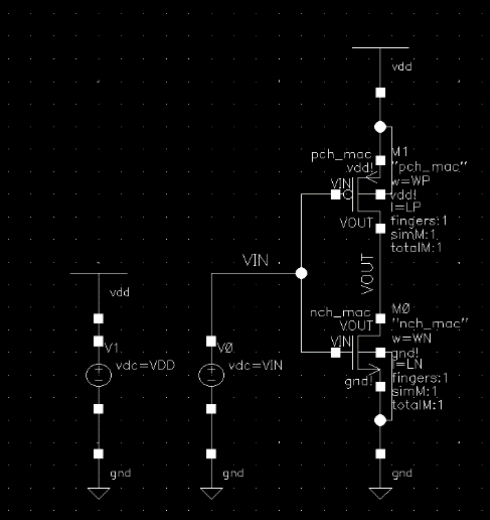
Using cadence draw an inverter with L = Lmin for both NMOS and PMOS device and W = 0.6 µm for NMOS and
W = 1.2 µm for PMOS and using Dc analysis only!

1. Draw the DC characteristics of Vout Vs Vin
2. Use the calculator to get it's gain vs Vin
3. Using parametric analysis repeat the exercise at 5 different temperature from −40 C to 125 C
4. Repeat the first two steps for L = Lmin and L = 3Lmin, what's your conclusion ?



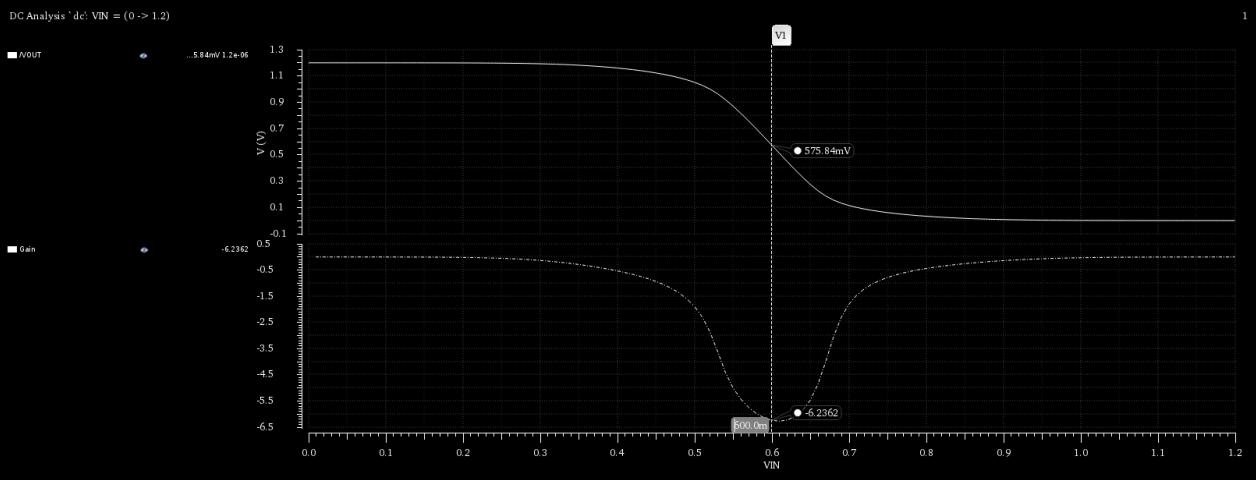


Figure 4: DC Characteristics and Gain Vs VIN

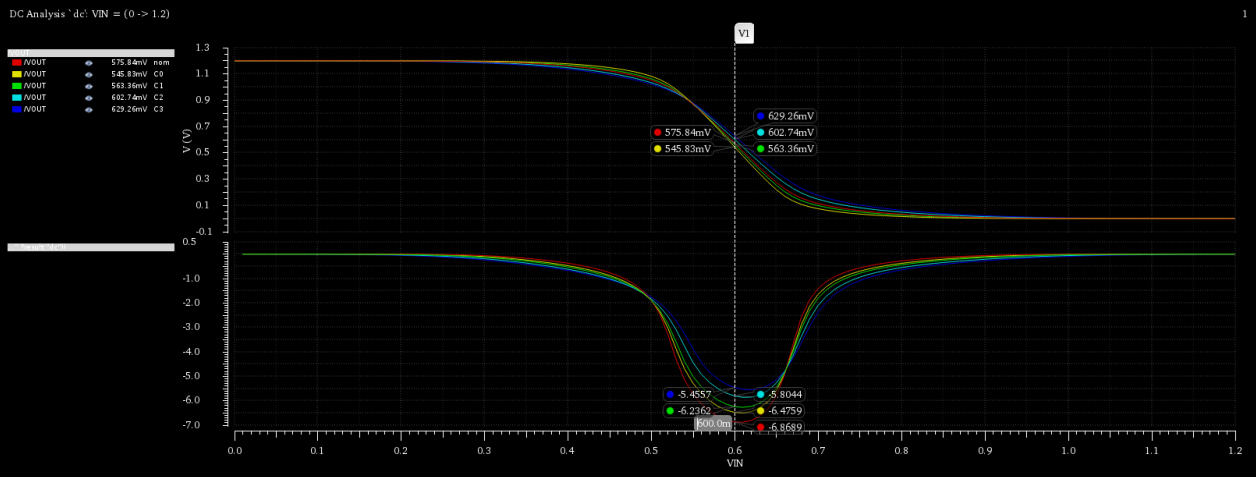


Figure 5: DC Characteristics and Gain Vs VIN Corners 27, -40, 0, 80, 125 respectively

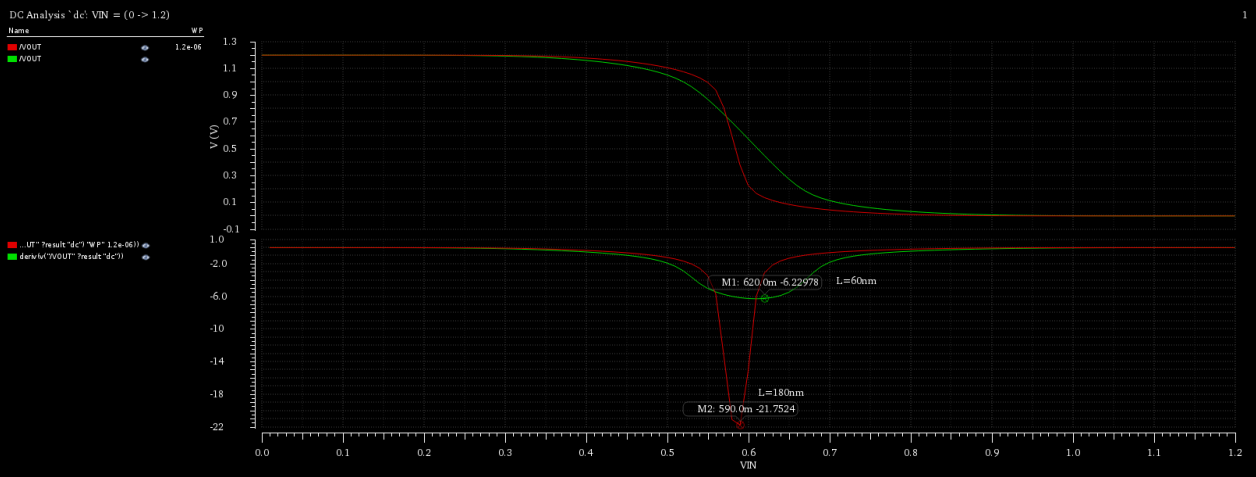


Figure 6: DC Characteristics and Gain Vs VIN for 180 nm

Increasing temperature decreases gain and makes the inverter input and output margins worse so the lower the temperature the better.
Increasing length increases gain and makes the inverter margins better for the same width.