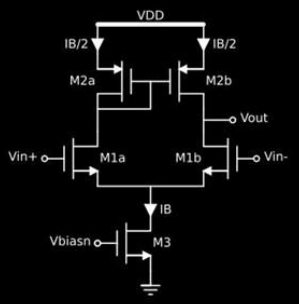
Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs. Use an ideal external 10uA DC current source in your test bench (not included in the OTA current consumption spec), but design your own current mirror.

Spec.	
Technology	65nm CMOS
Supply Voltage	1.2 V
Open loop DC voltage gain	≥ 34 dB
CMRR @ DC	≥ 74 dB
Phase Margin	≥ 70°
OTA Current Consumption	≤ 20 uA
Reference current	10 uA
CM input range low	≤ 0.6 V
CM input range high	≥ 1 V
GBW	≥ 5 MHz

Design steps

- Av not too high So, achieved by single stage
- CMIR Spec is 0.8 V < CMIR < 1.5 V Closer to the VDD rail, , I used NMOS input stage. The implemented architecture is shown in figure below.



$$\text{GBW} = \frac{g_{m1}}{2\pi C_L} \geq 5\ \text{MHz} \rightarrow g_{m1} \geq 157.1\ \text{uS}$$

$$g_{m1} = 175\ \text{uS} \rightarrow \because I_{SS} = 2 * I_{D1} \rightarrow I_{D1} = 10\ \text{uA}$$

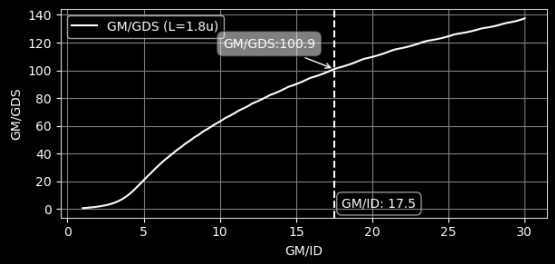
$$\therefore \frac{g_{m1}}{I_D} = \frac{175}{10} = 17.5$$

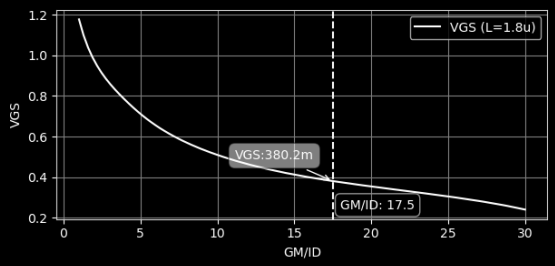
$$\because A_V = 50 = g_{m1}\,(r_{o1} \parallel r_{o2})$$

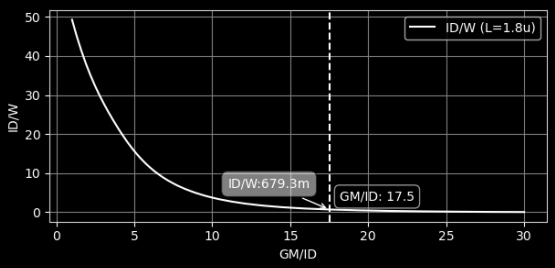
$$\text{Assume } r_{o1} = r_{o2} = r_o \rightarrow A_V = g_{m1}\frac{r_o}{2}$$

$$\text{Assume } V_{DS1} = V_{DS2} = 400\ \text{mV} \rightarrow V_{SB1} = 400\ \text{mV}$$

$$\therefore 100 = g_{m1}\, r_o \rightarrow L_1 = 1.8\text{u}$$







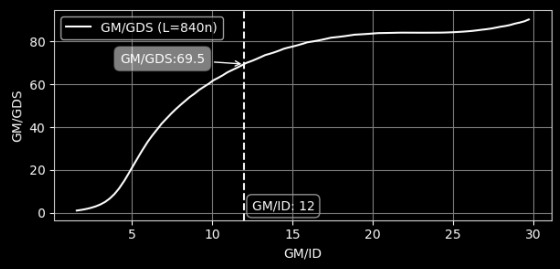
$$V_{GS1} = 380.2\ \text{mV}$$

$$\frac{I_D}{W_1} = 679.3\ \text{m} \rightarrow W_1 = 14.75\ \text{um}$$

Assume $\frac{g_{m2}}{I_D} = 12 \rightarrow g_{m2} = 120\ \text{uS}$

$\because A_V = g_{m1}\frac{r_o}{2} = 50 \rightarrow r_o = 571.5\ \text{k}\Omega$

$\therefore g_{m2}\, r_{o2} = 68.6$

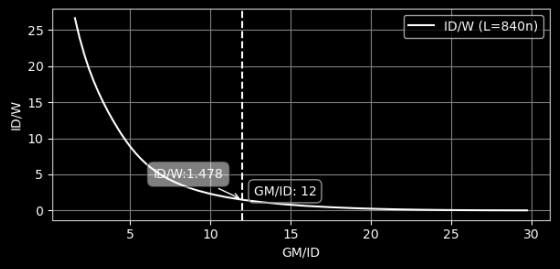


$\because \text{CMIR}_H \geq 1 \rightarrow \therefore V_{GS1} - V_1^* - V_{SG2} + V_{DD} \geq 1$

$V_{SG2} \leq 466\ \text{mV} \rightarrow \therefore \frac{g_{m,2}}{I_D}|\text{min} = 9.8\ \frac{S}{A}$

Choose same $\frac{g_{m2}}{I_D} = 12$ as my asumption

$L_2 = 840\ \text{nm} \rightarrow V_{GS2} = 419.8\ \text{m}$



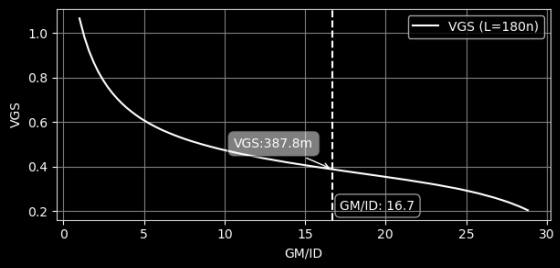
$\frac{I_D}{W_2} = 1.478 \rightarrow W_2 = 6.76\ \text{um}$

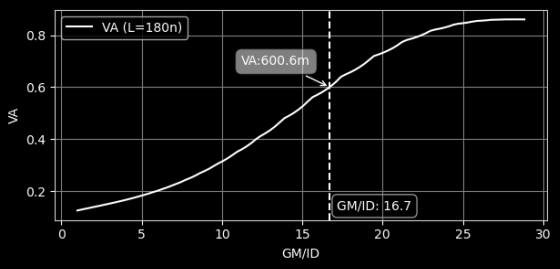
$\because A_{V,CM} = \frac{-1}{2\, g_{m,2}\, R_{SS}} = 34 - 74 = -40\ \text{dB}$

$\therefore R_{SS} \geq 417\ \text{k}\Omega \rightarrow r_{o3} \geq 417\ \text{k}\Omega$

Assume $L_{CM} = 3 * L_{min} = 180\ \text{nm}$

Assume $V_{DS,CM} = V^* = 120\ \text{mV} \rightarrow \frac{g_{mCM}}{I_D} = 16.7$



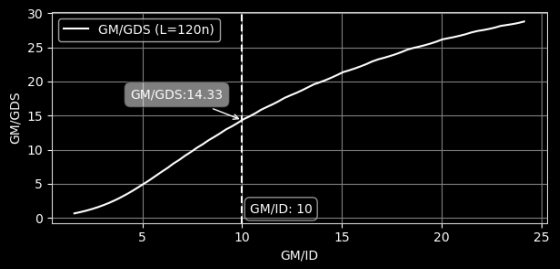


$\therefore V_{GS,CM} = 387.8\ \text{m} \rightarrow \therefore V_A = 600.6\ \text{mV}$

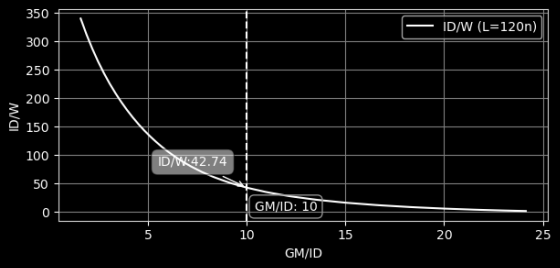
$r_{oCM} = 30\ \text{k}\Omega \rightarrow R_{out} = (g_m\, r_o)_{CASC}\, r_{oCM} = 420\ \text{k}$

$(g_m\, r_o)_{CASC} = 14$

bias it in SI $\left(\frac{g_m}{I_D}\right)_{CASC} = 10 \rightarrow$ for large r_o



$\therefore L_{CASC} = 120\ \text{nm} \rightarrow V_{GS,CASC} = 520.7\text{m}$



$\because \frac{I_D}{W_{CASC}} = 42.74 \rightarrow \therefore W_{CASC} = 470\ \text{nm}$

$\because I_{Ref} * R_{CM} = VGS_{CASC} + V^* - VGS_{CM}$

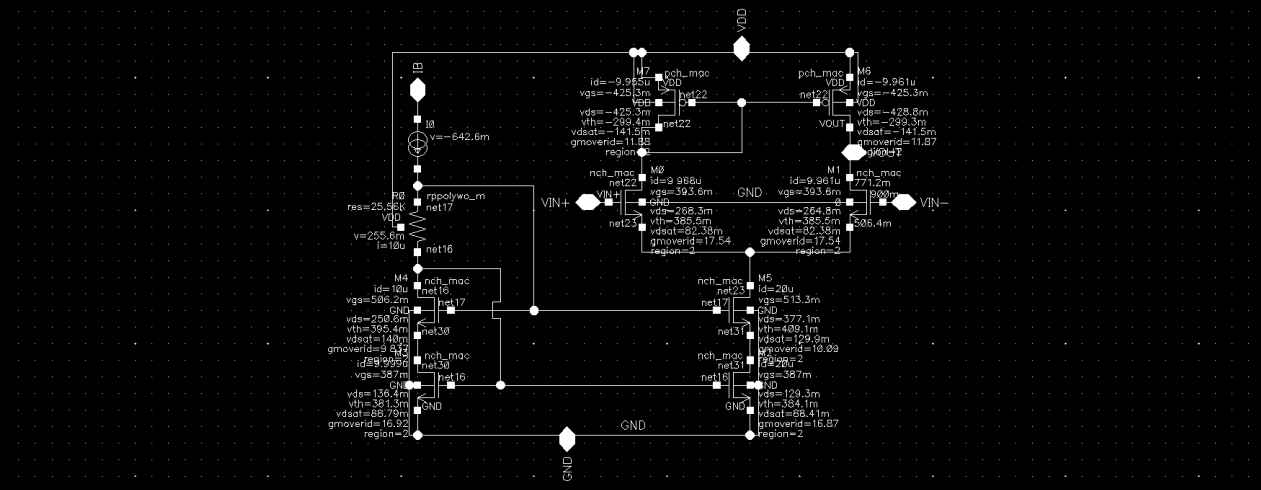
$R_{CM} = \frac{520.7\text{m} + 120\text{m} - 387.8\text{m}}{10\ \text{u}} = 25.3\ \text{k}\Omega$

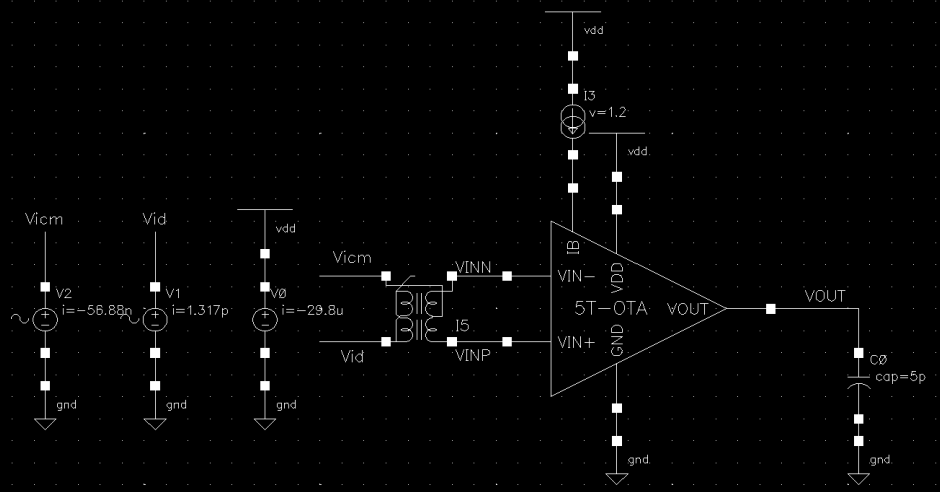
$\because \mathrm{CMIR_L} \leq 0.8 \rightarrow \therefore \mathrm{V_{GS1}} + V_{DsatCASC} + \mathrm{V_{CM}^*} \leq 0.6$

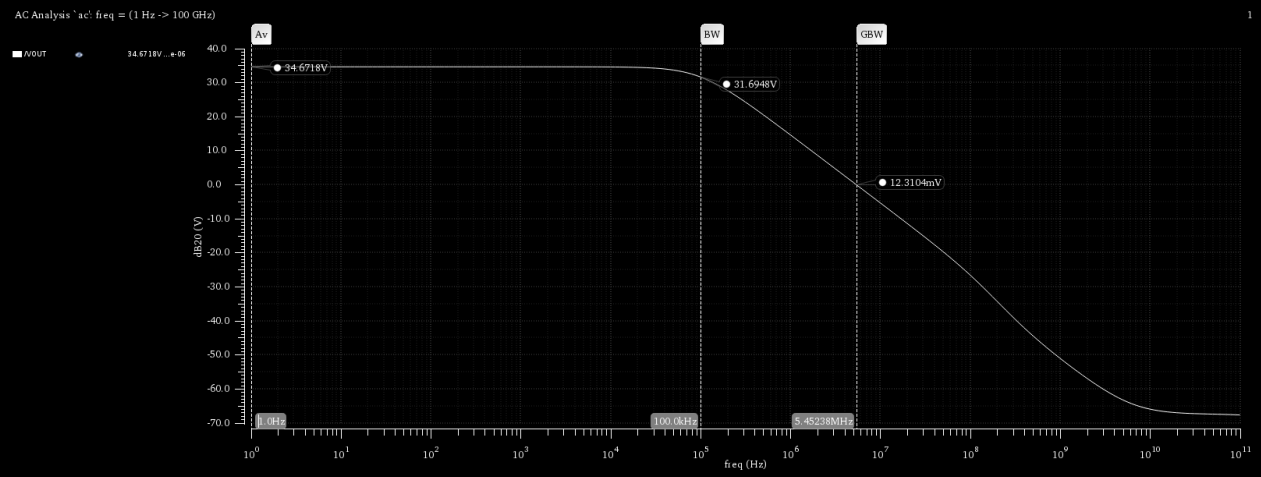
$V_{CASC}^* \leq 100\ mV \rightarrow \left.\frac{g_{m,CASC}}{I_D}\right|min = 10\ S/A$

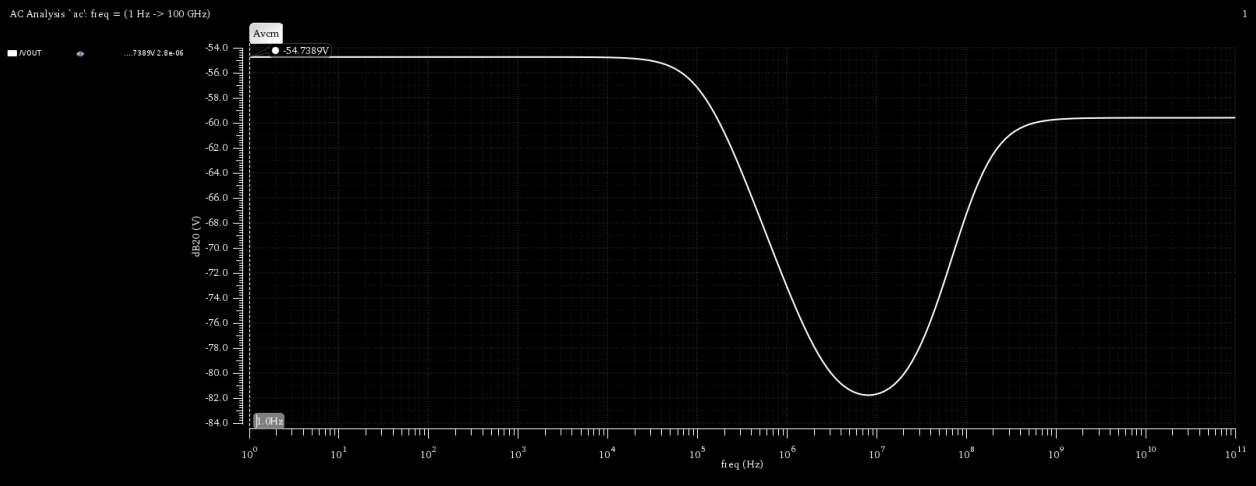
L1	1.8u	W1	14.75u
L2	840n	W2	6.76u
LCASC	120n	WCASC	470n
LCM	180n	WCM	2.8u

Simulations and Results








AC Analysis `ac': freq = (1 Hz -> 100 GHz)
1
/VOUT
....7389V 2.8e-06
Avcm
-54.7389V
-54.0
-56.0
-58.0
-60.0
-62.0
-64.0
-66.0
-68.0
-70.0
-72.0
-74.0
-76.0
-78.0
-80.0
-82.0
-84.0
dB20 (V)
1.0Hz
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^{10}
10^{11}
freq (Hz)