Analog Integrated Systems Design

Capacitive Digital-to-Analog Converter

Assignment No. 6

Lab Objective

1) To be able to model an op-amp with different types of imperfection.

2) To be familiar with the simulation and characterization of digital-to-analog converters.

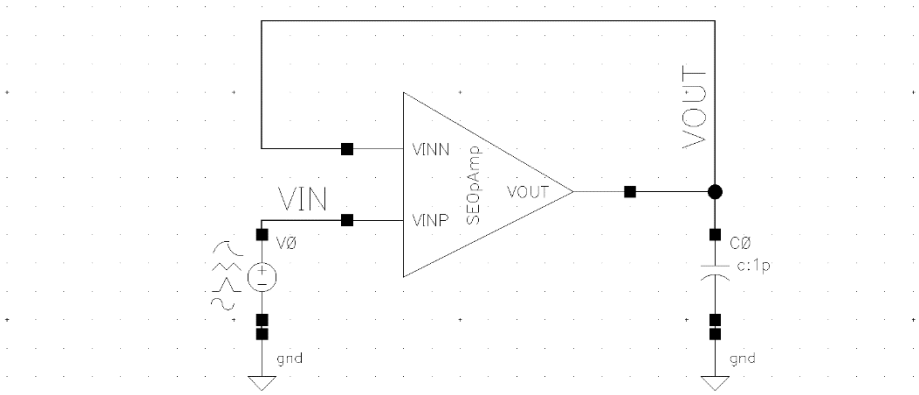
3) To be familiar with the operation of capacitive DACs.

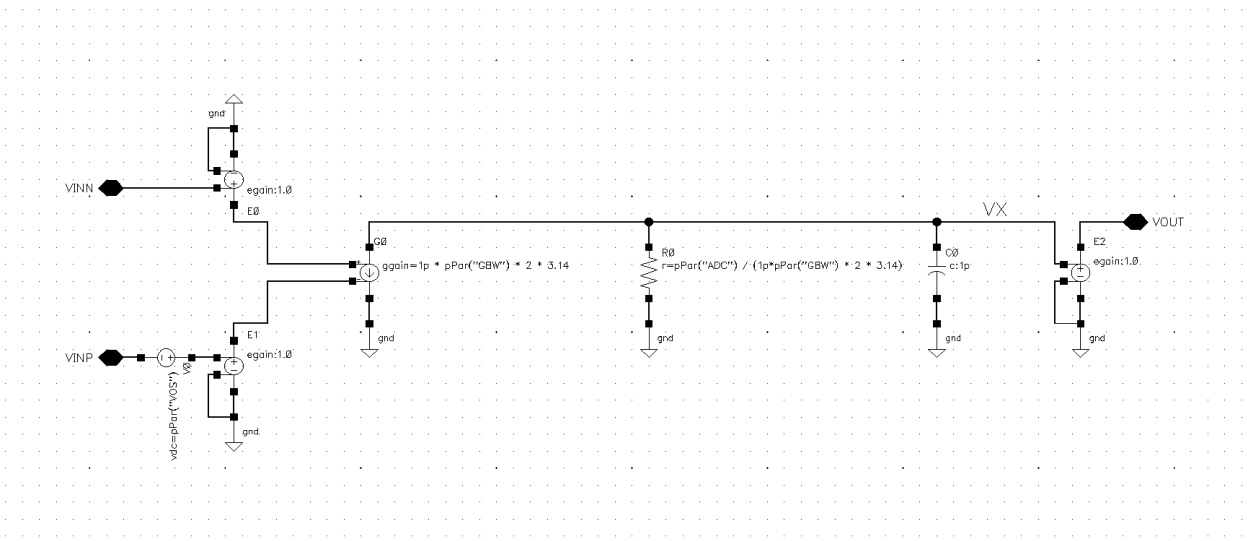
Apr. ١٦, 2022

Part 01 - Single-ended Output Op-amp Behavioral Model

1. Create the schematic shown below to model a single-ended output op-amp with finite gain, finite input range, finite output range, and finite GBW. Use vccs and vcvs from analogLib.
2. Create a simple testbench to verify your op-amp. An example testbench is shown below. Set the input as a sinusoidal signal (FIN, VDC, VPK). Run transient analysis for 4/VAR("FIN") conservative (four input cycles). You may develop more testbenches to verify input/output limiting, offset voltage, etc.

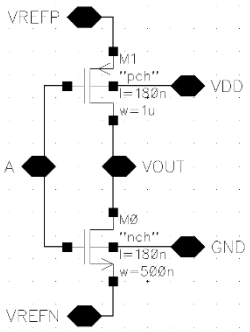
VDD	2	FIN	1k, GBW
VDC	VDD/2	VPK	VDD/4
VIN_Max	VDD – 0.2	VIN_Min	0.2
VOUT_Max	VDD – 0.2	VOUT_Min	0.2
ADC	1e5	GBW	10M
VOS	0		

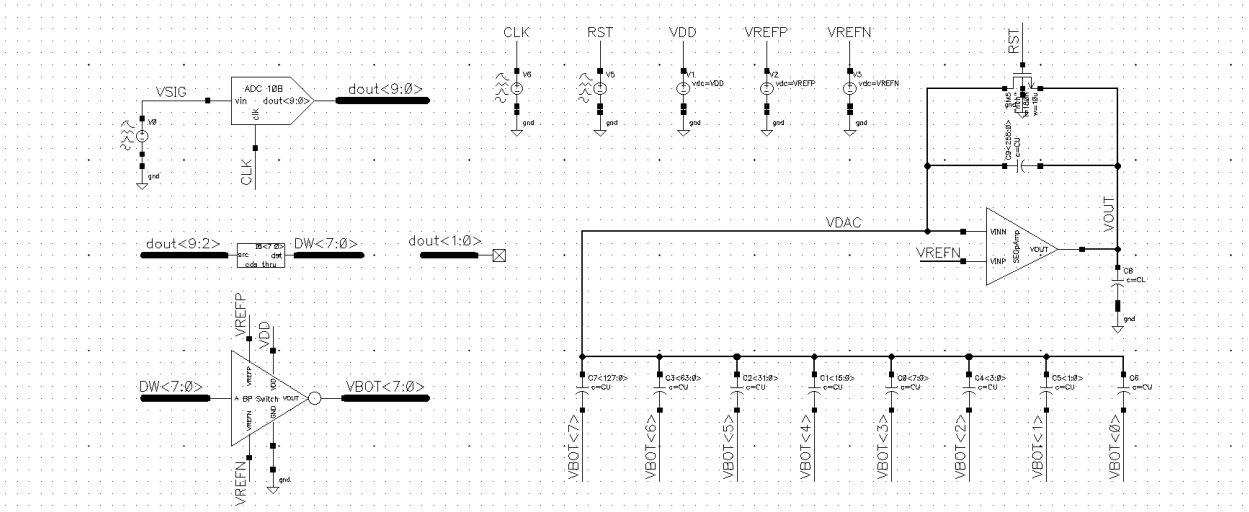


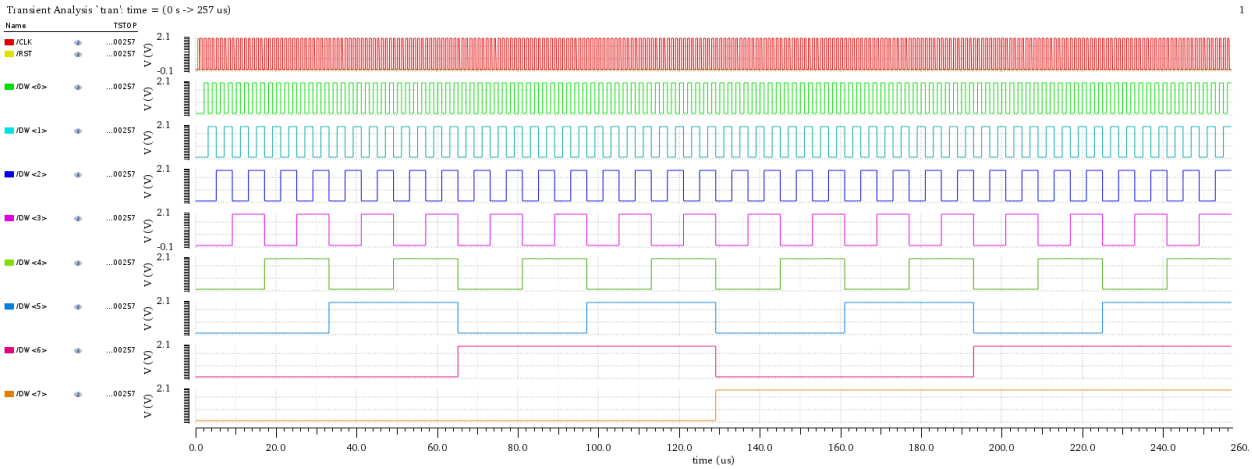


Part 02 - Capacitive DAC (Ramp Test)

1. Create a schematic for a bottom plate switch. It is similar to a digital inverter, but the bottom and top rails are defined by VREFN and VREFP instead of GND and VDD.
2. Create the schematic of the capacitive DAC shown below. Use cds_thru from basic library as a jumper to connect nets with different names. Use the Verilog-A ADC that you designed in Lab 02. Note that several elements of the schematic (including basic -> noConn) are defined as an array of elements. The feedback capacitance is also defined as an array of 2^N elements.







Transient Analysis `tran': time = (0 s -> 257 us)