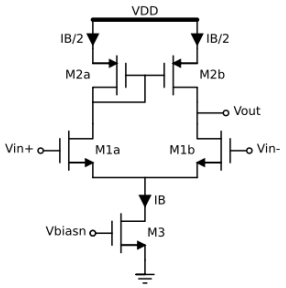
Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs.

Spec.		
Supply Voltage	1.2 V	
Open loop DC voltage gain	≥ 36 dB	
CMRR @ DC	≥ 50 dB	
BW	≥ 100 kHz	
Power Consumption	≤ 30 uW	
Reference current	10 uA	
Linear Range	90 mVpp	
Load	2 pF	

1. Design of input transistors

$$P_{cons} = V_{DD}\, I_{ss} \leq 30\ uW \rightarrow I_{ss} \leq 25\ uA$$

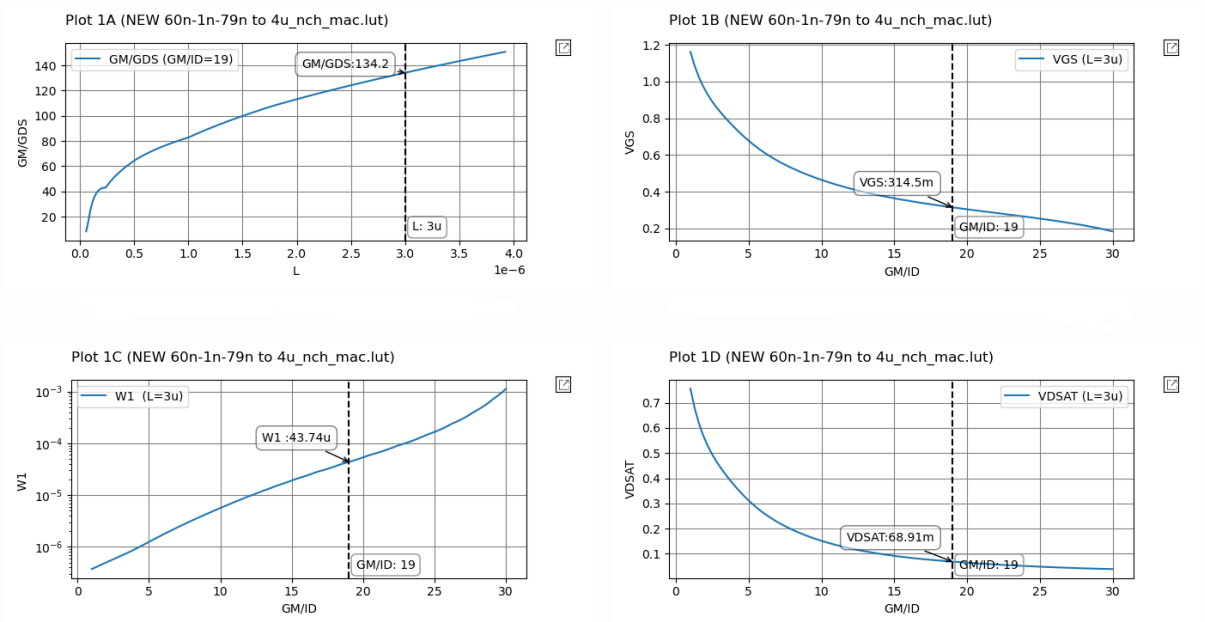
$$GBW = \frac{g_{m1}}{2\pi C_L} \geq 6.4\ MHz \rightarrow g_{m1} \geq 80.5\ uS \rightarrow \left(\frac{g_m}{I_D}\right)_1 \geq 6.44 \rightarrow \left(\frac{g_m}{I_D}\right)_1 = 19$$

$$g_m = 237.5\ uS$$

$$A_v = g_m R_{out} = 64 \rightarrow Rout = r_{o1} || r_{o2} = \frac{r_o}{2} \rightarrow r_o = 539\ k\Omega \rightarrow \left(\frac{g_m}{g_{ds}}\right)_1 \geq 128$$

$$L_1 = 3\ um, V_{GS1} = 314.5\ mV, W_1 = 43.74\ um, V_{Dsat1} = 68.91\ mV$$

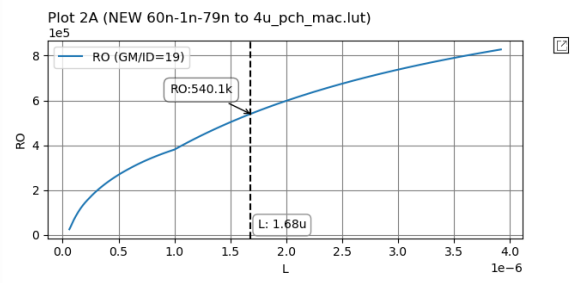
$$LR = 2\sqrt{2}\, V_{Dsat1} \rightarrow V_{Dsat1} \geq 32\ mV$$

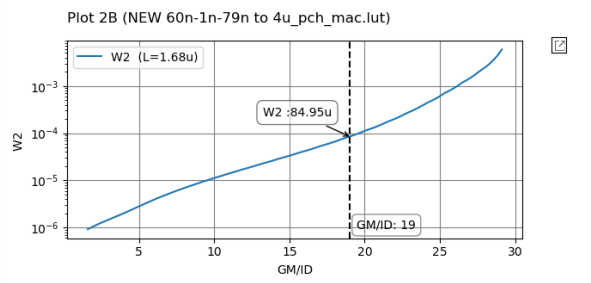


2. Diode connected load

$$r_{o2} = r_o = 539\ \text{k}\Omega, \text{assume } g_{m1} = g_{m2} = 237.5\ \text{us} \rightarrow \left(\frac{g_m}{g_{ds}}\right)_2 = 19$$

$$L_2 = 1.68\ \text{um}, W_2 = 84.95\text{u um}$$

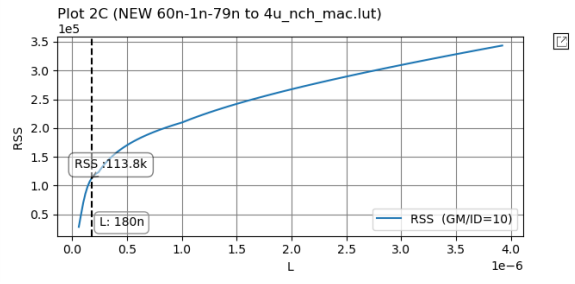


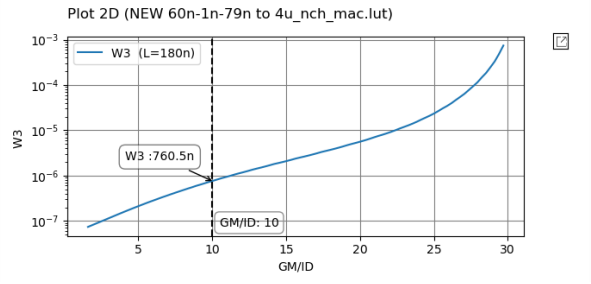


3. Current mirror

$$A_{VCM} = \frac{1}{2g_m R_{ss}} = (50 - 32)\ \text{dB} = 0.1995 \rightarrow R_{ss} = 10.6\ \text{k}\Omega$$

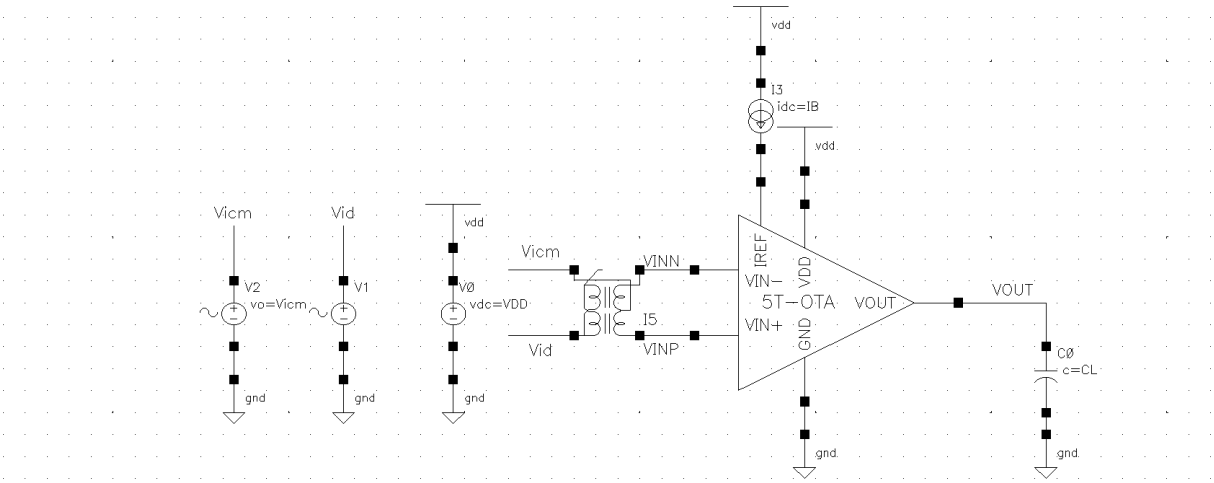
$$\text{Assume } M_3 \text{ biased in SI } (gmoverid = 10) \rightarrow L_3 = 180\ \text{nm}, W_3 = 760.5\ \text{nm}$$



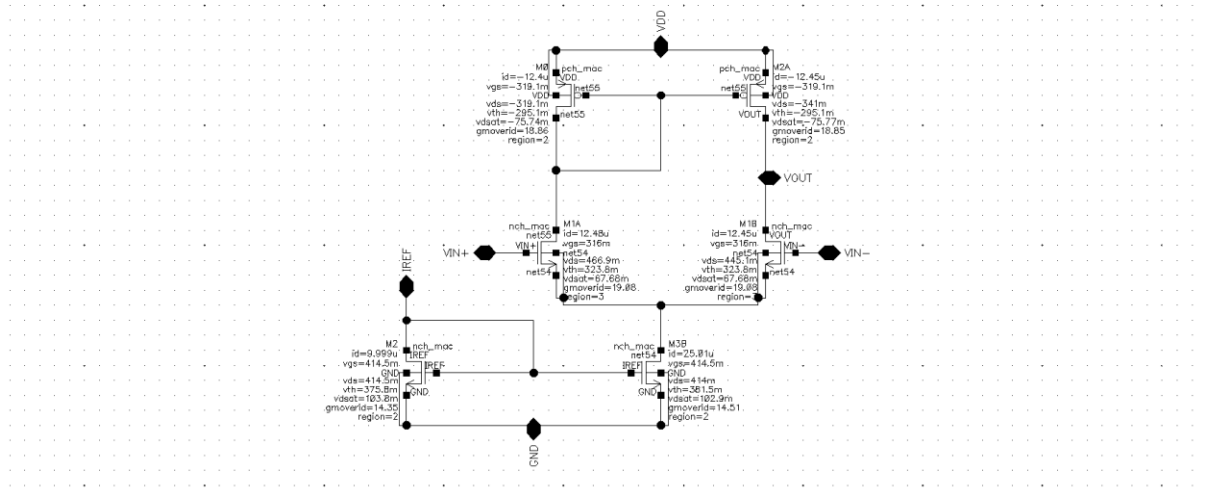


4. Simulation Results

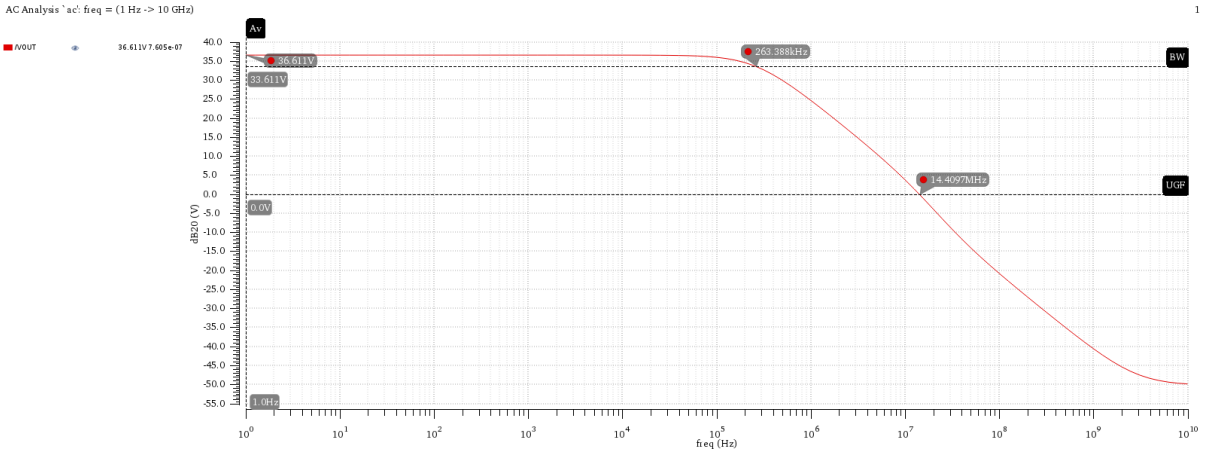
1. Circuit Test Bench



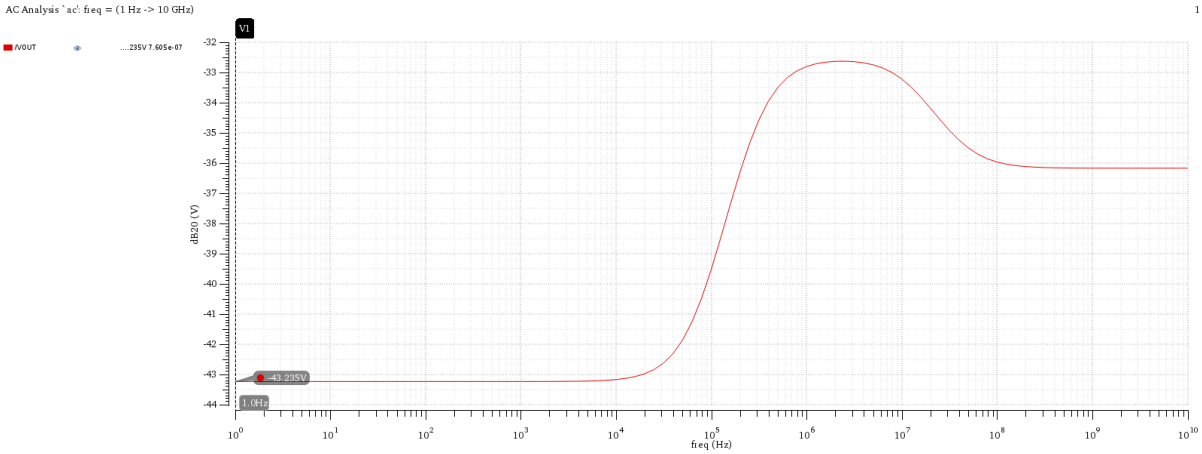
2. DC OP



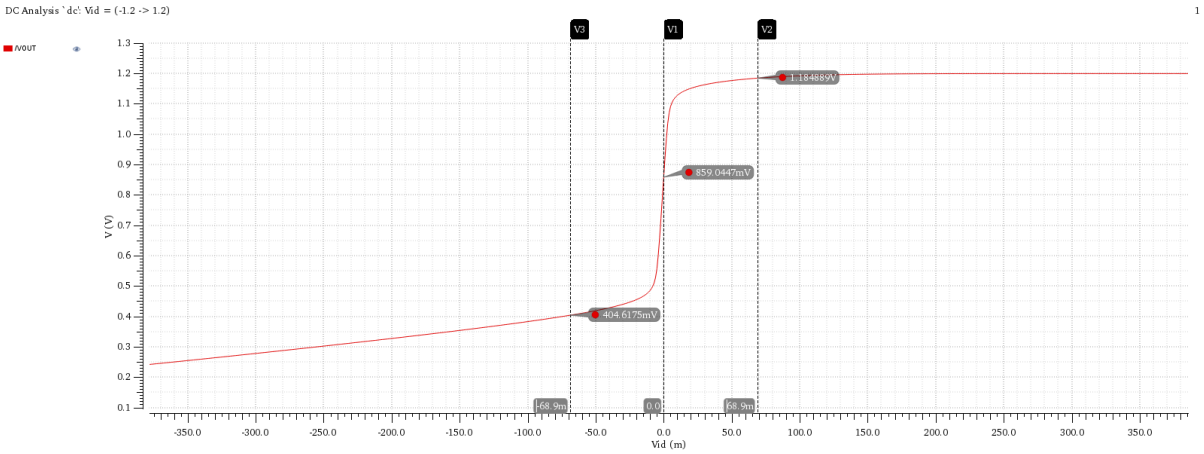
3. Diff Small Signal Analysis



4. CM Small Signal Analysis



5. Diff Large Signal



6. CM Large Signal