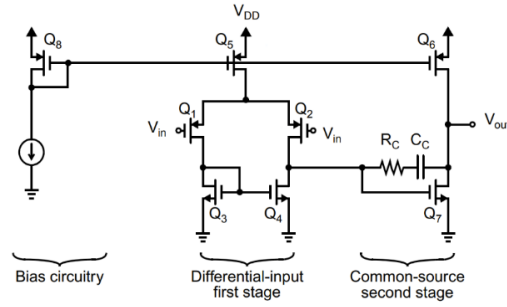


Design a Single Ended Two Stage Miller Compensated OTA meets the Specs (Use IREF = 10u)

Spec.	
DC Gain	$\geq 54$ dB
Unity Gain Frequency	$\geq 300$ MHz
Power Consumption	$\leq 1$ mW
Cap Load	1 pF

- Assume  $C_C = 0.5 C_L = 0.5$  pF
- Assume CMIR from 0.2  $\rightarrow$  0.6 V  $\rightarrow$  use PMOS input transistors
- Assign higher gain for the first stage  $A_V = A_{V1} \cdot A_{V2} = 28 * 18$



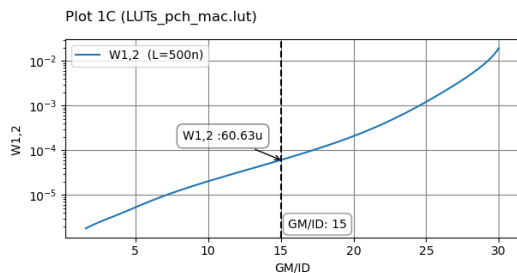
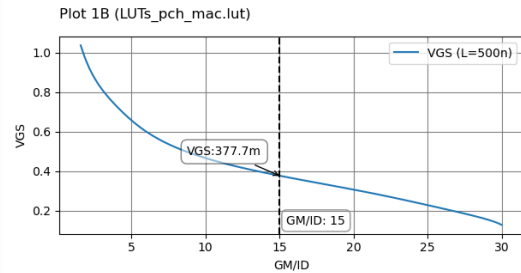
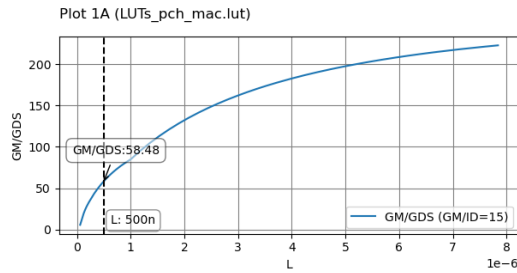
$$I_{\text{Cons,max}} = \frac{P_{\text{cons}}}{V_{\text{DD}}} \rightarrow I_{\text{Cons,max}} \leq 830 \text{ uA}$$

$$\text{UGF} = \frac{g_{m1,2}}{2\pi C_C} \geq 300 \text{ MHz} \rightarrow g_{m1,2} \geq 943 \text{ uS} \rightarrow g_{m1,2} = 1.2 \text{ mS}$$

$$\text{Assume } M_{1,2} \text{ in MI } \left( \frac{g_{m1,2}}{I_D} = 15 \right) \rightarrow I_{D1,2} = 80 \text{ uA} \rightarrow I_{B1} = 160 \text{ uA}$$

$$A_{V1} = \frac{g_{m1,2} r_{o2,4}}{2} (\text{Assume } r_{o2} = r_{o4}) \geq 28 \rightarrow r_{o2,4} = 47 \text{ k}\Omega \rightarrow (g_m r_o)_{1,2} = 56$$

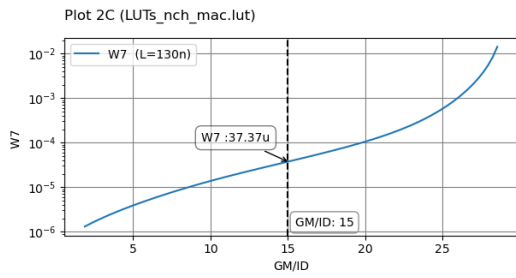
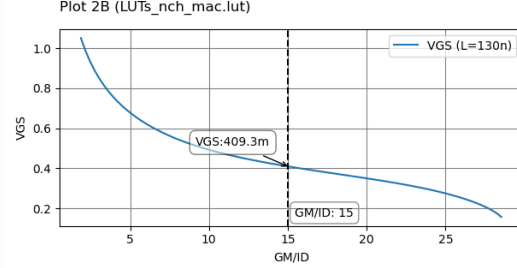
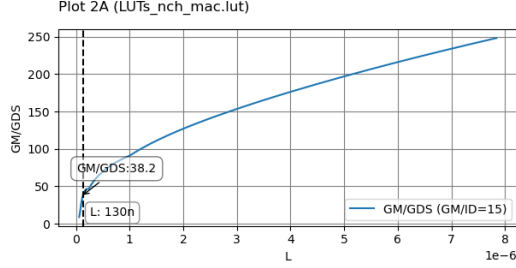
$$L_{1,2} = 500 \text{ nm}, V_{GS1,2} = 377.7 \text{ mV}, W_{1,2} = 60.63 \text{ um}$$



Choose  $\omega_{p2} = 4\omega_u \rightarrow g_{m7} = 8 g_{m1,2} = 9.6 \text{ mS} \rightarrow I_{B2} = 4I_{B1} = 640 \text{ uA}$

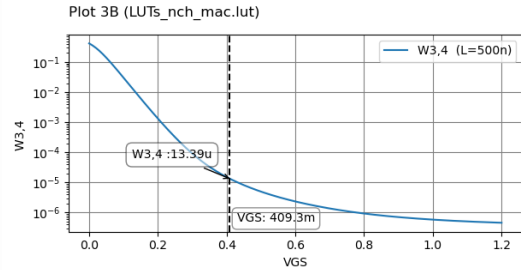
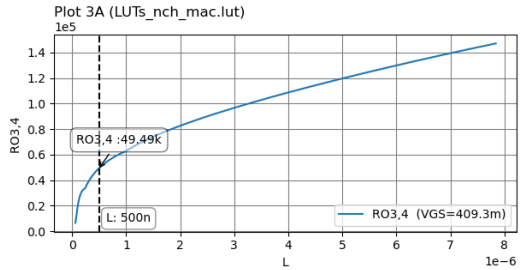
$A_{V2} = \frac{g_{m7} r_{o6,7}}{2} (\text{Assume } r_{o6} = r_{o7}) \geq 18 \rightarrow r_{o2,4} = 47 \text{ k}\Omega \rightarrow (g_m r_o)_7 = 32$

$L_7 = 130 \text{ nm}, V_{GS7} = 409.3 \text{ mV}, W_7 = 37.37 \text{ um}$



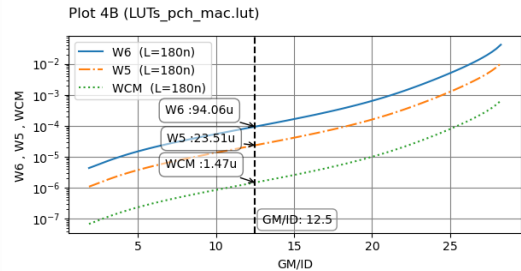
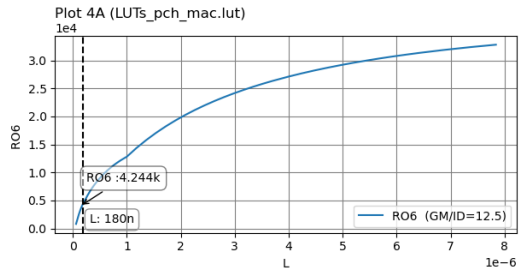
set  $V_{GS3,4} = V_{GS7} @ r_{o3,4} = 47 \text{ k}\Omega, I_D = 80 \text{ uA}$

$L_{3,4} = 500 \text{ nm}, W_{3,4} = 13.29 \text{ um}$



$CMIR_H = -V_{SG1,2} - V_5^* + V_{DD} = 0.6 \rightarrow V_5^* \leq 0.19 \text{ V} \rightarrow V_5^* = 0.16 \text{ V} \rightarrow \left(\frac{g_{m5}}{I_D}\right) = 12.5$

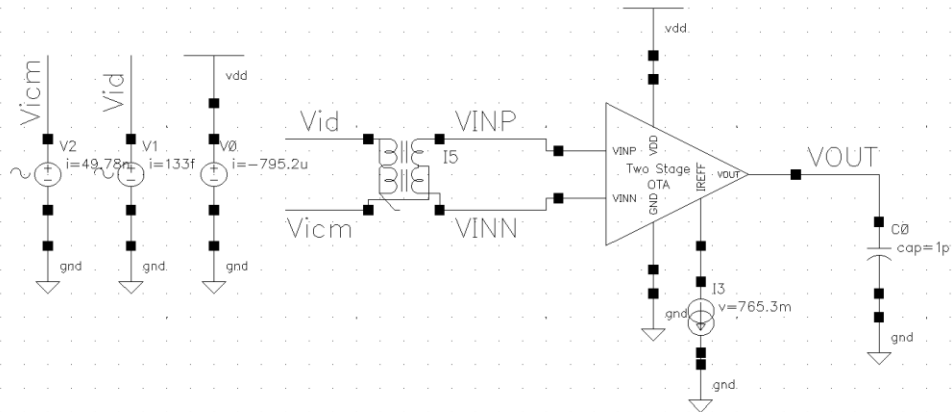
$L_{CM} = L_5 = L_6 = 180 \text{ nm}, W_{CM} = 1.47 \text{ um}, W_5 = 23.51 \text{ um}, W_6 = 94.06 \text{ um}$



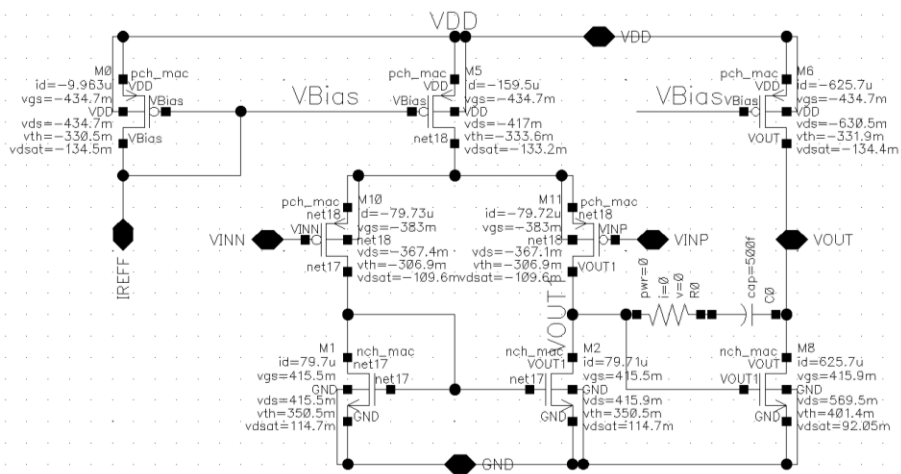
	M1	M2	M3	M4	M5	M6	M7	MCM
L	500n	500n	500n	500n	180n	180n	130n	180n
W	60.63u	60.63u	13.29u	13.29u	23.51u	94.06u	37.37u	1.47u

## Simulations Results

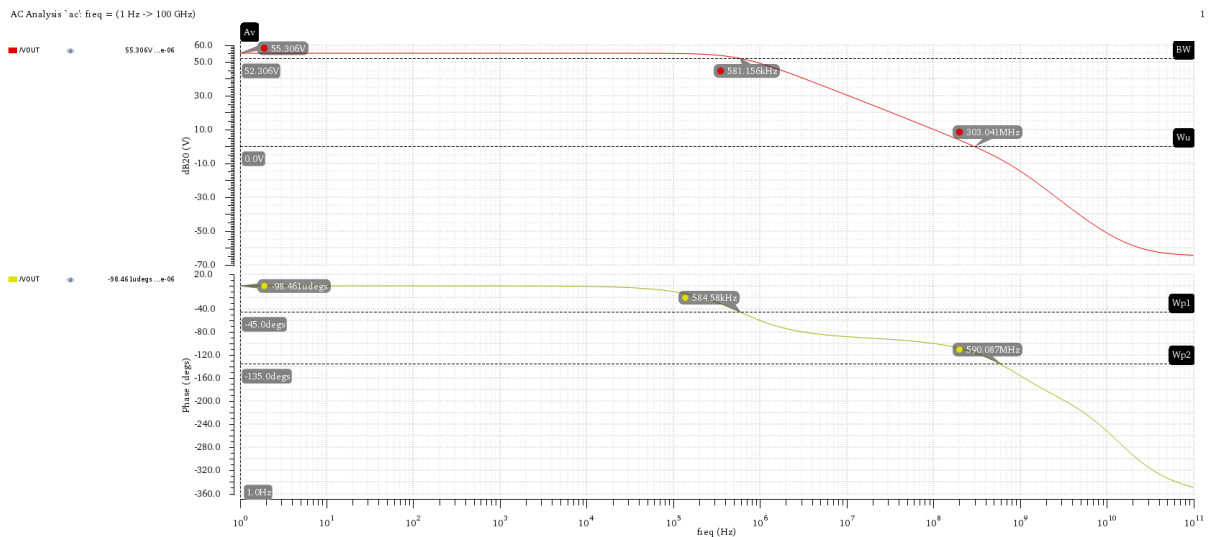
### - TB



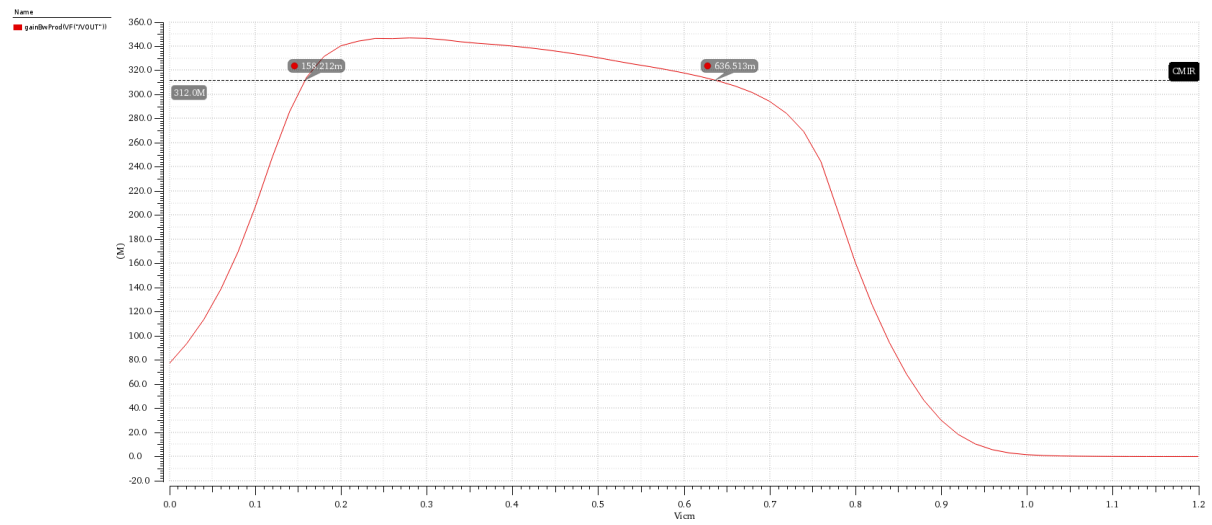
### - DC Operating Points



### - AC Analysis



## - CMIR Results



## - STB Analysis

