Design a Common Source Amplifier meets the following specs use PMOS input trans.

Spec.	
DC Gain	10 dB
BW	≥ 3 GHz
Power Consumption	≤ 1.2 mW
Cap Load	50 fF

$$P_{cons} = V_{DD}\, I_D \leq 1\ mW \rightarrow I_D \leq 1\ mA$$

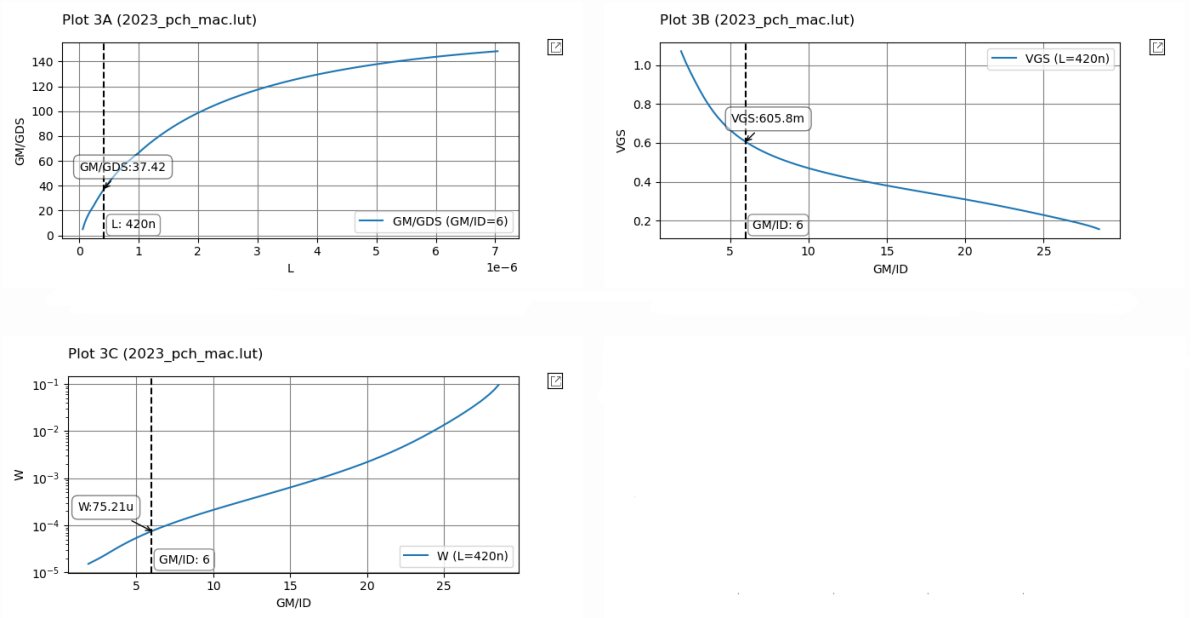
$$GBW = \frac{g_m}{2\pi C_{out}} \geq 3.2 * 3\ GHz \rightarrow g_m \geq 3.02\ mS$$

$$\text{Assume } V_{out} = \frac{V_{DD}}{2} = 0.6\ V \rightarrow R_D = \frac{0.6}{1\ mA} = 600\ \Omega \rightarrow R_{out} = 0.9\, R_D = 540\ \Omega$$

$$A_v = g_m R_{out} = 3.2 \rightarrow g_m = 6\ mS \rightarrow \frac{g_m}{I_D} = 6$$

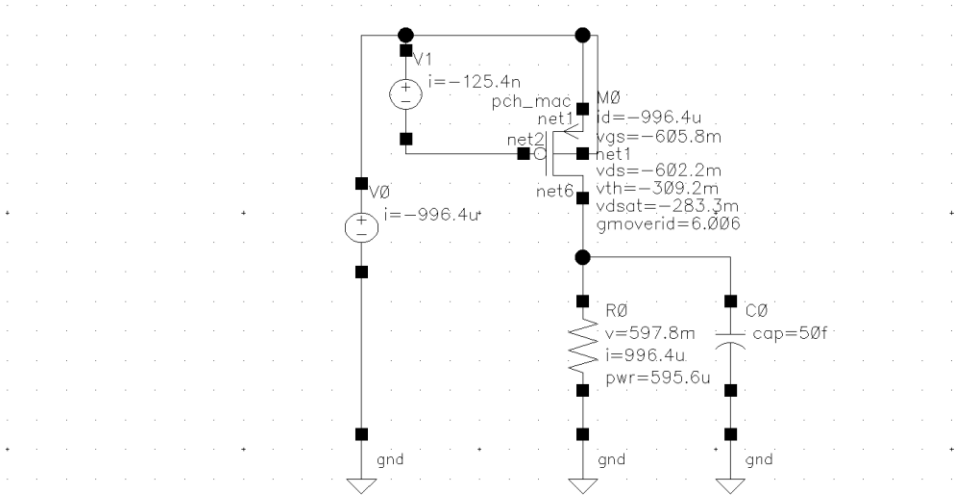
$$R_{out} = \frac{R_D . r_o}{R_D + r_o} = 540 \rightarrow r_o \geq 5400\ \Omega \rightarrow \frac{g_m}{g_{ds}} \geq 32.4$$

$$L = 420\ nm, V_{GS} = 605.8\ mV, W = 75.21\ um$$



Simulations Results

- DC Operating Points



- AC Analysis