

*Design a Degenerated CS Amplifier that meets the following specs*

Spec.	
DC Gain	6 dB
BW	$\geq 1$ GHz
Power Consumption	$\leq 0.4$ mW
Cap Load	100 fF

$$P_{\text{cons}} = V_{\text{DD}} I_D \leq 0.4 \text{ mW} \rightarrow I_D \leq 333 \text{ uA}$$

$$\text{GBW} = \frac{G_m}{2\pi C_{\text{out}}} \geq 2 * 1 \text{ GHz} \rightarrow G_m \geq 1.256 \text{ mS} \rightarrow G_m = 1.5 \text{ mS}$$

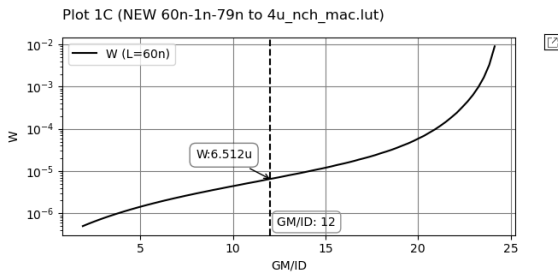
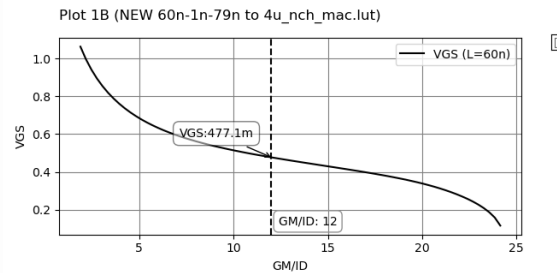
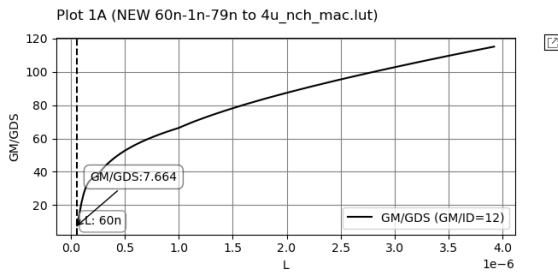
$$G_m = \frac{g_m}{1 + g_m R_S} = 1.5 \text{ mS} \rightarrow \text{Assume } \frac{g_m}{I_D} = 12 \text{ mS} \rightarrow g_m = 4 \text{ mS}$$

$$A_v = G_m R_{\text{out}} = 2 \rightarrow R_{\text{out}} = R_D || r_o(1 + g_m R_S) = 1.34 \text{ k}\Omega \rightarrow R_D = 1.82 \text{ k}\Omega$$

$$r_o = 1906 \text{ }\Omega \rightarrow R_S = 417 \text{ }\Omega \rightarrow \frac{g_m}{g_{ds}} \geq 7.62$$

$$V_{\text{DS}} = 1.2 - 330\text{u} * 1.82\text{k} - 330\text{u} * 417 = 0.46 \text{ V}$$

$$V_{\text{SB}} = 0.1375 \text{ V}$$



The diagram shows a common source amplifier circuit. The input signal  $V_{in}$  is applied to the gate of the NMOS transistor  $M0$ . The source of  $M0$  is connected to ground through a resistor  $R1$  (419.5  $\Omega$ ). The drain of  $M0$  is connected to  $V_{dd}$  through a resistor  $R0$  (1.835 k $\Omega$ ). The output voltage  $V_{out}$  is taken from the drain of  $M0$ . A load capacitor  $C0$  (100 fF) is connected between the output and ground. The circuit is biased with a DC current source  $I_{bias}$  (1.468 nA) connected to the gate of  $M0$  and the source of  $M0$  through a resistor  $R2$  (1.835 k $\Omega$ ). The gate of  $M0$  is also connected to  $V_{dd}$  through a resistor  $R3$  (1.835 k $\Omega$ ). The output voltage  $V_{out}$  is shown as a waveform.