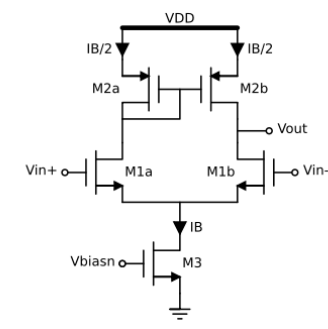Use gm/ID methodology to design a diff input SE output operational transconductance amplifier (OTA) that achieves the following specs.

| Spec.		
Supply Voltage	1.2 V	
Open loop DC voltage gain	$\geq$ 32 dB	
CMRR @ DC	$\geq$ 70 dB	
BW	$\geq$ 200 kHz	
Phase Margin	$\geq$ 70º	
Power Consumption	$\leq$ 30 uW	
Reference current	10 uA	
CM input range low	$\leq$ 0.6 V	
CM input range high	$\geq$ 1 V	
Load	2 pF	

1. As CMIR : 0.6 to 1v is closer to VDD, I used a NMOS input transistors

2. Design of input transistors

$$P_{cons} = V_{DD}\, I_{ss} \leq 30\ uW \rightarrow I_{ss} \leq 20\ uA$$

$$GBW = \frac{g_{m1}}{2\pi C_L} \geq 8\ MHz \rightarrow g_{m1} \geq 100.5\ uS \rightarrow g_m = 120\ uS \rightarrow \frac{g_m}{I_D} = 12$$

$$A_v = g_m R_{out} = 40 \rightarrow R_{out} = 335\ k\Omega \rightarrow Rout = r_{o1}||r_{o2} = \frac{r_o}{2} \rightarrow r_o = 670\ k\Omega$$
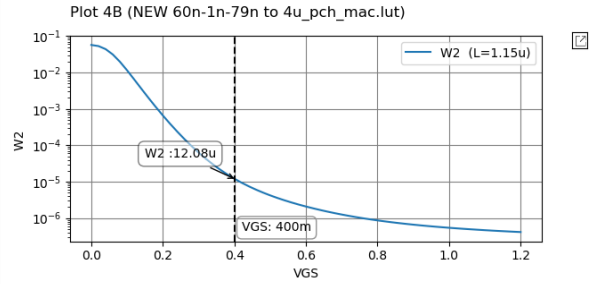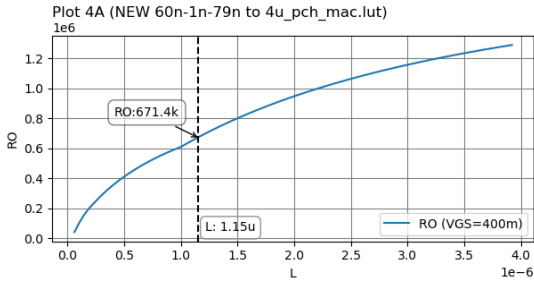
$$L_1 = 2.2\ um,\ V_{GS1} = 418.1\ mV,\ W_1 = 5.63\ um$$
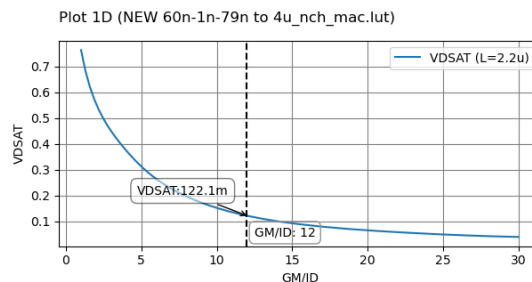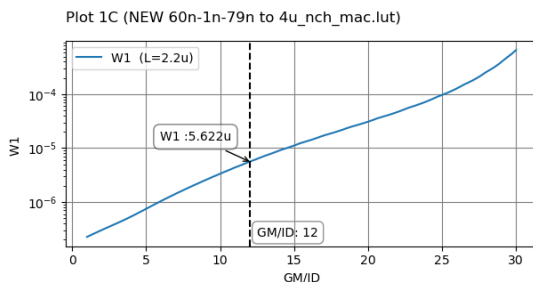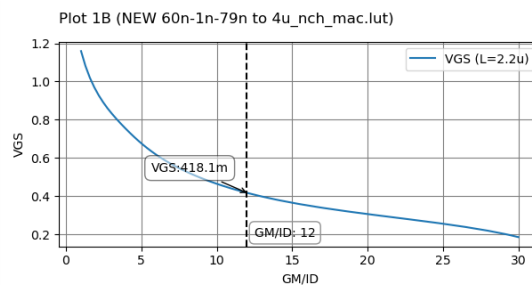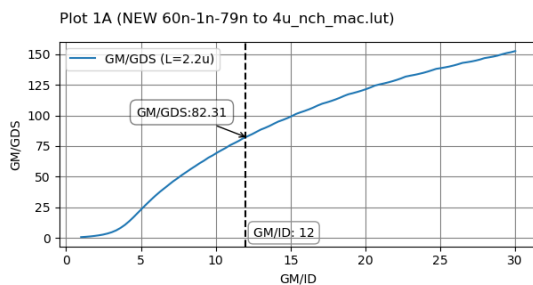
3. Diode connected load

$$\text{CMIR}_H \geq 1 \rightarrow V_{GS1} - V_1^* - V_{SG2} + V_{DD} \geq 1 \rightarrow V_{SG2} \leq 452\text{m}$$

$$V_{SG2} = 400\text{m and } r_{o2} = 670 \text{ k}\Omega \rightarrow L_2 = 1.15 \text{ um}, W_2 = 12.08 \text{ um}$$

Plot 4A (NEW 60n-1n-79n to 4u_pch_mac.lut)

Plot 4B (NEW 60n-1n-79n to 4u_pch_mac.lut)

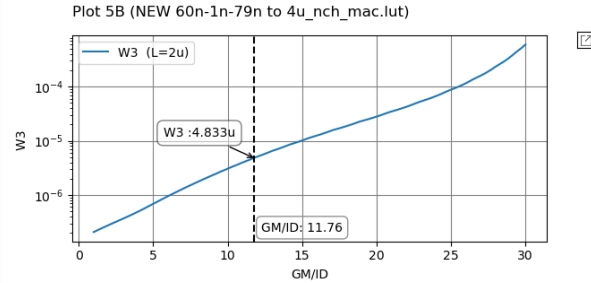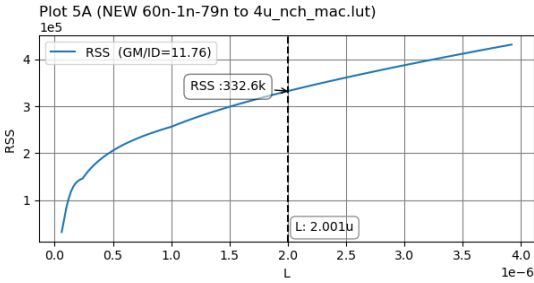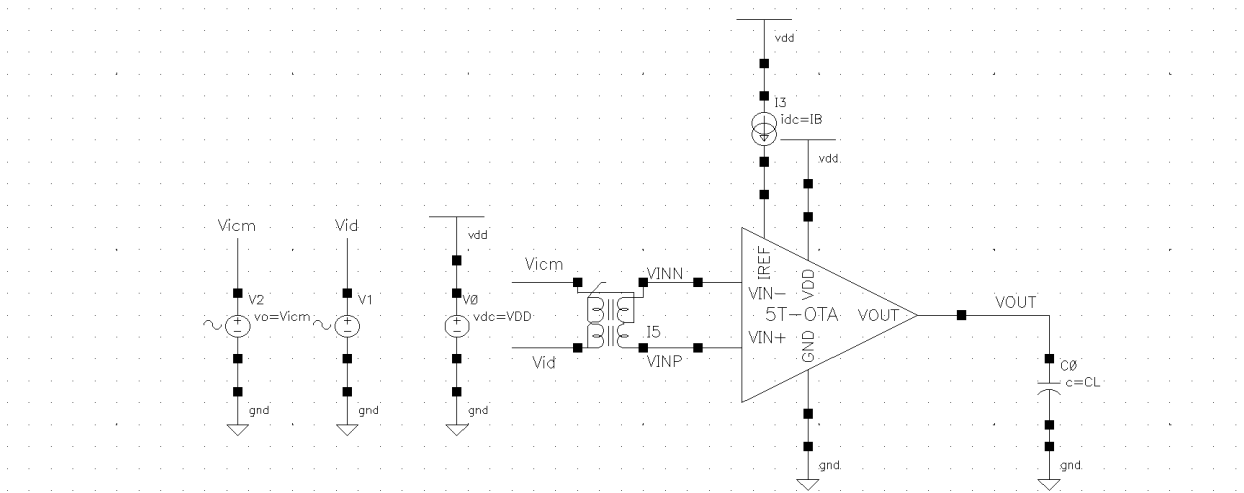4. Current mirror

$$A_{VCM} = \frac{1}{2g_m R_{ss}} = (70 - 32) \text{ dB} = 0.01259 \rightarrow R_{ss} = 331 \text{ k}\Omega$$

$$\text{CMIR}_L < 0.6 \rightarrow V_{GS1} + V_3^* \leq 0.6 \rightarrow V_3^* \leq 0.189 \rightarrow V_3^* = 0.17 \rightarrow \left(\frac{g_m}{I_D}\right)_3 = 11.76$$
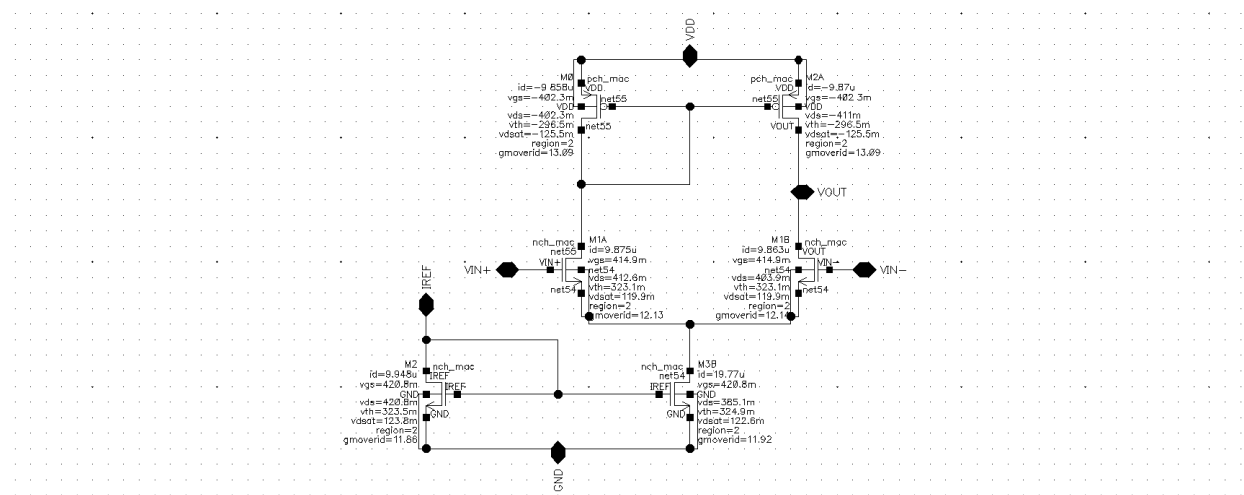
$$L_3 = 2 \text{ um}, W_2 = 4.833 \text{ um}$$

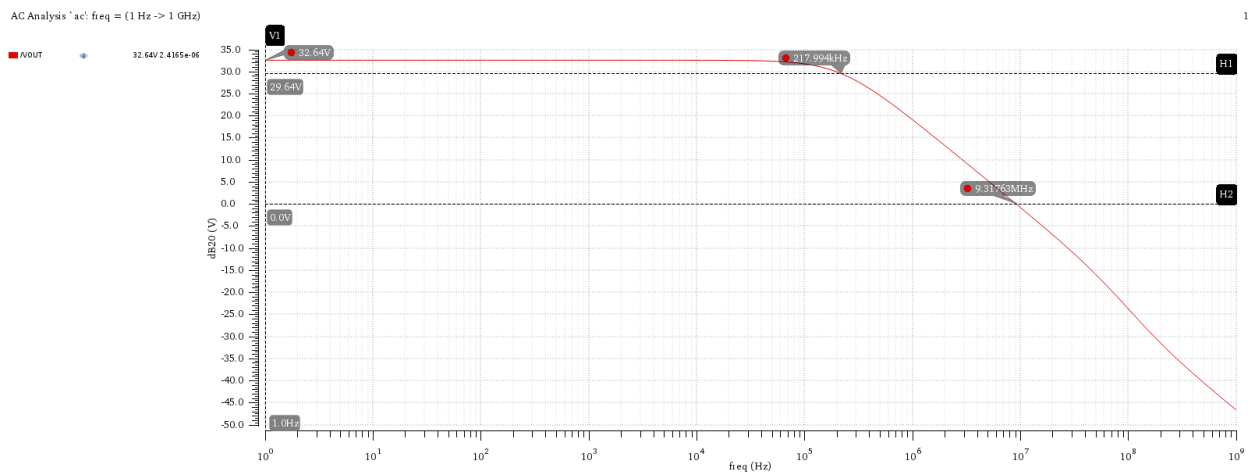Plot 5A (NEW 60n-1n-79n to 4u_nch_mac.lut)

Plot 5B (NEW 60n-1n-79n to 4u_nch_mac.lut)

1. Circuit Test Bench
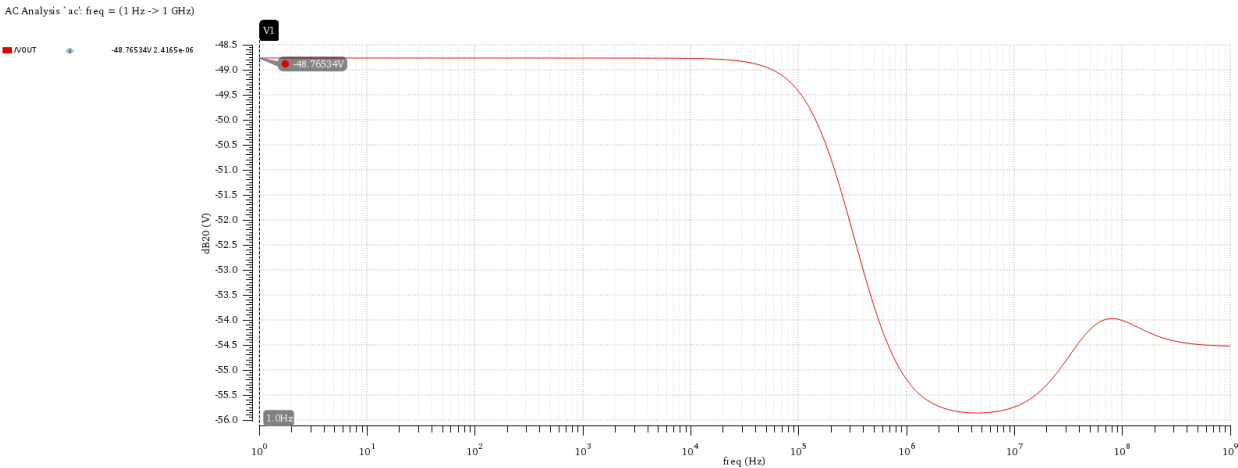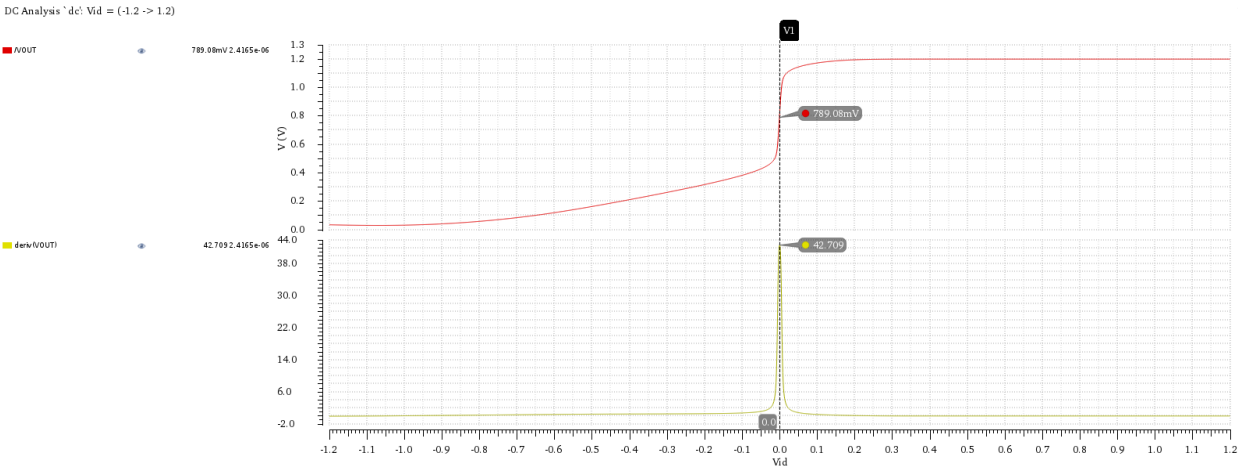

2. DC OP

3. Diff Small Signal Analysis

4. CM Small Signal Analysis

5. Diff Large Signal

6. CM Large Signal

gainBwProd(VF("/VOUT"))   1