Chapter 2

DATA CONVERTERS SPECIFICATIONS

Using or designing a data converter requires a proper under-standing of specifications. They provide general informations and describe the features and the limits of static and dynamic operation of data converters. The material of this chapter will provide a basis for evaluating and comparing existing devices, and for giving a guide for writing specifications of new devices. Moreover, the Chapter facilitates identifying technical requisites of data converters used in integrated systems.

The chapter deals only with the definitions of technical terms used in manufacturer-supplied specifications and clarify the ter-minology used. Testing methods for measuring the specification parameters are topic of a successive specific Chapter.

2.1 TYPE OF CONVERTER

The first specification defining a data converter concerns the type. The con-version algorithm normally provides this kind of information. For example, we have flash, sub-ranging, or sigma-delta converters. Various types of converters are classified into two main categories: Nyquist-rate and oversampling. The
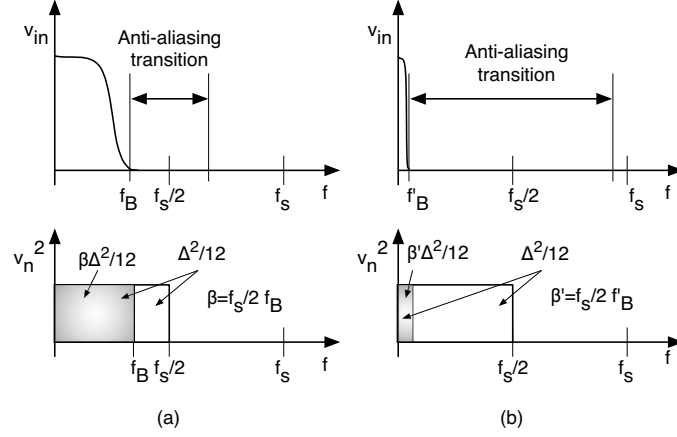
Fig. 2.1 - Comparing a Nyquist-rate and (a) an oversampling (b) strategies.

two categories correspond to one of the following design strategies: using a large fraction of the bandwidth available or having the input-band occupying a small part of the Nyquist range. The ratio between Nyquist limit and signal band, $f_s/2f_B$, is called *oversampling ratio* (*OSR*). The oversampling type categorizes converters with large *OSR*. Nyquist-rate converters have a small *OSR*, typically less than *8*.

We have seen that a large oversampling benefits the anti-aliasing design. The wide transition between pass-band and stop-band (Fig. 2.1) permits using low-order filters. In addition to this first advantage the anti-aliasing filter oversampling can improve the signal-to-noise ratio (*SNR*). The issue will be discussed in detail shortly. Here, we just observe that only a fraction $\beta = 2f_B/f_s$ of the $\Delta^2/12$ quantization noise power lies in the signal-band. Therefore, after the *A/D* conversion the portion of noise outside of the band of interest can be rejected. This would improve the *SNR* and, in turn, increase the equivalent number of bit.

2.2   CONDITIONS OF OPERATION

The features of data converters strongly depend on the experimental set-up. Before discussing about the data converter specifications, it is useful to examine how the operation environment possibly influences the data converter performances.

Two important conditions of use are supply voltage and temperature. A data-converter must comply with the requirements not only at the nominal voltage and at room temperature but also within given ranges of variation. The

supply voltage can fluctuate by ±5%; the temperature can change from *-20°C* to *85°C* (consumer applications) or *-55°C* to *125°C* (military applications). Specifications in a restricted range of supply voltage or temperature don't proper depict the on-field use. Keeping the performances over a wide range of supply voltage or temperature is difficult especially at high resolution. For example, a *14 bit* converter requires accuracies as good as *600 ppm/V* (*5 V* supply) or *0.3 ppm/°C* (consumer applications).

When measuring or using a data converter it is important to ensure that the printed circuit board (*PCB*) does not hamper results. Power supply couplings and poor ground connections are critical issues. Often high performance data-converters use separate pins for analog and digital supplies. The pins are connected together on the *PCB* to a single supply generator. The method is suitable for a proper spur rejection. However, the impedance in the pin path can lead to poor V_{DD} or ground terminations. The length of connecting lead must be as short as possible: the lead is equivalent to an inductor. Ground loops between two sides of the *PCB*, especially at *RF* frequencies must be carefully avoided. Multi-layer boards with separate ground and power planes are normally required to ensure a high level signal integrity.

> **KEEP NOTE**
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> The operational conditions of data converters are key for achieving (or measuring) specifications. Inaccurate set-up or *PCB* can totally mask excellent performances of a device.

Other important connection are the master clock and reference voltages. We know that the clock jitter degrades performances. It is therefore necessary to have low jitter not only at the output of the signal generator but also at the input pin. The *PCB* traces leading the clock must be short with a solid ground plane underneath. This forms a microstrip transmission line and enables impedance matching. When low-speed data converters use external references it is necessary to utilize a clean voltage generator which output impedance is low enough to avoid fluctuations within *1 LSB*. This is not easy: the discrete-time operation of the data-converter drains pulses of current out of the reference generator.

Often, to avoid ambiguity, some manufactures specify the condition of operation by providing evaluation boards and by giving detailed user guidelines explaining the evaluation procedures.

2.3 CONVERTER SPECIFICATIONS

A large set of specifications describes the performances of data converters. Specifications make it easier to interpret and understand the material in Catalogues and facilitate the use and characterization of products. The specifications are divided in the following categories:

- General features.
- Static specifications.
- Dynamic specifications.
- Digital and switching specifications.

2.3.1 General Features

Most of the general features of data converters are obvious or self-explaining. However, for some of them it is worth recalling the definition.

Type of Analog Input: The input of a data converter can be single-ended, pseudo-differential or differential. Single-ended inputs are referred to a common ground that is connected to the analog ground of the converter. Pseudo-differential inputs are symmetrical with respect to a fixed reference voltage. that can differ from the analog ground of the converter. Differential inputs are not necessarily symmetrical with respect to a fixed level. Signals are the difference between the inputs or outputs regardless of the common mode value.

Resolution: it is the number of bits that the *ADC* uses to represent the analog input. The resolution, together with the reference voltage determines the minimum detectable voltage: the quantization step.

Dynamic range: it is the ratio between the largest signal level the converter can handle to the noise level, expressed in *dB*. The dynamic range determines the maximum *SNR*.

Absolute maximum ratings: they are the limiting values to be used, and beyond which the service capability of the circuit may be impaired. The functional operation is not necessarily affected. However, exposure to absolute maximum rating conditions for an extended period of time influences the device reliability. Maximum ratings are divided into two categories: electrical and environmental. The environmental category includes the operating temperature range, the maximum chip temperature, the lead temperature and the maximum soldering time, the storage temperature range and, for airborne system applications, the vibration range.

ESD (electrostatic discharge) notice: all the *IC* are sensitive to high electrostatic high-voltage. The human body and test equipment can electrostatic charge at voltages as high as *4000 V* and discharge through the device. All the *IC*s feature protection circuitry; however, permanent damage may occur because of high-energy electrostatic shocks, Manufacturers always recommend proper *ESD* precautions to avoid loss of functionality.

Pin function descriptions and pin configuration: a table with the number of pin, the name and the performed function is provided with the specifications. Moreover, a drawing of the package provides the pin configuration.
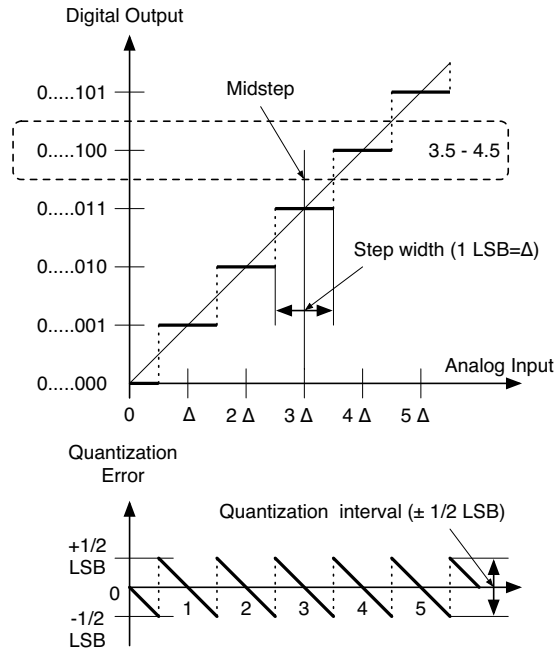
Fig. 2.2 - Ideal input-output transfer function of an A/D converter.

Warm-up time: it is the amount of time recommended for stabilize the performances after the converter has been powered up. The parameter accounts for the change of performances due to the temperature transient after powering the converter.

2.3.2 Static Specifications

The input-output transfer characteristic depicts the static behaviour of a data converter. For an ideal case the input-output characteristic is a staircase with uniform steps over the entire dynamic range. Fig. 2.2, plots the initial part for a generic number of bit. The digital output codifies analog quantization intervals symmetrical with respect to multiples of Δ. Consequently, the first code *0...000* represents only half quantization interval. Even the last code represents half quantization step. Therefore, for obtaining 2^n interval the full scale range is divided by 2^n-*1* instead of 2^n to have Δ. Fig. 2.2 outlines that a quantization interval can be codified using both digital code or midstep point (*0...011* or *3Δ*). Also, Fig. 2.2 shows the quantization error. As known, the quantization error ranges between $\pm\Delta/2$ and is equal to zero at the midstep.

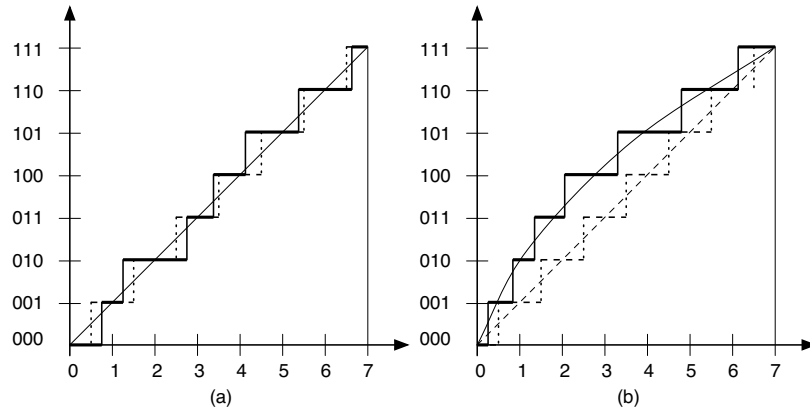Deviations from the ideal transfer characteristic produce results like the ones

Fig. 2.3 - Input-output transfer characteristic of a real data converter.

shown in Fig. 2.3. The curve of Fig. 2.3 a) shows an almost random variation of the quantization intervals. There is no correlation between successive errors and the interpolating curve is a straight line running from the origin to the full scale. The characteristics of Fig. 2.3 b) displays small quantization intervals at the beginning and large quantization interval at the end of the curve. As a result, the interpolating line get away from the straight line leading to a distorted response. These features are quantified by the *INL* and *DNL*, two of the static specifications defined below.

Resolution: it is the smallest analog increment corresponding to a *1 LSB* code change. For example, the resolution of a *16-bit* converter with $X_{FS} = 1$ is $15.26 \cdot 10^{-6} = 15.26 \ \mu$.

Analog Input Range: it is the single ended or differential peak-to-peak signal (voltage or current) that must be applied to the converter to generate a full-scale response. A peak differential signal is the signal on a single terminal and subtracted to the signal from the other terminal, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference between both peak measurements gives the peak-to-peak differential.

Offset: the offset describes a shift for zero input. Offset is an error that affects either the *ADC* and the *DAC*. Fig. 2.4 a) shows the input-output transfer characteristics for a real and an ideal *ADC*. The offset changes the transfer characteristics so that all the quantization steps are shifted by the *ADC offset*. The offset affecting a *DAC* is defined by using the real response depicted in Fig. 2.4 b). It is not a perfect straight line. Moreover, the interpolating line does not start from *0* but from the offset: the analog signal generated by the digital code *0…0000* defines the *DAC offset*.
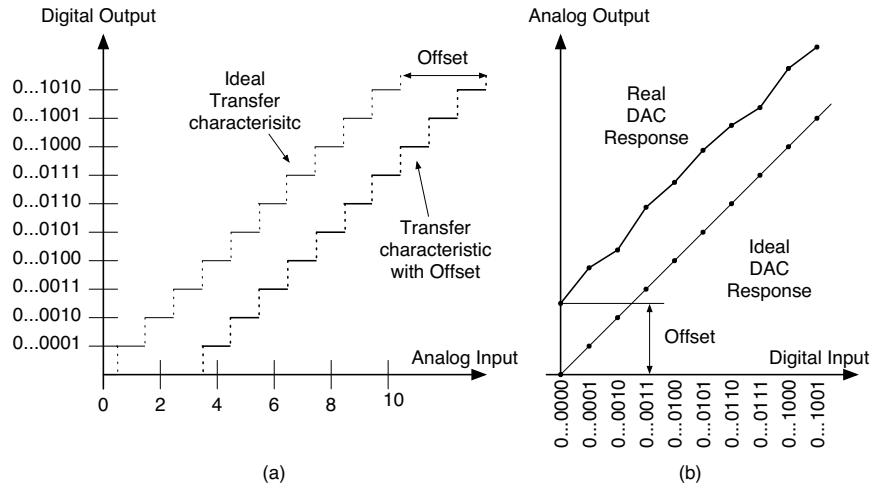
Fig. 2.4 - Offset error for an analog-to-digital (a) and a digital-to-analog (b) converter

The offset error is measured in *LSB*, absolute value (*volt or ampere*), percent or *ppm* of the full scale.

Gain error: it is the error on the slope of the straight line interpolating the transfer curve. For an ideal converter the slope is D_{FS}/X_{FS}, where D_{FS} and X_{FS} are the full scale digital code and full scale analog respectively. Since D_{FS} represents X_{FS}, we normally say that the ideal slope is one. The gain error defines the deviation of the slope of a data converter from the expected value. Fig. 2.5 shows the input-output diagrams for a real and an ideal *ADC* (a) and *DAC* (b).
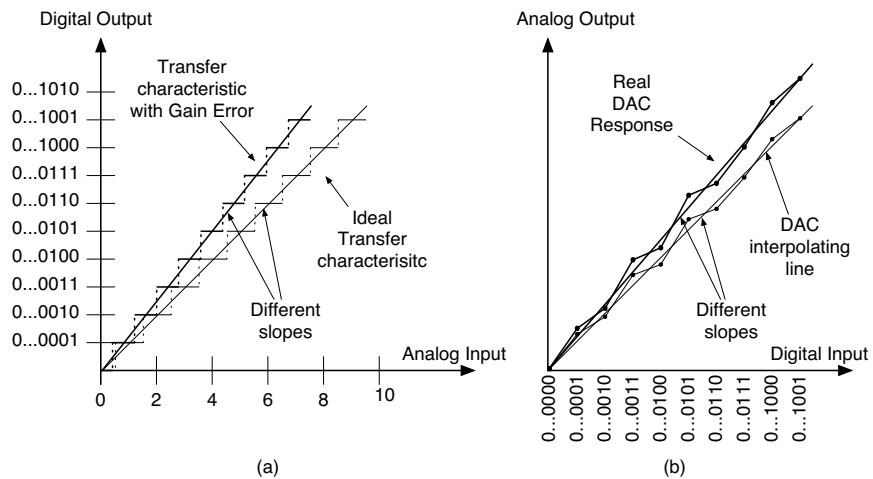
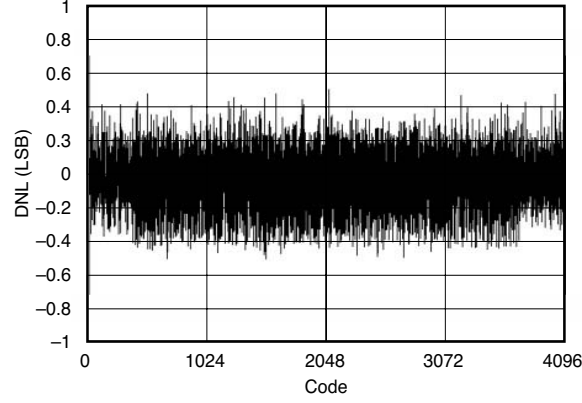**Fig. 2.5** - Gain error for an analog-to-digital (a) and a digital-to-analog (b) converter

Fig. 2.6 - Differential non-linearity error (*DNL*).

Another measure of the gain error is given by the difference between the input voltage causing a transition to the full scale and the reference (minus half *LSB*). When using this definition the gain error is named full scale error.

Differential non-linearity error (DNL): it is the diagram representing the deviation of the step size of a real data converter from the ideal code bin width Δ. Assuming that X_k is the transition point between successive codes *k-1* and *k*, the width of code bin *k* is $\Delta_r(k) = (X_{k+1}-X_k)$; the differential non-linearity is

$$DNL(k) = \frac{\Delta_r(k) - \Delta}{\Delta} \ . \tag{2.1}$$

The function is also called differential linearity error (*DLE*). Fig. 2.6 shows an example of *DNL* of a *12-bit ADC*. The diagram is within a ± *0.5 LSB* interval over the entire dynamic range. Fig. 2.6 measures the *DNL* in *LSB*. The DNL can be also measured in *Volt* (or *Ampere* when the input is a current) or as percent of *p.p.m.* of the full scale.

The maximum differential nonlinearity is the maximum of *|DNL(k)|* for all *k*. Often the maximum of the *DNL* is simply referred to as *DNL*. An additional specification given by some data sheet is the *RMS* of the *DNL*

$$DNL_{RMS} = \left(\frac{1}{2^N - 2} \sum_{k=1}^{2^N - 2} \{DNL(k)\}^2 \right)^{1/2} \tag{2.2}$$

Monotonicity: it is the feature of an *ADC* that produces output codes that are consistently increasing with increasing input signal and consistently decreasing with decreasing input signal. Therefore, the output code always remains
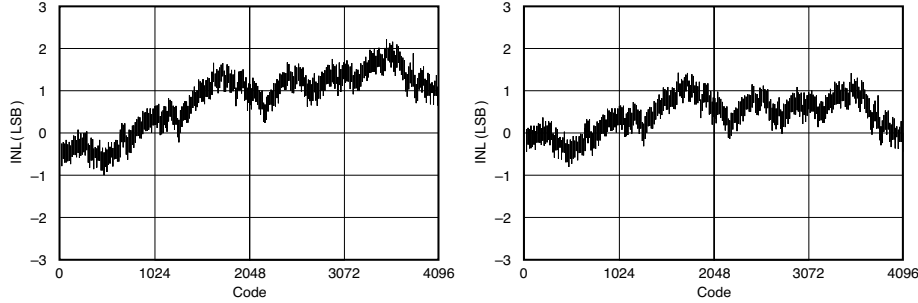
Fig. 2.7 - Integral non linearity plot of a 12 bit *ADC* measured using as reference the ideal interpolation line (left), and the endpoint-fit line (right).

constant or changes in the same direction relative to the change in input.

Hysteresis: it is the limit that denotes a dependence of the output code on the direction by which the transfer curve is traversed (i.e., increasing or decreasing signal). If this happens hysteresis is the maximum of such differences.

Missing code: it denotes when digital codes are skipped or never appear at the *ADC* output. Since missing codes cannot be reached by any analog input the corresponding quantization interval is zero. Therefore, the *DNL* becomes *-1*.

Integral non-linearity (INL): it is the measure of the deviation of the transfer function from the ideal interpolating line. Another definition of the integral non-linearity measures the deviation from the endpoint-fit line. The use of the endpoint-fit line corrects the gain and offset error (defined below). The second definition is chosen as standard since it is more informative for estimating harmonic distortion. Fig. 2.7 shows an example of *INL* plot drawn using the two definitions. The left curve does not start from zero and shows an *INL* climbing up. The right curve corrects the two limits being zero at the two endings of the quantization range.

The maximum of the *INL* is the maximum of |*INL(k)*| for all *k*. Often, it is referred just as *INL*. For the case illustrated in Fig. 2.6 the *INL* is more than *2 LSB* using the first definition it is *1.3 LSB* measuring the deviation from the endpoint-fit line. The *INL*, as for the *DNL*, is in *LSB*. It can be also measured using absolute value (*Volt* or *Ampere*), percent or *p.p.m.* of the full scale.

Let us consider the endpoint-fit line which is the transfer curve with corrected offset and gain. An iterative use of *(2.1)* gives the transition point between codes after correction, *X'*

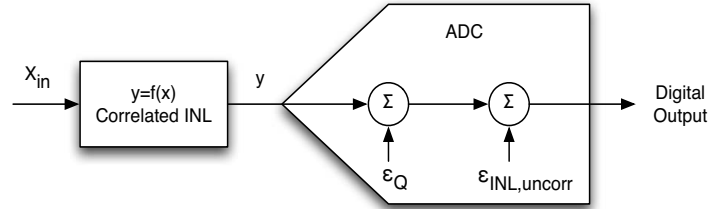$$X'_k = \Delta' \cdot \left[k_{os} + \sum_{i=1}^{k} DNL(i) \right] \qquad (2.3)$$

Fig. 2.8 Equivalent system describing the INL error as pre-distortion effect.

Where $\Delta'=\Delta(1+G)$; G gain error; k_{os} is the offset measured in *LSB*. The offset compensated for the endpoint-fit line is $k_{os}\Delta'$. The *INL* in *LSB* becomes

$$INL(k) = \frac{X'_k - k\Delta'}{\Delta} = (1+G)\sum_{i=1}^{k} DNL(i) \qquad (2.4)$$

Showing that the *INL* at bin k is the running sum of the *DNL*.

The *DNL* and *INL* provide information with different consequences on the noise spectrum. Assume to separate the uncorrelated and the correlated part of the *INL*. If the correlated part of the *INL* is few *LSB* over the entire range its effect on the *DNL* is not distinguishable: the *DNL* plot looks like a noise. Therefore, the *DNL* mainly describes an

> **KEEP NOTE!**
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> A large integral non-linearity denotes harmonic distortion. A large differential non-linearity means extra noise worsening the SNR

increase of the output noise floor. By contrast the correlated part of the *INL* represents the deviation of the transfer curve from a straight line reflecting non-linearity in the converter response.

Fig. 2.8 shows a model of the above. The non-linear block $f(x)$ models the distortion. The quantizer adds the quantization noise and accounts for the uncorrelated part of the *INL* with an extra noise term.

Example 2.1

Evaluate the harmonic distortion caused by the INL. Use the model given in Fig. 2.8 and construct a 1.2 LSB INL response. Estimate the output spectrum due to an input sine wave which amplitude approaches the full scale.

Solution: *The Matlab code given in the file Ex2_1 provides a basis for studying the problem. The INL is made by two terms, a*
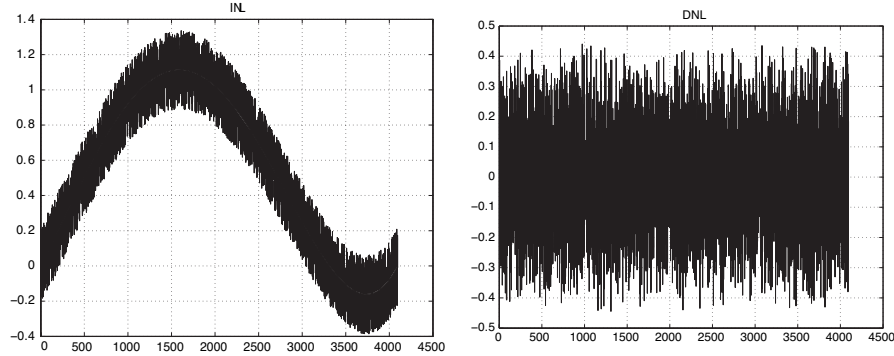
Fig. Ex. 2.1 - a) - INL (left curve) and b) DNL (right curve).

random sequence of number which maximum is ± 0.45 and the polynomial function

$$y = x + a \cdot x^2 + b \cdot x^3 + c \cdot x^4; \quad x = (n - 2^{N-1})/2^{N-1}$$

where n is the running bin and N=12.
Using a= -0.01, b= 0.01 and c= 0.02 gives the INL plot of Fig. Ex 2.1 a). The corresponding DNL is shown in Fig. Ex 2.1 b). As expected the correlated term does not affect the DNL whose limits are ± 0.45. The input is the 12-bit quantization of a 61 periods sine wave (2^{12} samples). We expect the spectrum of Fig. Ex 2.1 c). The average of the spectral lines is the noise floor: -107.1 dB (SNR=74 dB, processing gain=33.1 dB). Fig. Ex 2.1 d) shows the effect of INL on the signal spectrum. Since the uncorrelated part of the INL plot is ± 0.2 LSB, the noise floor increases by just fractions of dB. The correlated part of the INL causes tones. The parabolic shape of the INL denotes a dominant second order term. In fact, the biggest tone is the second harmonic with value -76 dB.
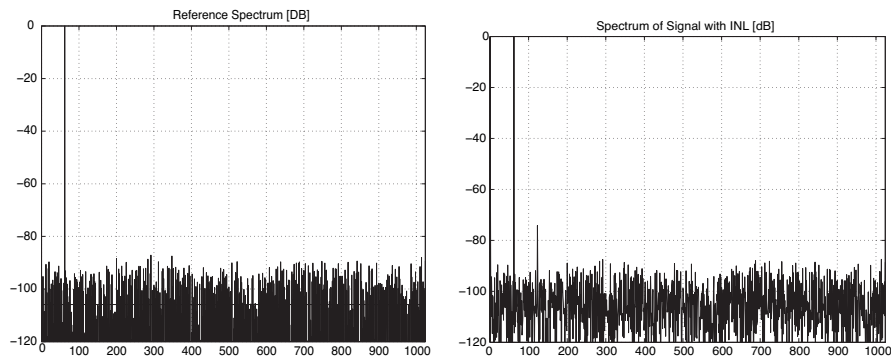

Fig. Ex. 2.1 - c) - Normalized reference spectrum and d) effect of the INL.

2.3.3 Dynamic Specifications

The frequency response and speed of the used analog circuits affect the performances of data converters. Obviously, the performances impair with wide-band inputs and very high conversion-rates. For this reason the dynamic specifications are usually given as a function of input frequency, time, or conversion data-rate. System designers normally desire to use converters with unchanged specifications in the entire dynamic range of operation. This is a very challenging request for the circuit designers.

The parameters described below are the most frequently used in catalogues and products data-sheets. They are also standards as defined by *IEEE* [1].

Analog Input Bandwidth: it specifies the frequency at which a full-scale input leads to a reconstructed output 3 dB below its low frequency value. The definition differs from the one used for conventional amplifiers: for an *ADC* the input is not a "small signal": the amplitude can be the full scale.

Input Impedance: it is the impedance between the input terminals of the *ADC*. At low frequency the input terminals show a resistive load; ideally the input resistance should be infinite for voltage inputs and zero for current inputs (obtaining an ideal measurement of voltages or currents).

KEEP NOTE

High-speed converters need matching input networks capable to account for bonding and packaging.

At high frequency the input impedance is dominated by a capacitive term. At very high frequency the input establishes a termination impedance that must match the impedance of the input generator. It is necessary to ensure impedance matching and avoid reflection that would affect the conversion.

Settling-time: it is the time at which the step response of a *DAC* enters and subsequently remains within a specified error band around the final value. The input is a step signal applied at time $t = 0$. The final value is defined to occur after a long time the beginning of the step (the standard is *1 sec*).

Cross-talk: it measures the energy that appears in a signal because of undesired coupling with other signals. In addition to coupling at the *IC* level a poor printed circuit board design can cause crosstalk. Traces carrying critical signal running in parallel on the same layer of the *pcb* must be avoided.

Aperture uncertainty (Clock Jitter): it is the standard deviation of the sampling time. It is also called *aperture jitter* or *timing phase noise*. It is assumed that the noise spectrum caused by clock jitter is white.

Equivalent input referred noise: it is the measure of the electronic noise produced by the circuits of the *ADC*. For a constant *DC* input the output is not

$$V_{in} = \frac{x}{2^N} \cdot V_{FS}$$

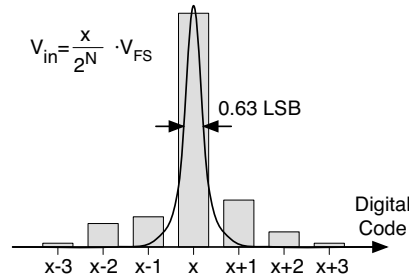0.63 LSB

Digital Code

x-3 x-2 x-1 x x+1 x+2 x+3

Fig. 2.9 - Estimation of the input referred noise using the histogram of dc input measures.

fixed but there is a distribution of codes centred around the nominal value of the output code. With a large number of output samples the code histogram is approximately Gaussian. The standard deviation of the distribution defines the equivalent input referred noise. It is normally expressed in terms of *LSBs* or *rms* voltage. Fig. 2.9 shows the histogram at the output of a possible data converter affected by a *0.63 LSB* noise.

Signal-to-Noise Ratio (SNR): it is the ratio between the power of the signal (normally a sinewave) and the total noise produced by the quantization and the noise of the circuit. The *SNR* accounts for the noise in the entire Nyquist interval. The *SNR* can depend on the frequency of the input signal. It diminishes proportionally to the input amplitude. Fig. 2.10 shows the *SNR* of an hypothetical *12-bit* data converter with *50 MHz* sampling frequency. The *SNR* for a *-0.5 dB* input is *67 dB*. The noise caused by the electronics almost equals the quantization noise. When the input signal is *-20 dB*, as expected, the *SNR* is *48 dB*. Observe that the *SNR* works well: it is almost constant in the entire Nyquist range. It drops few *dB* for frequencies in the second Nyquist zone. Therefore,
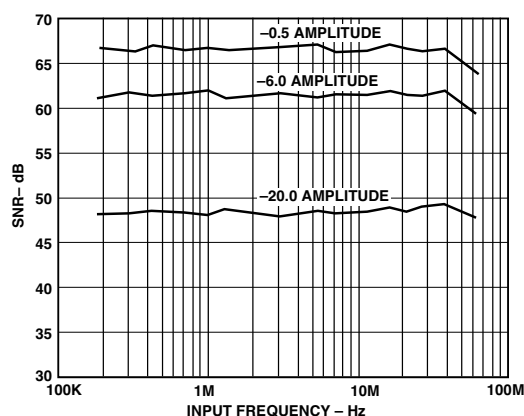

Fig. 2.10 - Signal-to-Noise Ratio versus the input frequency at different input levels.
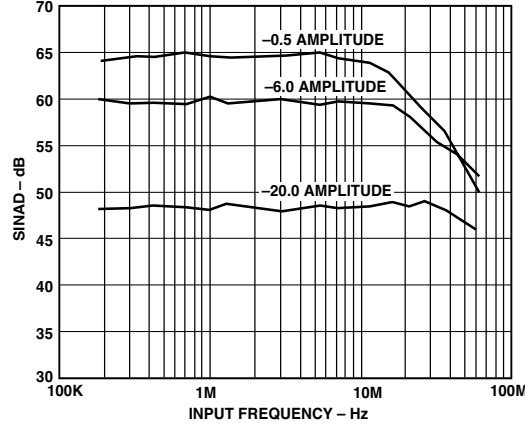
Fig. 2.11 - SINAD versus input amplitude and input frequency (f_{ck}=50 MHz).

the converter is suitable for an undersampling use. The input signal can stay in the second Nyquist-zone and the anti-aliasing filter is band-pass around the signal band.

*Signal-to-Noise-and-Distortion Ratio (SINAD)***:** its definition is similar to the one of the *SNR*. The input sine wave causes, in addition to noise, non linear distortion terms. The *SINAD* is the ratio between the root-mean-square of the signal and the root-sum-square of harmonic components plus noise (excluding *dc*). Static and dynamic limitations cause non-linear response. Therefore, both amplitude and frequency of the input sine wave affect the parameter. Fig. 2.11 shows the *SINAD* for the same hypothetical converter of Fig. 2.10. *SNR* and *SINAD* shows that harmonic terms are negligible if the input is - *20 dB$_{FS}$* or less. Bigger input amplitudes bring about distortion especially at high frequencies. The *SINAD* degrades significantly in the second Nyquist zone; thus, the part is not suitable for undersampling.

*Effective-Number-of-Bit (ENOB)***:** it measures the signal-to-noise and distortion ratio (*SINAD*) using bits. The relationship between *SINAD* in *dB* and *ENOB is*

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02} \qquad (2.5)$$

*Total Harmonic Distortion (THD)***:** it is the ratio between the root-mean-square of the signal and the root-sum-square of harmonic components including aliased terms. Unless otherwise specified the *THD* accounts for the second through the tenth harmonics: it is normally assumed that harmonic terms higher than the tenth have negligible effects. If f_{in} is the frequency of the input signal and f_s is the sampling frequency, the *n-th* harmonic component is at fre-
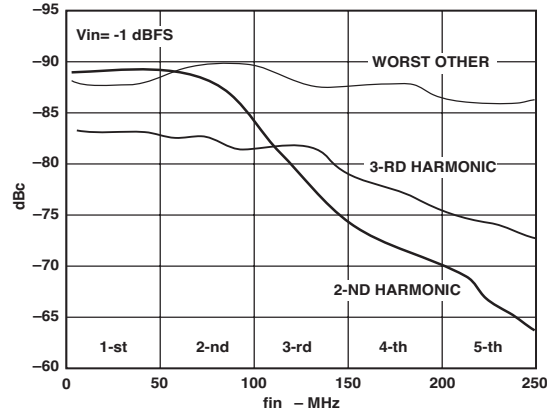
Fig. 2.12 - Harmonic terms as a function of the input frequency. Observe that the harmonic
is good on the top side of the diagram and is bad in the bottom side.

quency $|\pm nf_{in} \pm kf_s|$, where k is a suitable number that folds the harmonic term
into the first Nyquist zone. At high input amplitude the largest terms are the
second and the third harmonic. Some data sheets provide a plot of their ampli-
tude as a function of the input frequency in *dBc* (*dB* below carrier). Fig. 2.12
shows the harmonics of an hypothetical *100 MHz* clock, *12-bit ADC*. The fig-
ure is for input frequencies up to *250 MHz* (*5-th* Nyquist zone). A fully differ-
ential operation makes negligible the second harmonic term in the first two
Nyquist zones. At high frequency the benefit of the fully-differential architec-
ture vanishes and the second harmonic distortion becomes dominant.

Example 2.2

*Identify the frequency of the first ten harmonic distortion tones in
the output spectrum of a non-linear data converter. Use computer
simulations to verify the achieved results.*

Solution: *We use a sampling frequency of 2^{14}=16.4 kHz and an
input frequency equal to 671 Hz. The tenth harmonic is at 6.71 kHz,
below the Nyquist limit. All the harmonic tones will show up
sequential on the frequency axis.*

*Assume now an input frequency equal to 1.711 kHz. The fifth har-
monic is at 8.555 kHz, higher than $f_s/2$=8.192 kHz. The aliasing
mirrors that term at f_s-5·f_{in}=7.829 kHz. The harmonic #6, #7, #8
and #9 are also folded once. The tenth term is at 17.11 kHz. Alias-
ing folds it twice leading the tone at 10·f_{in} - f_s=726 Hz.*

*The codes Ex2_2.mod and Ex2_2launch.m are the description of
the computer simulation model. A polynomial function and suitable*
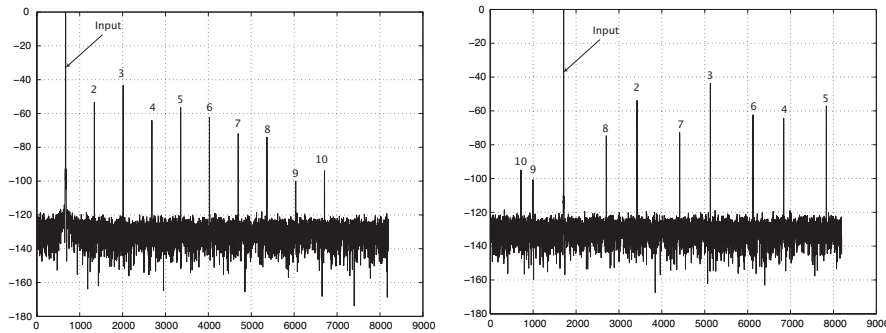
coefficients describe the harmonic distortion.

Fig. Ex. 2.2 - Harmonic tones for fin=671 Hz and 1.711 kHz (fs=16.38 kHz).

> *By comparing the two spectra in Fig. Ex. 2.2 it is possible to verify the foresees aliasing with input frequencies equal to 671 Hz to 1.711 kHz. The diagrams show tones well separated from the input. However, if f_{in} is close to f_s/n (with n integer) harmonics goes very near the input signal (try, for example, f_{in}=2339 Hz).*

Spurious Free Dynamic Range (SFDR): it is the ratio of the root-mean-square signal amplitude to the root-mean-square value of the highest spurious spectral component in the first Nyquist zone. The *SFDR* provides information similar to the total harmonic distortion but focus on the worst tone. For signals near full scale one of the first input harmonics determine the highest spectral spur. As the signal falls several *dB* below full scale, other spurs which are not direct harmonics of the input signal can become dominant. Remember that all possible sources of distortion, regardless of their origin, determine *SFDR*.

> **KEEP NOTE**
>
> Near the full scale one of the harmonics of the input determines the SFDR. At low input amplitude other spurs dominate the SFDR.

The *SFDR* is an important parameter for data converters used in communication systems. Often it is required to convert from analog-to-digital a small signal representing a channel that the antenna receives together with other big channels. At worst the highest spur generated by one of the large signals falls very close to the small channel thus masking the associated information. Fig. 2.13 illustrates the problem. The input signal is made by two bands, one is big (*0 dB*) and is around *6.72 MHz*, the other, is centred around *3.8 MHz* has amplitude *-90 dB*. The sampling frequency is *16.4 MHz*. The big component generates a big third harmonic spur at *20.16 MHz* that is folded at *3.76 MHz*, at just *40 kHz* from the second chan-
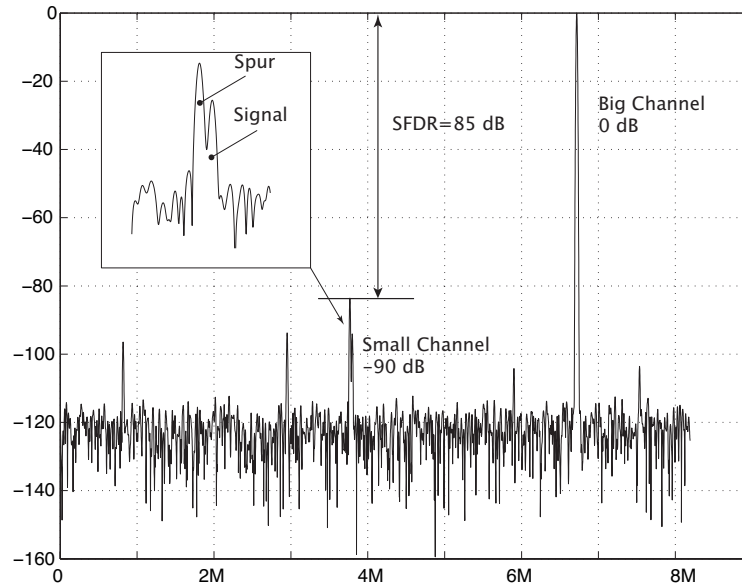
Fig. 2.13 - Spectrum of a small channel corrupted by the bigger spur due to a large channel.

nel. Even if the *SFDR* is *85 dB* the effect of the spur on the *-90 dB* signal is significant.

The *SFDR* is generally plotted as a function of the signal amplitude. It is expressed in *dBc*. In some cases product data sheets provide the value of the highest spur *rms* normalized to the *ADC* full scale (*dBFS*). Fig. 2.14 shows the
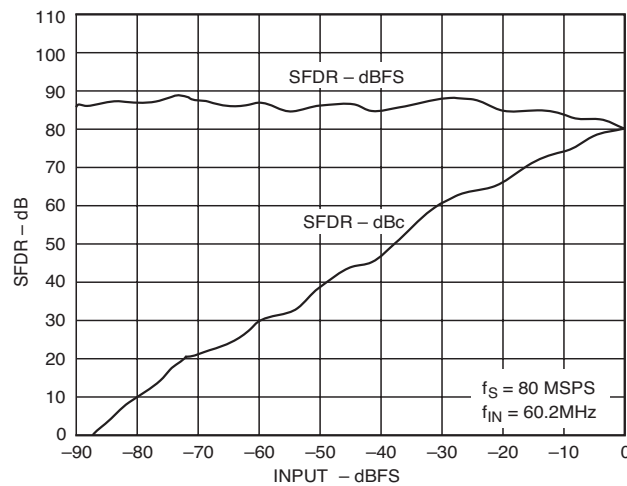

Fig. 2.14 - SFDR plot expressed in terms of dBc and dBFS.

SFDR plots of an hypothetical converter. The curves are for input and sampling frequencies equal to *60.2 MHz*, *80 MHz* respectively. The diagrams refer to operation in the second Nyquist zone. The *SFDR* in *dBFS* shows that the power of the highest spur is almost independent on the input amplitude. Accordingly, the *SFDR* in *dBc* drops linearly (input is in *dB*). The *SFDR* is *0 dBc* at *-86 dBFS* input. At this level the maximum spur is equal to the input.

KEEP NOTE

The second or third-order intercept points defined for amplifiers used in communication systems doesn't have ADC equivalents.

The ADC acts as a hard limiter as the signal exceeds the ADC input range. The ADC suddenly produces an extreme amount of distortion because of clipping.

***Intermodulation Distortion (IMD)*:** it accounts for spur tones caused by the non-linearity when the input is a complex signal. Non-linearity is not only responsible of distortion of a pure tone; when the input is made by multiple sine waves the interaction between them produces the intermodulation terms. The non-linearity of the data converter causes the mixing of the spectral components thus generating spurs at sum and difference frequencies for all possible integer multiples of the input frequency tones.

Two tones Intermodulation Distortion (IMD2): it is the ratio of the *rms* value of either input tone to the *rms* value of the worst third order intermodulation product reported in *dBc*. The input is made by two closely spaced tones f_1 and f_2. Often the specification accounts for the third order spurs only. They are at *(2f_1-f_2)*, *(2f_2-f_1)*. The reason of considering third order terms only is that they are close to the input frequencies $f_1 \approx f_2$. Other intermodulation terms are far away from the input and can be filtered out in the digital domain.

Example 2.3

Determine with computer simulations the IND2 tones caused in a 14-bit ADC with $x+10^{-4}x^3$ transfer response.

Solution: *The code Ex2_3.m provides the basis for the computer solution. The sampling frequency is 16.38 kHz. The two tones at 1.169 kHz and 1.231 kHz have the same amplitude, 1. The full scale is ± 2. The quantization step is $V_{FS}/2^{14}=1/2^{12}$. A non linear block models the distortion of the transfer characteristic of the converter.*
The Fig. Ex2.3 gives the output spectrum in the frequency range 500 Hz 4 KHz. The figure outlines four intermodulation products (2f_1-f_2), (2f_2-f_1), (2f_1+f_2), (2f_2+f_1). The first two tones are the
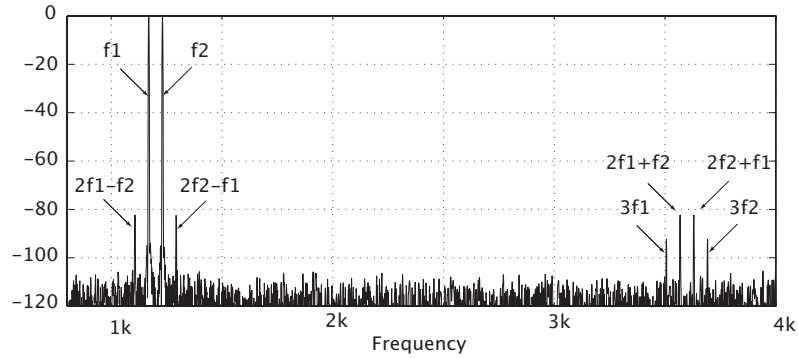
Fig. Ex. 2.3 - Spectrum of the output signal showing the IND2 tones.

closest to the input frequencies. The figure also shows the effect of the third order non linearity that produces two tones at $3f_1$ and $3f_2$.

Multi-Tone Power Ratio (MTPR): this parameter is specific for data converters used in communication systems. It specifies the distortion for multi-tone transmission systems. The parameter is measured using a sequence of tones with equal amplitude A_0 and placed at frequency that are multiple of a fundamental frequency f_0. Few tones are left out. The harmonic distortion produces interference signals in the position of the missing tones. The *MTPR* is defined as the ratio of the *rms* signal amplitude A_0 to the *rms* value of the tones at the missing tones frequencies.
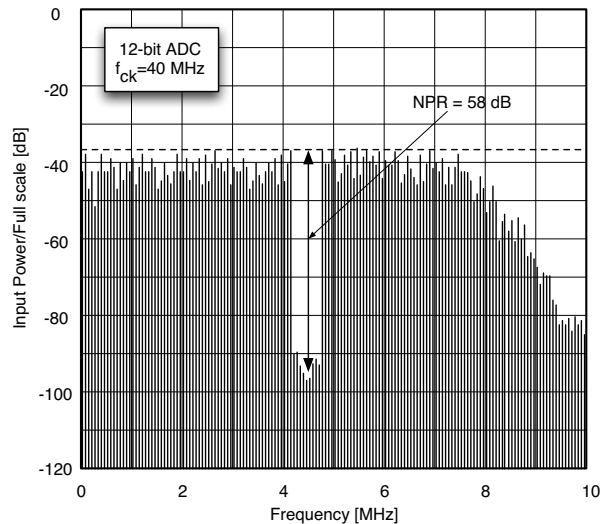

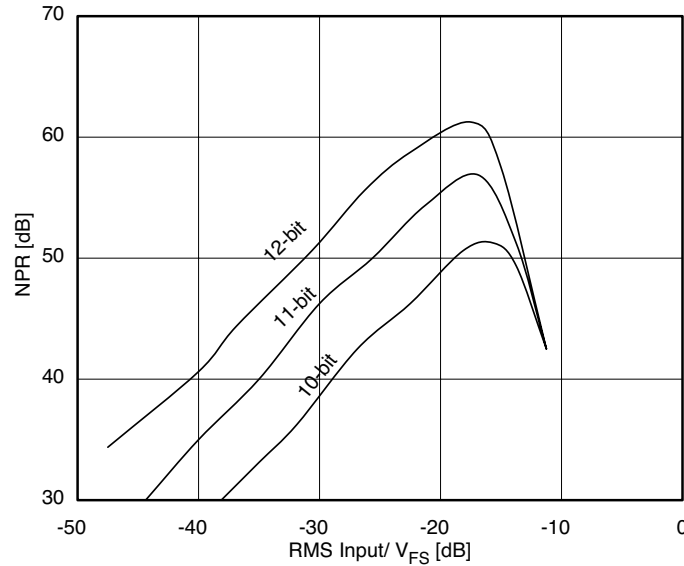**Fig. 2.15** - Output spectrum used to measure the NPR.

Fig. 2.16 - NPR for different ADC resolutions versus the RMS input amplitude.

Noise-power ratio (NPR): similarly to the *MTPR* it describes the linear performances when the *ADC* is used in frequency division multiplexed (*FDM*) links. *NPR* is a parameter used to specify power amplifiers but the same concept is also used for data converters. In an *FDM* system the signal is made by many carriers with different amplitude and phase. The signal looks like a white noise passed through a band-pass filter. Assume to remove one of the channels. As a result the spectrum will show a deep notch at the frequency of the missing channel. If we use the obtained signal to excite the *ADC* the converter noise and the *IMD* will tend to fill in the notch. The depth of the notch after the *ADC* gives the *NPR*. Fig. 2.15 shows a typical spectrum used to determine the *NPR*.

The *NPR* depends on the *rms* value of the input. For low input levels the notch is mainly filled by the quantization noise and the thermal noise contributions. They are almost independent on the input power. For high inputs the *ADC* saturation and distortion terms become dominant causing a quick drop of the *NPR* (Fig. 2.16).

2.3.4 Digital and Switching Specifications

The digital features are specified by a given set of parameters. They ensure the proper interfacing with internal or external circuits and are useful for the

synchronization logic signals in the data converted.

The specification given below are the most used in commercial data sheets.

Logic levels: it is the set of non overlapping range of amplitudes used to represent the logic state. The used logic levels ensure the compatibility with defined logic standard (like the *CMOS* or *TTL*).

Encode or clock rate: it is the range of possible encode rate that ensures the performances of the specifications. It can vary by one decade or more. The best is to use the data converter with a maximum clock that is about *25%* of the maximum guaranteed by the specification.

Clock timing: it specifies the features of the clock. The information is normally given using a diagram. The external clock is normally regenerated at the input since edge-triggered flip-flops latch the input on the rising or the falling edge. The clock duty cycle can be chosen arbitrarily under some constraints. A *50%* duty cycle normally is the best for optimum dynamic performances.

Clock Source: the clock signal specifies the timing operation of the converter. Circuits requiring a very low jitter generate the clock using a differential input sine wave. The input sine wave is obtained by a crystal clock oscillator and/or external filters. This ensures sine wave purity and provides accurate zero-crossing times. Internal amplifiers square the input sine wave and generate the internal clock.

Sleep mode: it specifies a power-down mode that turns off the main bias current and minimizes the power consumption. The power-down mode is activated by applying a logic level to a proper pin. The power-up and the power-down activation times depend on the time constant associated with the sleep circuit. It may take few *μs* to go in the seep mode and few *ms* to power the circuit back.

2.4 PROBLEMS

2.1 Search on the Web-site of a main data-converter manufacturer and list the various type of produced data converters. Draft a table with type, resolution and maximum clock-rates.

2.2 Plot the input-output transfer curve of an *8-bit* data converter. Assume a random *DNL* with maximum variance *0.4 LSB*. The interpolating curve is *y=x + 0.01(x-0.5)³; 0 > x > 1*.

2.3 Download from the Web the data-sheet of a *12-bit ADC*. Estimate the interpolating curve reproducing the *INL*. Calculate the output spectrum for a full scale sine wave.

2.4 Repeat the example 2.1 with the following distortion coefficients: *a=*

0.02, b=-0.005 c= 0.01. Determine the harmonic distortion for an input sine wave. The amplitude changes from full scale to -20 dBFS. Keep *a* constant and change the values of *b* and *c* so that the harmonic distortion is optimised for an input full scale sine wave. Plot, using the optimum values, the distortion as a function of the input amplitude.

2.5 Perform a computer simulation to collect *5000* samples and plot the histogram at the output of *12-bit* data converter. The input amplitude is constant equal to *0.372 V_{FS}*. A *20 μV_{FS} RMS* random noise affects the input stage of the converter.

2.6 Repeat the example 2.2 using *3.7 kHz* and *4.2 kHz* input sine waves. Determine the output spectra when the input sine wave are replaced by square waves at the same frequency. Justify the obtained results.

2.7 Repeat the example 2.3 by using the following transfer response: $y= x + 10^{-4}x^2$. Use two sine waves one with half-scale and the other with full-scale amplitude. The frequencies are *1.23 kHz ± 50 Hz*.

2.5 **REFERENCES**

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