Bandgap Reference Cookbook

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1. Reference Circuits Introduction

- **What is reference circuit?**

A circuit used to generate a **Stable** DC voltage or current

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→ Little dependence on process and supply voltage
→ Well-defined dependence on temperature : Not necessary independent

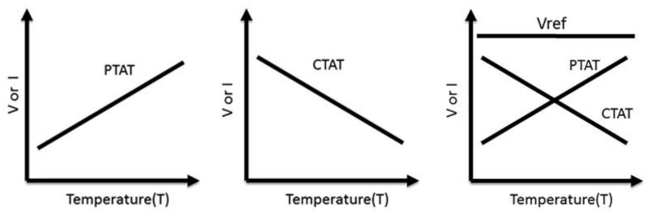
- **Types of Temperature dependence**

→ Most process parameters vary with temperature so, if we achieve a temperature independent reference it will be also a process independent

→ Reference circuits not necessary to be temperature independent

→ Temperature dependence could be

- Positive temperature coefficient (+ ve TC): Proportional to absolute temperature
- Negative temperature coefficient (- ve TC): Complementary to absolute temperature
- Zero temperature coefficient (zero TC): Temperature independent PTAT + CTAT

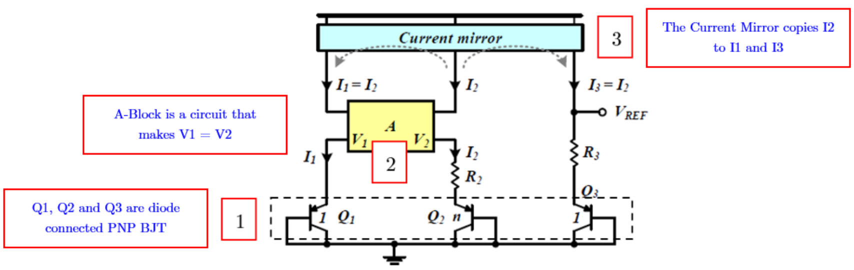


2. Basic operation of BGR (How Vref is ZTAT?)

- **Analysis of BGR**

→ Using Simple diode model ($V_{BE1} = V_{BE2} = V_{BE}$) and since V1 = V2 you may expect I2 = 0 but it's invalid approx.

→ Q2 is n BJTs diode connected in parallel → $I_{C1} = I_1$ and $I_{C2} = {}^{I_2}/_{n}$



→ Using BJTs instead of simple diodes because of Accurate spice models and Base connection may provide more design options.

$$I_C = I_s\, e^{\frac{|V_{BE}|}{V_T}} \rightarrow |V_{BE}| = V_T \ln\frac{I_C}{I_S}$$

$$\Delta V_{BE} = |V_{BE1}| - |V_{BE2}| = V_T \ln n = \frac{KT}{q}\ln n$$

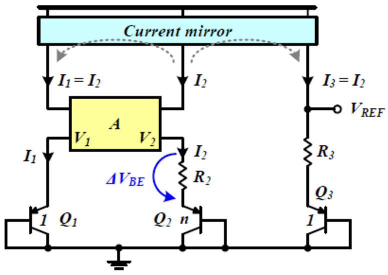
$$I_2 = \frac{\Delta V_{BE}}{R_2} = \frac{KT}{q}\ln n \times \frac{1}{R_2} \rightarrow \therefore\ I_2 \text{ is a PTAT}$$

→ V_T : the thermal voltage approx. 26mV @ 300k

→ I_s : the saturation current and it is constant

→ K : Boltzmann's constant

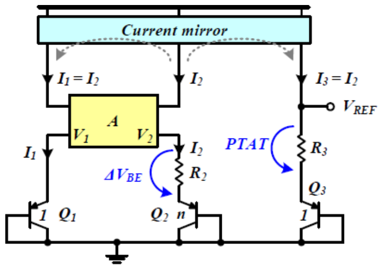
→ q : the elementary charge of an electron



$$V_{R3} = I_3 R_3 = \frac{KT}{q}\ln n \times \frac{R_3}{R_2} \rightarrow \text{ is a PTAT}$$

$$V_{R3} = 0.086 \ln n \times \frac{R_3}{R_2}\left(\frac{mV}{K}\right) @\ 300K$$

Since I3 is a copy of I2 → I3 will be a PTAT current and VR3 will also be a PTAT voltage



It can be shown that $|V_{BE}| = V_T \ln\frac{I_C}{I_S} = V_{G0} - b_1 T$ is a CTAT although I_C and V_T are PTAT but I_s is a strong function of temperature, **Why?**

$$I_s \propto \mu K T n_i^2$$

$$\mu(\text{mobility of holes}) \propto \mu_o T^m,\ m \approx -\frac{3}{2} \text{ and } n_i^2 \text{ (intrinsic carriers)} \propto T^3 e^{-\frac{Eg(\text{bandgab energy})}{KT}}$$

$$I_s \propto \mu_o \times T^{m+4} \times K \times e^{-\frac{Eg(\text{bandgab energy})}{KT}}$$

$$I_s = b \times T^{m+4} \times e^{-\frac{Eg(\text{bandgab energy})}{KT}} \rightarrow \text{Strong function of Temperature} \rightarrow |V_{BE}| \text{ is CTAT}$$

Get b1 from simulations: Usually b1 ≈ 1.5 – 2 mV/K

$$V_{ref} = V_{R3} + V_{BE3} = a_1 \times T + V_{G0} - b_1 \times T = V_{G0}\ (\text{if } a_1 = b_1)$$

$V_{G0} = \frac{Eg}{q} \rightarrow$ Bandgap voltage, it's constant = 1.2V at absolute zero kelvin *and* it is related silicon

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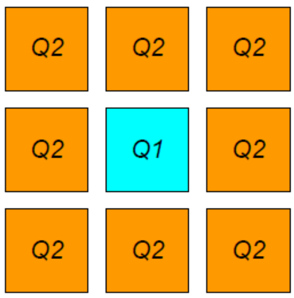
- **Design Considerations (1)**

To design a bandgap we need to determine 3 parameters n, R2, R3

1. **n :** Due to layout considerations, two values of n are usually used **n** = 8 (better matching) and **n** = 24 (better ΔV_{BE})

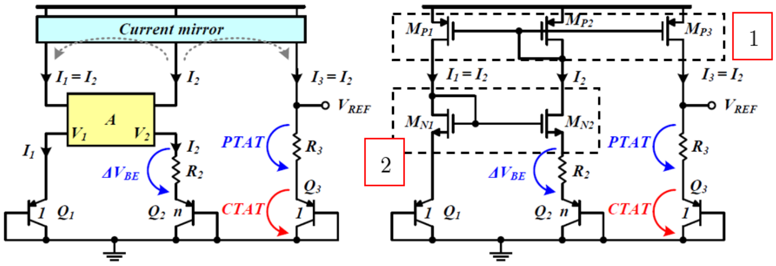
2. **R_2 :** Given current consumption, select R_2 where
$$I_2 = \frac{\Delta V_{BE}}{R_2} = \frac{KT}{q}\ln n \times \frac{1}{R_2}$$

3. **R_3 :** Chosen to achieve ZTAT Vref (set a1 = b1)
$$a1 = 0.086 \ln n \times \frac{R_3}{R_2}\left(\frac{mV}{K}\right) \text{ and get b1 from simulations}$$



3. Practical CMOS implementation of BGR

- **No. 1: Basic Implementation**



Simple current mirror using $M_{P1\text{-}3}$

A-Block: $M_{N1\text{-}2}$ → Same Current → Same VGS

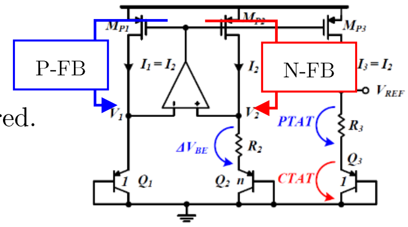
- **Design Consideration (2)**

1. Use Large L (≥ 1um) is usually used because
2. For low supply voltage, bias the transistors in MI or WI ($g_m/I_D \geq 15$)

- Reduce V_{DS} dependence CLM
- Reduce flicker noise as the low frequency behavior is more important in this circuit
- Large area gives better matching

- **No. 2: Op-AMP Implementation**

  - The op amp keeps V1 and V2 at the same voltage.
  - The op amp can be implemented as a simple 5 T OTA.
  - Folded cascode may be used if wide input range is required.
  - Bias the op amp using a constant gm circuit. Or use the BGR itself to bias it (self biased)!



Negative or Positive Feedback?

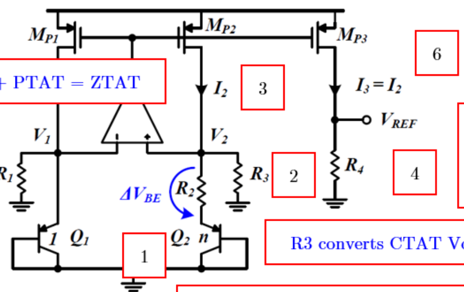
Both Negative and Positive Feedback loop are exist so, we must guarantee $B_N > B_P$

$$B_N = g_{mP2}(R_2 + 1/gm_Q)$$
$$B_P = g_{mP1}(1/gm_Q)$$

As R2 is always +ve Value so, $B_N > B_P$

  - This circuit gives Vref = 1.2 V but For modern technologies, this value is higher than VDD itself so, How to get Low Voltage BGR
  - The solution is to add PTAT and CTAT in the current domain.

- **No. 3: H. Banba's Implementation**



I2 = I@R3 + I@Q2 = CTAT + PTAT = ZTAT

R1 maintains IE1 = IE2

$VBG = R_4\left(\frac{\Delta VBE}{R_2} + \frac{V_{BE1}}{R_3}\right) < 1.2V$

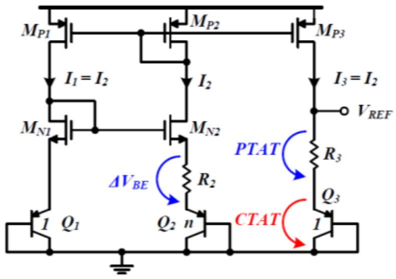
I3 is a copy of I2 (ZTAT Current) Converted by R4 to a Vref (ZTAT Voltage)

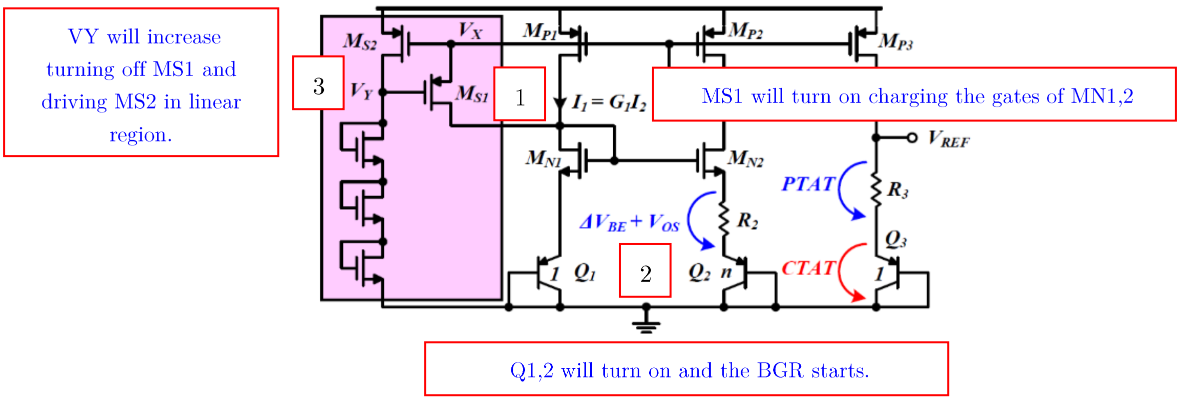
R3 converts CTAT Voltage (VBE1) to a CTAT Current

R2 converts PTAT Voltage (ΔV_{BE}) to PTAT Current

4. The Start-up Problem

- All currents = 0 is another valid solution for the circuit!
- Start up circuit must drive the circuit out of the zero bias point, Then it should automatically turn off or consume little current
- Start up verified by ramping up VDD from zero in DC sweep and transient simulations.
- Startup problem means VX = VDD and VY = 0





<u>Lets Design</u>