Bandgap Reference Cookbook

By : Abdelrahman Hassan Muhammed

Design a band gap circuit in 65nm CMOS with the specifications listed in table

Parameters	Conditions	Units	Target Specs.		
			Min.	Typ.	Max.
Operating Temperature		°C	-40	25	125
Supply Voltage	Nominal supply (1.1V) ±10%	V	0.99	1.1	1.21
BG Output Voltage		V		0.5	
PVT Variation	Process, Voltage, and Temperature	%	-3		+3
Mismatch Variation	Monte Carlo Variation (3σ) for 1000 run @TT	%	-4		+4
BG PSRR	At DC	dB	-50		
Phase Margin	of any loop	Deg.	50		
Gain Margin	of any loop	dB	10		
Startup Time	After asserting "enable" while supply is present	µs			10

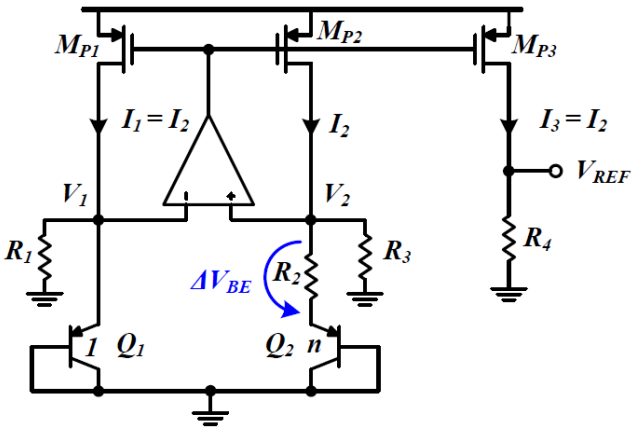
Design Procedures

1. Select the topology

We can achieve ZTAT behavior by adding PTAT and CTAT via two approaches:

- Currents summation approach.
- Voltage summation approach.

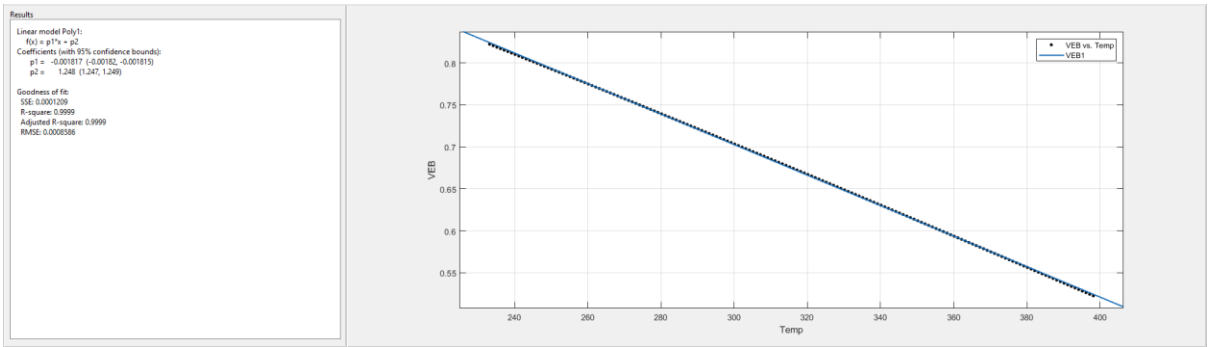
Voltage approach can not achieve reference voltage lower than 1.2V, on the other side, current approach can achieve sub1V references, So we will use current



2. Choose I1, I2, I3

- Since no constrain on power consumption, I prefer choosing low ID to get low variation in PTAT and CTAT and low power consumption which make it suitable for modern applications.
- Assume R4 = 50K Ohm → Vref = 0.5 → I3 = 10 uA
- We will mirror current with same aspect ratio so, $I_1 = I_2 = I_3 = 10$ uA

3. See the characteristics for BJT and get the CTAT slope



$$V_{EB} = 1.248 - 0.0018717 \times T\ ;(T \text{ in Kelvin})$$

4. Design BGR Core (n, R1, R2, R3, R4)

- First choose n = 8 for small size on chip and Since we get R4 = 50K Ohm before and

$$V_{ref} = I_3R_4 = I_2R_4 = R_4\left(\frac{V_{EB1}}{R_3} + \frac{V_T \ln n}{R_2}\right) = \frac{1.248 \times R_4}{R_3} + \frac{KT \ln n \times R_4}{q \times R_2} - \frac{0.0018717 \times T \times R_4}{R_3}$$

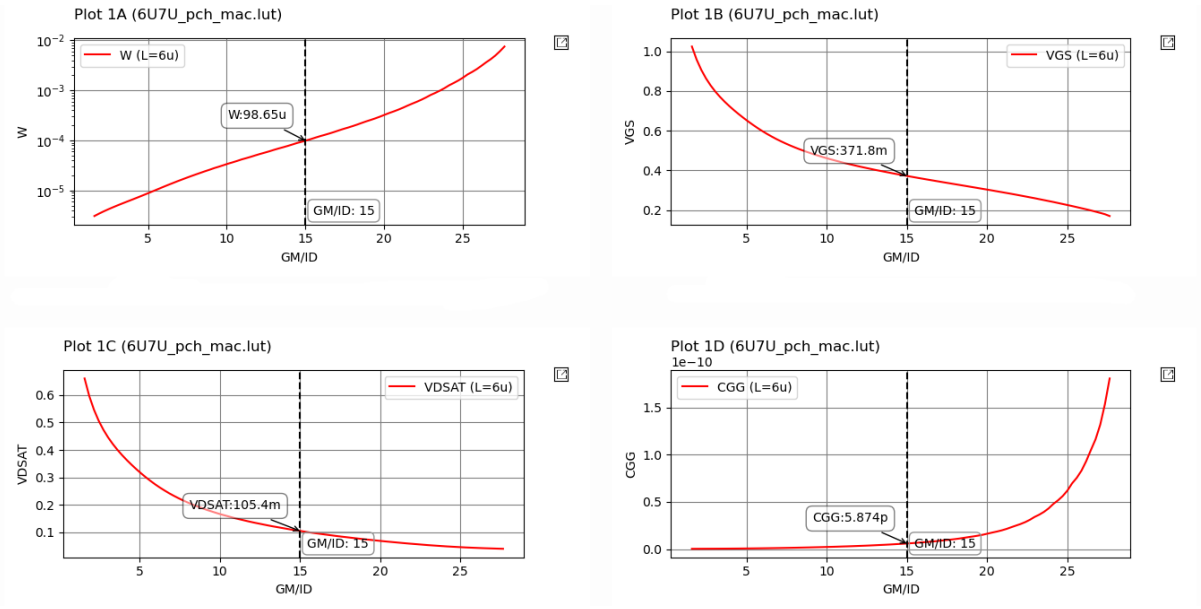
- From previous equation we need

$$\frac{K \ln n}{q \times R_2} = \frac{0.0018717}{R_3} \rightarrow (2) \text{ and } \frac{1.248 \times R_4}{R_3} = 0.5 \rightarrow (3)$$

- From (3) $R_4 = 50K\,\text{Ohm} \rightarrow R_3 = 124.8K\,\text{Ohm} = R_1 \rightarrow$ Substituting in (2) $R_2 = 12.307K\,\text{Ohm}$

5. Design of the Current Mirrors

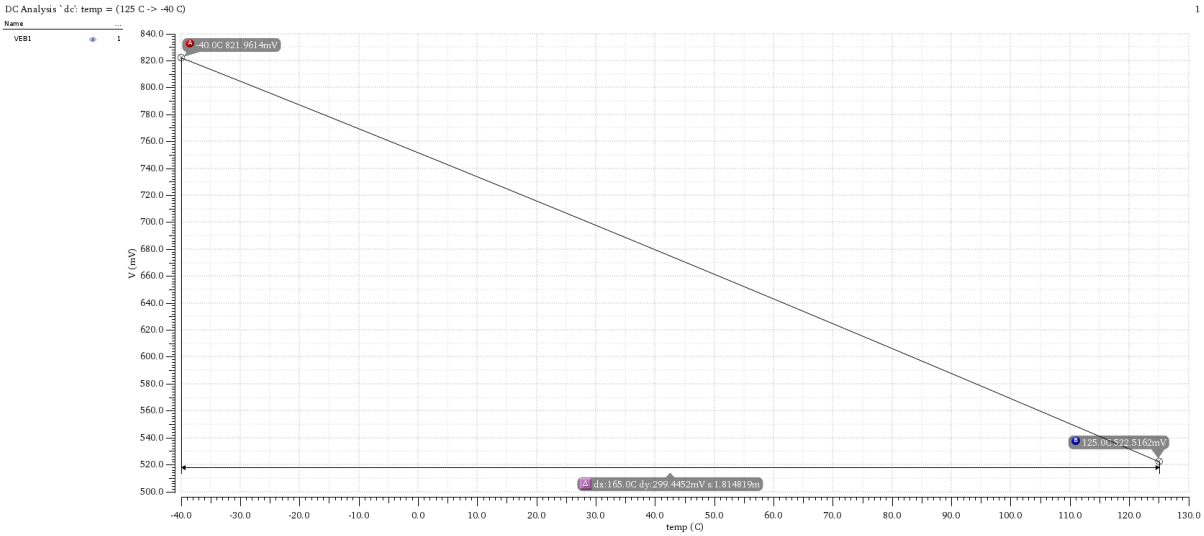
- Use Large L ($\geq 1um$) is usually used because
  1 | Reduce V_{DS} dependence CLM
  2 | Reduce flicker noise as the low frequency behavior is more important in this circuit
  3 | Large area gives better matching and Better for PSR
- For low supply voltage, bias the transistors in MI or WI ($\frac{g_m}{I_D} \geq 15$)
- Use L = 6 um and $\frac{g_m}{I_D} = 15 \rightarrow$ using gm/ID charts



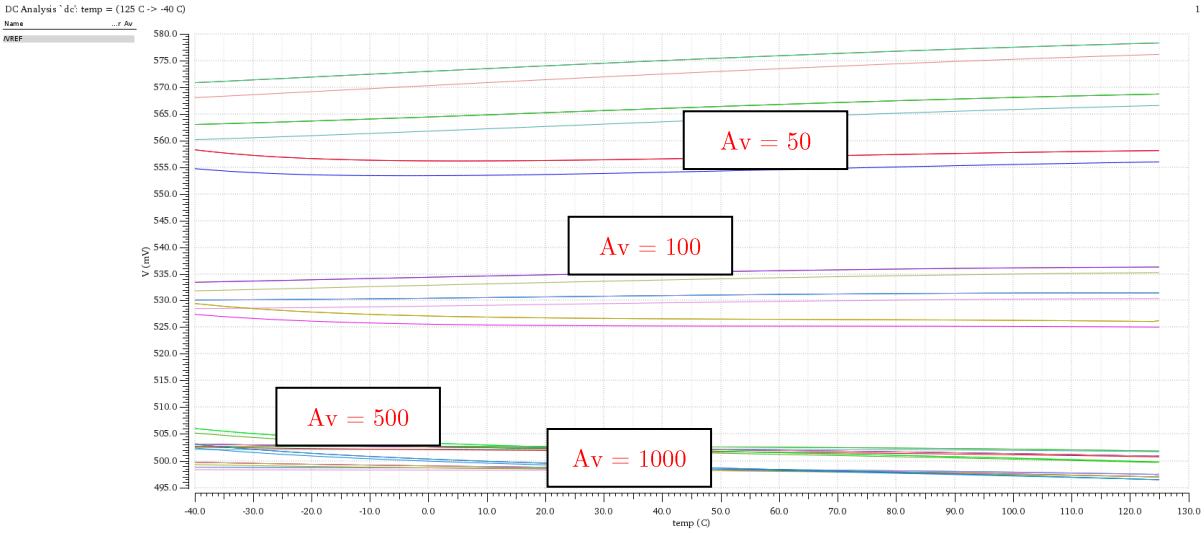
6. Design of the Op-Amp

- There are three specs we can approximate for the Op-Amp

1 | CMIR : From BJT characterization we can see that VBE of BJT changes in range from 516 mV to 822 mV, the input common mode of the Op-Amp must be able operate normally through that range, so CMIR of Op-Amp must be at least the same as that range with some margin say CMIR = 480 mV : 850 mV



2 | Gain (Av) : by replacing the Op-Amp by a VCVS and measuring the effect of this gain on the Vref across PVT, we find that we need voltage gain $A_V \geq 500$ to maintain nominal error in the BGR across PVT



3 | Cout : Summation of the Cgg of the current mirrors + suitable margin for output transistors parasitic capacitance $C_L = 16\ pF$

- Designer choices

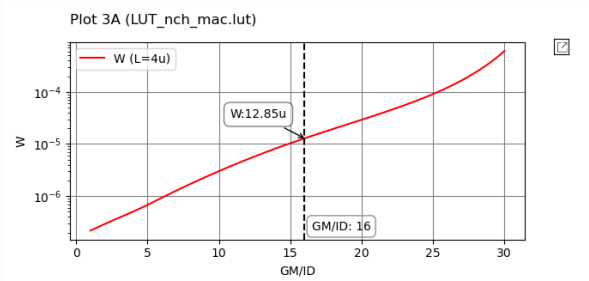
1 | The CMIR is closer to VDD rail → NMOS input stage

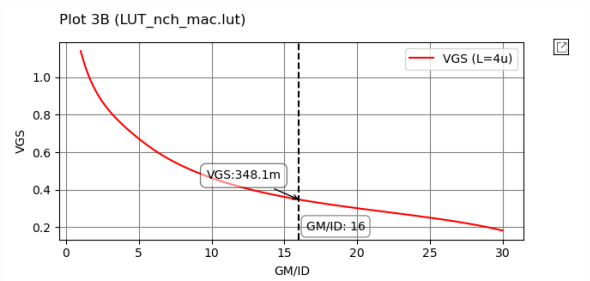
2 | The required gain is quite high → Use Two Stage OTA

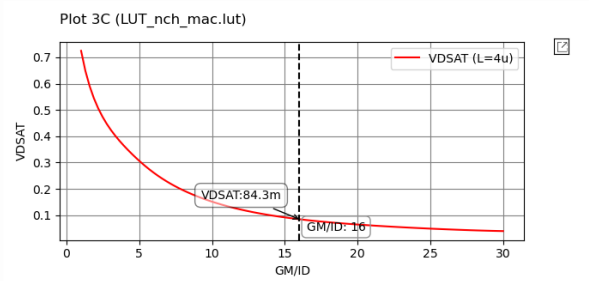
→ <u>Design of OTA input pair M1 and M2</u>

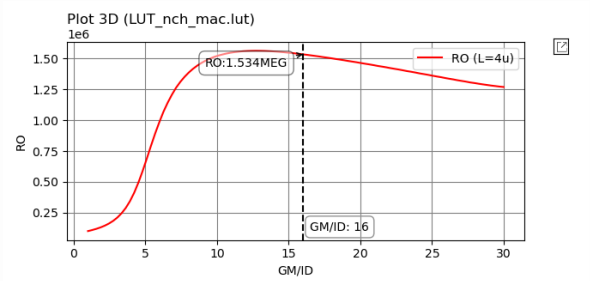
$$\text{Assume Large L} = 4\text{ um and large}\frac{gm}{I_D} = 16 \text{ to achive large output resistance and small } V_{GS} \text{ for } CMIR_L$$

$$@\ I_D = 5\text{ uA} \rightarrow W_{1,2} = 12.85\text{ um}$$







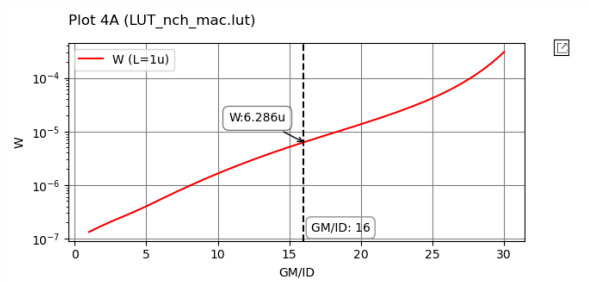


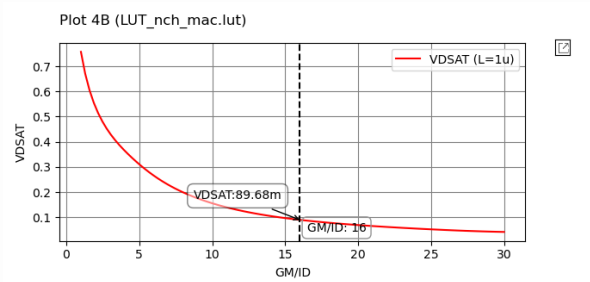
→ Design of the current mirror of first stage M5

$$CMIR_L = V_{GS1,2} + V_5^* \leq 480\ mV$$

$$V_5^* \leq 154.6\ mV \rightarrow \text{Choose } V_5^* = 125\ mV \rightarrow \frac{gm}{I_D} = 16$$

$$\text{Assume } L_5 = 1u \rightarrow W_5 = 6.286\ um$$

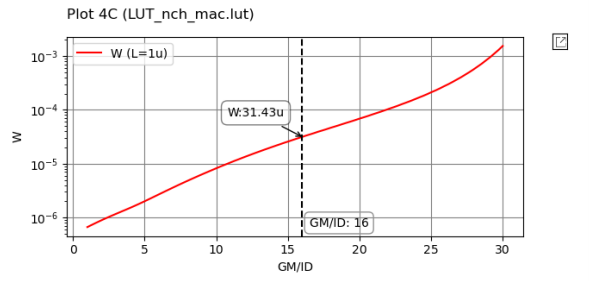


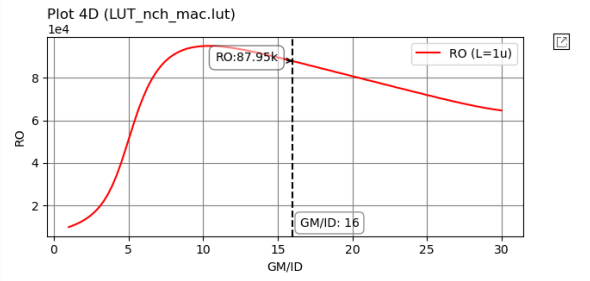


→ Design of the current mirror of second stage M7

$$\text{set } I_{B2} = 5I_{B1} = 50\ uA \rightarrow \text{to increase the PM}$$

$$\text{Choose } L_7 = L_5 \text{ and } V_{GS7} = V_{GS5}$$





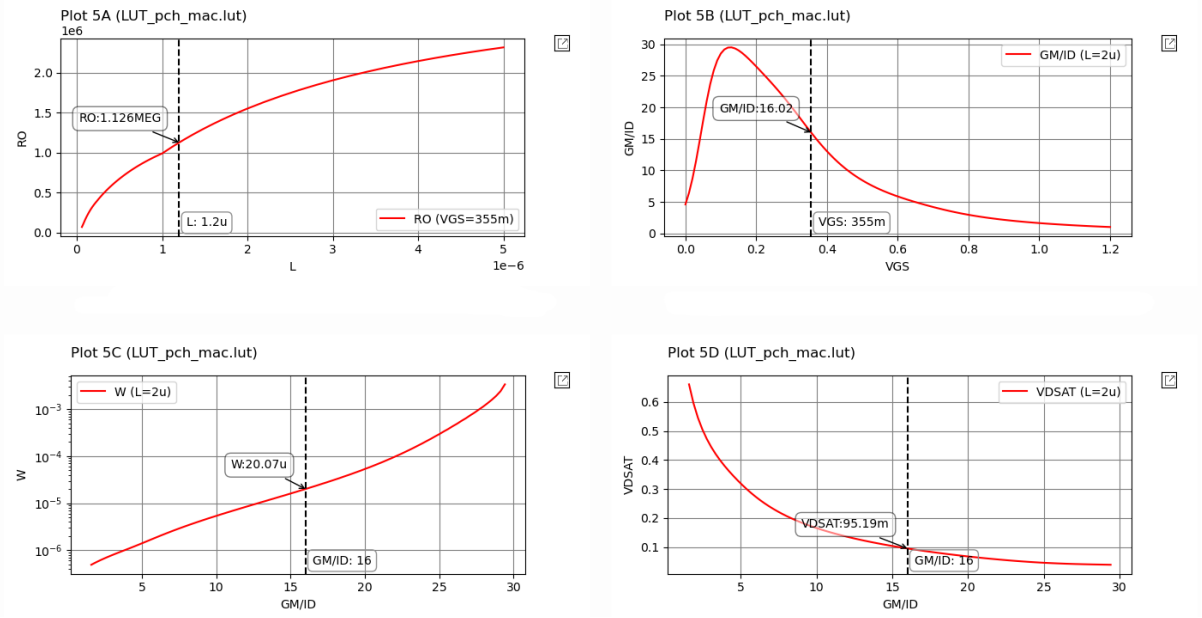
→ Design of the active load of first stage M3 and M4

$$A_{V_1} \geq 50 \rightarrow g_{m1,2} \times R_{out1} = g_{m1,2} \times r_{o1,2} || \, r_{o3,4} \geq 50$$

$$r_{o3,4} \geq 1.07M\ Ohm \rightarrow L_{3,4} \geq 1.2\ um$$

$$CMIR_H = V_{GS1,2} - V_{1,2}^* - V_{SG3,4} + V_{DD} = 850\ mV \rightarrow V_{SG3,4} \leq 0.4642\ V \rightarrow V_{GS3,4} = 0.355\ mV$$

$$\text{Choose } L_{3,4} = 2\ um \rightarrow W_{3,4} = 20.3\ um$$

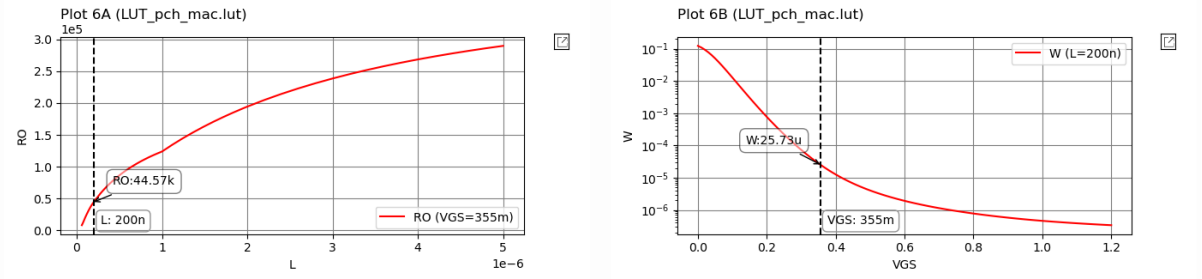


→ <u>Design of the input transistor of second stage M6</u>

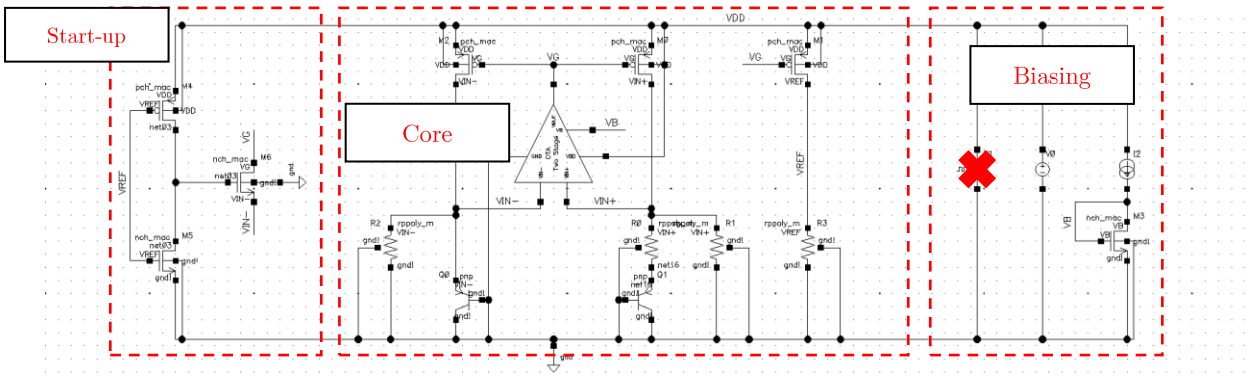
$$\text{use } \left(\frac{g_m}{I_D}\right)_6 = \left(\frac{g_m}{I_D}\right)_{3,4} \text{ to cancel the systematic offset}$$

$$A_{V_2} \geq 10 \rightarrow g_{m6} \times R_{out2} = g_{m6} \times r_{o6} || r_{o7} \geq 10 \rightarrow r_{o6} \geq 15k\ Ohm$$

$$\text{Choose } L_6 = 200\ nm \rightarrow W_6 = 25.73\ um$$

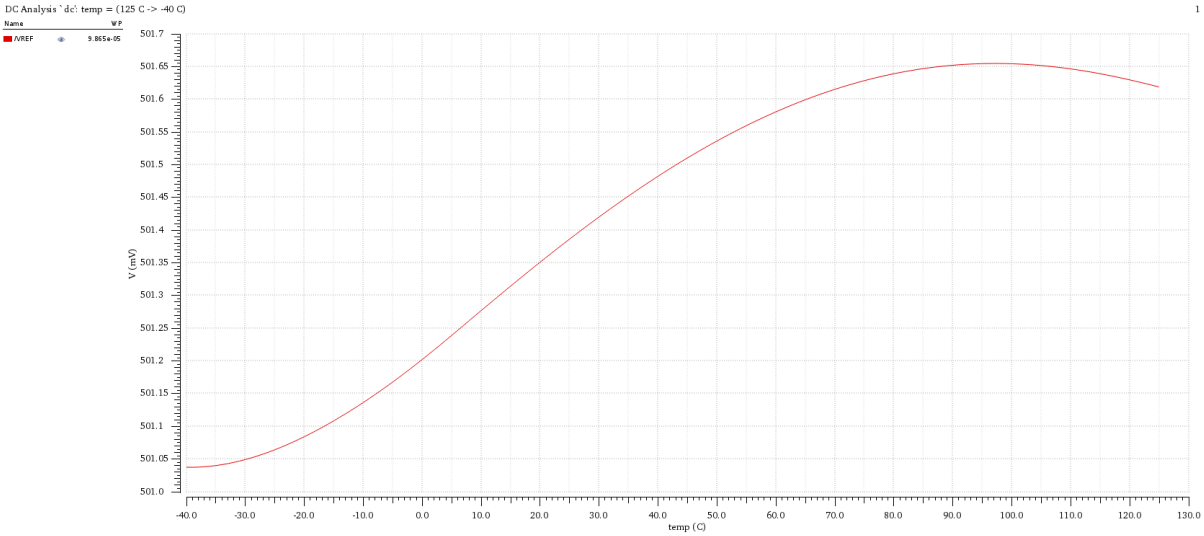


7. Schematic

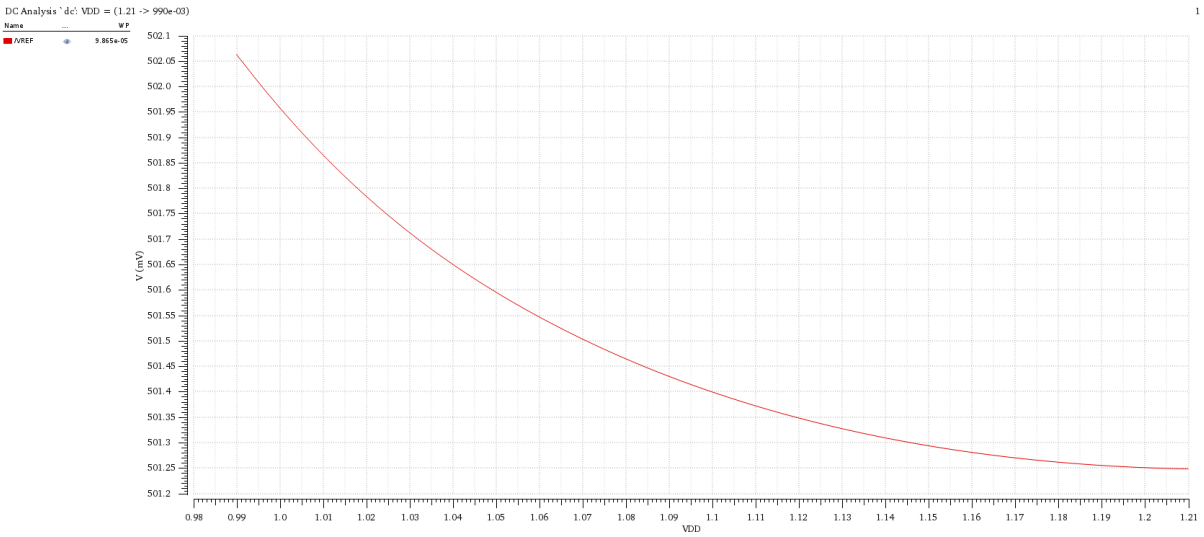


8. Results

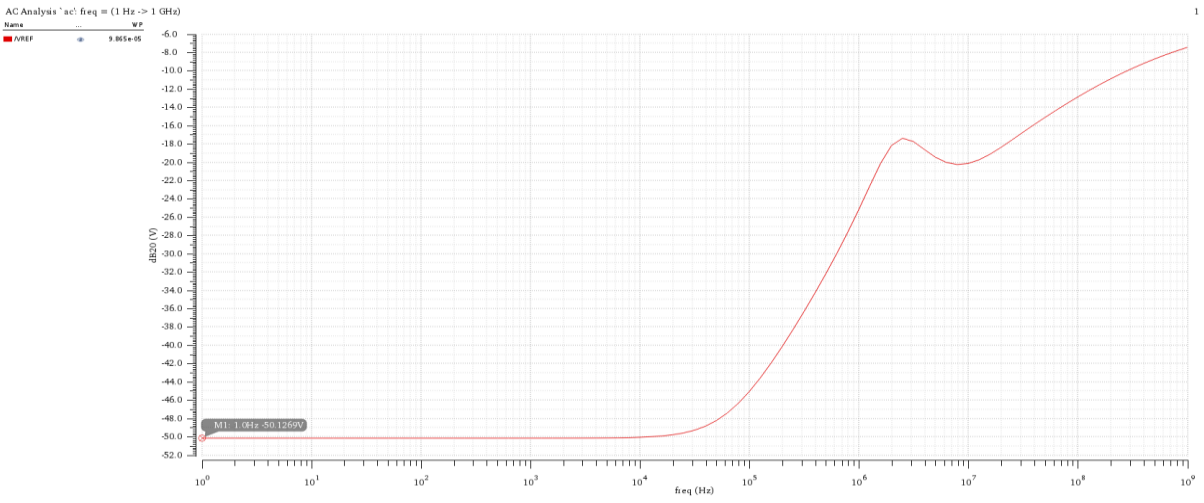
- VREF Vs Temp @ Nominal



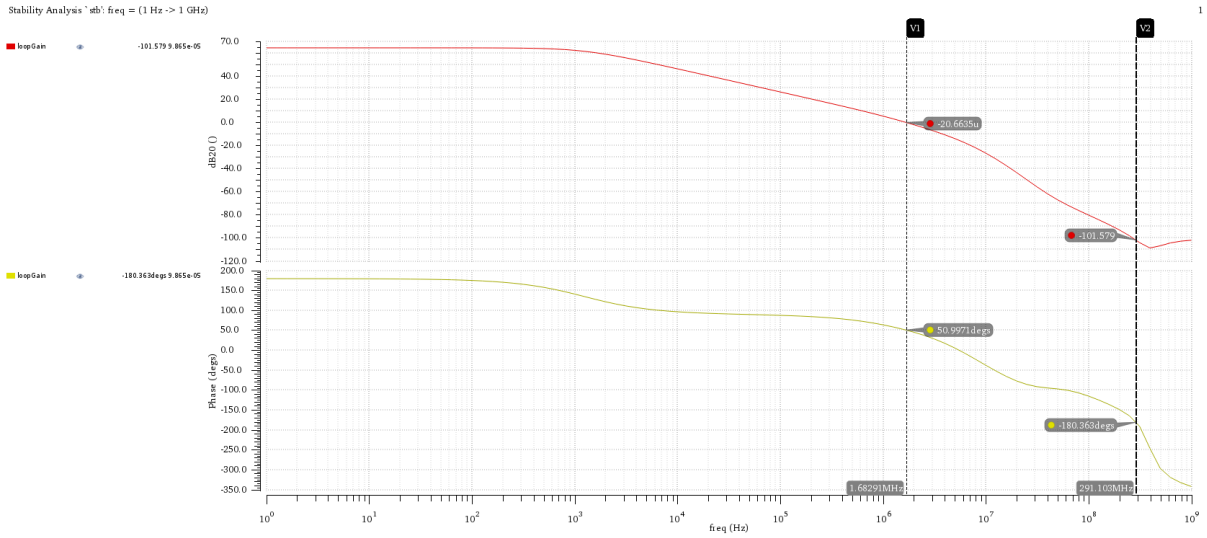
- VREF Vs VDD @ Nominal



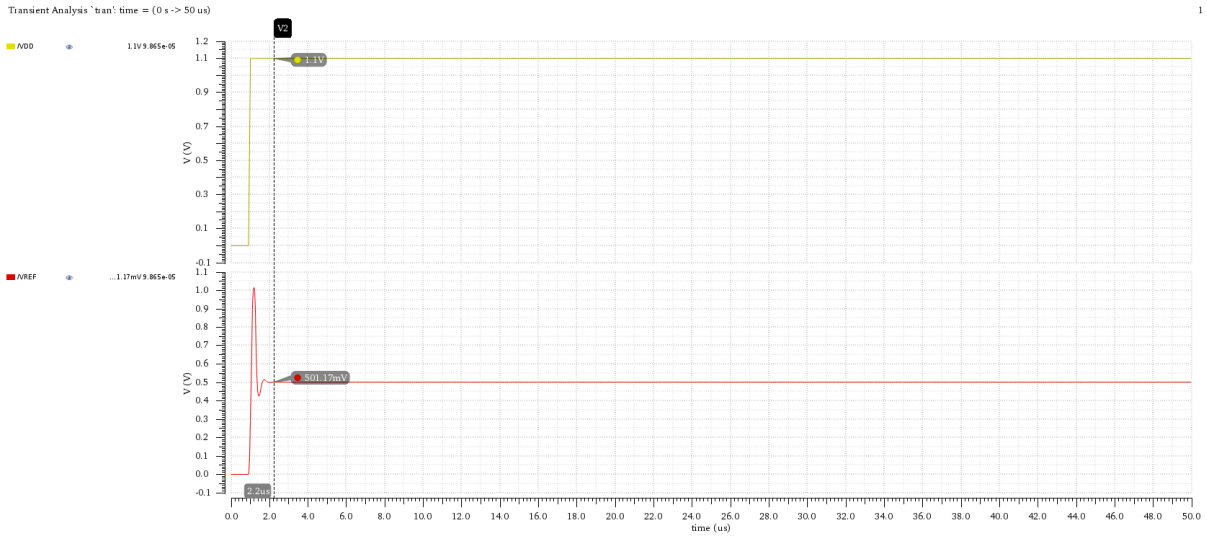
- PSR @ Nominal



- STB Analysis



- Startup time



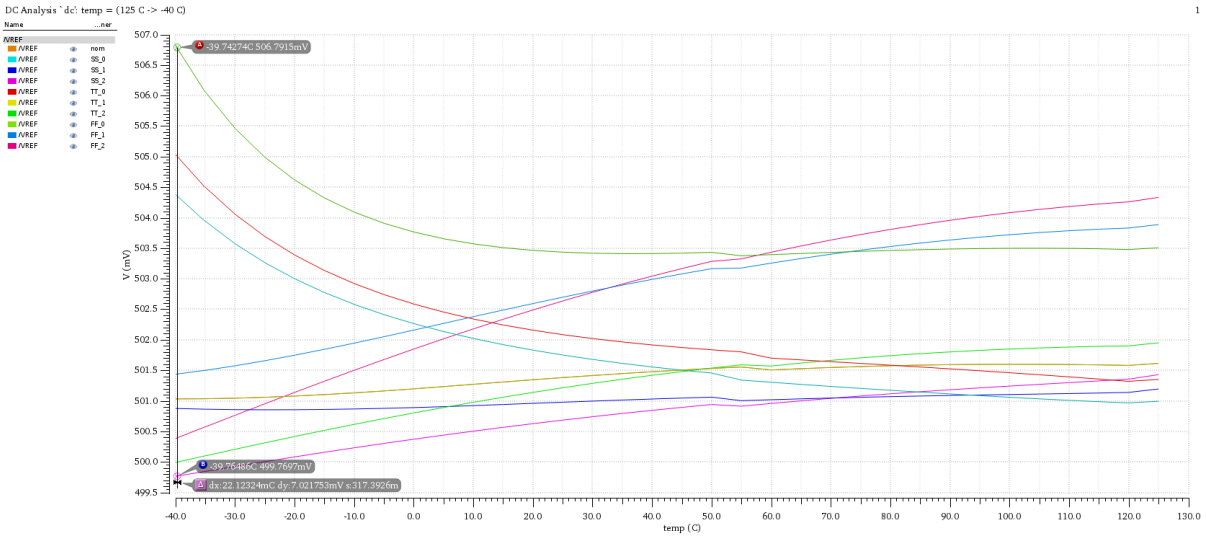
- Corners

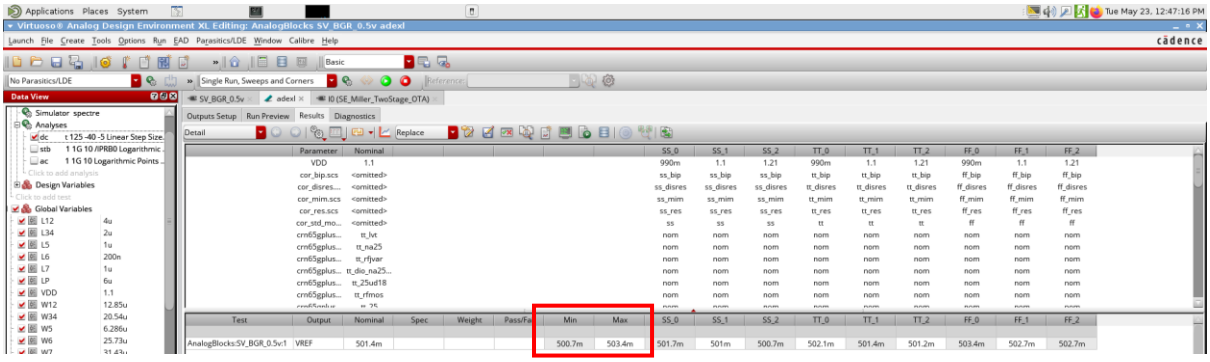
  - Setup

Corners Setup

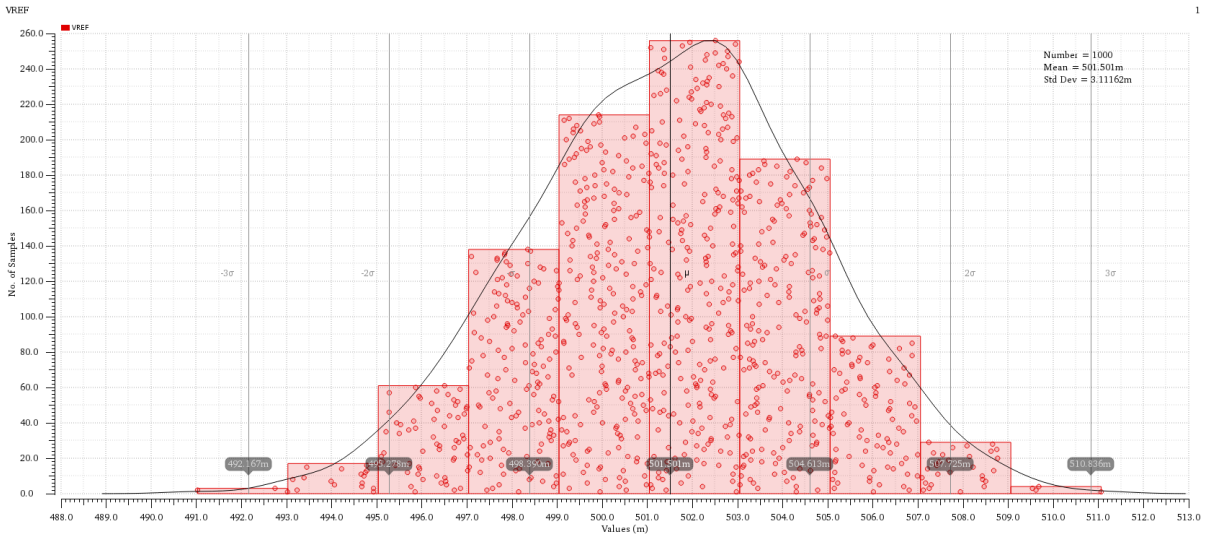
Corners	Nominal	SS	TT	FF
Temperature				
Design Variables				
VDD		0.99,1.1,1.21	0.99,1.1,1.21	0.99,1.1,1.21
Click to add				
Parameters				
Click to add				
Model Files				
cor_bip.scs		ss_bip	tt_bip	ff_bip
cor_mim.scs		ss_mim	tt_mim	ff_mim
cor_std_mos.scs		ss	tt	ff
cor_disres.scs		ss_disres	tt_disres	ff_disres
cor_res.scs		ss_res	tt_res	ff_res

- Variations

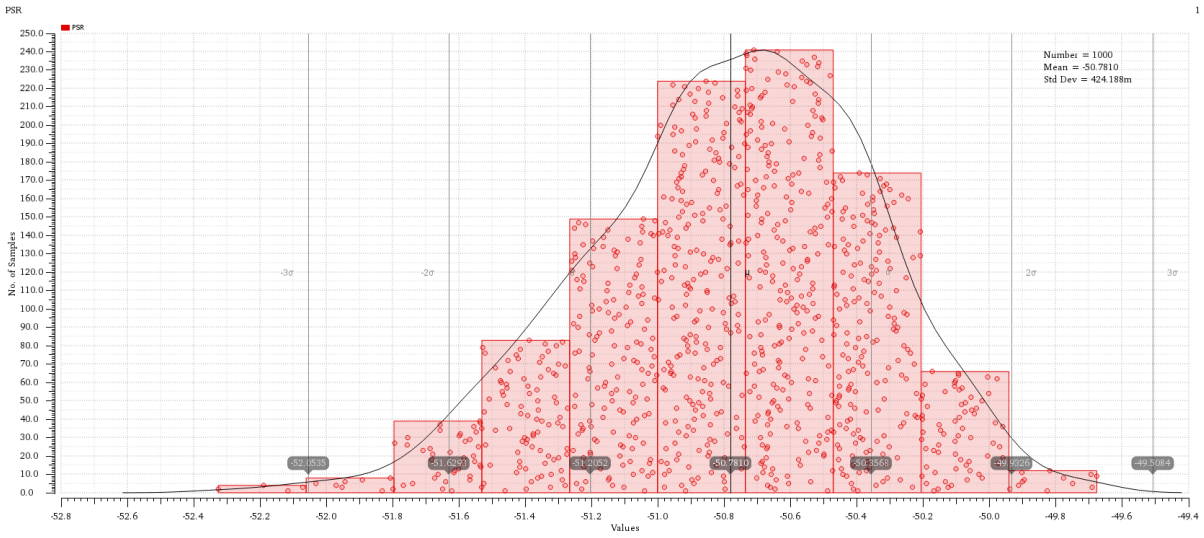




- VREF MC 1000 points



- PSR MC 1000 points



- PM MC 1000 points