ECE601 | Advanced Analog Integrated Circuits

Variable Gain Amplifier

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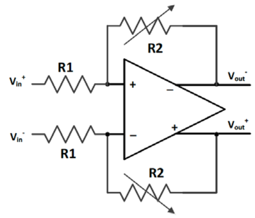
Task

In this project, you are required to implement a fully differential variable gain amplifier (VGA) based on the inverting amplifier shown below.



Requirements

Supply Voltage	1.2 V	BW	25 MHz
Programmable Gain	3dB : 5dB : 23dB	Output Swing	> 1.6 Vpp
Gain Error	< 1%	Input Referred Thermal Noise	< 100 uVrms
Load Capacitance	1.5 pF	PM Differential Loop	> 60º
Current Consumption	< 1.5 mA	PM Common-Mode Loop	> 45º

- Use two different common mode feedback circuits.
- Minimize area of your design
- Assume that you have a current source of 50μA coming from VDD (PMOS direction). Any voltages or currents needed should be generated from VDD or the current source using biasing circuits.

Design Procedures

Step 1 | Error Amplifier

01. The open loop gain of error amplifier depends on the maximum error we can accept in the closed loop gain

$$A_{VCL} = \frac{A_{VOL}}{1+\beta A_{VOL}} \rightarrow \text{ideally } A_{VCL} = \frac{1}{\beta}$$

$$\epsilon_s = \left|\frac{\text{Ideal} - \text{Actual}}{\text{Ideal}}\right| \rightarrow \frac{1}{100} \geq \left|\frac{\frac{1}{\beta} - \frac{A_{VOL}}{1+\beta A_{VOL}}}{\frac{1}{\beta}}\right| \approx \frac{1}{\beta A_{VOL}} \rightarrow \therefore \beta A_{VOL} \geq 100 = \ 40\text{ dB}$$

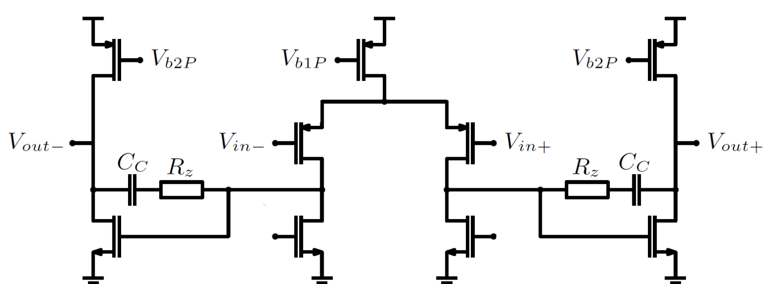
$$\text{for } \beta_{min} \rightarrow A_{VOL} \geq 1430 = 63\text{ dB}$$

02. The Unity gain frequency of the error amplifier is equal to the closed loop

$$\text{UGF} = A_{cl} \times BW_{cl} = A_{ol} \times BW_{ol}$$

$$14.2 \times 25\text{ MHz} = 1430 \times BW_{ol} \rightarrow \therefore\ BW_{ol} \geq 250\text{ kHz}$$

03. Since no spec on the CM input range so, I used PMOS input Stage, and for the differential OpAmp topology chosen is the Differential Two Stage Miller Compensated OTA due to its high gain and its higher output swing.



04. Since no constrains on CMIR → Choose PMOS input devices as they give better matching and better f_{nd}

05. General considerations

- $C_L = \alpha \times C_C \rightarrow$ Choose $\alpha = 2$ and $C_C = \beta \times C_{GS4} \rightarrow$ Choose $\beta = 3$ and $\omega_{p2}/\omega_u = \gamma \rightarrow$ Choose $\gamma = 2$

06. Since no constrains on CMIR → Choose PMOS input devices as they give better matching and better f_{nd}

07. Design Methodology

Choose α, β, and γ

Find min f_t required for specific GBW

Find L for 2nd stage input that achieve the required ft at gmoverID

For a gmoverID get
ID4 = ID/CGS * CGS6
W = ID4 * JD

From gmoverID charts find W3 and W5 and calc Av2 and Av1

M3,5 biased in SI with large L to increase mirroring accuracy and

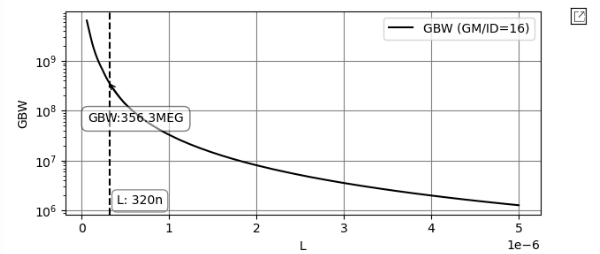
From γ get gm1 for chosen gmoverID

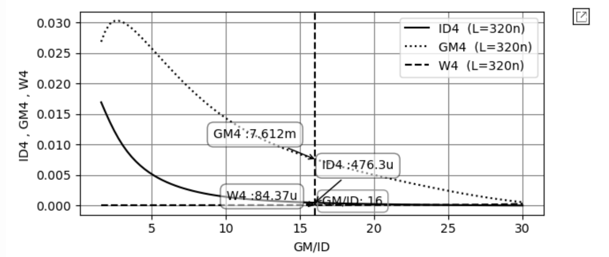
Set L2 = L4 and bias M2 at the same bias point as M4 to cancel systematic offset

Determine L1 needed to achieve Av1 at chosen gmoverID

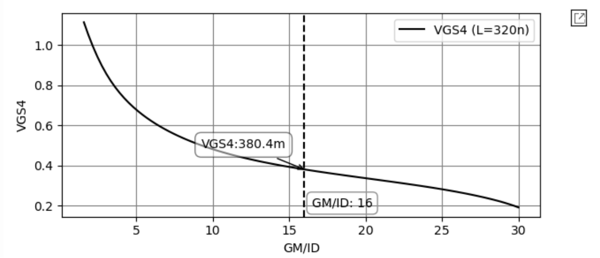
08. M4 Sizing

- $\because$ GBW $= \left({}^{g_{m1}}/_{2\pi \times C_c}\right)$ and $f_{nd} = \left({}^{g_{m4}}/_{2\pi \times C_L}\right) \rightarrow \therefore$ GBW $= \frac{f_{nd}}{\gamma} = {}^{g_{m4}}/_{2\pi \times \alpha\beta\gamma \times C_{gs4}} \rightarrow \therefore$ GBW $= {}^{f_{T4}}/_{\alpha \times \beta \times \gamma} = {}^{f_{T4}}/_{12}$
- Bias M4 @ MI $\rightarrow {}^{g_m}/_{I_D} = 16 \rightarrow L_6 = 320$ nm $\rightarrow I_{D6} = 476.3$ uA $\rightarrow W_6 = 84.37$ um $\rightarrow g_{m6} = 7.612$ mS $\rightarrow R_o = 7.5$ kΩ

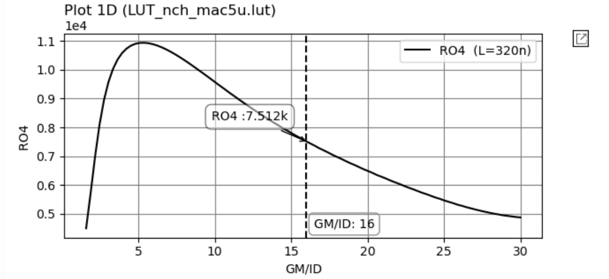




Plot 1C (LUT_nch_mac5u.lut)

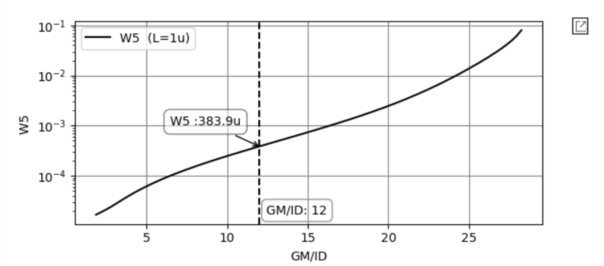


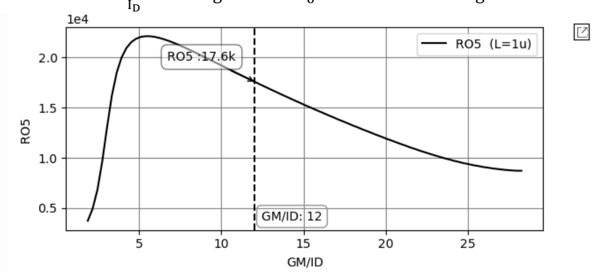
Plot 1D (LUT_nch_mac5u.lut)



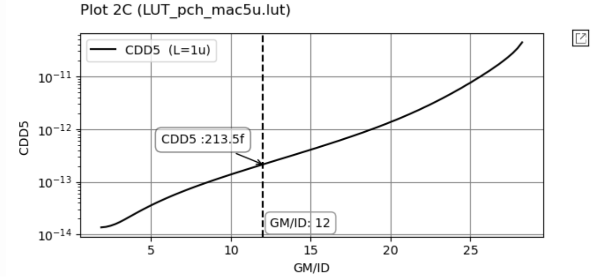
09. Sizing of Current Mirror M5

- Since no spec on CMRR → Assume relatively long $L_5 = 1$ um and bias it in SI $\frac{g_m}{I_D} = 12$ to get better R_o and better mirroring

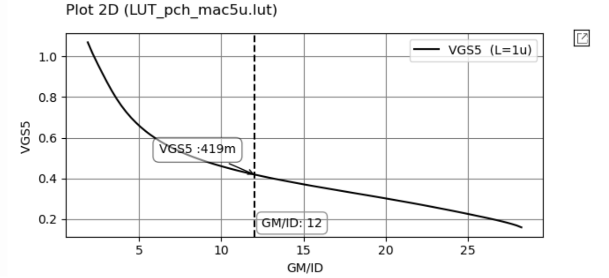




Plot 2C (LUT_pch_mac5u.lut)



Plot 2D (LUT_pch_mac5u.lut)

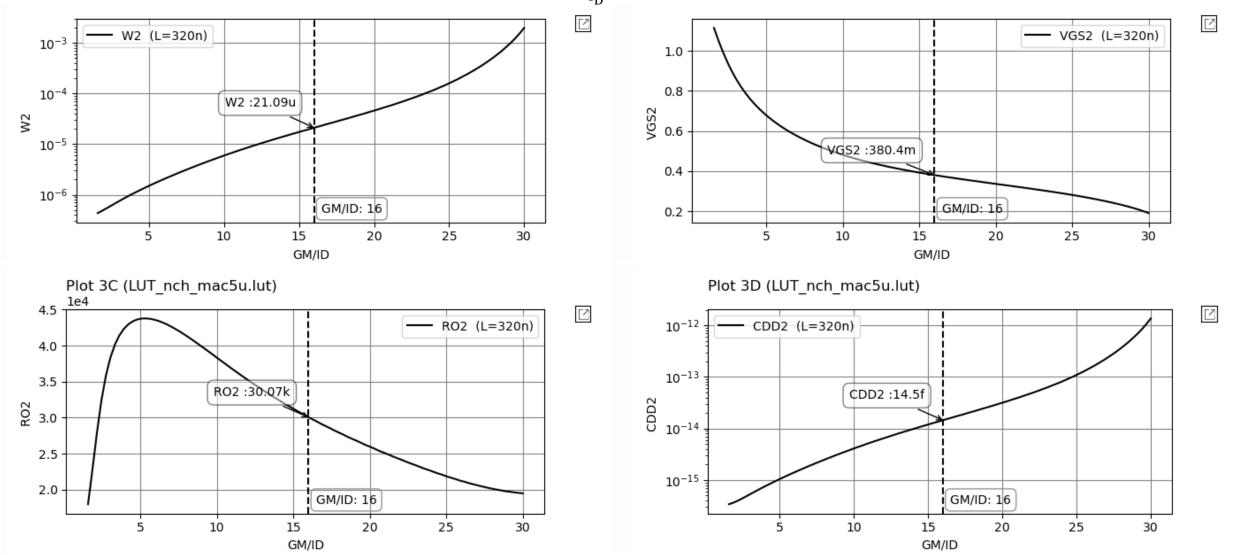


- $\because A_{V2} = g_{m4} \times (r_{o4} \parallel r_{o5}) = 40 \rightarrow A_{V1} = {}^{A_V}/_{A_{V2}} = 36$

10. Sizing of M2A, M2B

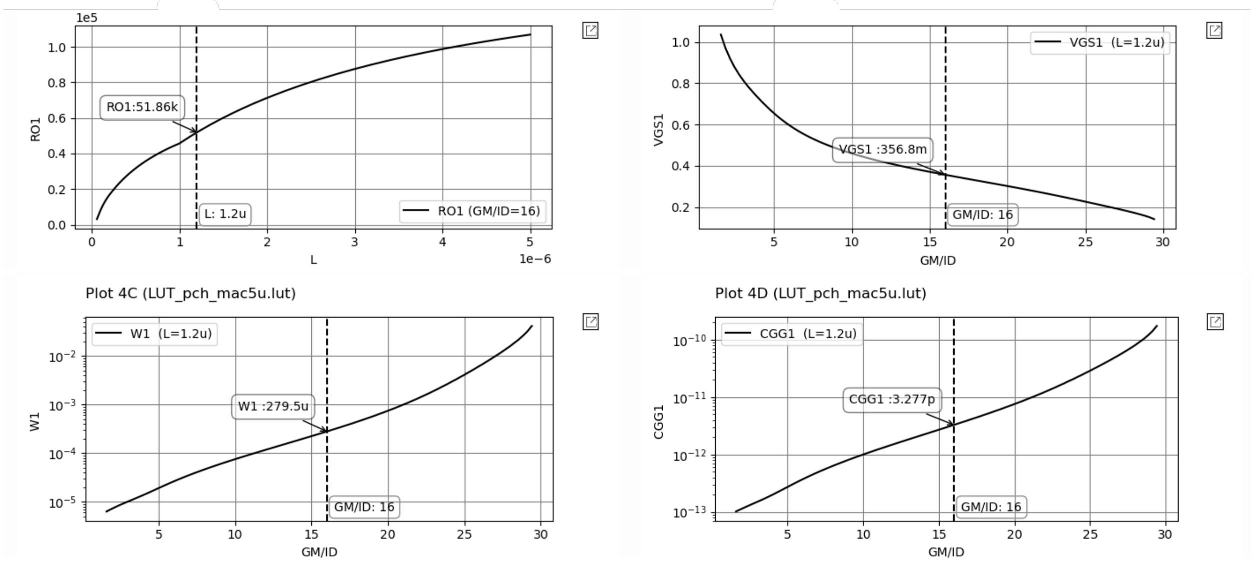
- $\because \omega_{p2}/\omega_u = 2 \rightarrow g_{m4}/g_{m1} = 4 \rightarrow g_{m1} = 1.9$ mS
- Biasing M1 in MI ${}^{g_{m1}}/_{I_D} = 16 \rightarrow I_{D1} = I_{D2} = 119$ uA $\rightarrow I_{B1} = 238$ uA

- set $L_2 = L_4 = 320$ nm and bias it at the same point ${}^{g_{m2}}/_{I_D} = 16 \rightarrow$ to cancel systematic offset $\rightarrow W_2 = 21.09$ um $\rightarrow R_{o2} = 30\ k\Omega$



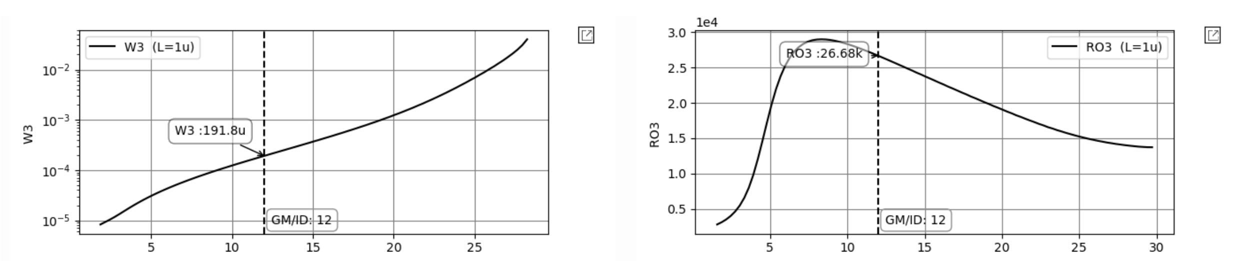
11. Sizing of M1A, M1B

- $A_{V1} = g_{m1} \times (r_{o1} \parallel r_{o2}) = 36 \rightarrow R_{o1} \geq 51\ k\Omega \rightarrow \because\ {}^{g_{m1}}/_{I_D} = 16 \rightarrow L_1 = 1.2$ um $\rightarrow W_1 = 279.5$ um and $V_{SG1} = 356.8$ mV



12. Sizing of Current Mirror M3

- $I_{D3} = 2I_{D1} = 238$ uA $\rightarrow$ Assume relatively long $L_3 = 1$ um and bias it in SI to get better mirroring ${}^{g_m}/_{I_D} = 12$



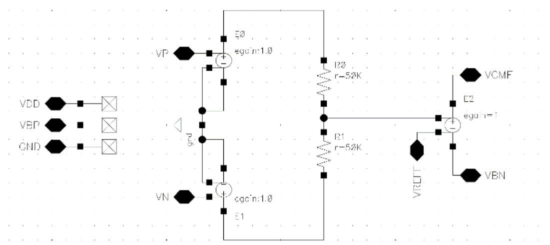
13. Sizing Summary

	M1A	M1B	M2A	M2B	M3	M4	M5
L	1.2 um	1.2 um	320 nm	320 nm	1 um	320 nm	1 um
W	279.5 um	279.5 um	21 um	21 um	191.8 um	84.37 um	383.9 um
gmoverID	16	16	16	16	12	16	12

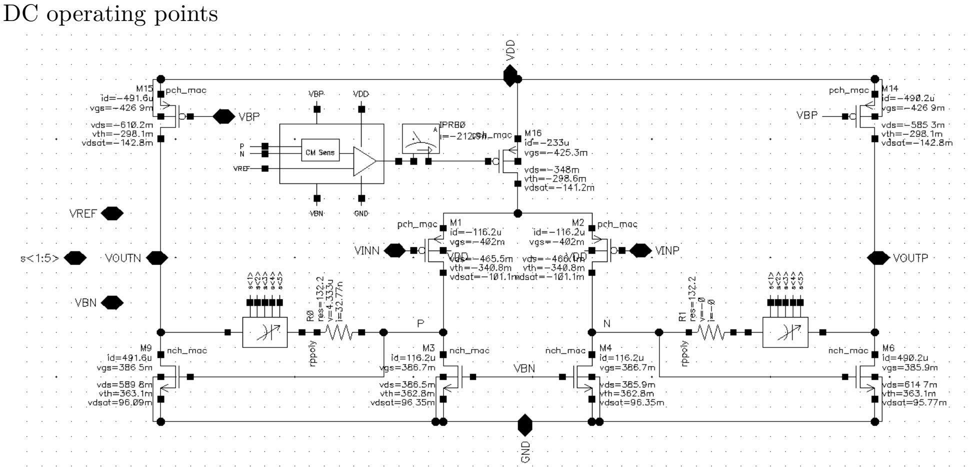
14. From the assumed V*, select suitable common mode input

$$-V_{SG1} - V_3^* + V_{DD} > V_{incm} > -V_{SG1} + V_1^* + V_{GS4} \rightarrow 0.67 > V_{incm} > 0.148.6$$

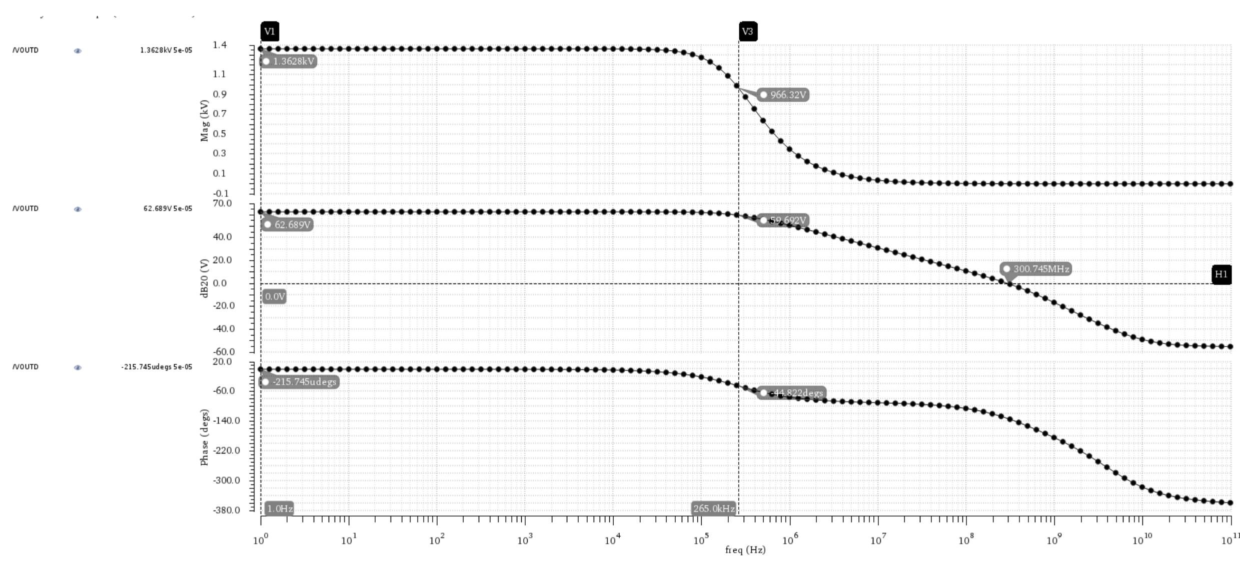
15. We will start with a behavioral CMFB network like the one shown below. We use ideal buffers to avoid loading the OTA output with the CM sensing resistors. Note that we don't need high gain in the CMFB loop; thus, we use a gain = 1 in the error amplifier



16. Apply DC operating points

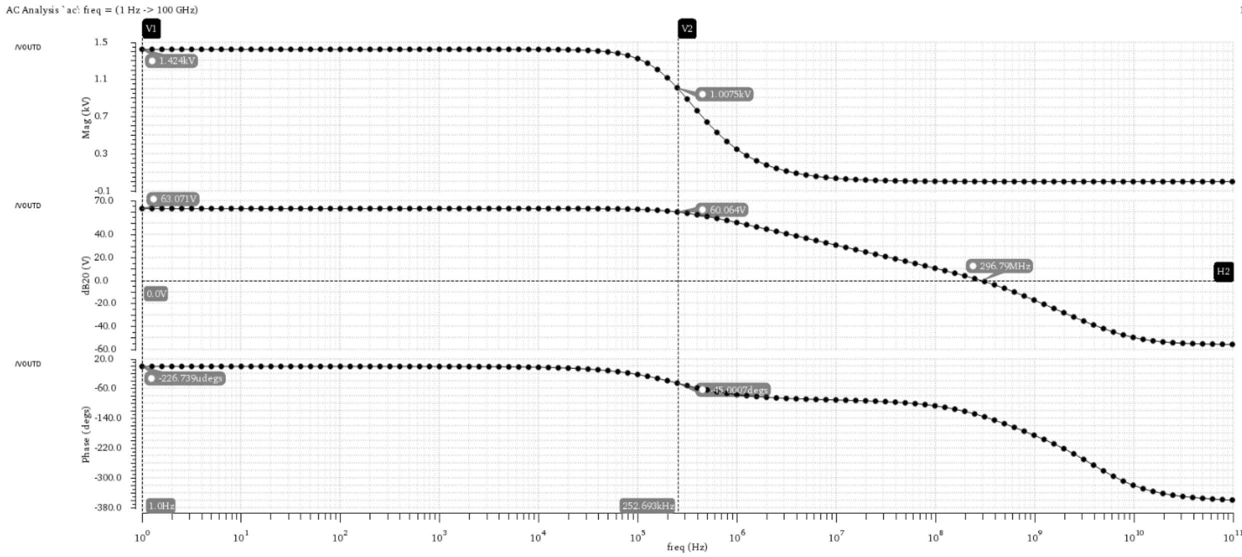


17. Apply AC Analysis



18. Fine Tuning

- The Required gain is not achieved and there’s a margin in the BW, so I increase the L2 from 320n to 330nm



Step 2 | Common Mode Feedback

<u>Circuit No1 : Buffered CMFB</u>

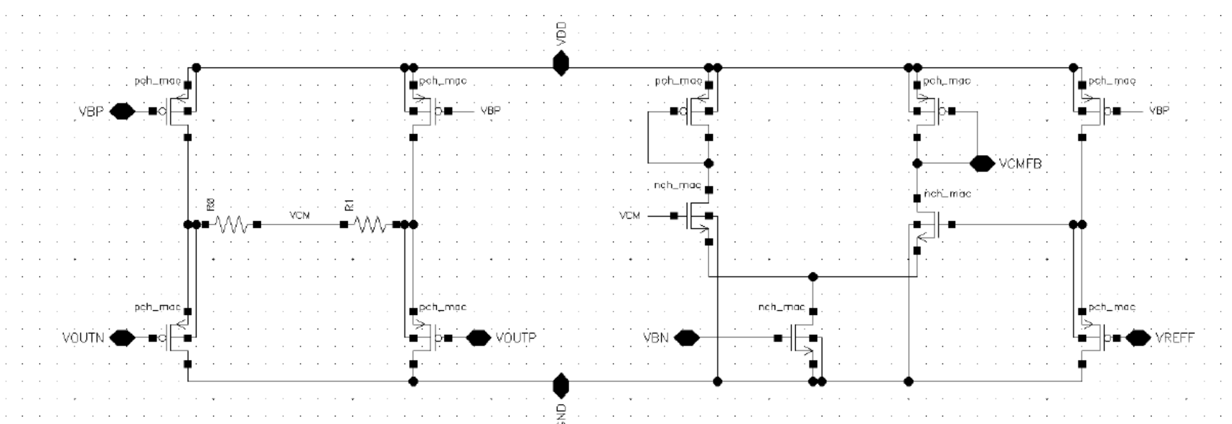
- 20uA current is divided between the CMFB branches. I assumed L = 1um and gm/ID = 15 for all transistors with unknown L or gm/ID for simplicity

- The CD (buffers) were used to buffer the OTA output to avoid loading the OTA with sensing resistors.

- The 20µA current was chosen to be distributed unequally among the branches, where the differential pair transistors were designed to get higher current to increase the differential input range and avoid full steering of the current [5.5µA was chosen for each branch of the differential pair and 3µA in the other branches].

- The sensing resistors are chosen such that the max current lowing through them (when diff sig is max) is less than the CD bias current, this avoids starving the CD when the diff output sig has its max excursion

- An extra buffer was used for Vref such that it experiences the same VSG shift as the OTA output

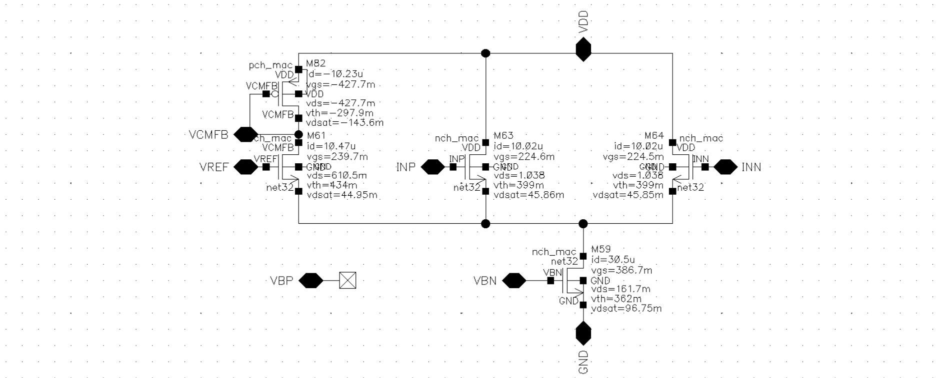


<u>Circuit No2 : Comparator CMFB</u>

- CM sensing circuit rejects differential signals as long as the sensing differential pair remains linear

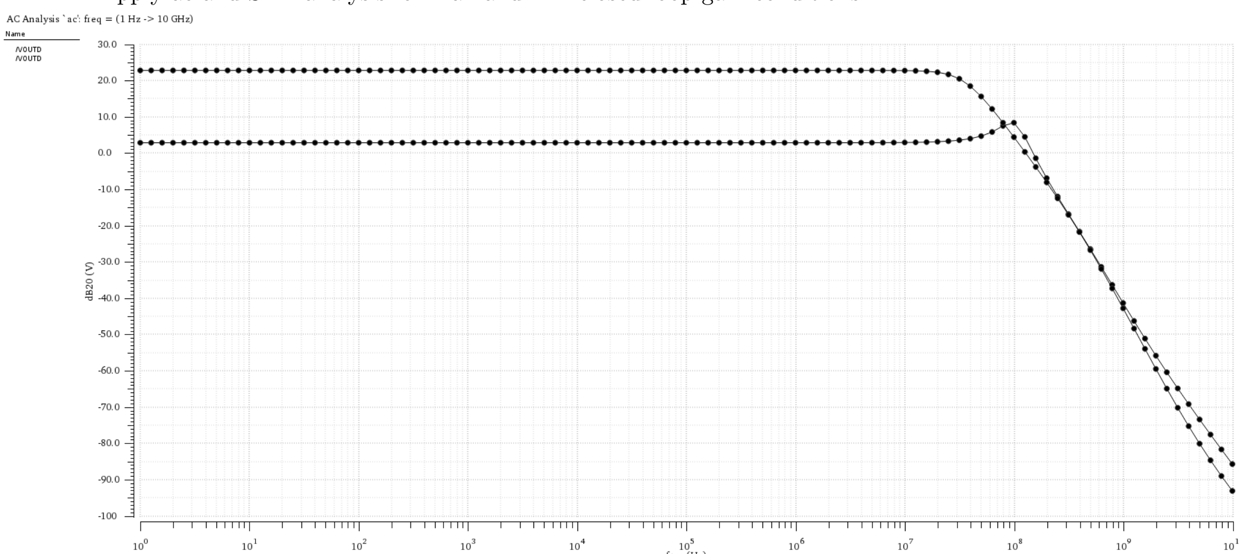
- Choose Veff of sensing MOSs large enough to sustain largest possible output swing.

- 30uA current is divided between the CMFB branches equally.



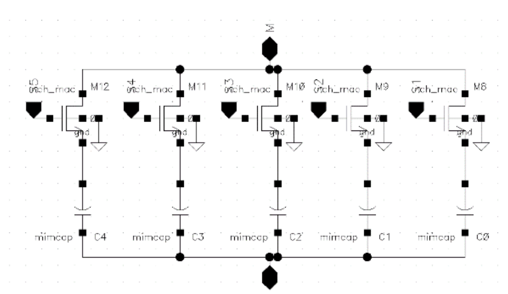
Step 3 | Closed loop Feedback

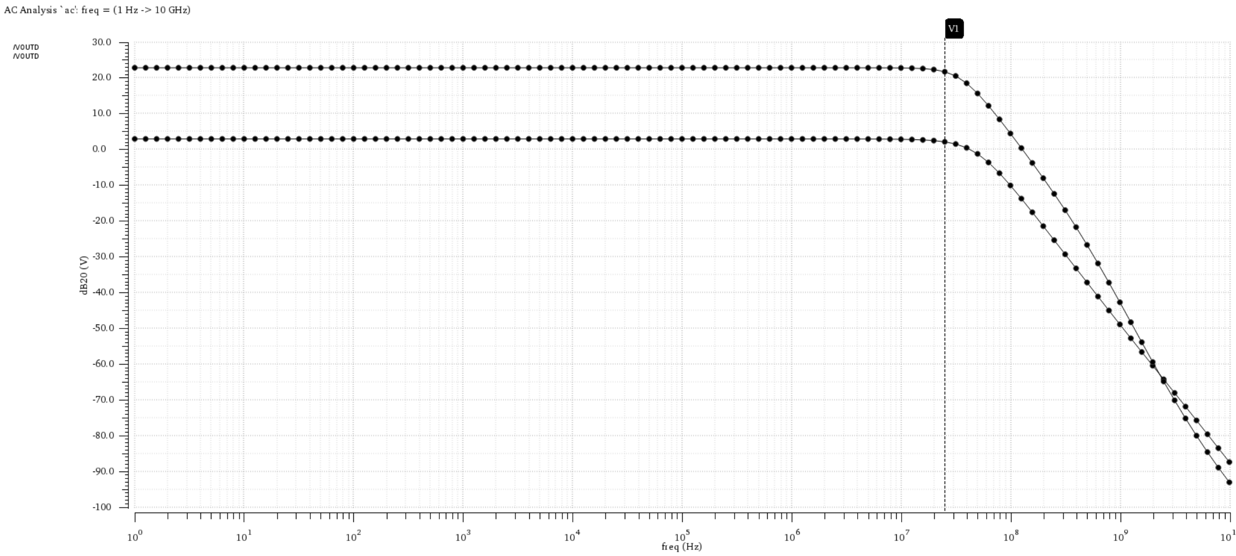
1. Apply ac and STB analysis for max and min closed loop gain conditions



At Higher gain both BW and PM requirements are achieved with the required accuracy but at lower gain, the PM is about 30 degree which doesn't meet the requirements and the BW is extended beyond the spec so, the compensation capacitor needs to be tuned between the max and min gain settings

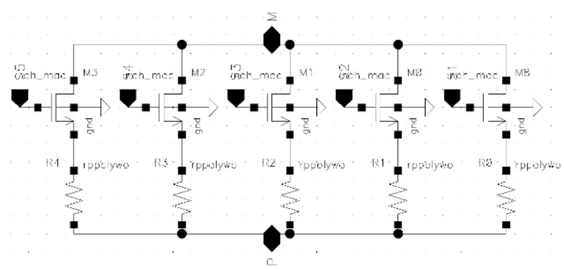
2. Programable Cc





With programmable Cc we achieve the required STB PM at the required BW

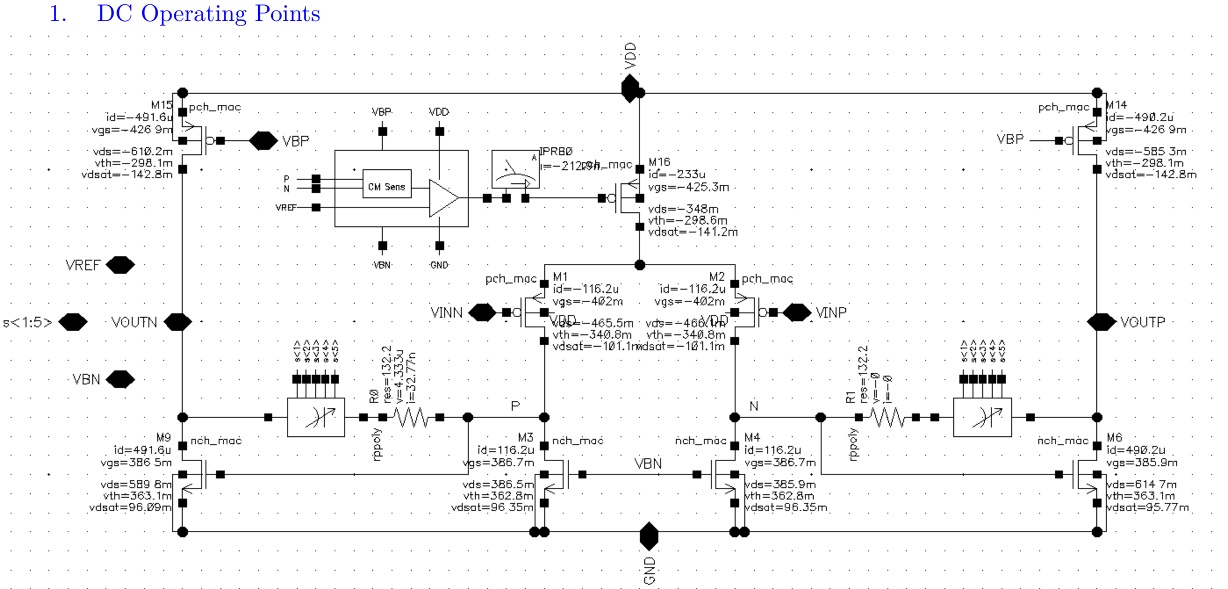
3. Resistor Bank



The feedback resistance will be a bank of resistors in parallel where R varies from 3.3 kΩ to 14.2 kΩ and Rin = 1 kΩ

Step 4 | Reporting

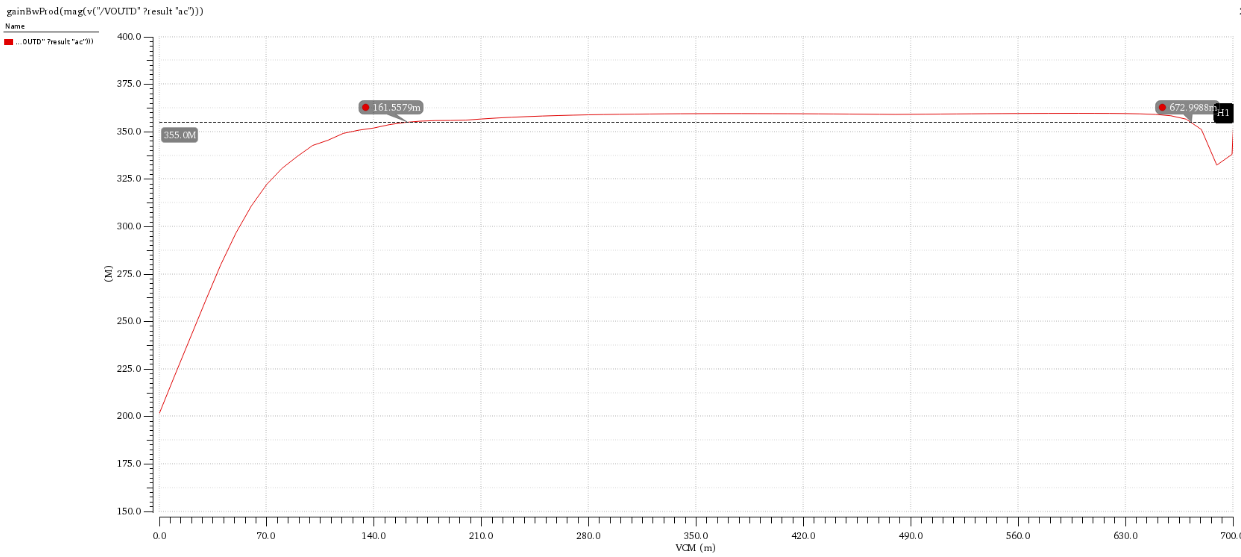
1. DC Operating Points



2. Calculate the Op-amp's input common-mode range and total power consumption.

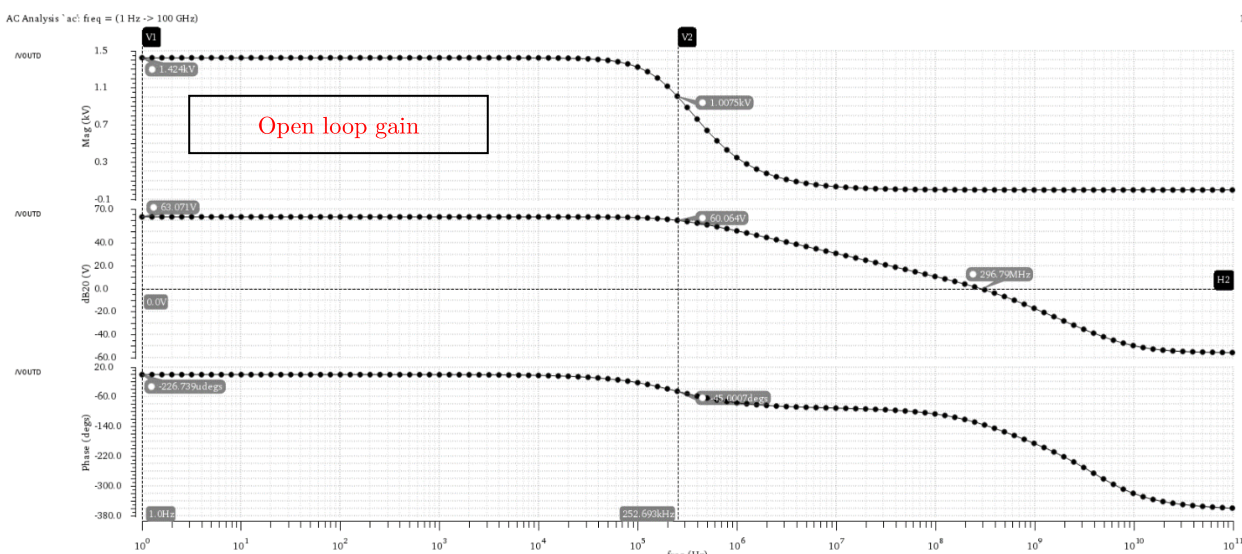
$$-V_{SG1} - V_3^* + V_{DD} > V_{incm} > -V_{SG1} + V_1^* + V_{GS4}$$

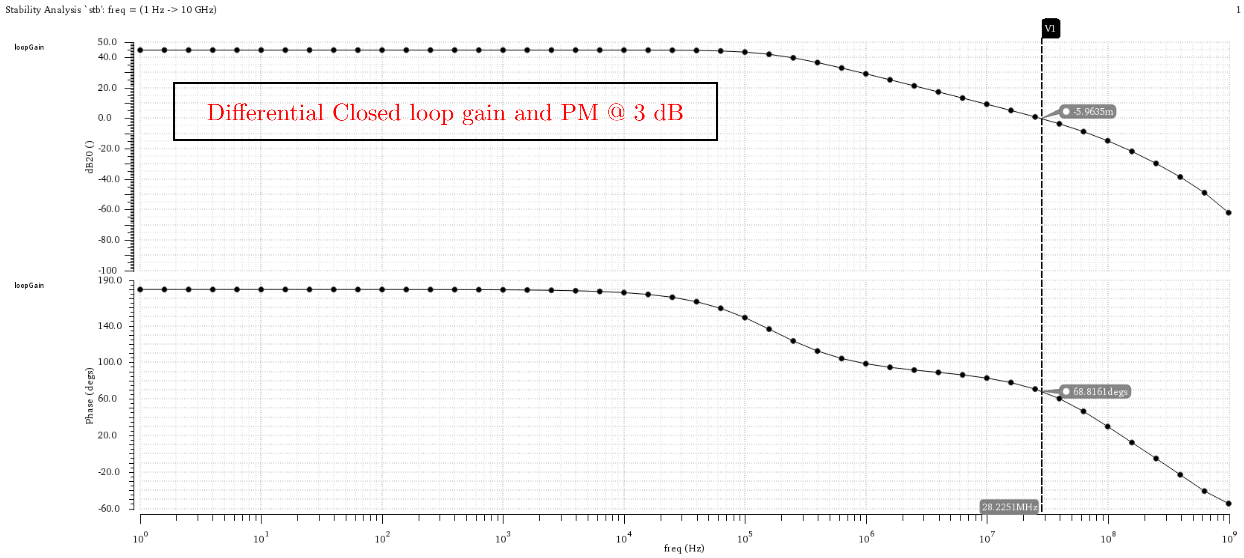
$$0.67 > V_{incm} > 0.148$$

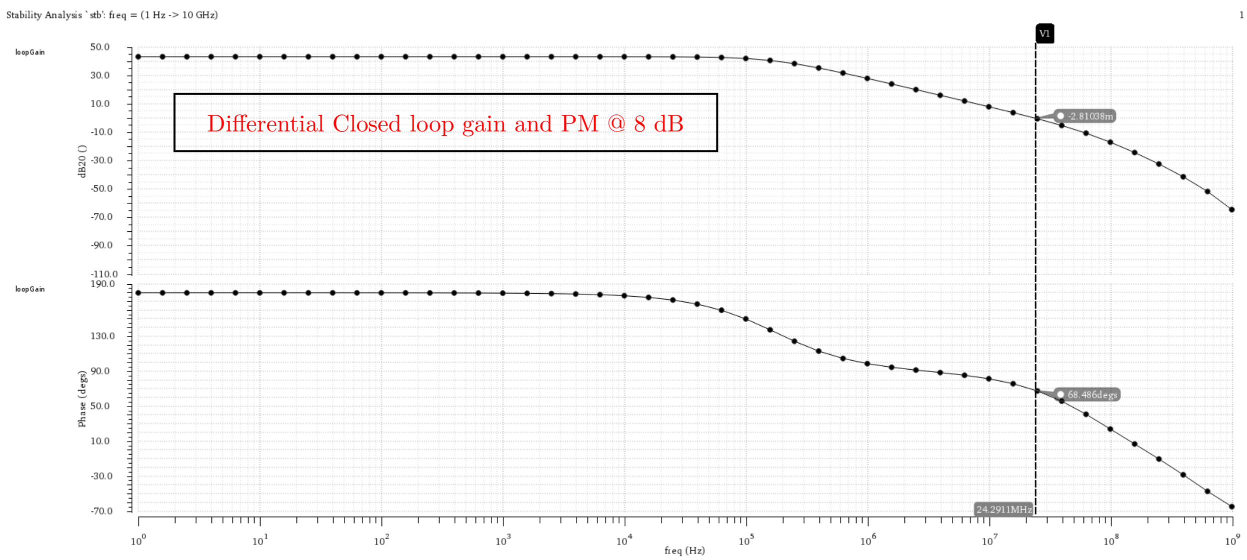


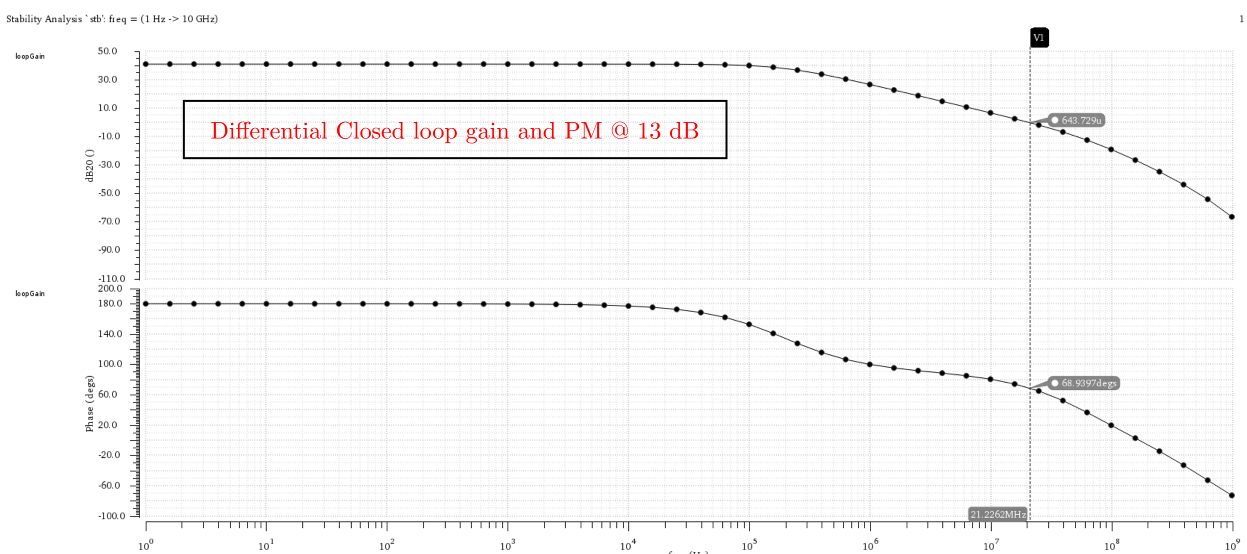
Total current consumption for the amplifier and the common mode feedback circuit is 1.34 mA which equal 1.608 mW

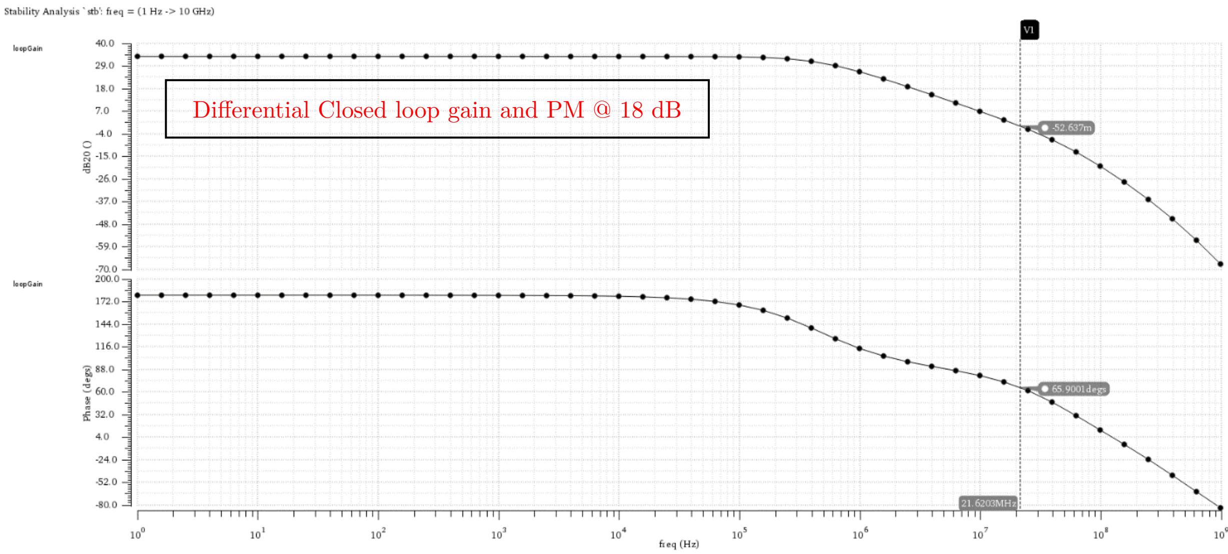
3. Plot the AC response (gain, phase) of the open loop (use stability analysis of Cadence) for all gain settings. Show the GBW and PM of the differential loop and the common-mode feedback loop.

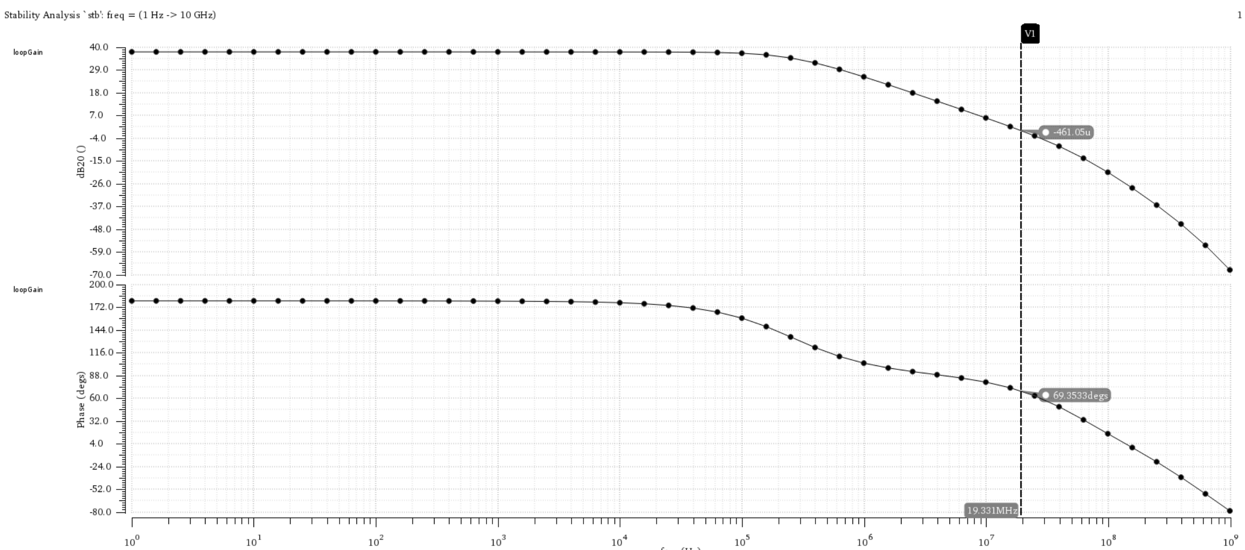


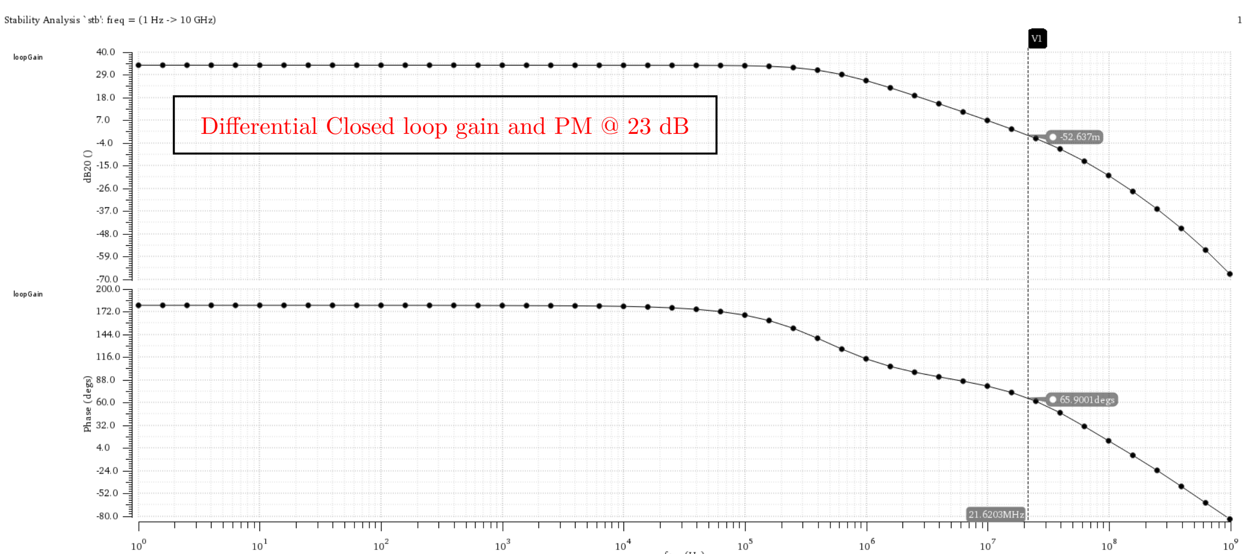

Stability Analysis `stb': freq = (1 Hz -> 10 GHz)
Differential Closed loop gain and PM @ 3 dB
V1
-5.9635m
68.8161degs
28.2251MHz
freq (Hz)
dB20 ()
Phase (degs)
loopGain


Stability Analysis `stb': freq = (1 Hz -> 10 GHz)
Differential Closed loop gain and PM @ 8 dB
V1
-2.81038m
68.486degs
24.2911MHz
freq (Hz)
dB20 ()
Phase (degs)
loopGain


Stability Analysis `stb': freq = (1 Hz -> 10 GHz)
Differential Closed loop gain and PM @ 13 dB
V1
643.729u
68.9397degs
21.2262MHz
freq (Hz)
dB20 ()
Phase (degs)
loopGain


Stability Analysis `stb': freq = (1 Hz -> 10 GHz)
Differential Closed loop gain and PM @ 18 dB
loopGain
dB20 ()
Phase (degs)
V1
-52.637m
65.9001degs
21.6203MHz
freq (Hz)

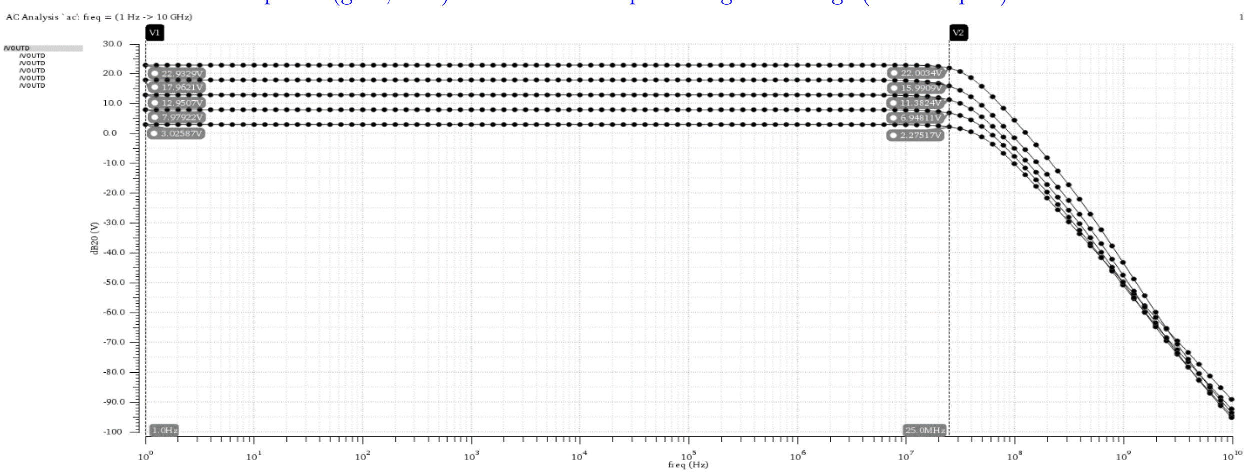

Stability Analysis `stb': freq = (1 Hz -> 10 GHz)
loopGain
dB20 ()
Phase (degs)
V1
-461.05u
69.3533degs
19.331MHz
freq (Hz)


Stability Analysis `stb': freq = (1 Hz -> 10 GHz)
Differential Closed loop gain and PM @ 23 dB
loopGain
dB20 ()
Phase (degs)
V1
-52.637m
65.9001degs
21.6203MHz
freq (Hz)

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: Decoder_value=1						
1	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	PM CM Loop	55.81		@ 23 dB	
1	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	GBW CM Loop	5.262M			
Parameters: Decoder_value=3						
2	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	PM CM Loop	64.61		@ 18 dB	
2	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	GBW CM Loop	3.141M			
Parameters: Decoder_value=7						
3	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	PM CM Loop	65.62		@ 13 dB	
3	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	GBW CM Loop	2.639M			
Parameters: Decoder_value=15						
4	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	PM CM Loop	63.3		@ 8 dB	
4	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	GBW CM Loop	2.506M			
Parameters: Decoder_value=31						
5	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	PM CM Loop	60.11		@ 3 dB	
5	AnalogIC:FINAL_FD_TWO_STAGE_MILLER_OTA_CL_TB:1	GBW CM Loop	2.521M			

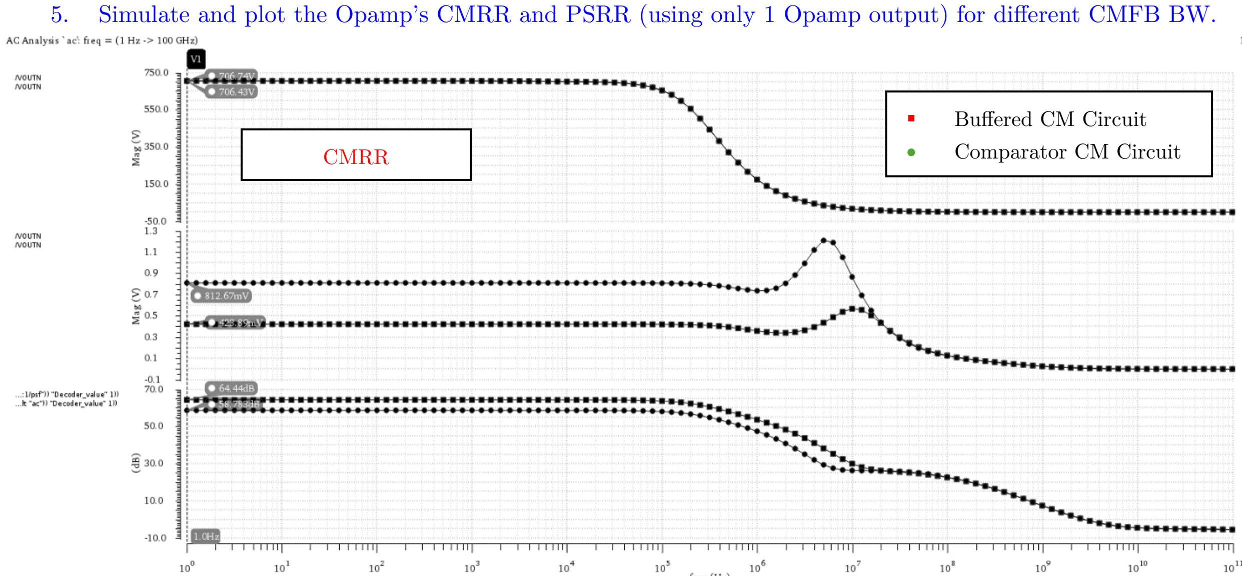
- The Differential STB Phase Margin is within 65.9 and 68.9 degree which is within the specs
- The Common-Mode STB Phase Margin is within 55.8 and 65.6 degree which is within the specs

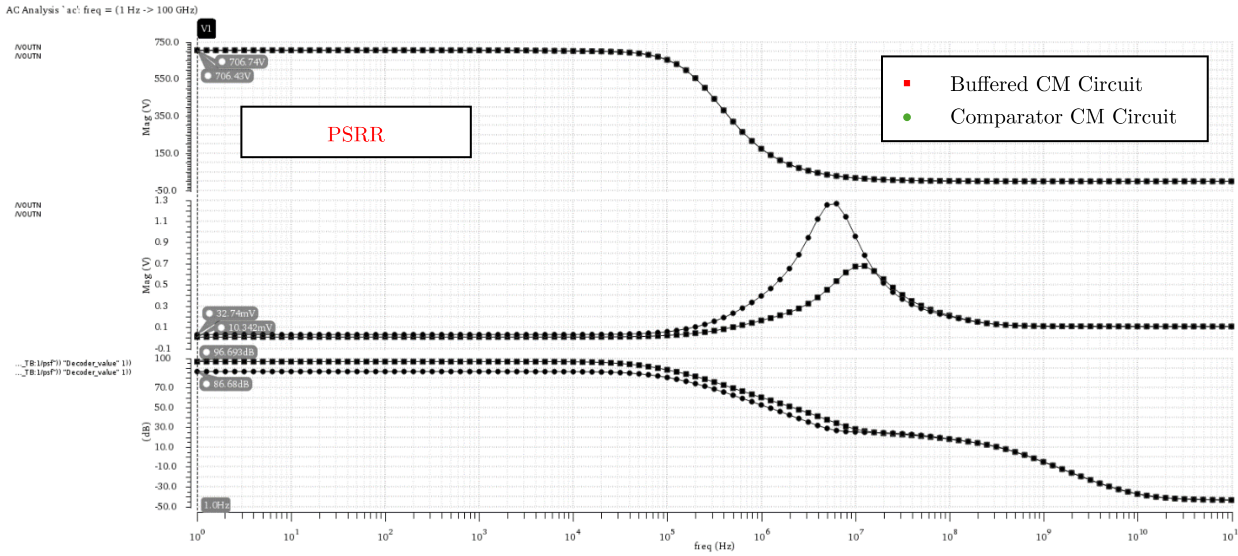
4. Plot the AC response (gain, BW) of the closed loop for all gain settings (in same plot).



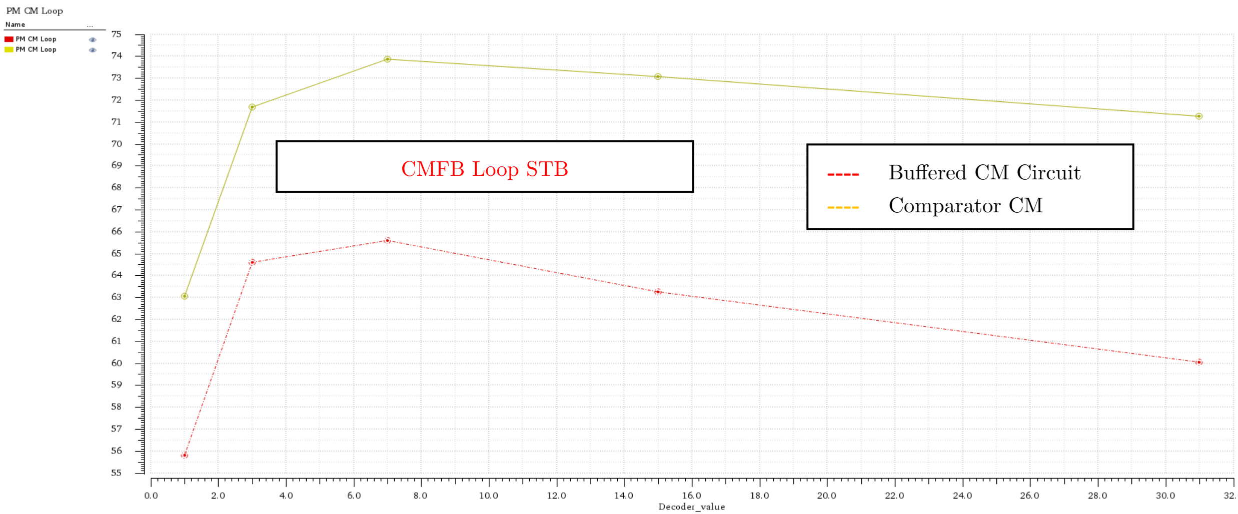
- Figure shows the different gain states and shows that within the Bandwidth which is 25 MHz the error in gain is less than 1%

5. Simulate and plot the Opamp's CMRR and PSRR (using only 1 Opamp output) for different CMFB BW.

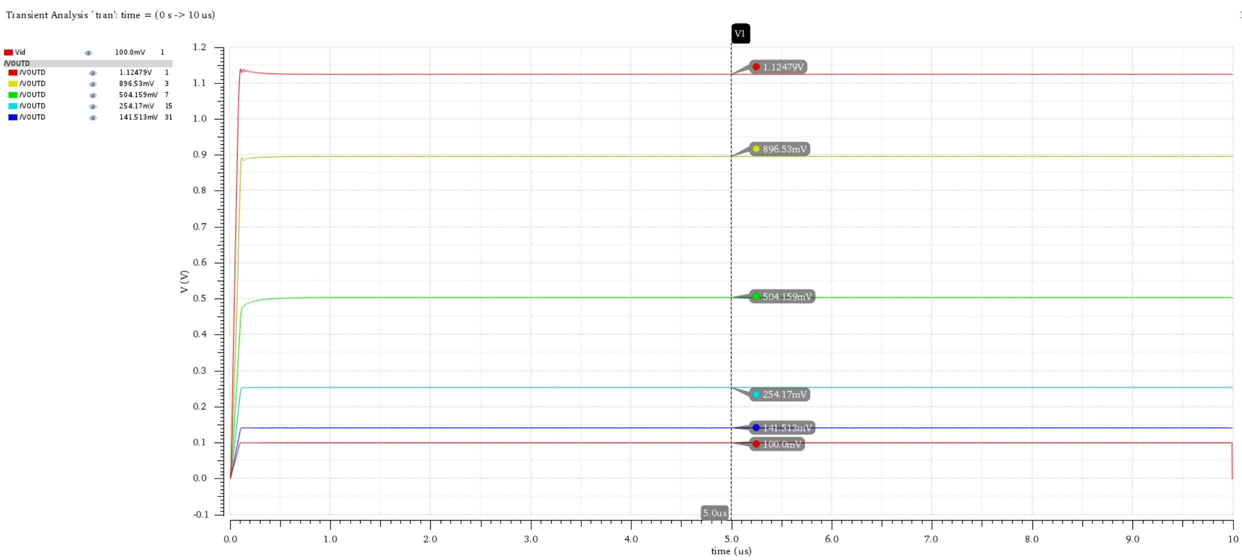




6. Compare performance of different common feedback circuits used in terms of stability, CMRR, PSRR, effect on differential gain (you have to run Monte-Carlo in order to get effect of mismatch)

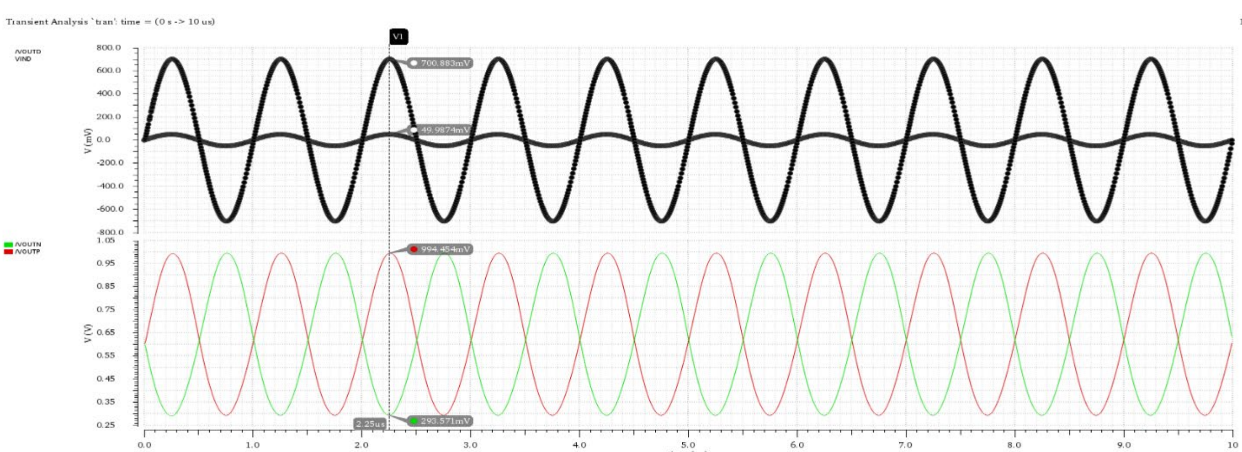


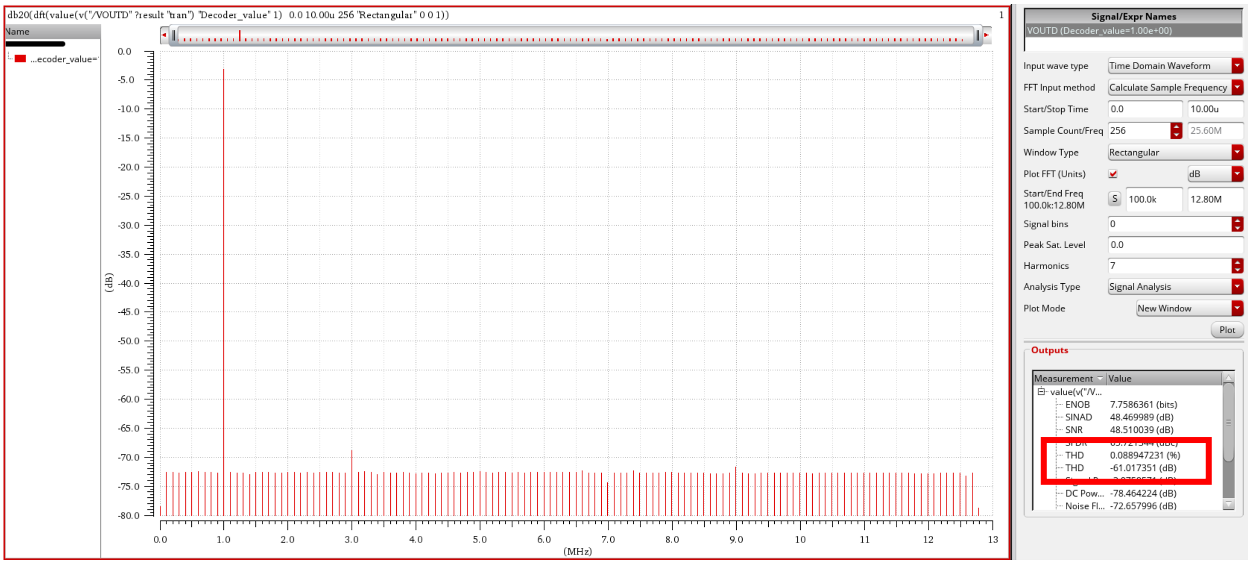
7. Plot the transient response for a small differential step input (100mV) for all gain settings (in same plot).



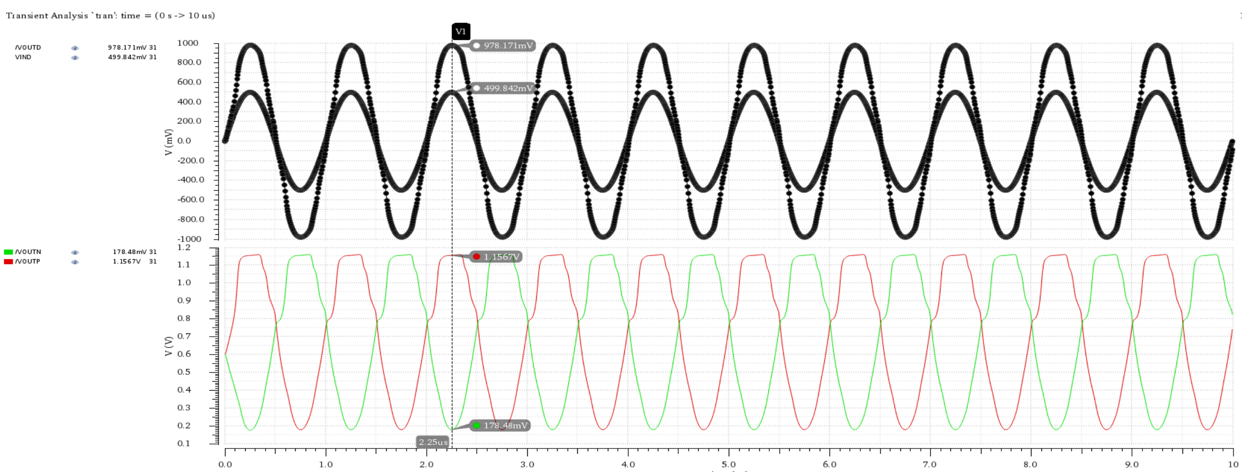
8. Plot the transient response (single-ended outputs and differential output) for the following inputs

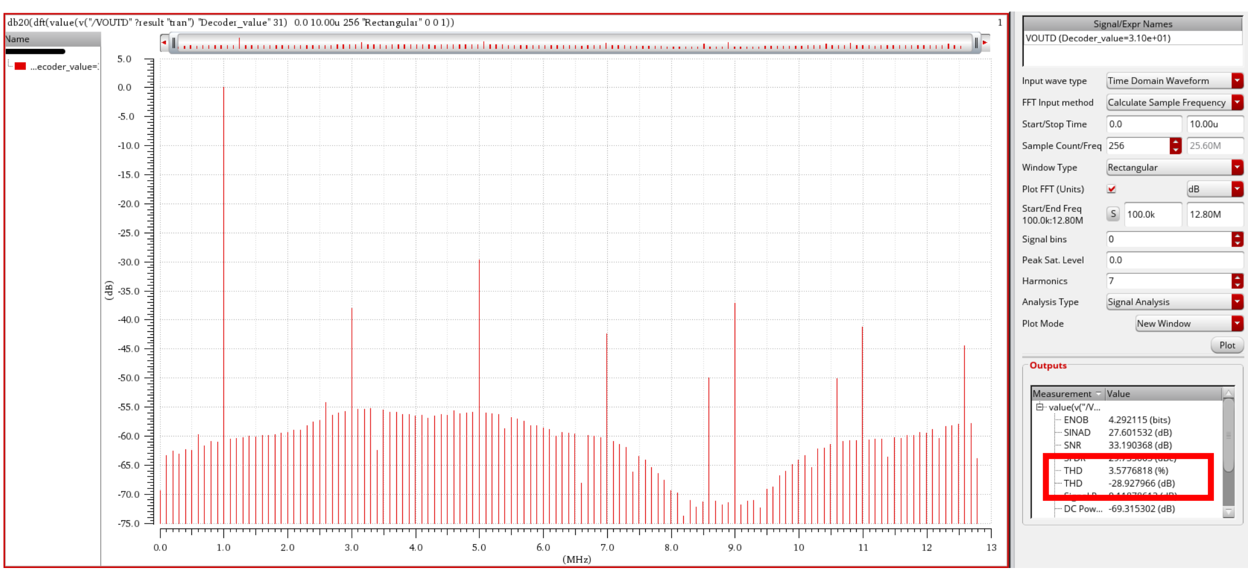
a. Sine signal of 100mVpp (differential) at 1MHz and max gain. Plot DFT (in log scale) and calculate THD in dB.



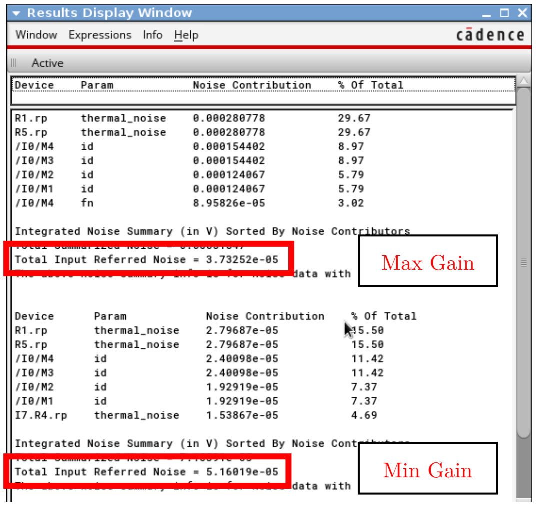


b. Sine signal of 1Vpp (differential) at 1MHz and min gain. Plot DFT (in log scale) and calculate THD in dB.



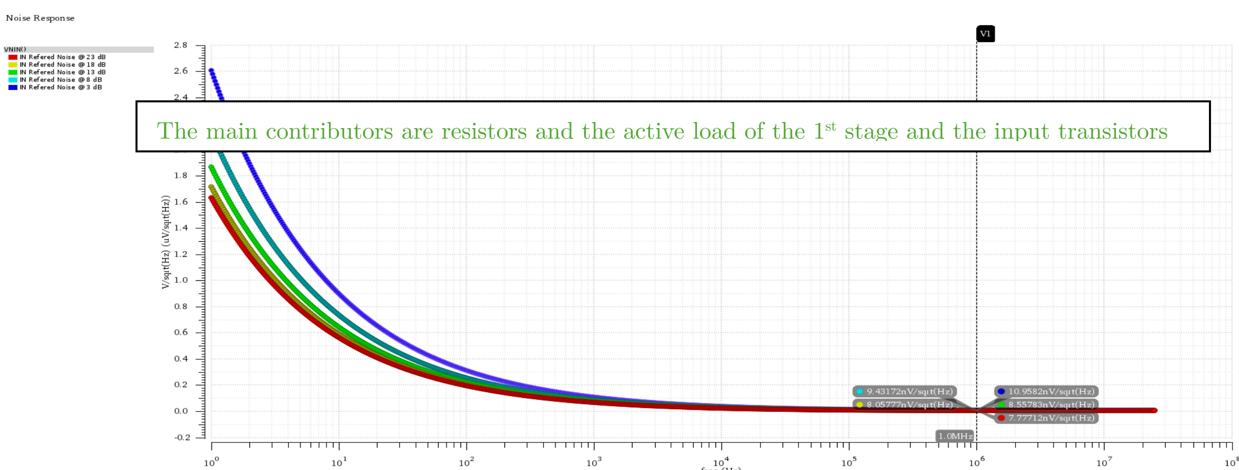


9. Show the input referred noise plot and noise summary for worst case gain setting.



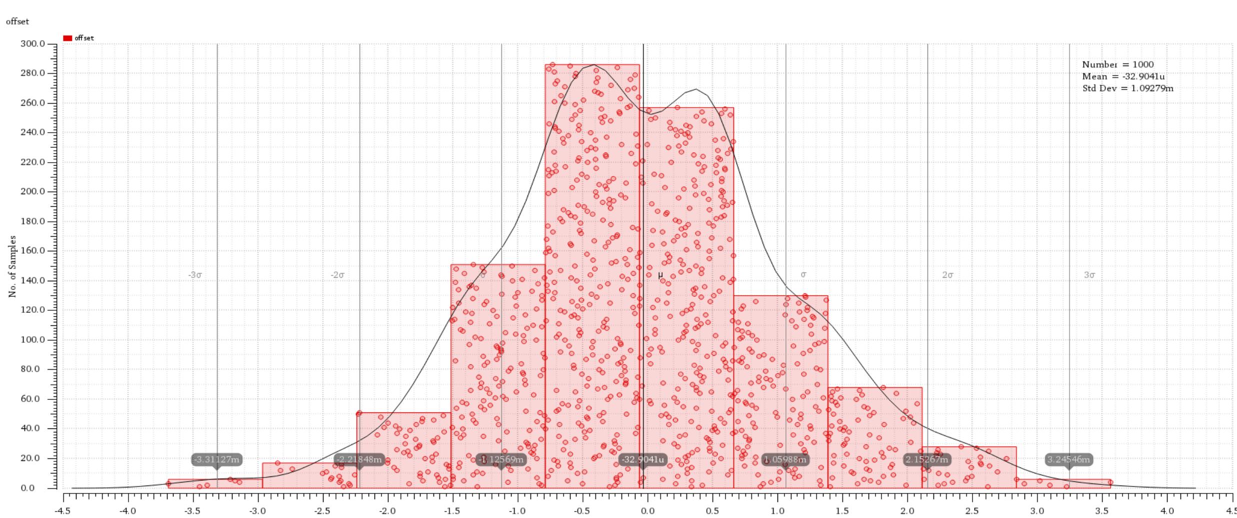
- The input referred noise at min gain is 51.6 uVrms which is within the spec of 100uVrms

10. Show noise PSD at 1MHz and integrated noise from 1kHz to BW. What are the main noise contributors?



The main contributors are resistors and the active load of the 1st stage and the input transistors

11. Simulate the input referred random offset of the Op-amp (Using Monte-Carlo).



12. Results Summary

Spec	Required	Achieved
Gain	3dB : 5dB : 23dB	3dB : 5dB : 23dB
Gain Error (%)	1%	$<$ 0.8%
BW	25 MHz	36 MHz
Output Swing (VPP)	1.6V Differential	1.95V Differential
Input Referred Thermal Noise	$<$ 100 uVrms	51 uVrms
Differential Loop PM	$>$ 60	$>$ 65.9
Common-Mode Loop PM	$>$ 45	$>$ 63
Current Consumption (mA)	1.5 mA	1.35 mA
Area um^2	-	54145 um^2