ECE601 | Advanced Analog Integrated Circuits

Band gap & Constant current Cores

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Task

Design a constant VBG across PVT and also a digitally-programmable 100µA (T=25̊C) PTAT current using 2bits.

Spec.	Target	Units	Comments
Temperature range	-40 to +125	Co	
Supply Variation	-10 to +10	%	From the nominal supply value
Process Corners	TT, SS, FF		
Nominal VBG Voltage	0.5	V	
Worst case ΔVBG across Temperature	± 1	%	For TT Corner
Worst case ΔVBG across supply	± 0.5	%	
Worst case ΔVBG	± 3	%	Across PVT
Worst case ΔVBG sigma across MC	± 1	%	For TT Corner
Nominal IPTAT Current	100	uA	@ 25º, Across PV
IPTAT Slope accuracy	--	%	Across PVT and 4 Setting
IPTAT Slope step	-12.5	%	Across PVT
IPTAT Min Slope	-50	%	Across PVT
Worst case ΔIPTAT across supply	± 1		
Worst case ΔIPTAT	± 3		Across PVT
Worst case ΔVBG sigma across MC	± 1		For TT Corner
loop PMs	> 60º	Deg	Across PVT
Startup Current	--	uA	Across PVT
Supply voltage	1.2	V	
Power consumption	--	mW	

Concept Design Review

Why we need a reference?

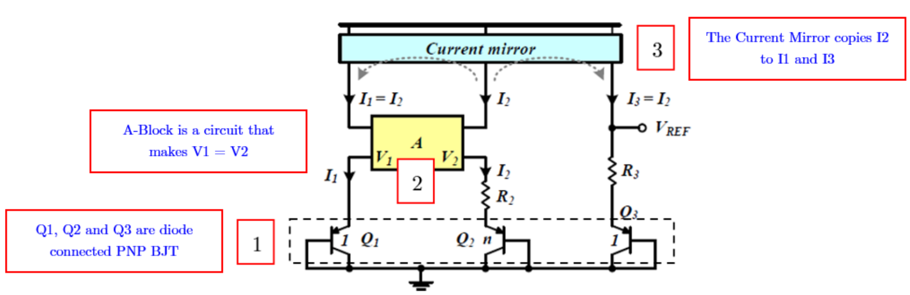
- Reference voltage generators are critical components in analog circuits, generators are required to be stabilized over process variations (P) and voltage changes (V) and Temperature changes (T)
- Poor man's reference: using voltage divider $V_{ref} = \frac{R_2}{R_1+R_2} \times V_{DD}$ .. good design makes Vref independent of P and T, but it still depends on VDD for absolute value and variations
- Bandgap Reference solve this and generate a stable reference over PVT

Temperature Coefficients

- Positive temperature coefficient (+ ve TC): Proportional to absolute temperature → $X_{PTAT} = a \times T$
- Negative temperature coefficient (- ve TC): Complementary to absolute temperature → $X_{CTAT} = C - b \times T$
- Zero temperature coefficient (zero TC): Temperature independent PTAT + CTAT

Basic operation

- BGR consists of 3 main parts



- Q2 is (n) BJTs diode connected in parallel → $I_{C1} = I_1$ and $I_{C2} = {}^{I_2}/_{n}$ → ∴ $V_{BE1} \neq V_{BE2}$ → there's ΔV_{BE}
- $|V_{BE}| = V_T \ln {}^{I_C}/_{I_S}$ → $\Delta V_{BE} = {}^{KT}/_{q} \ln n$ → $I_2 = \frac{\Delta V_{BE}}{R_2} = \frac{KT}{q} \ln n \times \frac{1}{R_2}$ → I_2 will have PTAT charactristics and so I_3 will be
- It can be shown that $|V_{BE}| = V_T \ln \frac{I_C}{I_S} = V_{G0} - b_1 T$ is a CTAT although I_C and V_T are PTAT but I_s is a strong function of temperature, **Why?**

$$I_s \propto \mu K T n_i^2 \text{ and } \mu(\text{mobility of holes}) \propto \mu_o T^m, m \approx -\frac{3}{2} \text{ and } n_i^2 \text{ (intrinsic carriers)} \propto T^3 e^{-\frac{Eg(\text{bandgab energy})}{KT}}$$

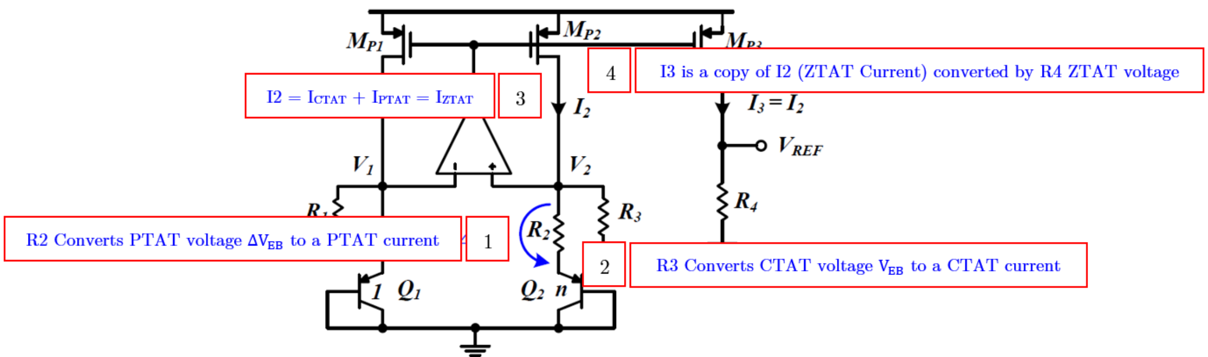
$$I_s \propto \mu_o \times T^{m+4} \times K \times e^{-\frac{Eg(\text{bandgab energy})}{KT}}$$

$$I_s = b \times T^{m+4} \times e^{-\frac{Eg(\text{bandgab energy})}{KT}} \rightarrow \text{Strong function of Temperature} \rightarrow |V_{BE}| \text{ is CTAT}$$

$$V_{ref} = V_{R3} + V_{BE3} = a_1 \times T + V_{G0} - b_1 \times T = V_{G0} \ (\text{if } a_1 = b_1)$$

$$V_{G0} = \frac{Eg}{q} \rightarrow \text{ Bandgap voltage, it's constant} = 1.2V \text{ at zero Kelvin}$$

Sub-1V BGR



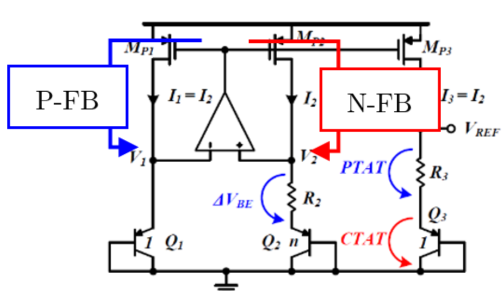
BGR Stability

Negative or Positive Feedback?

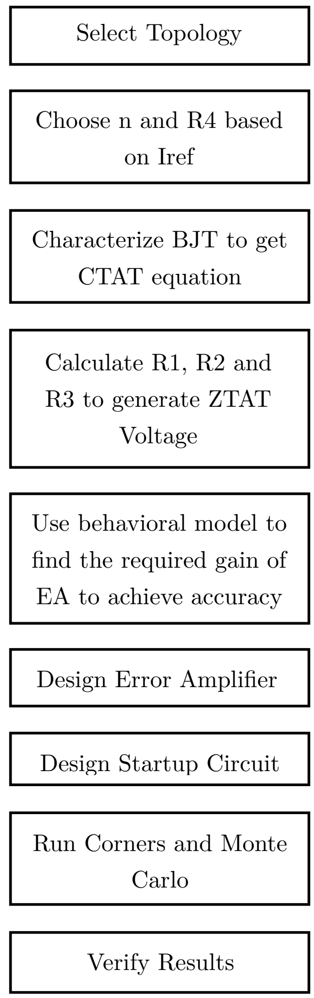
Both Negative and Positive Feedback loop are exist so, we must guarantee BN > BP

$$B_N = g_{mP2}(R_2 + 1/gm_Q)$$
$$B_P = g_{mP1}(1/gm_Q)$$

As R2 is always +ve Value so, BN > BP

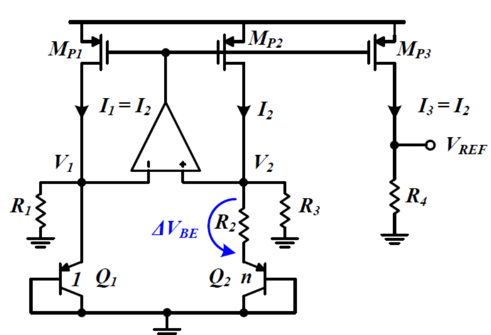


Design Flow



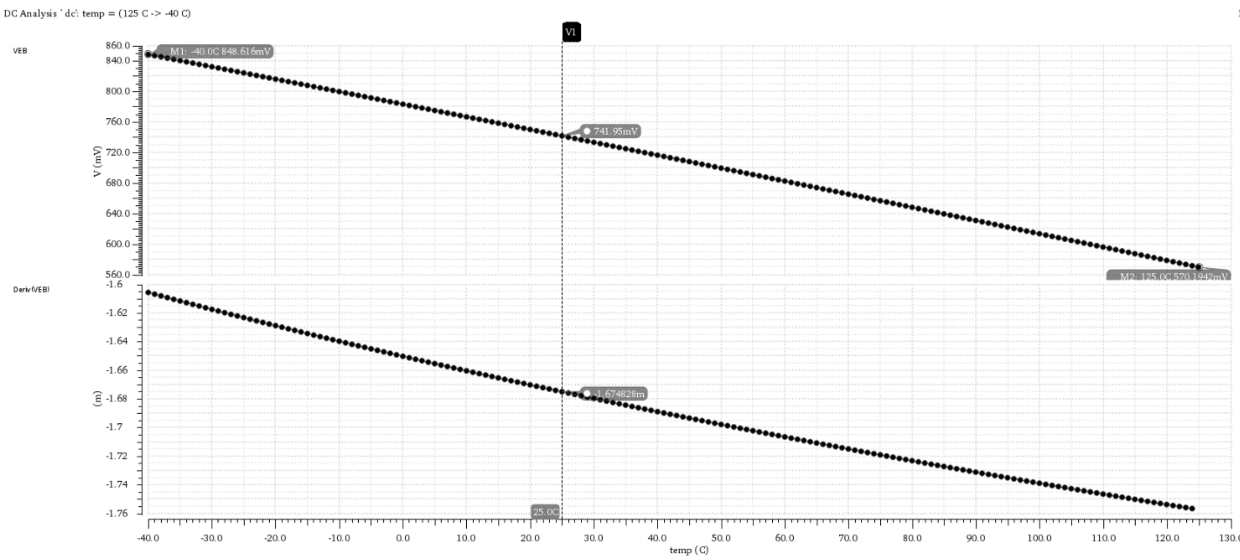
1. ZTAT behavior can be achieved by adding PTAT and CTAT via two approaches:
   - Currents summation approach.
   - Voltage summation approach.

Voltage approach can not achieve reference voltage lower than 1.2V, on the other side, current approach can achieve sub1V references, So we will use current



2. Choose n and R4
   - Choice of n : Due to layout considerations two values of n are usually used, 8 which gives better matching in layout and area and 24 which gives better precision (better ΔV_{BE}), I choose n = 24 to get small offset
   - Since no constrain on power consumption, I prefer choosing low ID to get low variation in PTAT and CTAT and low power consumption which make it suitable for modern applications.
   - Assume $I_3 = 20\text{ uA} \rightarrow$ Vref = 0.5 V → R4 = 25 kΩ, Current mirrored with same ratio so, $I_1 = I_2 = I_3 = 20\text{ uA}$

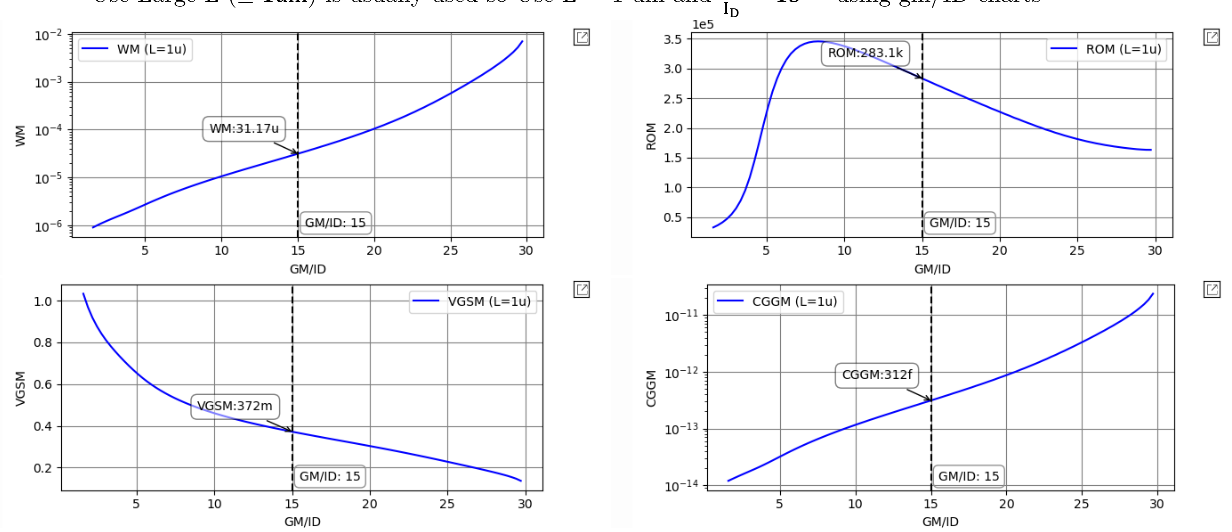
3. BJT Characterization
   - Characterizing BJT using simple diode connected TB gives CTAT equation that helps to find R1, R2, and R3



$$V_{EB} = 1.2375 - 1.675\text{m} \times T \qquad \text{where (T in Kelvin)}$$

4. Calculate R1, R2 and R3
   - $V_{ref} = I_3 R_4 = I_2 R_4 = R_4\left(\frac{V_{EB1}}{R_3} + \frac{V_T \ln n}{R_2}\right) = \frac{1.2375 \times R_4}{R_3} + \frac{KT \ln n \times R_4}{q \times R_2} - \frac{1.675\text{m} \times T \times R_4}{R_3}$
   - From previous equation we need $\frac{K \ln n}{q \times R_2} = \frac{1.675\text{m}}{R_3} \rightarrow (2)$ and $\frac{1.2375 \times R_4}{R_3} = 0.5 \rightarrow (3)$
   - From (3) $\because R_4 = 25\text{K Ohm} \rightarrow R_3 = 61.875\text{K Ohm} = R_1 \rightarrow$ Substituting in (2) $R_2 = 10.117\text{K Ohm}$

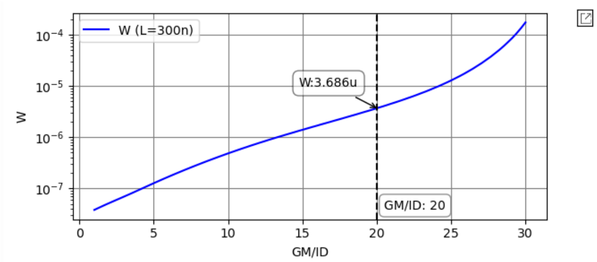
5. Design of the Current Mirrors
   - Use Large L ($\geq 1\text{um}$) is usually used so Use L = 1 um and $\frac{g_m}{I_D} = 15 \rightarrow$ using gm/ID charts

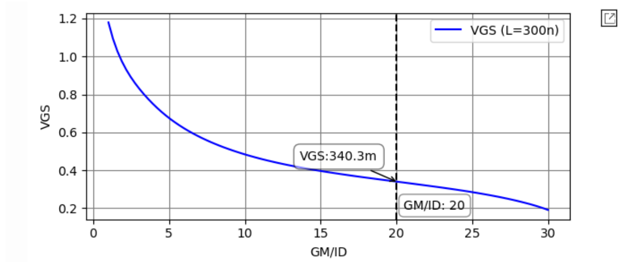


6. Design of the EA, I Choose SE Folded Cascode OTA

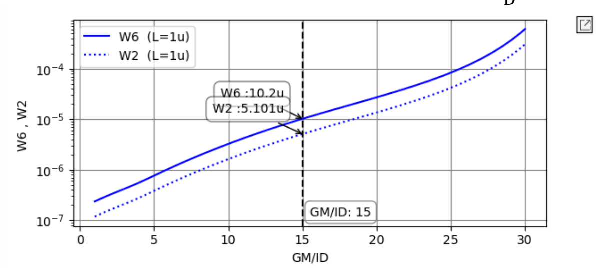
- Assume total current for OTA equals 40 uA and it is divided equally between the two branches

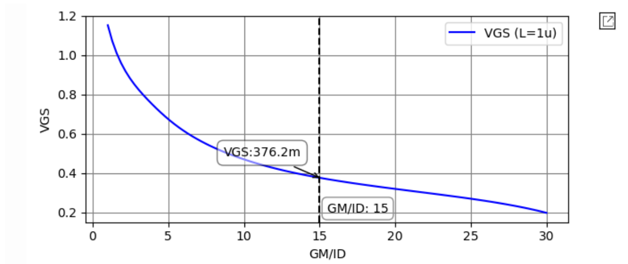
  - M1 → L = 0.3 um and ${g_m}/{I_D} = 20$



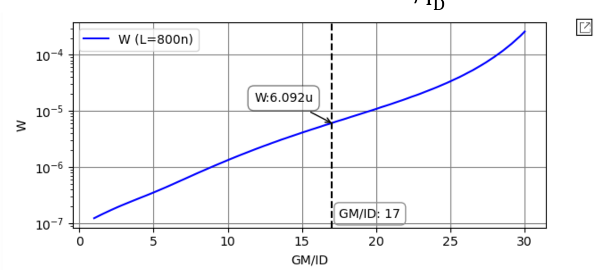


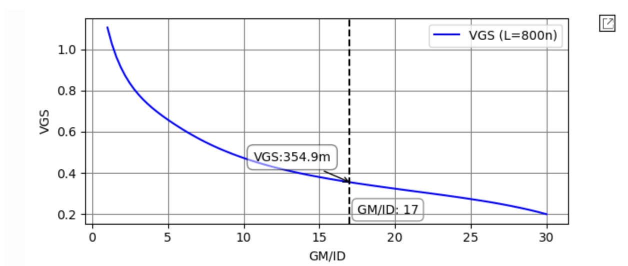
  - M2 and M6 → L = 1 um and ${g_m}/{I_D} = 15$



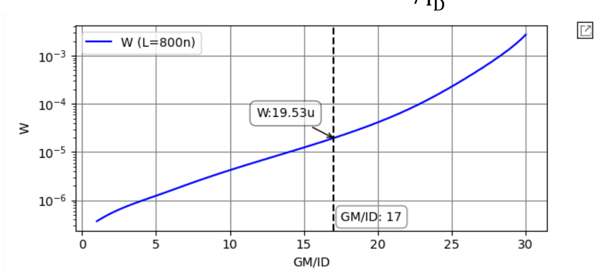


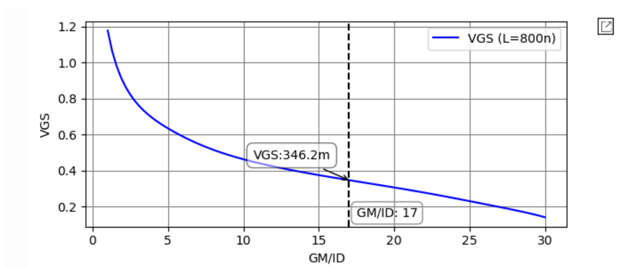
  - M3 → L = 0.8 um and ${g_m}/{I_D} = 17$



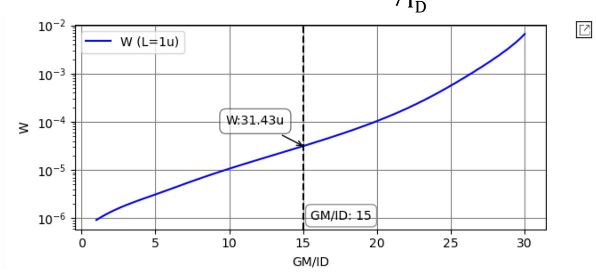


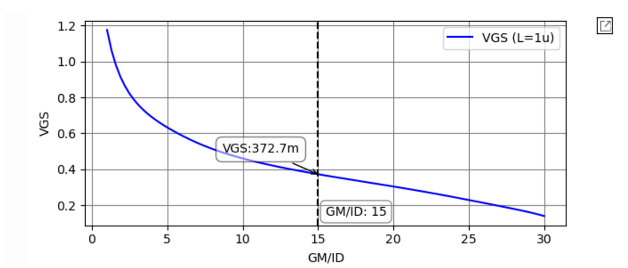
  - M4 → L = 0.8 um and ${g_m}/{I_D} = 17$





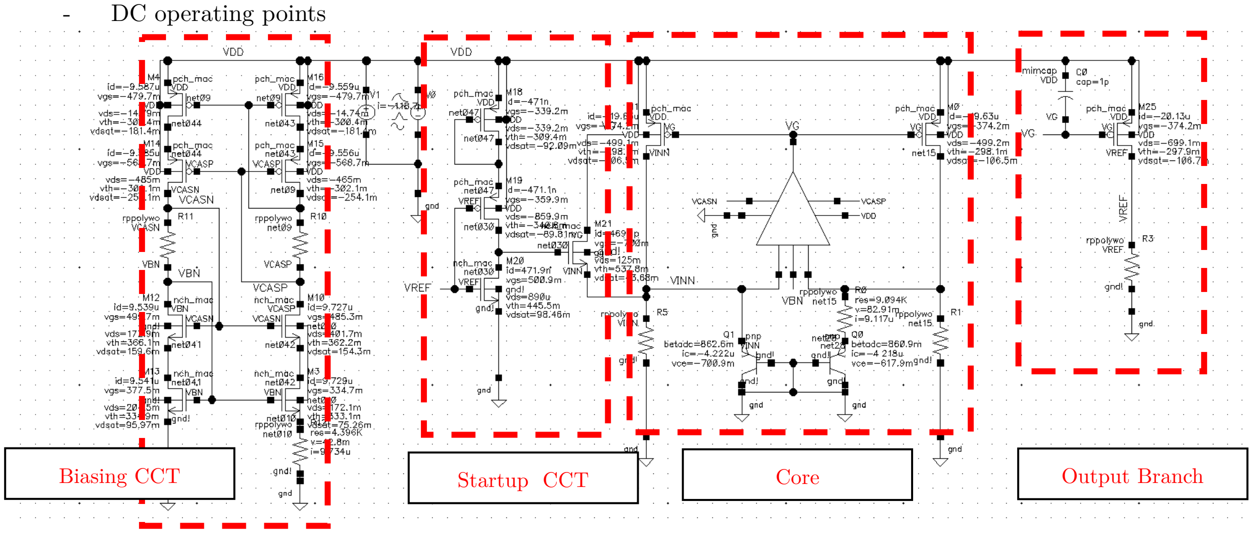
  - M5 → L = 1 um and ${g_m}/{I_D} = 15$



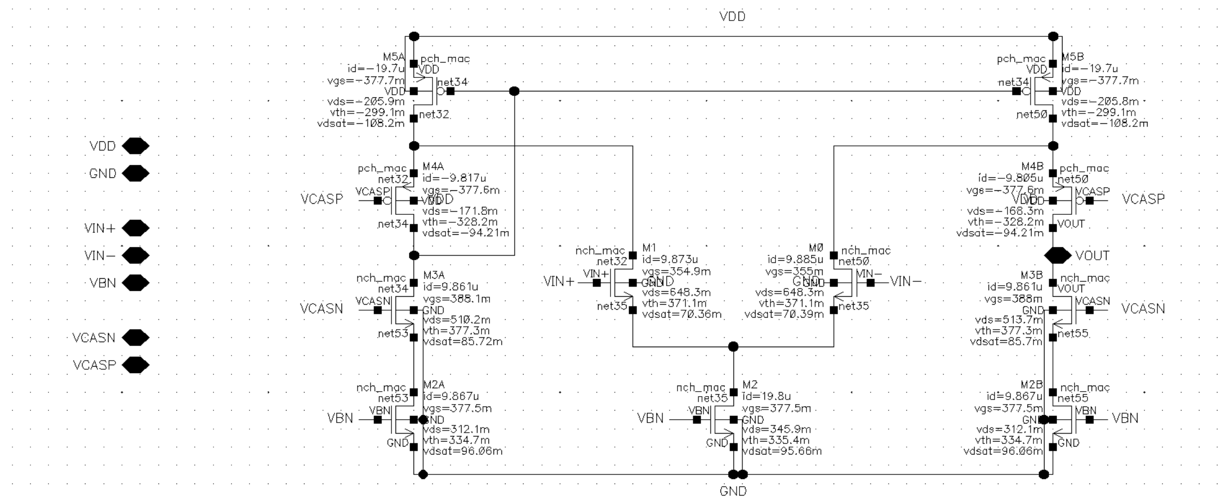


7. BGR

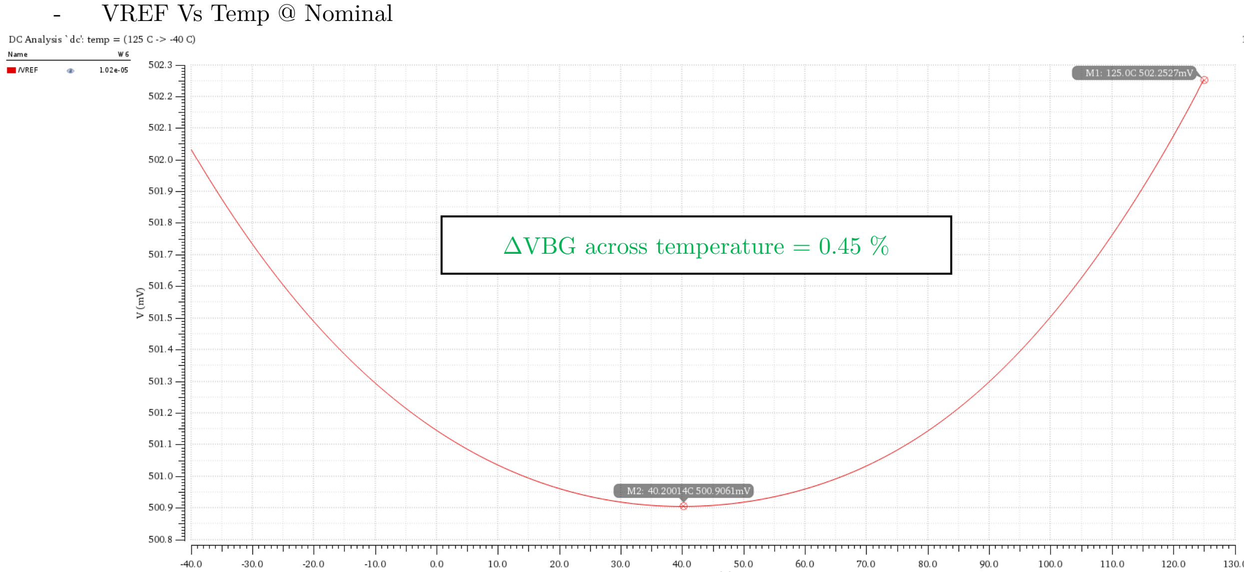
- DC operating points



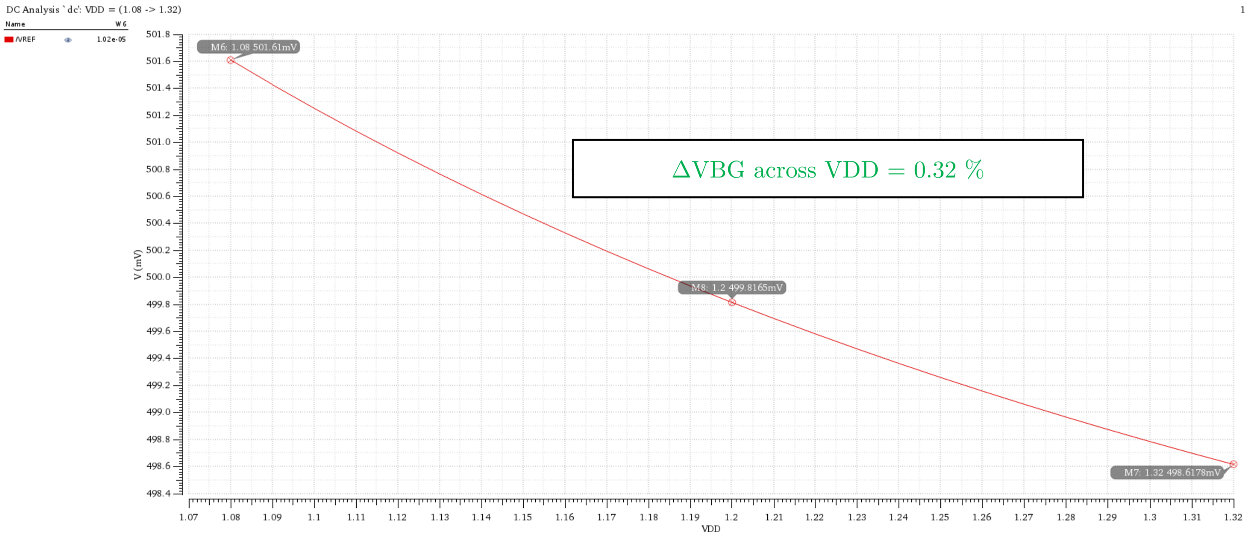
- OP Amo Operating Points



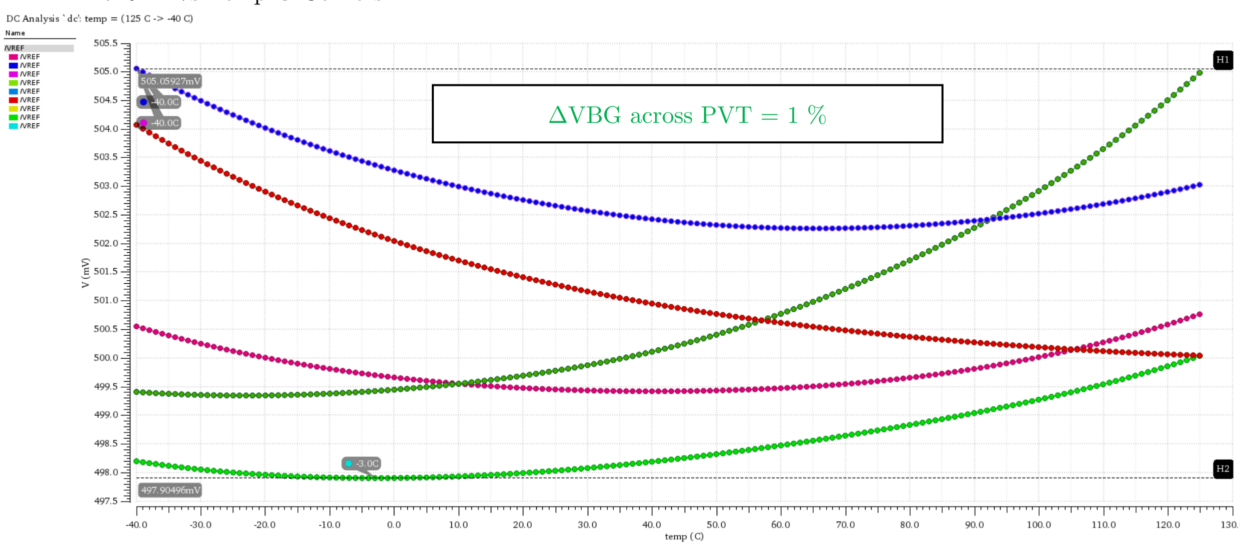
- VREF Vs Temp @ Nominal



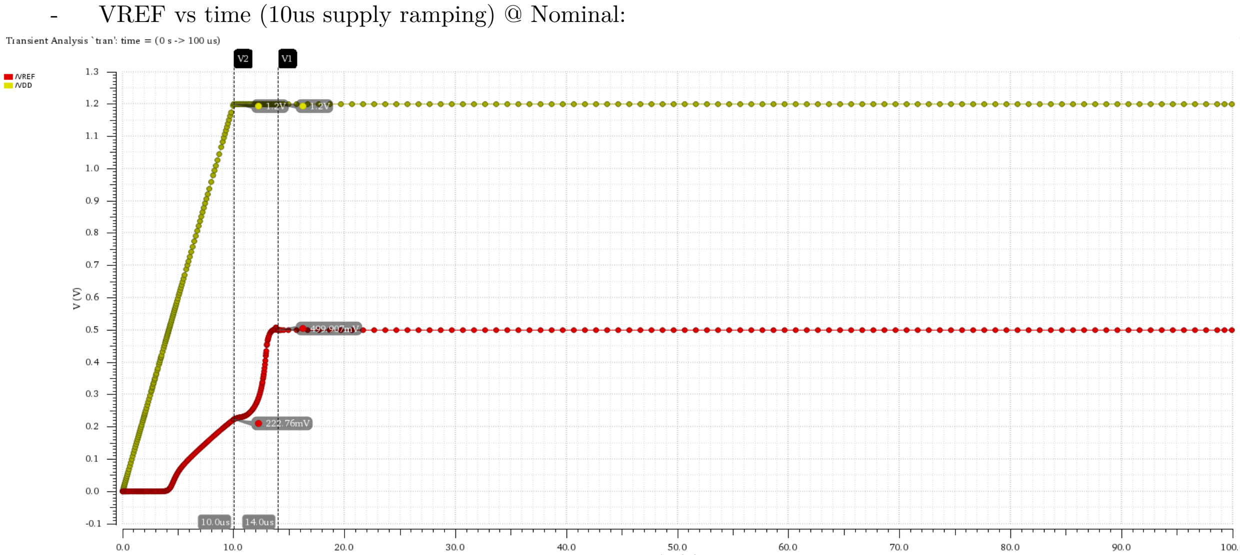
- VREF Vs VDD @ Nominal



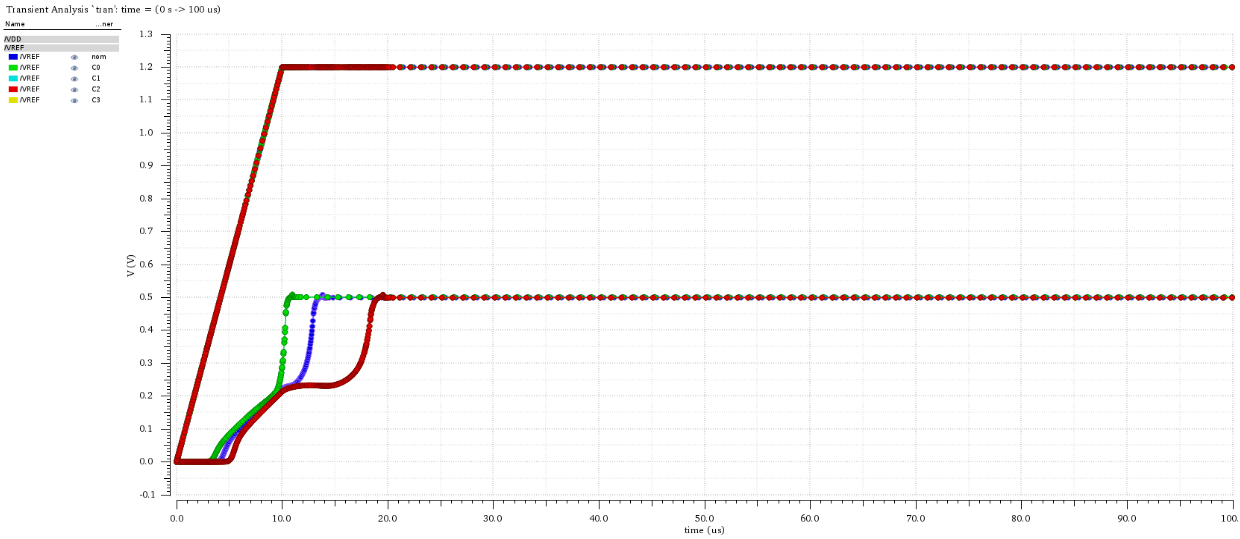
- VREF Vs Temp @ Corners



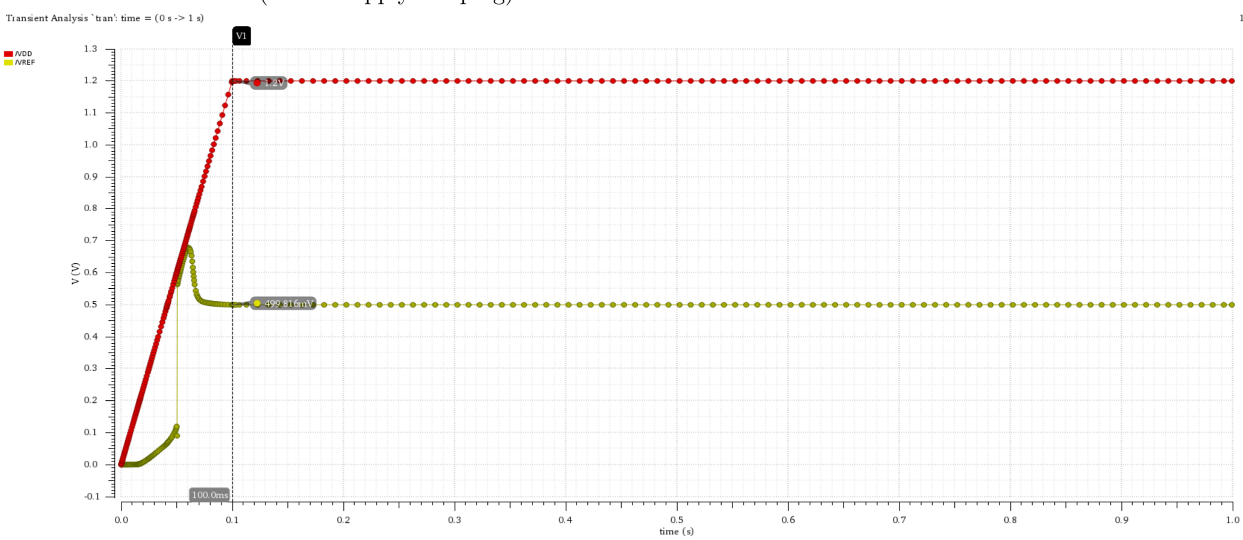
- VREF vs time (10us supply ramping) @ Nominal:



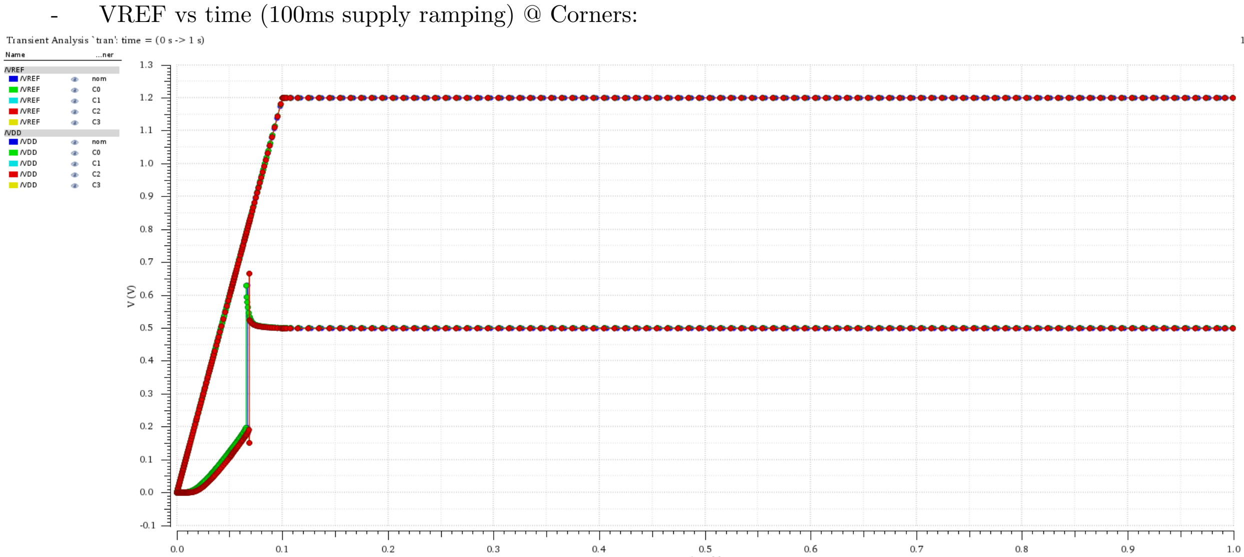
- VREF vs time (10us supply ramping) @ Corners:



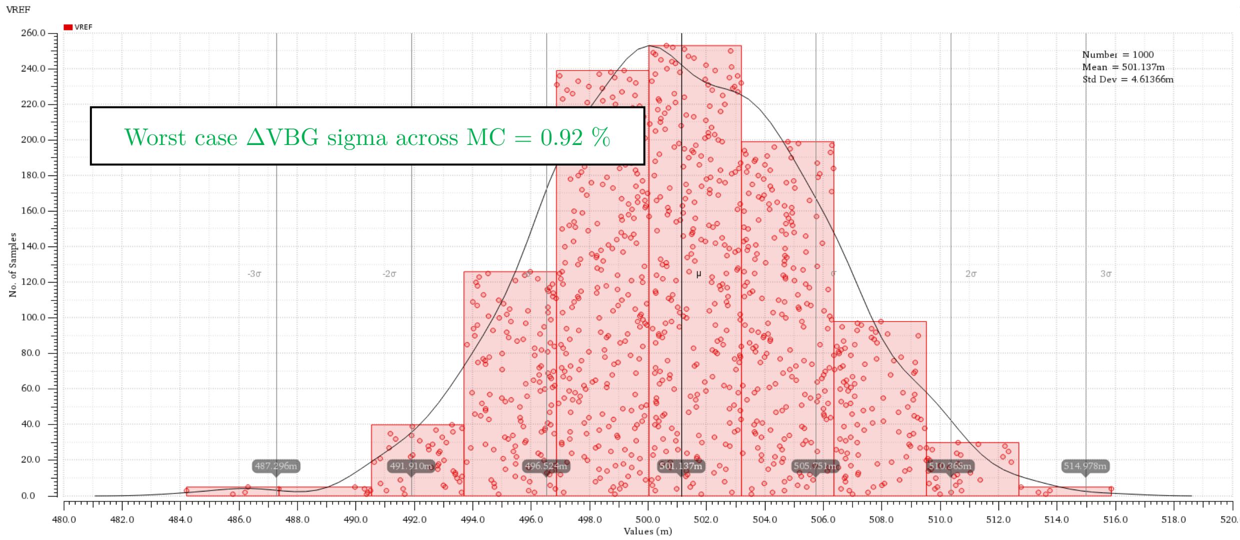
- VREF vs time (100ms supply ramping) @ Nominal:



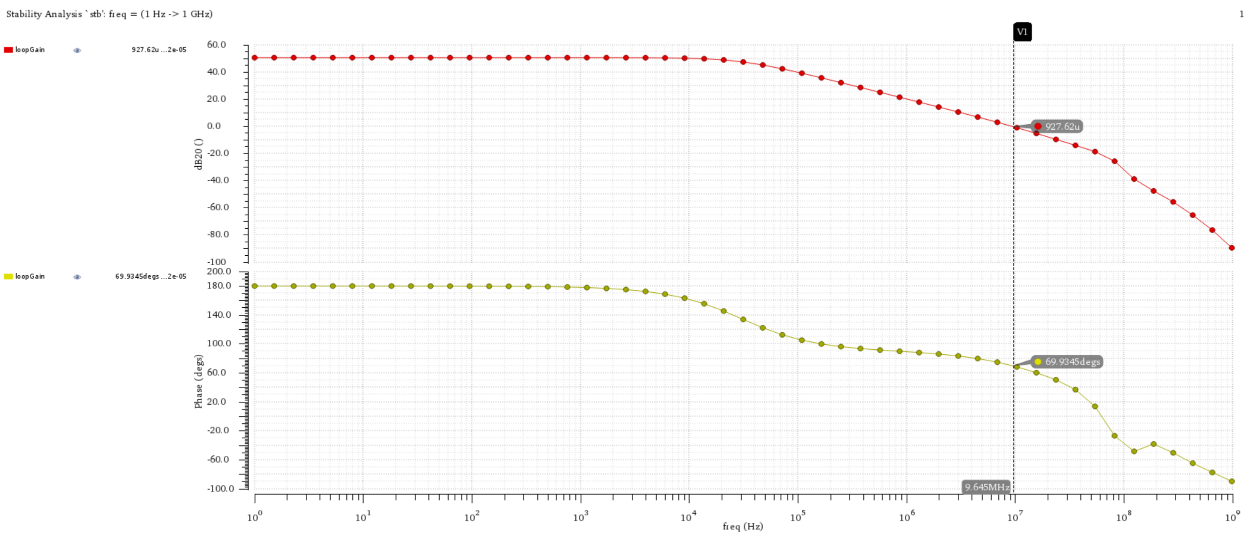
- VREF vs time (100ms supply ramping) @ Corners:



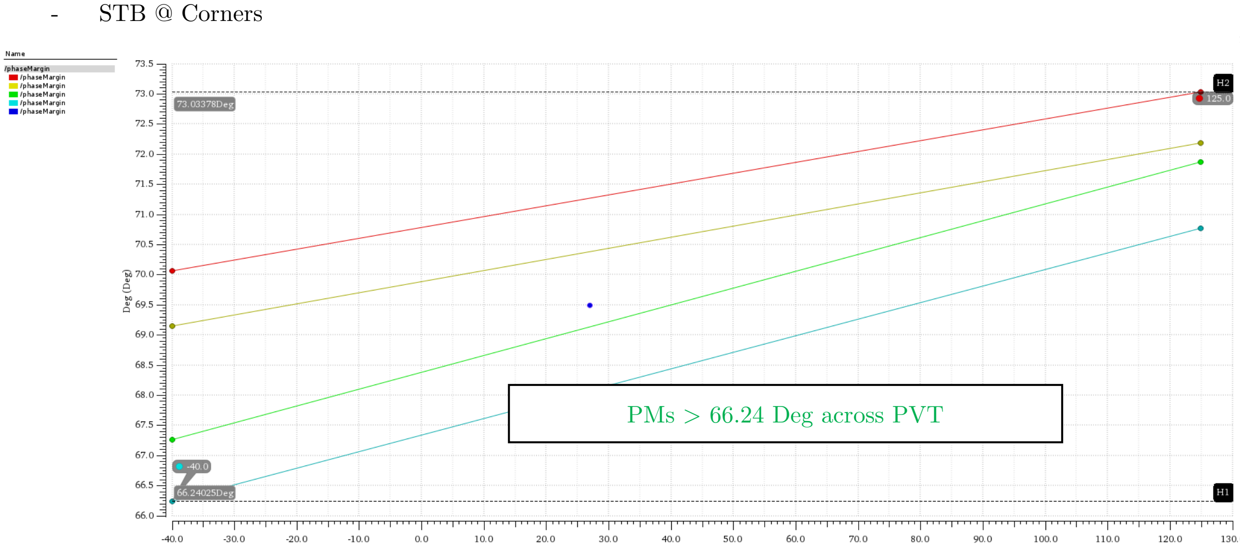
- MC Results



- STB @ Nominal

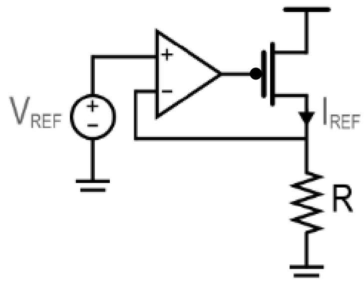


- STB @ Corners

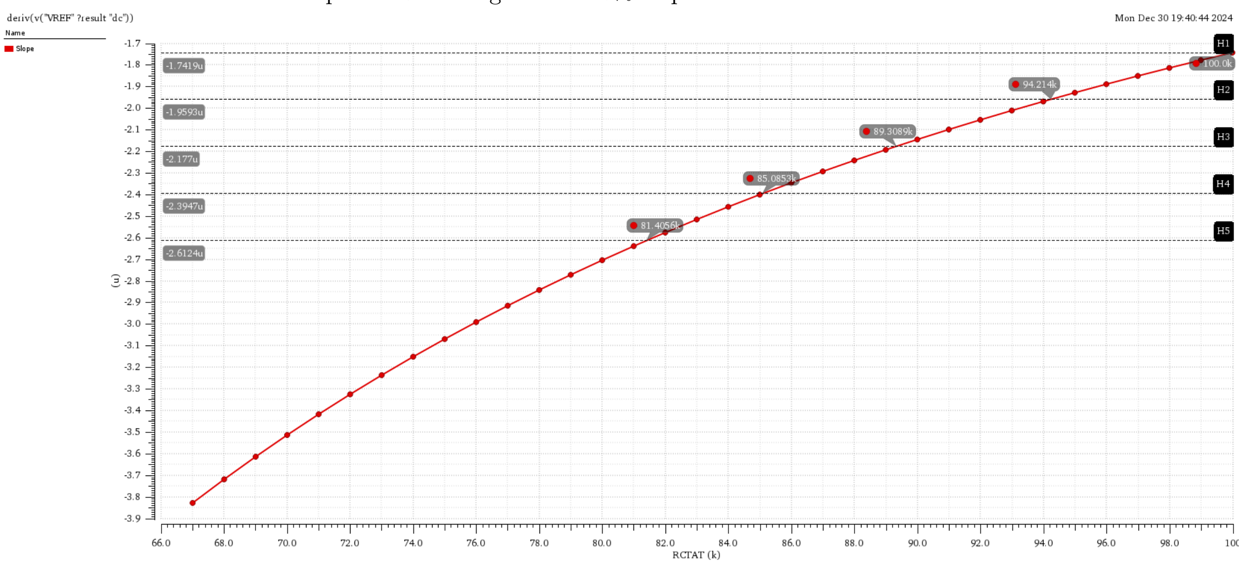


8. PTAT Current Generator

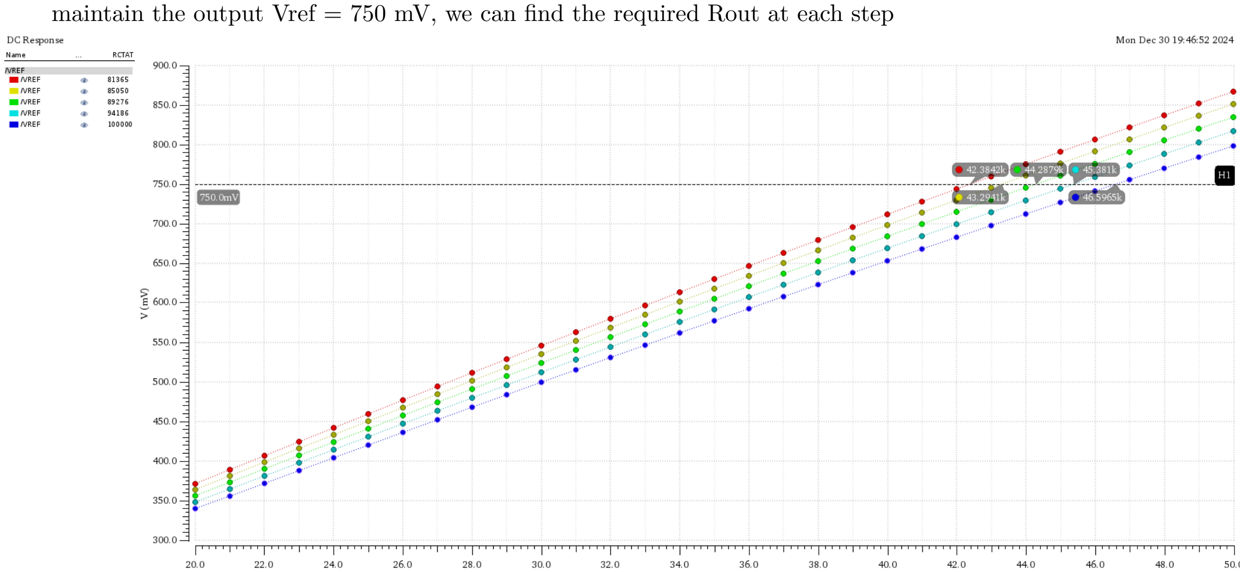
- We intentionally make VREF a PTAT voltage and generate a PTAT current from it using shown circuit



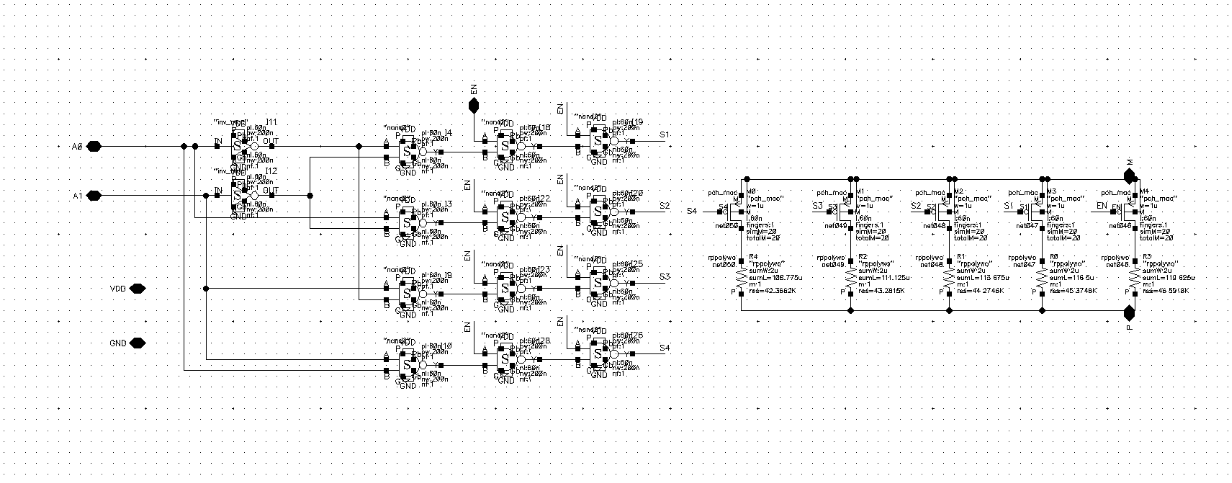
- The PTAT slope is controlled by the Rctat of the BGR core so, we get the max slope of the Vref Vs Rctat and determine the required Rctat to get the 12.5% step from it



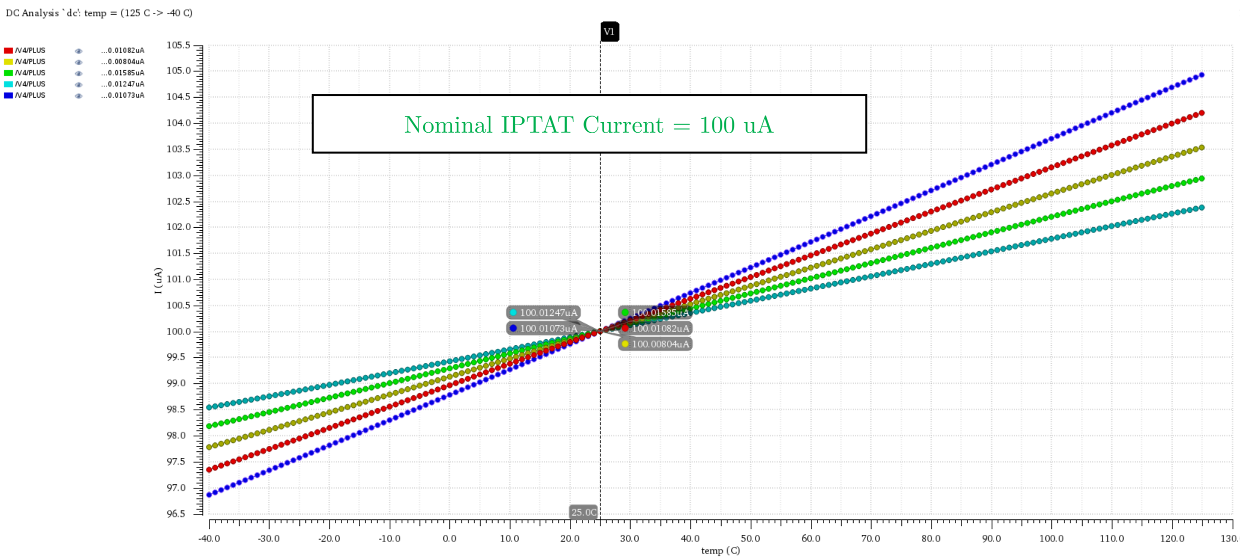
- In order to maintain the Vref constant the output resistance will be also variable, so sweeping the Rout to maintain the output Vref = 750 mV, we can find the required Rout at each step



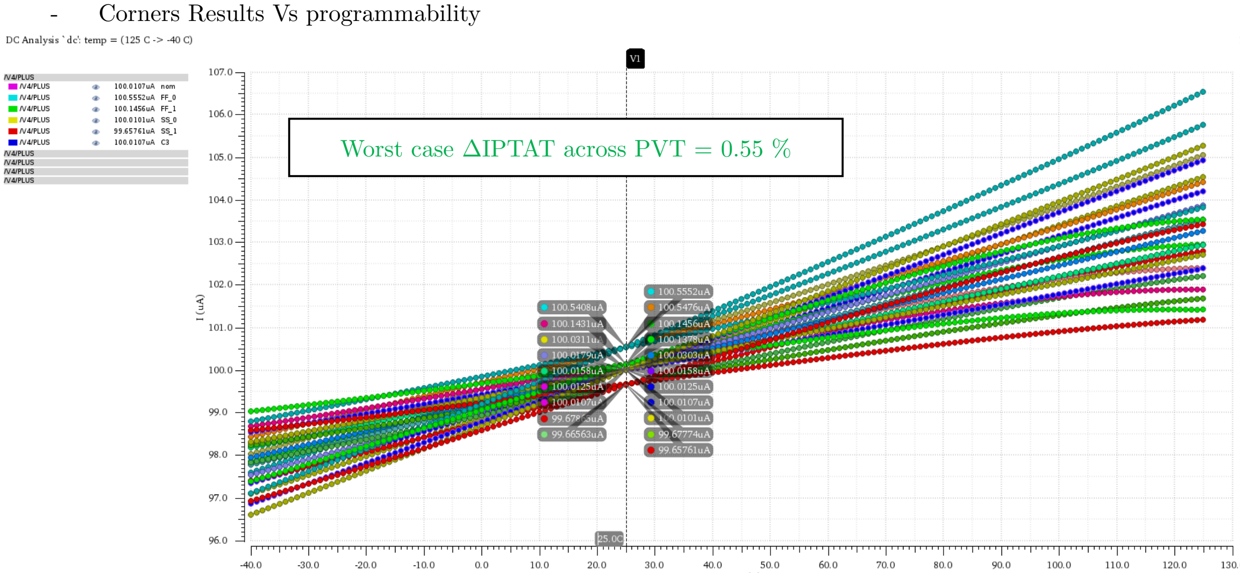
- Making the following selector to get the required R at each step with 2 bits A0 and A1 and Enable pin



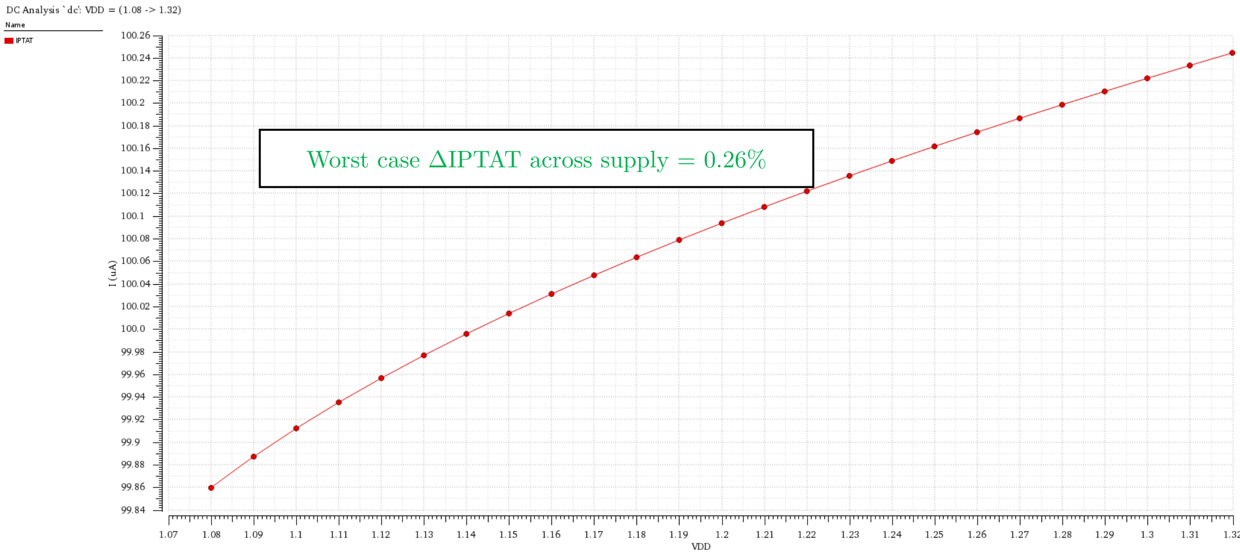
- Typical Results Vs programmability



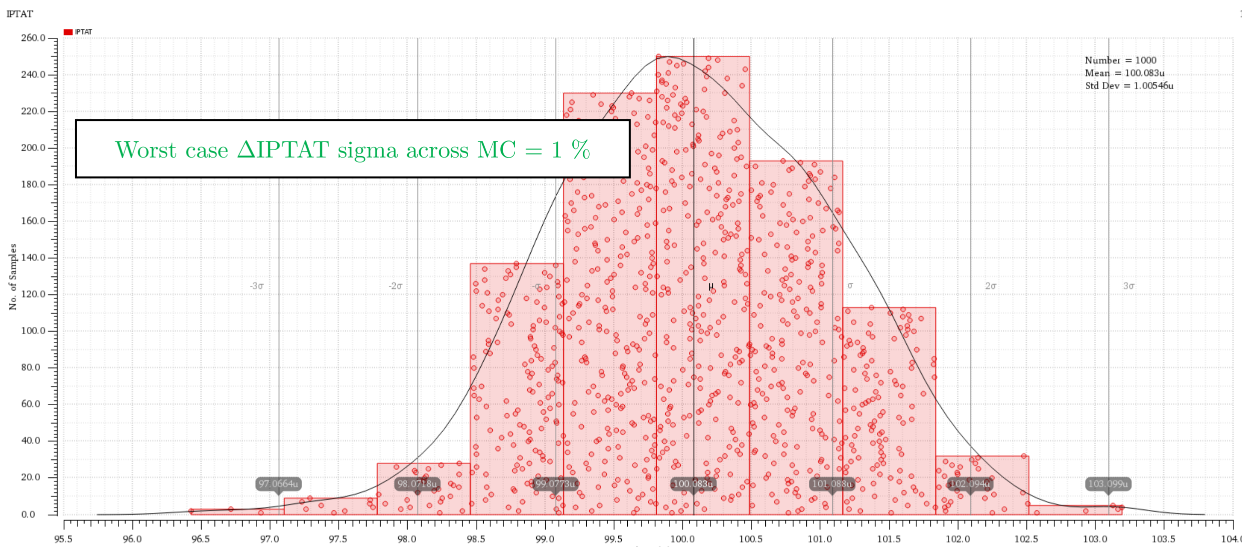
- Corners Results Vs programmability



- IPTAT Vs VDD @ Nominal



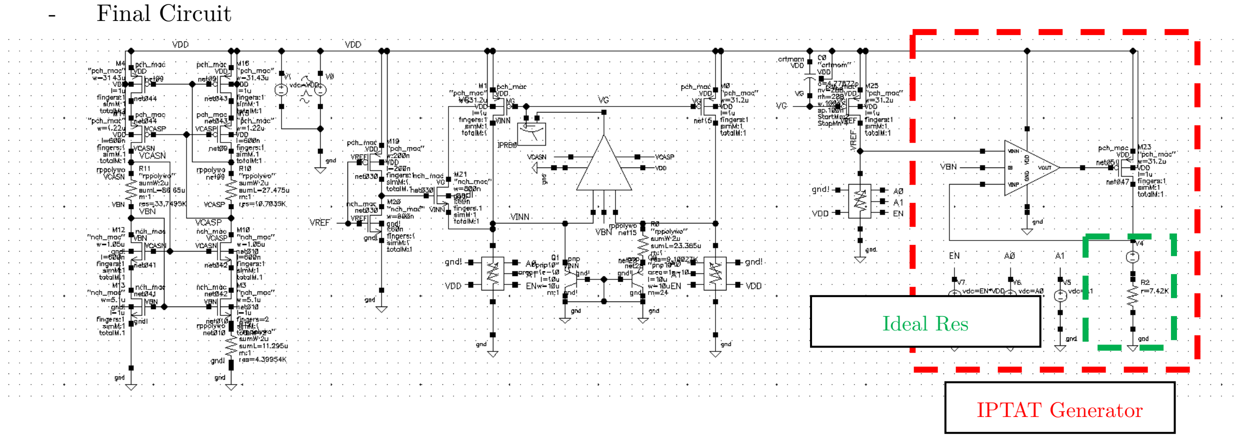
- MC Results



- STB across PVT

Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	FF_0	FF_1	SS_0	SS_1	C3
AnalogIC:BGR:1	/V4/PLUS											
AnalogIC:BGR:1	PMs	69.43				65.13	73.51	65.13	66.76	72.1	73.51	69.39

- Final Circuit



9. Results Summary

Spec.	Target	Units	Achieved	Comments
Temperature range	-40 to +125	C°	-40 to +125	
Supply Variation	-10 to +10	%	-10 to +10	From the nominal supply value
Process Corners	TT, SS, FF		TT, SS, FF	
Nominal VBG Voltage	0.5	V	0.5	
Worst case ΔVBG across Temperature	± 1	%	0.45 %	For TT Corner
Worst case ΔVBG across supply	± 0.5	%	0.32 %	
Worst case ΔVBG	± 3	%	1 %	Across PVT
Worst case ΔVBG sigma across MC	± 1	%	0.92 %	For TT Corner
Nominal IPTAT Current	100	uA	100	@ 25°, Across PV
IPTAT Slope accuracy	--	%	--	Across PVT and 4 Setting
IPTAT Slope step	-12.5	%	-12.5	Across PVT
IPTAT Min Slope	-50	%	-50	Across PVT
Worst case ΔIPTAT across supply	± 1		0.26	
Worst case ΔIPTAT	± 3		0.55	Across PVT
Worst case ΔVBG sigma across MC	± 1		1	For TT Corner
loop PMs	> 60°	Deg	> 65°	Across PVT
Startup Current	--	uA	0.5	Across PVT
Supply voltage	1.2	V	1.2	
Power consumption	--	mW	0.267	