ECE601 | Advanced Analog Integrated Circuits

Assignment No. 2

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Design amplifier using inductors/capacitors from design kit that achieve GT>9dB at 12GHz including matching network. Use kit inductors/capacitors to match transistor input and output impedance to 50 Ω , make sure your design is unconditionally stable. Plot GT, Gp, Ga, S21, S12, S11, S22, NF, k factor versus frequency. You can choose number of fingers=10

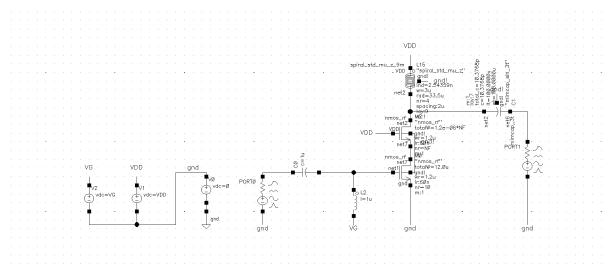
Design procedures

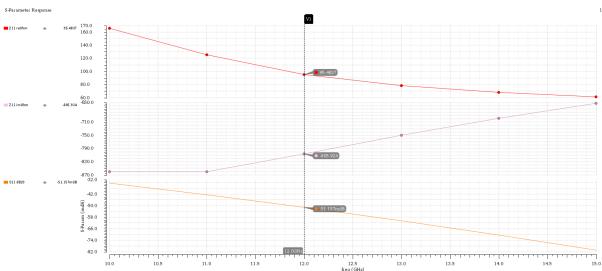
Step 1 (Choosing topology) : a basic common source stage with two modifications

- A Inductive degeneration : used to tune input matching to get the real part of the input impedance equal to 50 Ω directly and for the remaining imaginary part a single inductor is added in series to cancel it which simplifies the input matching network a lot. Also, this inductive degeneration helps in improving stability of the amplifier.
- B Cascode Transistor is added to isolate the output from the input and also to increase the gain that can be obtained from the amplifier.

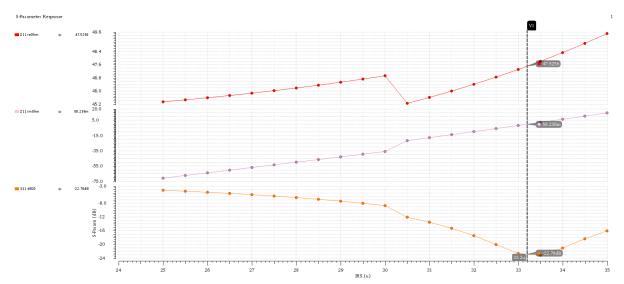
Step 2 (Matching the Input) : A series inductor at the gate used to cancel the imaginary part of the Zin and another one at the tune the real part to get the 50Ω

A – The circuit input impedance with no matching at the input

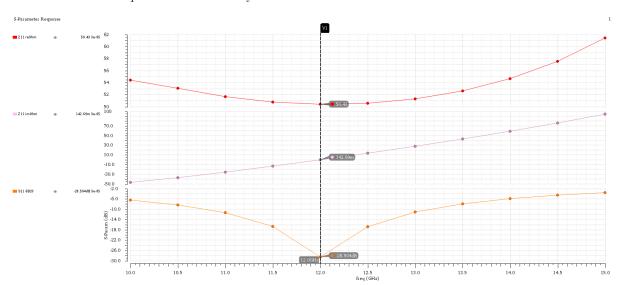




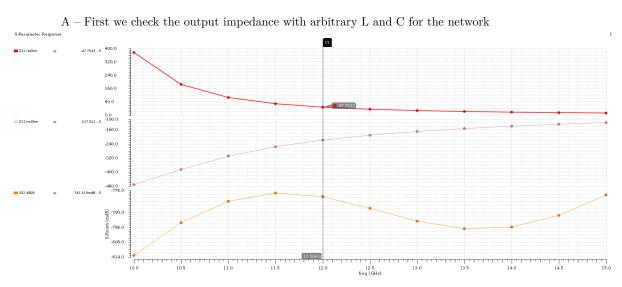
 ${\bf B}$ – The maximum value of one inductor of the kit is not enough to cancel the imaginary part of Zin so I use two inductors in series and tune the L needed by changing the inner radius of the inductor



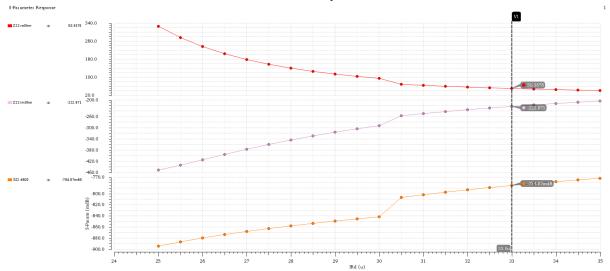
C – The real part of Zin achieved by the inductor at the source



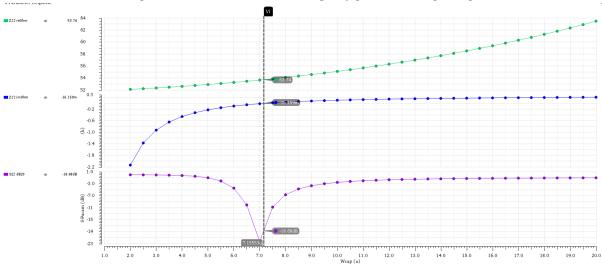
Step 3 (Matching the output) : An output matching network is added to match the output impedance to 50Ω . This network is an L matching network for simplicity.



B – The inductor is tuned to achieve 50Ω at the output

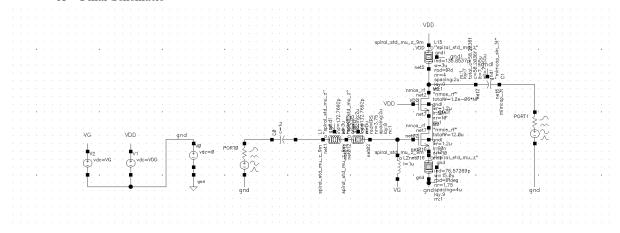


C – Then the Cap value is tuned to cancel the imaginary part of the output impedance

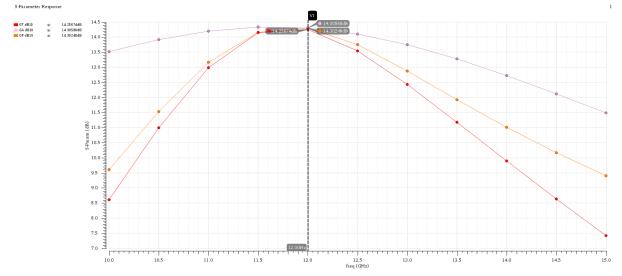


Step 4 (Final Design Results) :

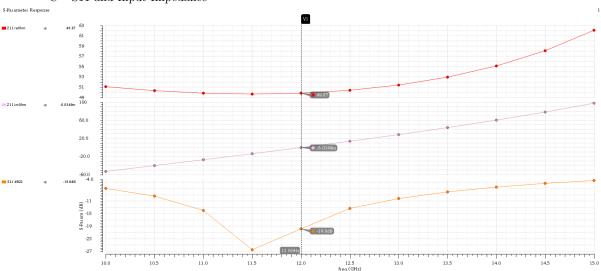
$A-Final\ Schematic$



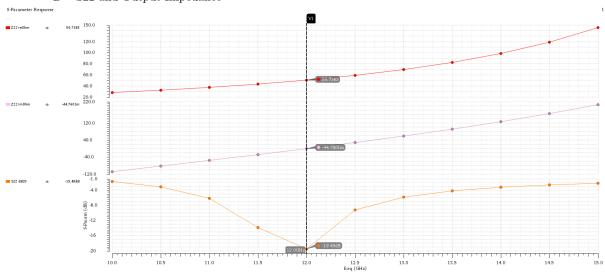


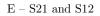


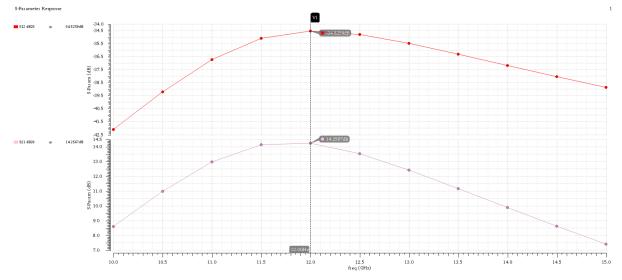
$\mathrm{C}-\mathrm{S}11$ and Input Impedance



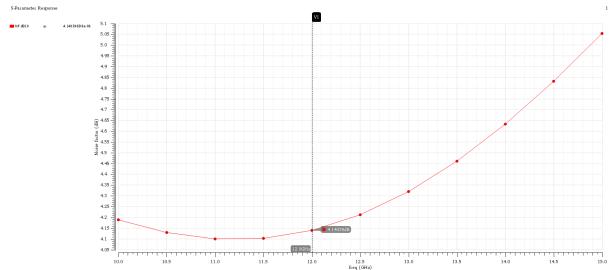
$\mathrm{D}-\mathrm{S}22$ and Output Impedance

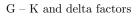


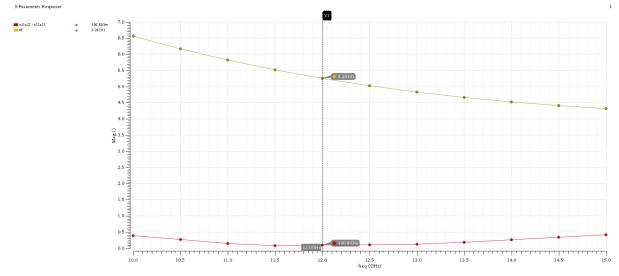




F – Noise Factor







The K factor > 1 and the delta is $< 1 \rightarrow$ So the design is unconditionally stable