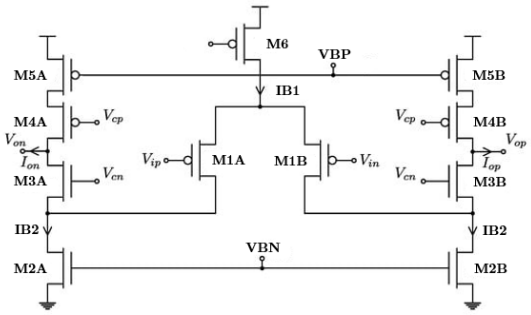
Analog Integrated Circuits Designs
Fully Differential Folded Cascode Amplifier

Specifications			
Supply Voltage	1.2 V	Closed Loop Gain	2
Phase Margin	$\geq 70^{o}$	Closed Loop BW	10 MHz
Differential Output Swing	≥ 0.6 V pk $-$ to $-$ pk	OTA Current Consumption	≤ 80 uA
CM Input Range	$0 \geq CM > 0.6$ V	CMFB Current Consumption	≤ 40 uA
Load	1 pF	DC Loop Gain	50 dB

- Design Steps

01 | Since CM input range is close to GND rail → Choose PMOS input devices



02 | Assume current split equally for each branch of the design → $I_{B2} = {80\ uA}/{2} = 40\ uA \rightarrow I_{B1} = I_{B2} = 40\ uA$

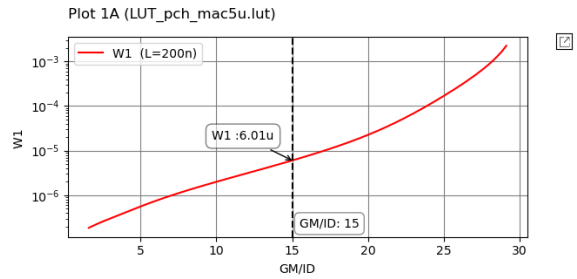
03 | $\because A_{VCL} = {1}/{\beta} = 2 \rightarrow \beta = {1}/{2}$ and $UGF = A_{VCL} \times BW_{CL} = 20\ MHz \rightarrow g_{m1} \geq 125\ uS \rightarrow {g_{m1}}/{I_D} = 6.5$

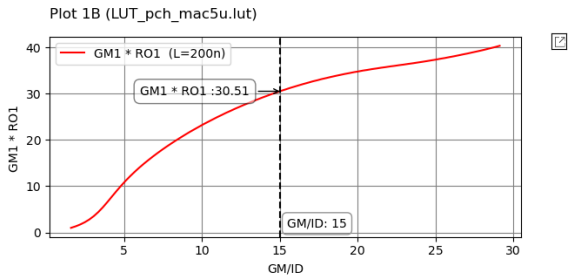
04 | $\because LG = 50\ dB = A_{VOL} * \beta \rightarrow A_{VOL} \geq 56\ dB$

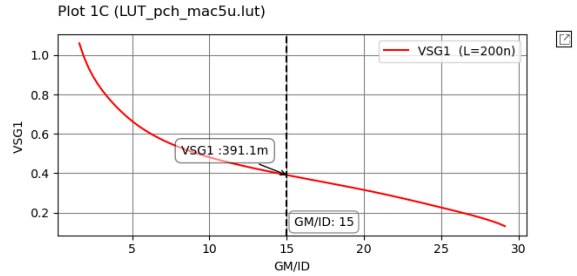
05 | Since this is a relatively difficult design, we will directly assume values for L and gm/ID based on designer's experience and folded cascode trade-offs matrix.

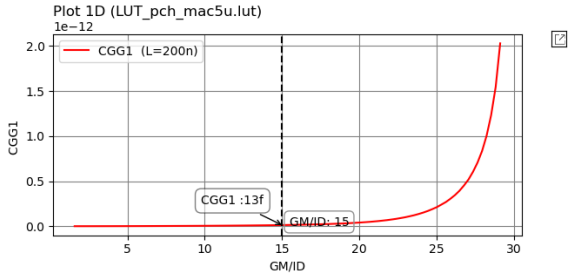
A | Input Pair M1

Assume Short L = 0.2 um and gm/ID = 15, This maximizes the GBW (good efficiency) and minimizes the input capacitive loading (avoid reducing the DC LG).





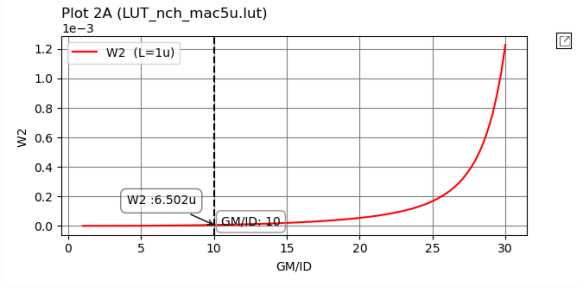


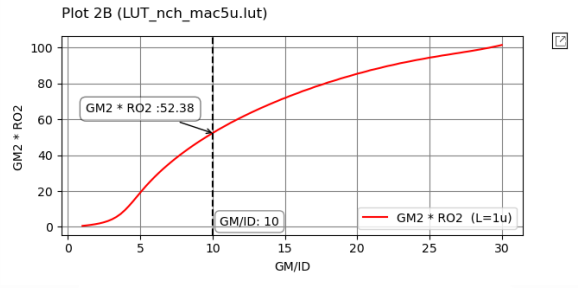


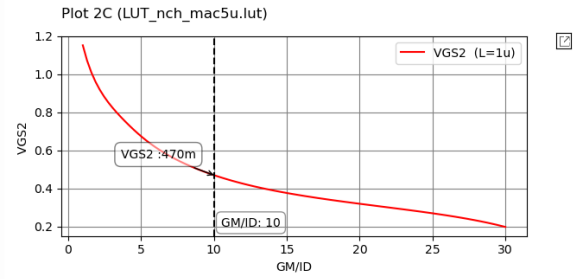
B | Current Mirrors

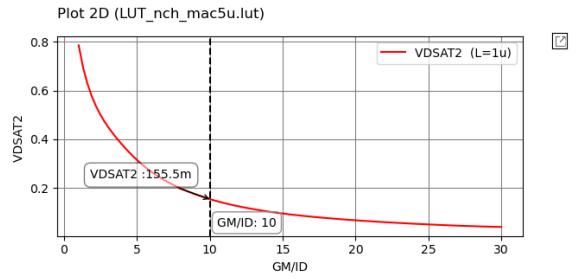
For the current source transistors use relatively long L and bias them in SI, L = 1 um and gm/ID = 10, These transistors contribute significant offset and noise. A large gm will not help the gain but will increase the noise.

- NMOS Current Mirror M2

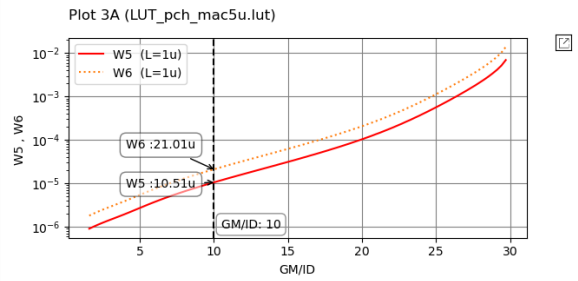


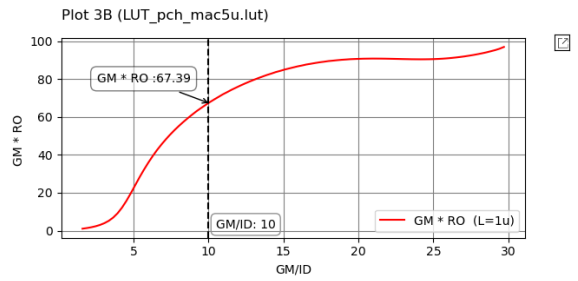


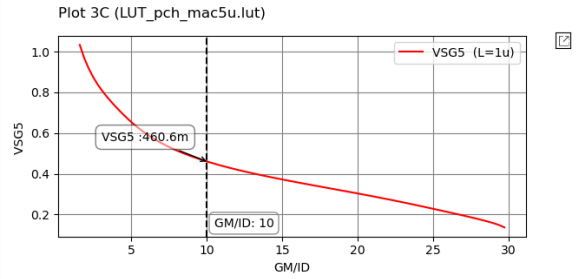


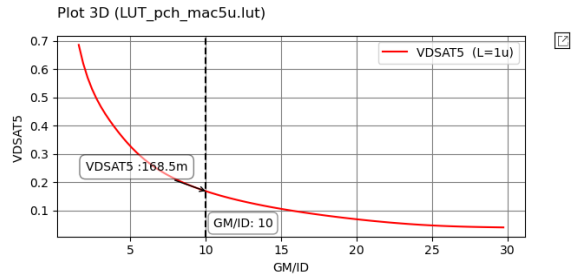


- PMOS Current Mirror M5 and M6





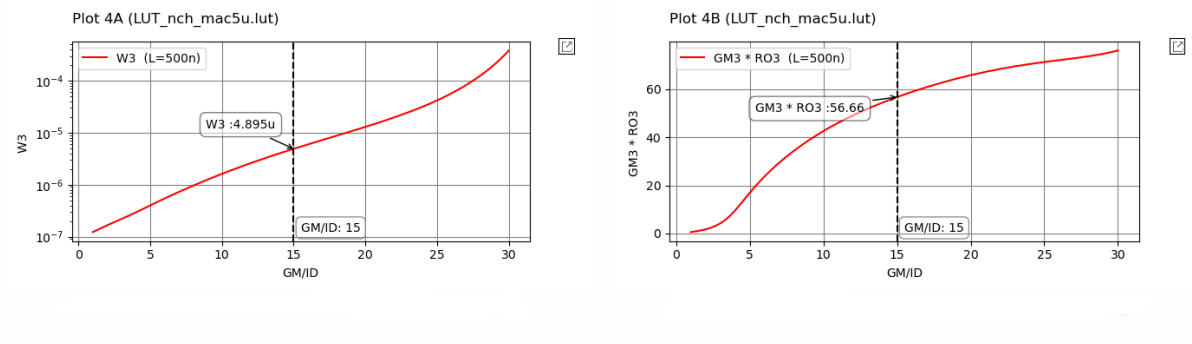


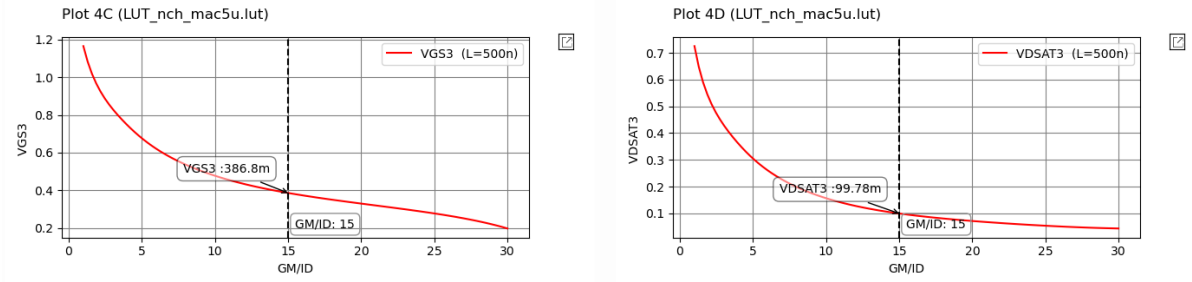


C | Cascode Transistors

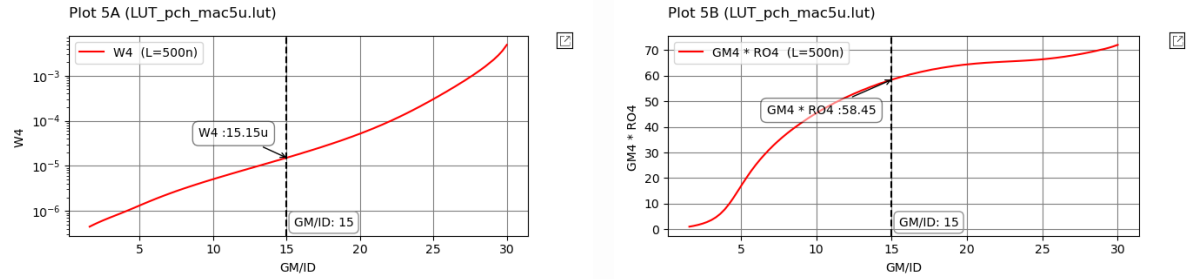
For the cascode transistors use moderate L and bias them in MI or WI, L = 0.5 um and gm/ID = 15, These transistors do not contribute significant offset and noise, so they don't need to be large. A large gm helps the gain and doesn't increase the noise.

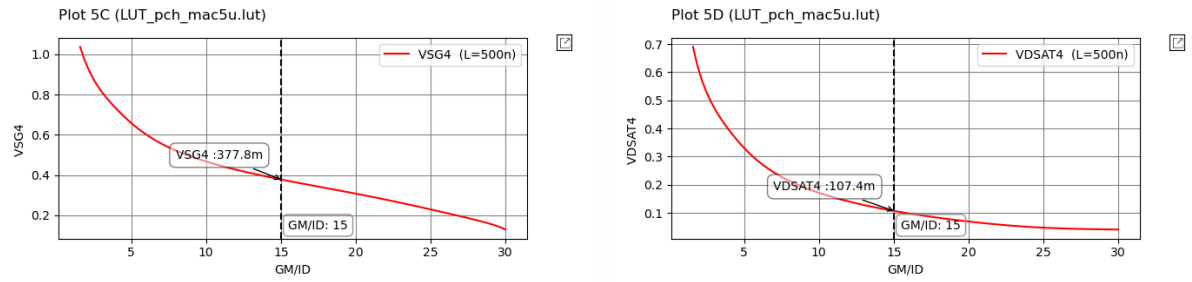
- NMOS Cascode





- PMOS Cascode



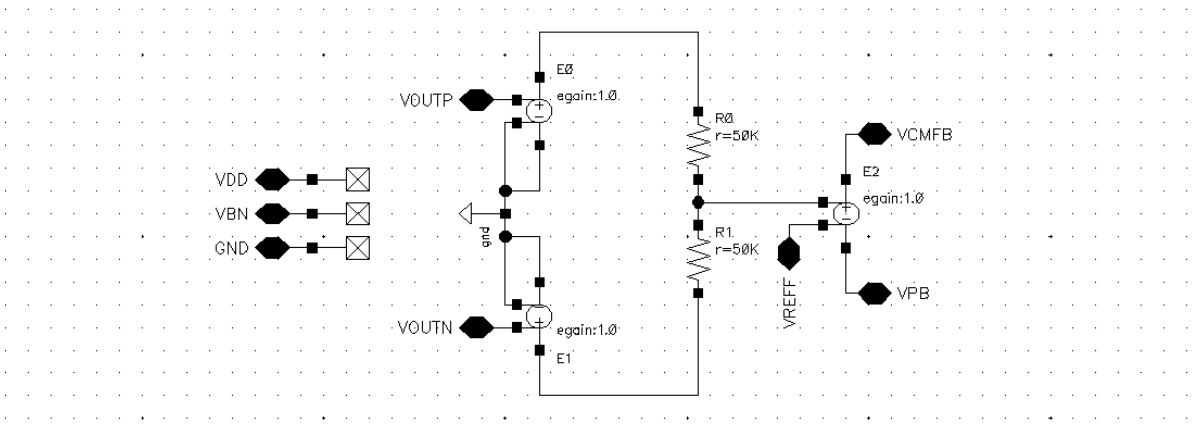


06 | From the assumed V*, select suitable biasing for the cascode transistors (VCP and VCN).

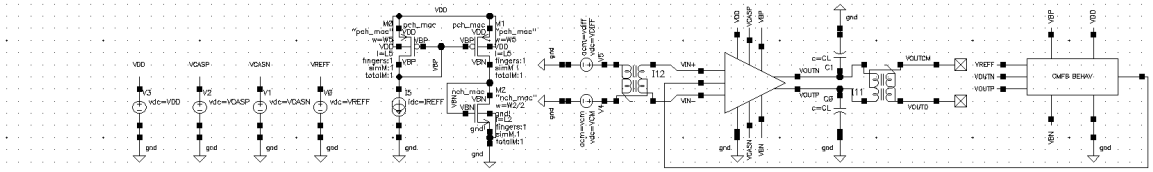
$$VCASN > V_{GS3} + V_2^* = 386.8\,mV + 200\,mV = 586.8\,mV \rightarrow VCASN = 786.8\,m$$

$$VCASP < -V_{SG4} - V_5^* + V_{DD} = -377.8\,mV - 200\,mV + 1.2 = 622\,mV \rightarrow VCASP = 422\,mV$$

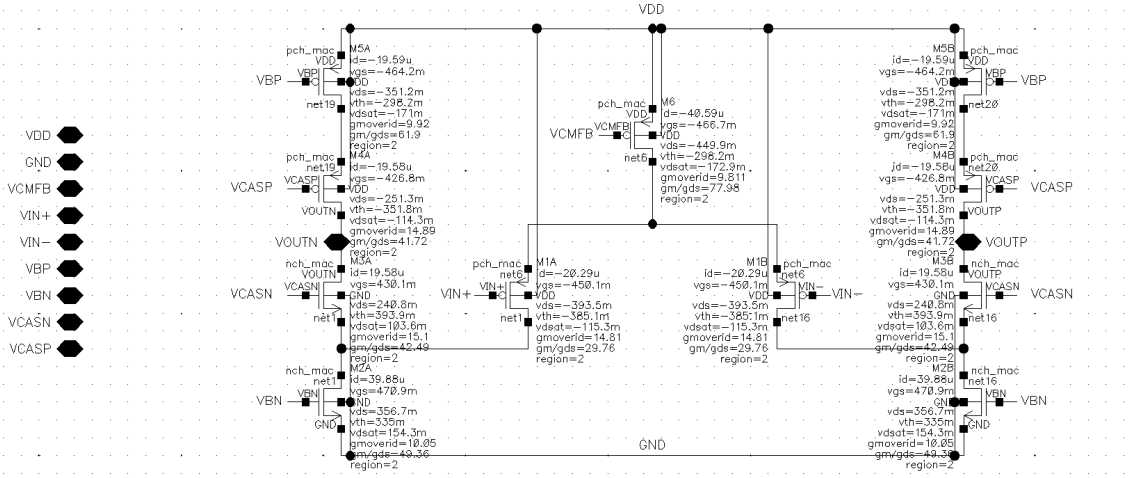
07 | We will start with a behavioral CMFB network similar to the one shown below. We use ideal buffers to avoid loading the OTA output with the CM sensing resistors. Note that we don't need high gain in the CMFB loop; thus, we use a gain = 1 in the error amplifier



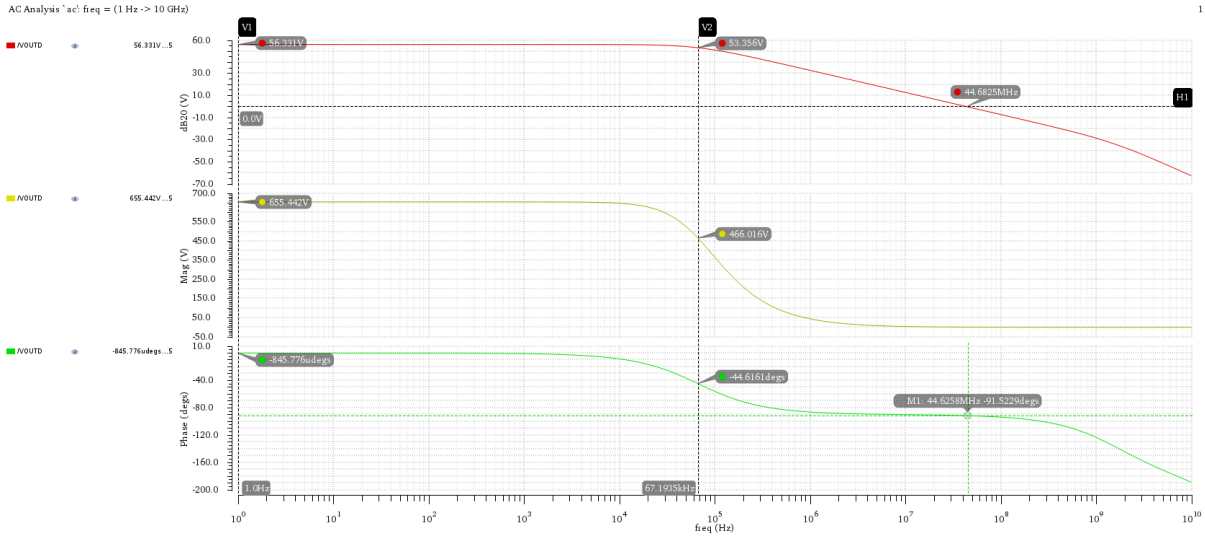
08 | Using calculated values and the behavioral CMFB in the following TB to get the initial points to tune design



09 | Apply DC operating points



10 | Apply AC analysis



11 | Since $A_{OL} \geq 56$ dB → there is no need to change in the design

	M1	M2	M3	M4	M5	M6
L	0.2 um	1 um	0.5 um	0.5 um	1 um	1 um
W	6 um	6.5 um	4.9 um	15.15 um	10.5 um	21 um
gmoverID	15	10	15	15	10	10

12 | Real CMFB Design Considerations

A | The 40uA current is divided between the CMFB branches. I assumed L = 1um and gm/ID = 15 for all transistors with unknown L or gm/ID for simplicity

B | The CD (buffers) were used to buffer the OTA output to avoid loading the OTA with sensing resistors.

C | The 40µA current was chosen to be distributed unequally among the branches, where the differential pair transistors were designed to get higher current to increase the differential input range and avoid full-steering of the current [11 µA was chosen for each branch of the differential pair and 6 µA in the other branches].

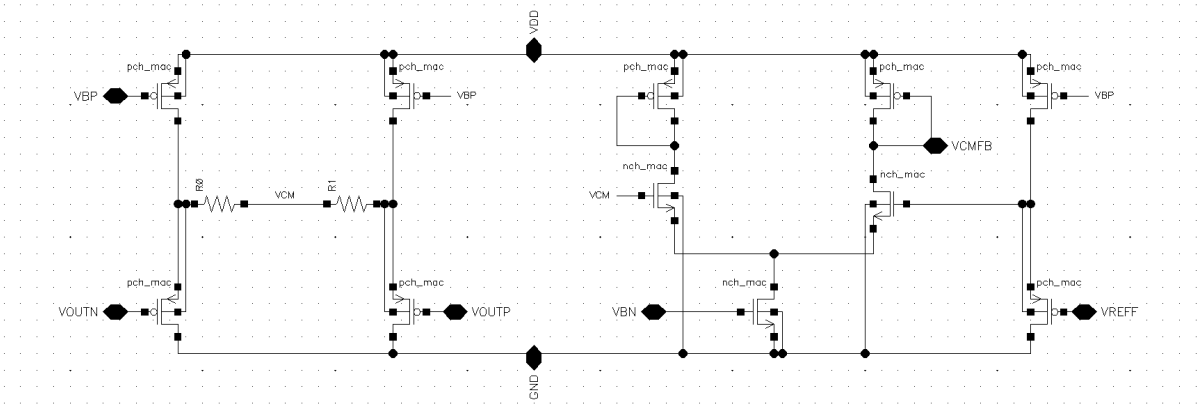
D | The sensing resistors are chosen such that the max current flowing through them (when diff sig is max) is less than the CD bias current, this avoids starving the CD when the diff output sig has its max excursion

E | The value of sensing resistors were chosen to sink at most 33% of the buffer bias current [at the case of maximum differential output swing which is 0.6 Volts] as follows:

$$\frac{0.6}{2R_{sen}} < \frac{1}{3} * 6 * 10^{-6} \rightarrow R_{sen} = 150\ k\Omega$$

F | An extra buffer was used for Vref such that it experiences the same VSG shift as the OTA output

G | The CMFB limits the output swing, the new output range is approx. $2V^*$: $V_{DD} - V^* - V_{SGbuff}$ → VREF was set to a value in the middle of the new output range (0.5 Volts approximately).



13 | Real CMFB Sizing

A | M_{BUFF_LOAD} : Assume L = 1u → ∵ @I_D = 20 uA → W = 10.5 um → ∴ @I_D = 6 uA → W = 3.15 um

B | M_{BUFF_IN} : Assume L = 1u → ∵ $A_{VBUFF} \approx 1 \rightarrow {}^{g_{mIN}}/_{I_D} = {}^{g_{mLOAD}}/_{I_D}$ → W = 3.15 um

C | M_{EA_5} : Assume L = 1u → ∵ @I_D = 40 uA → W = 6.5 um → ∴ @I_D = 22 uA → W = 3.575 um

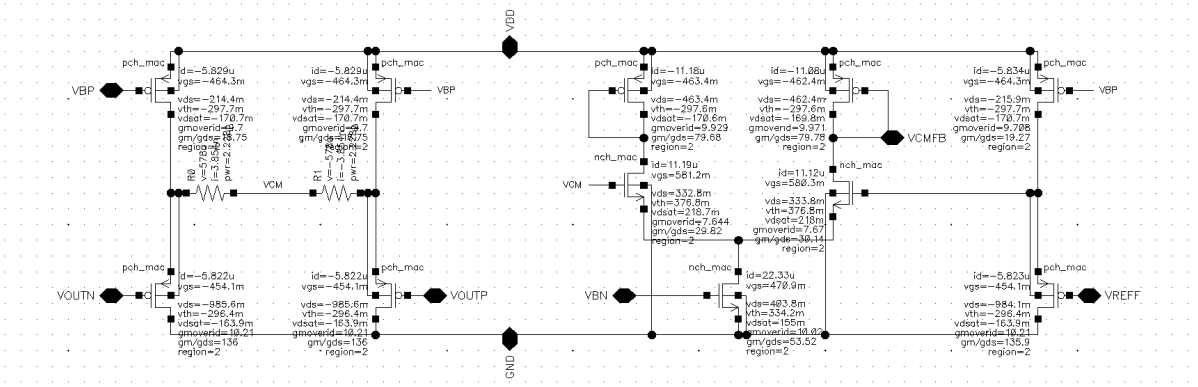
D | M_{EA_12} : Assume L = 1u and ${}^{g_m}/_{I_D} = 15$ → W = 5.6 um

E | M_{EA_34}: Assume L = 1u and ∵ $VSG_{EA2} = VSG_6 = 466$ mV → ${}^{I_D}/_{W} = 2$ → W = 5.5 um

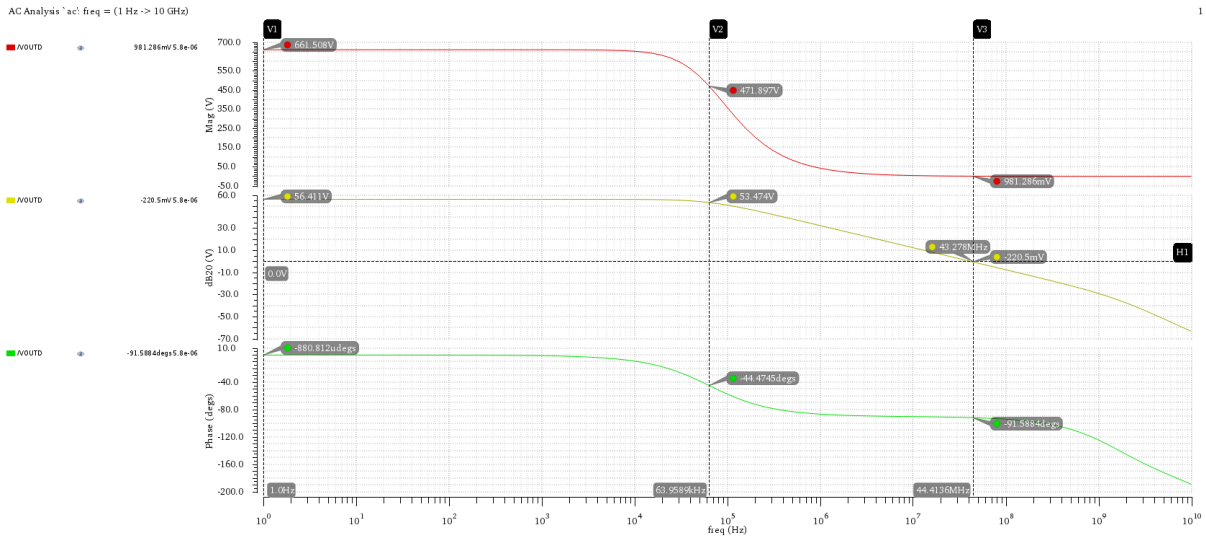
	M_{BUFF_LOAD}	M_{BUFF_IN}	M_{EA_12}	M_{EA_34}	M_{EA_5}
L	0.2 um	1 um	0.5 um	0.5 um	1 um
W	3.15 um	3.15 um	5.6 um	5.5 um	3.575 um

14 | Re-Analysis

A | CMFB DC operating points

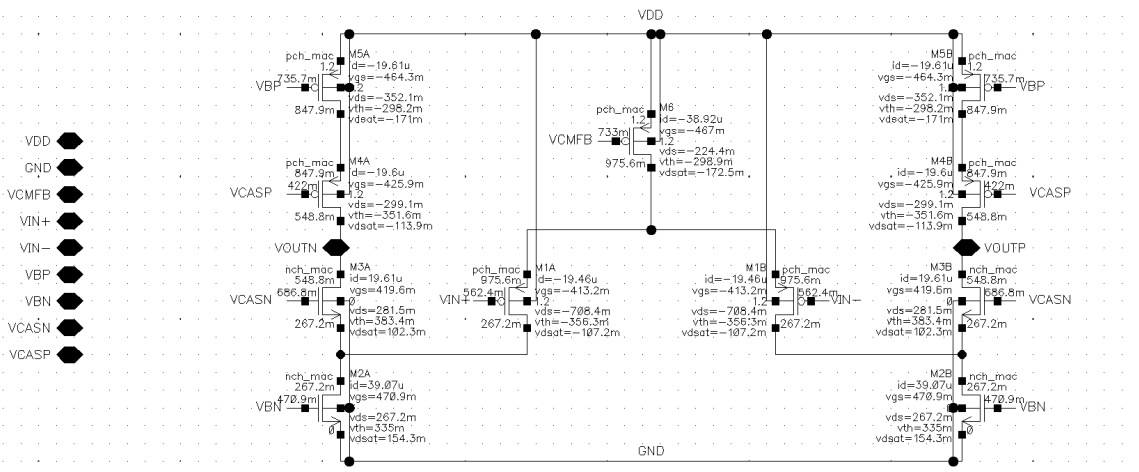


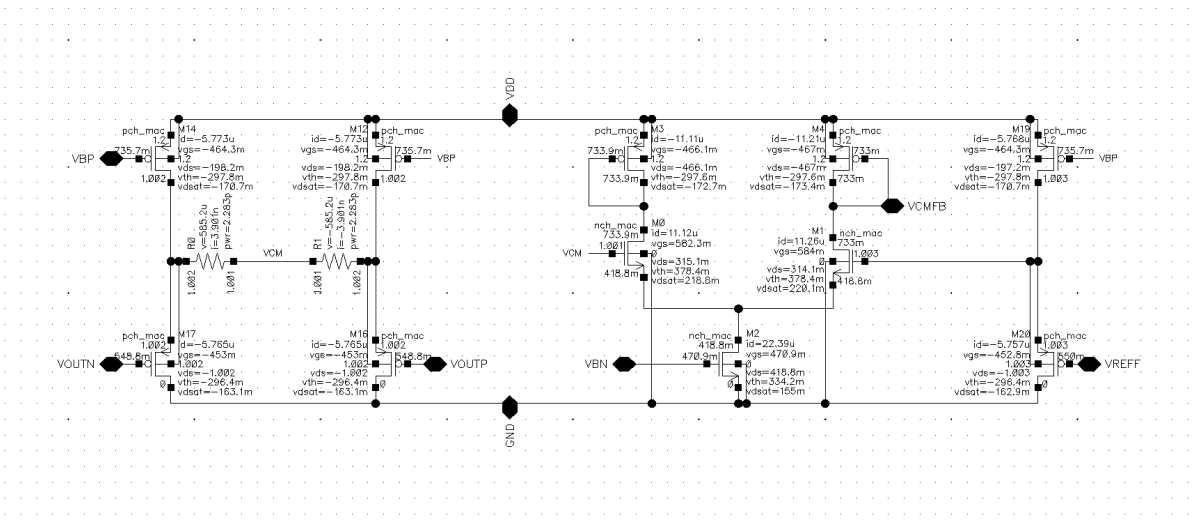
B | AC Analysis



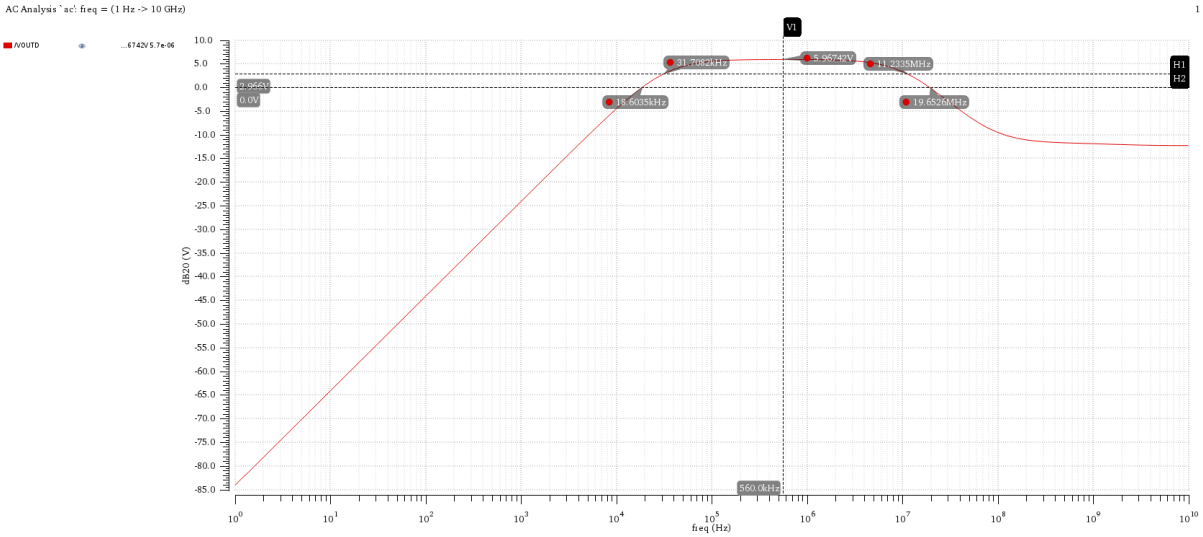
15 | Closed Loop Simulations

A | DC Operating Points





B | AC Analysis



16 | STB Analysis