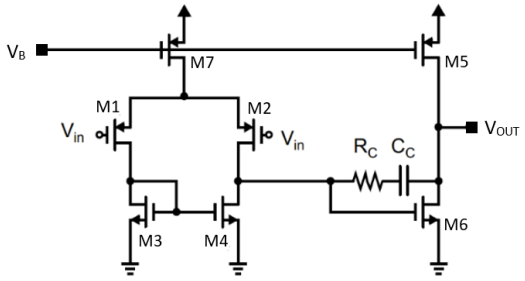
Analog Integrated Circuits Designs
Single Ended Two Stage Miller Compensated OTA

Design No. 2			
Av	≥ 54 dB	PM	≥ 60°
UGF	≥ 300 MHz	CL	1 pF
Power Consumption	≤ 1mW	Reference Current	10 uA

01 | Since no constrains on CMIR → Choose PMOS input devices as they gives better matching



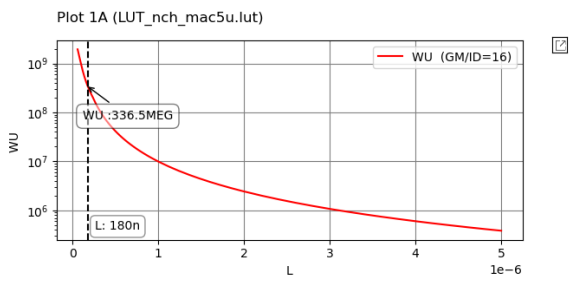
02 | General considerations

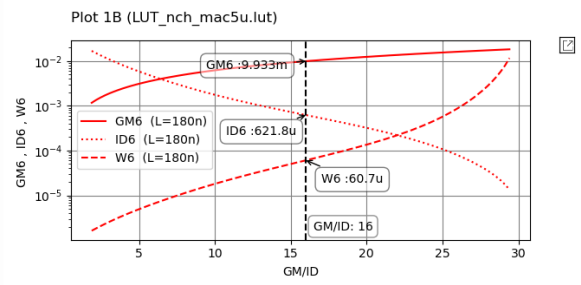
- $C_L = \alpha \times C_C \rightarrow$ Choose $\alpha = 2$
- $C_C = \beta \times C_{GS6} \rightarrow$ Choose $\beta = 5$
- ${}^{\omega_{p2}}/_{\omega_u} = \gamma \rightarrow$ Choose $\gamma = 4 \rightarrow$ Fastest Settling time without peaking

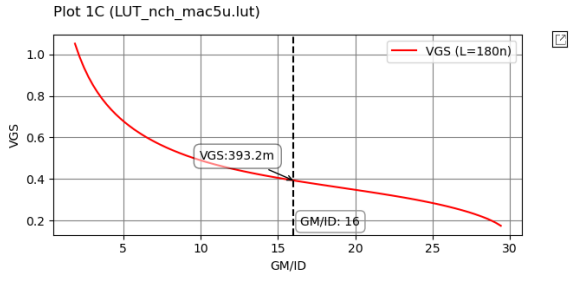
M6 Sizing

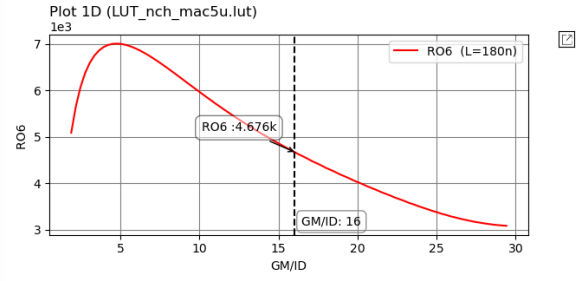
03 | $\omega_u = {}^{\omega_{p2}}/_{\gamma} \approx \left({}^{g_{m6}}/_{2\pi \times C_L}\right)\left({}^{1}/_{\gamma}\right) = \left({}^{g_{m6}}/_{2\pi \times C_{GS6}}\right)\left({}^{1}/_{\alpha \times \beta \times \gamma}\right) = f_{T6}\left({}^{1}/_{\alpha \times \beta \times \gamma}\right) = {}^{f_{T6}}/_{40}$

04 | Bias M_6 @MI $\rightarrow {}^{g_{m6}}/_{I_D} = 16 \rightarrow L_6 = 180$ nm $\rightarrow I_{D6} = 621.8$ uA $\rightarrow W_6 = 60.7$ um, $g_{m6} = 9.933$ mS, $r_{o6} = 4.6$ kΩ



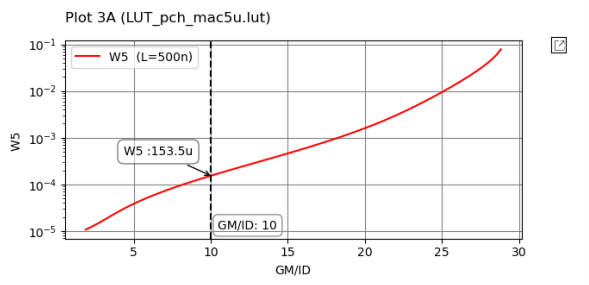


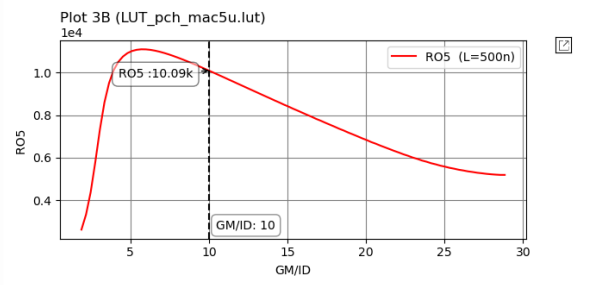


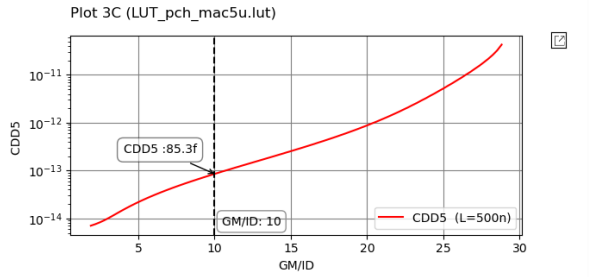


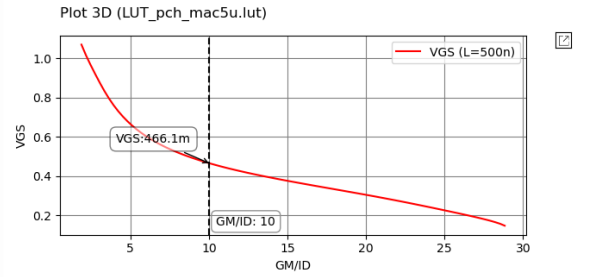
Sizing of Current Mirror M5

05 | Since no spec on CMRR → Assume relatively long $L_5 = 500$ nm and bias it in SI ${}^{g_{m5}}/_{I_D}$ 10 to get better mirroring









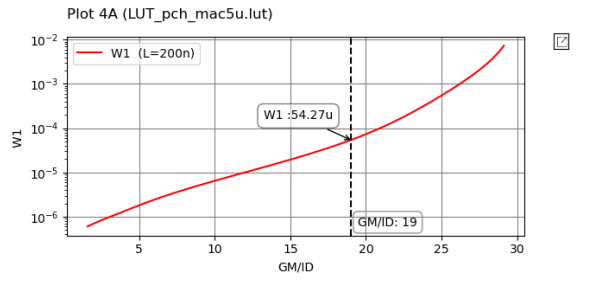
06 | $\because A_{V2} = g_{m6} \times r_{o6} \parallel r_{o5} = 31 \rightarrow A_{V1} = {}^{A_V}/_{A_{V2}} = 16.5$

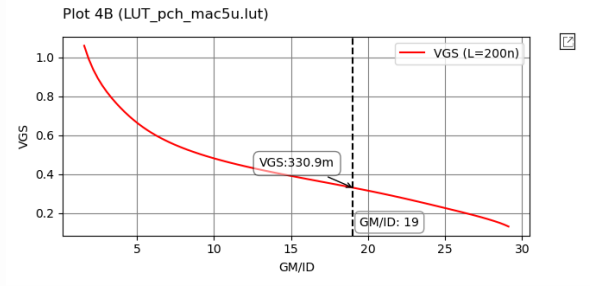
Sizing of M1, M2

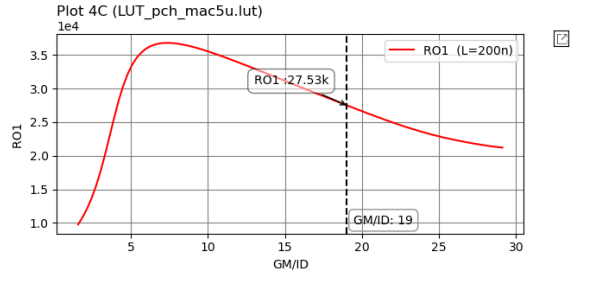
07 | $\because {}^{\omega_{p2}}/_{\omega_u} = 4 \rightarrow {}^{g_{m6}}/_{g_{m1}} = 8 \rightarrow g_{m1} = 1.241\ \text{mS}$

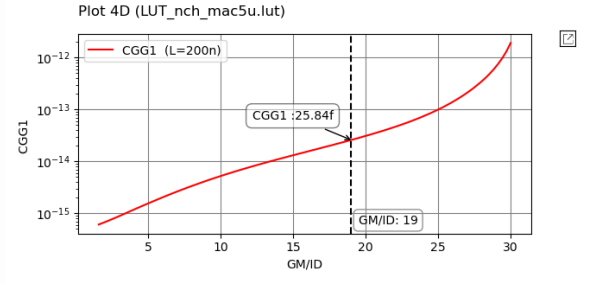
08 | Choose short L = 200 nm for input device to avoid cloosed loop capacitive loading

09 | Baising it in WI ${}^{g_{m1}}/_{I_D} = 19$ to maximize efficiency $\rightarrow I_{D1} = 65.3\ \text{uA} \rightarrow I_{B1} = 130.6\ \text{uA}$





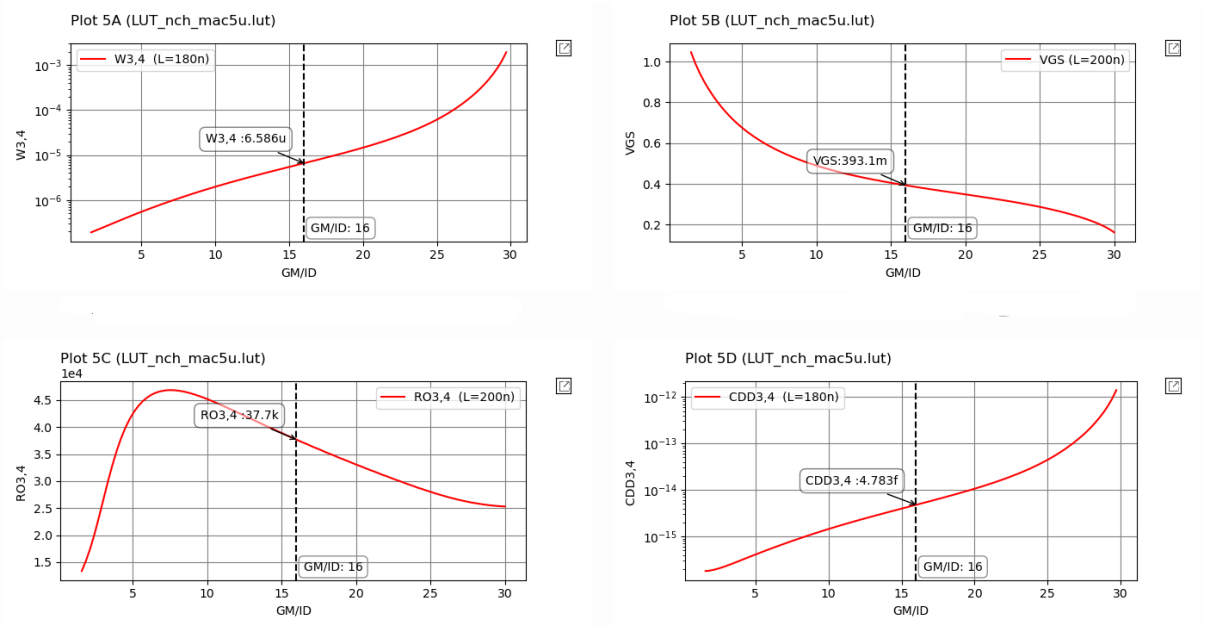




Sizing of M3, M4

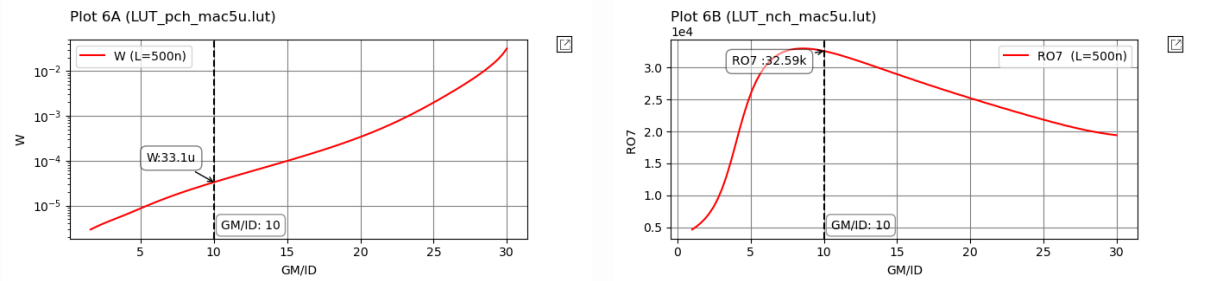
10 | Set $L_{3,4} = L_6 = 180\ \text{nm} \rightarrow$ and ${}^{g_{m3,4}}/_{I_D} = {}^{g_{m6}}/_{I_D} = 16 \rightarrow W_{3,4} = 6.6\ \text{um} \rightarrow r_{o3,4} = 37.7\ \text{k}\Omega$

11 | $A_{V1} = g_{m1} \times r_{o1,2} \parallel r_{o3,4} = 19 \rightarrow A_V = 589$



Sizing of Current Mirror M7

12 | $I_{D7} = 2I_{D1} = 130.6$ uA → Assume relatively long $L_5 =$ 500 nm and bias it in SI $^{g_{m7}}/_{I_D}$ 10 to get better mirroring

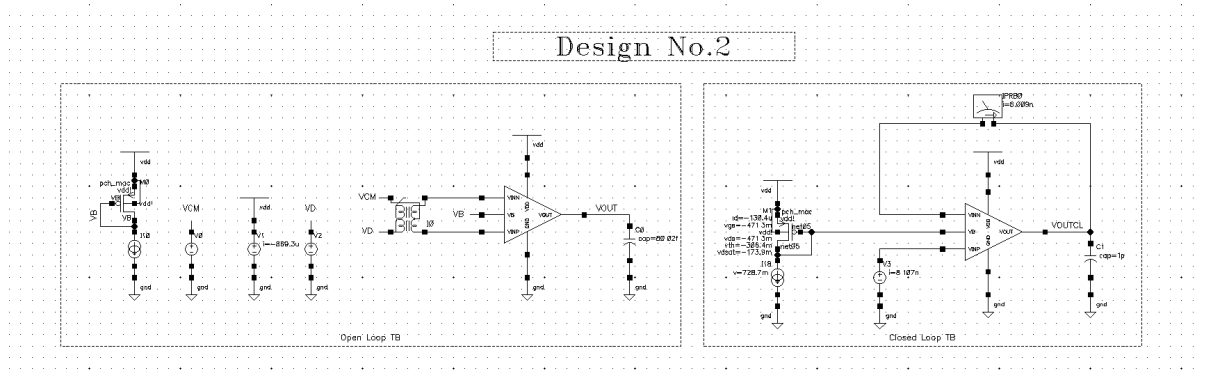


Sizing Summary

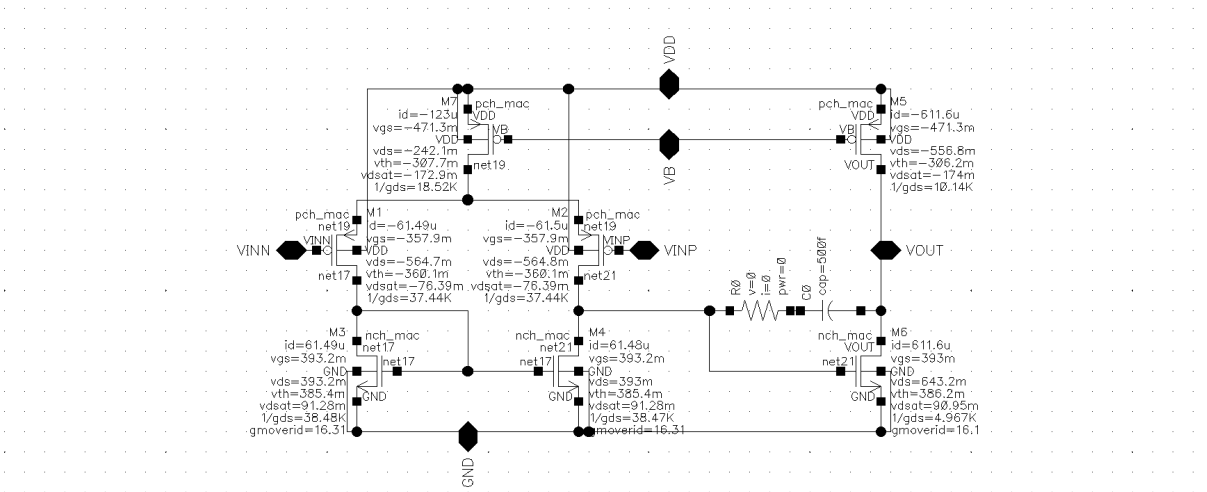
	M1	M2	M3	M4	M5	M6	M7
L	200 nm	200 nm	180 nm	180 nm	500 nm	180 nm	500 nm
W	54.3 um	54.3 um	6.6 um	6.6 um	153.5 um	60.7 um	33.1 um
gmoverID	19	19	16	16	10	16	10

Test Bench and Results

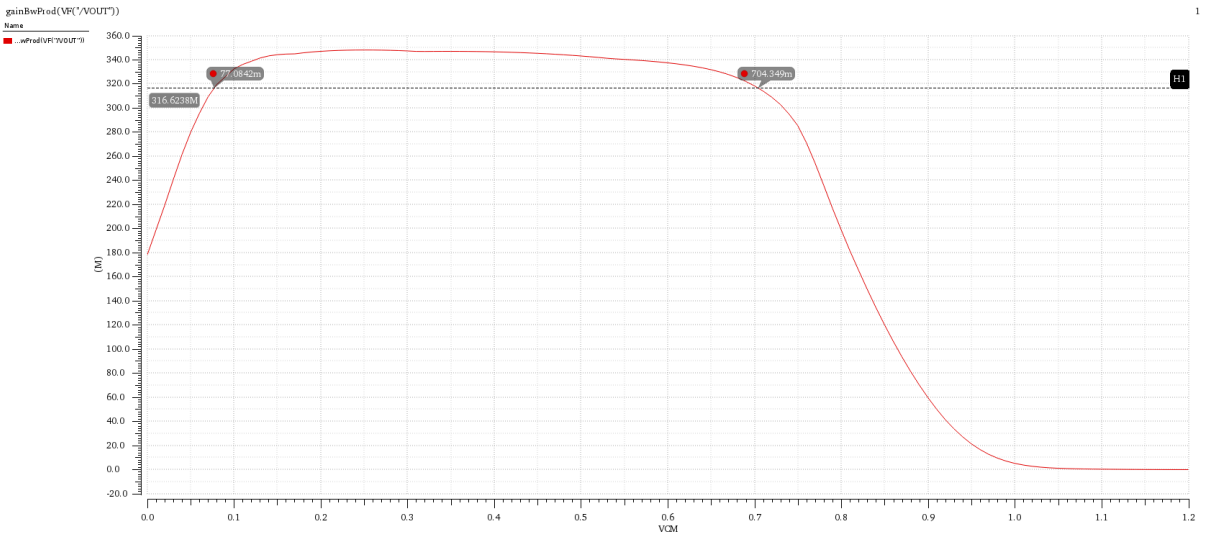
01 | Test Bench



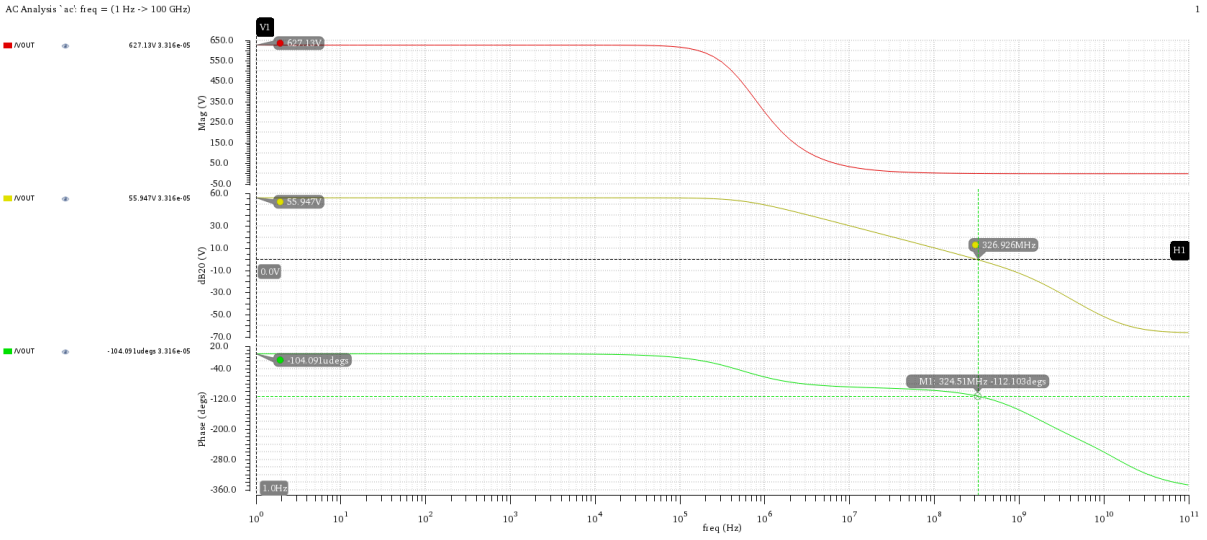
02 | DC Operating Points



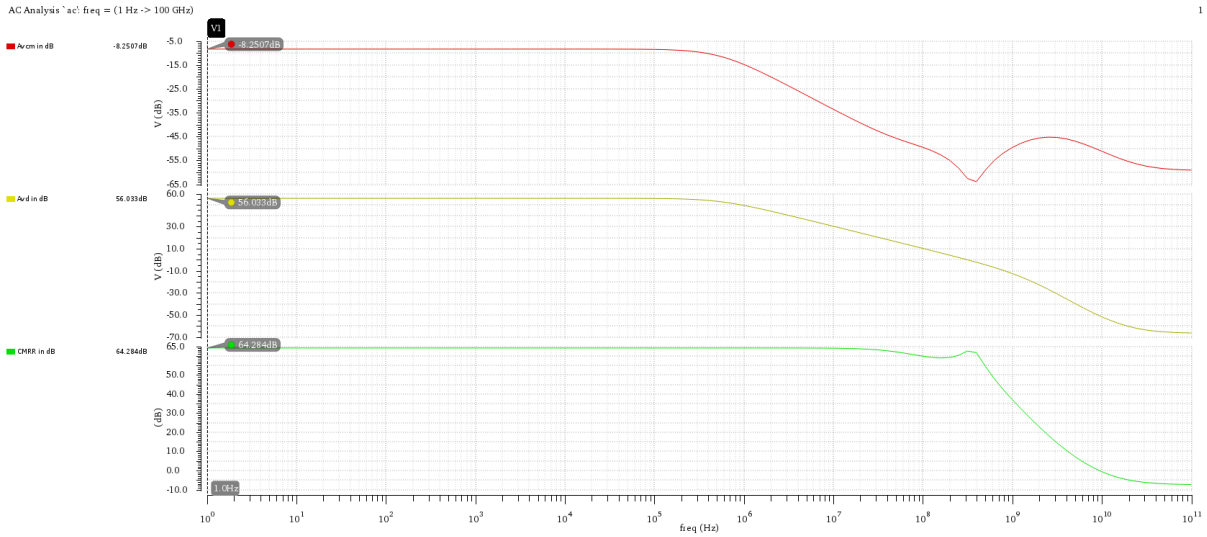
03 | CM Input Range



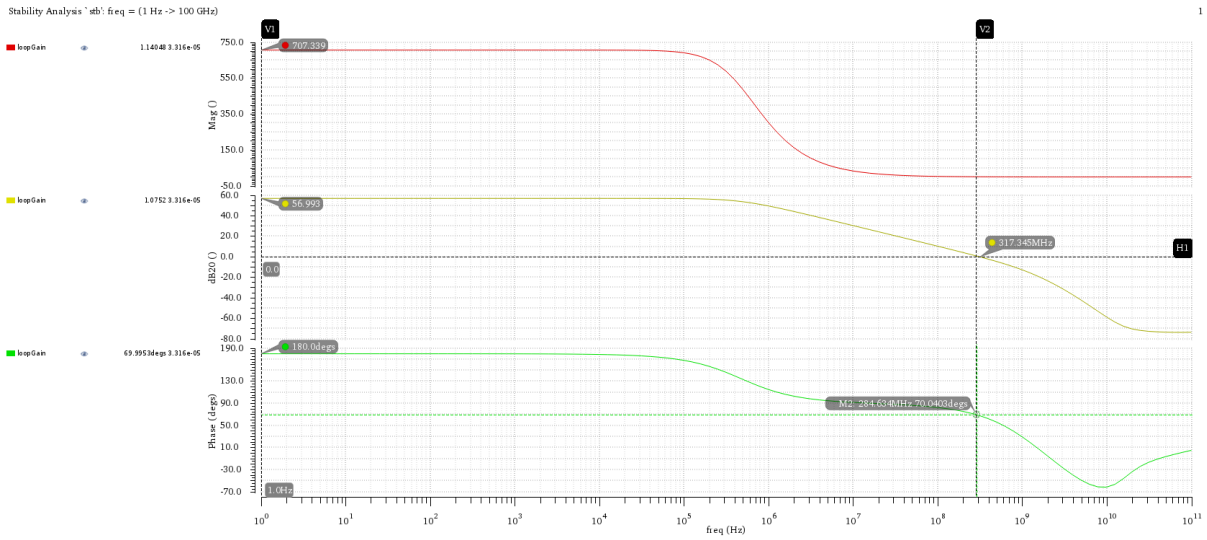
04 | AC Open loop



05 | Common Mood Rejection Ratio



06 | AC Closed Loop



Results Summary

Spec	Required	Achieved
Av	≥ 54 dB	55.9 dB
UGF	≥ 300 MHz	326 MHz
Power Consumption	≤ 1mW	880 uW
PM	≥ 60°	70°