Project 1 -----> Abdelrahman Khaled Fouad Abdelrahim

Design code:

Workspace Trust | P1.v | basys_master.xdc

D: > new hard > Sessions Digital design and verification > mini project > P1.v

```
//instantiated module among the whole project
module Register_Mux #(parameter WIDTH=18,REG_IDENTIFIER=1,RSTTYPE="SYNC") (input [WIDTH-1:0] X,input CLK ,rst,EN,output  [WIDTH-1:0] out);
reg [WIDTH-1:0] X_reg;
always@(posedge CLK, posedge rst) begin
    if(RSTTYPE=="ASYNC") begin
        if(rst) X_reg<=0;
        else if(EN) X_reg<=X;
    end
end
always@(posedge CLK) begin
    if(RSTTYPE=="SYNC")begin
        if(EN) begin
            if(rst) X_reg<=0;
            else  X_reg <=X;
  end
end
end
assign out =(REG_IDENTIFIER)?X_reg:X;
endmodule

module DSP48A1_Project (A,B,D,C,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
//parameters declaration
parameter A0REG=0;
parameter A1REG=1;
parameter B0REG=0;
parameter B1REG=1;
parameter CREG=1;
parameter DREG=1;
parameter MREG=1;
parameter PREG=1;
parameter CARRYINREG=1;
parameter CARRYOUTREG=1;
parameter OPMODEREG=1;
parameter CARRYINSEL= "OPMODE5";
parameter B_INPUT ="DIRECT";
parameter RSTTYPE ="SYNC";
//input/output declaration
input [17:0] A,B,D,BCIN;
input [47:0] C,PCIN;
input [7:0] OPMODE;
input CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
output  [17:0] BCOUT;
output  [47:0] PCOUT,P;
output  [35:0] M;
output  CARRYOUT,CARRYOUTF;
//internal signals
wire [17:0] A0_reg,A1_reg,B0_input,B0_reg,B1_input,B1_reg,D_reg,Pre_add_sub_out;
wire [47:0] C_reg,concat_out,X_out ,Z_out;
wire [48:0] Post_add_sub_out;
wire[35:0] M_reg,multiplier_out;
wire [7:0] OPMODE_reg;
wire CARRYIN reg,CYI,CYO;
//Project Main
assign B0_input =(B_INPUT=="DIRECT")?B:BCIN;
Register_Mux #(18,DREG,RSTTYPE) D_register (D,CLK,RSTD,CED,D_reg);
Register_Mux #(18,B0REG,RSTTYPE) B0_register (B0_input,CLK,RSTB,CEB,B0_reg);
Register_Mux #(18,A0REG,RSTTYPE) A0_register (A,CLK,RSTA,CEA,A0_reg);
Register_Mux #(18,A1REG,RSTTYPE) A1_register (A0_reg,CLK,RSTA,CEA,A1_reg);
Register_Mux #(48,CREG,RSTTYPE) C_register (C,CLK,RSTC,CEC,C_reg);
Register_Mux #(8,OPMODEREG,RSTTYPE) OPMODE_register (OPMODE,CLK,RSTOPMODE,CEOPMODE,OPMODE_reg);
assign CYI =(CARRYINSEL=="OPMODE5")?OPMODE_reg[5]:(CARRYINSEL=="CARRYIN")?CARRYIN:0;
Register_Mux #(1,CARRYINREG,RSTTYPE) CARRYIN_register (CYI,CLK,RSTCARRYIN,CECARRYIN,CARRYIN_reg);
//Pre_adder/Subtracter
assign Pre_add_sub_out =(OPMODE_reg[6])?(D_reg-B0_reg):(D_reg+B0_reg);
assign B1_input =(OPMODE_reg[4])?Pre_add_sub_out:B0_reg;
Register_Mux #(18,B1REG,RSTTYPE) B1_register (B1_input,CLK,RSTB,CEB,B1_reg);
assign BCOUT = B1_reg;
//Multiplier
assign multiplier_out = A1_reg*B1_reg;
assign concat_out ={D[11:0],A1_reg,B1_reg};
Register_Mux #(36,MREG,RSTTYPE) M_register (multiplier_out,CLK,RSTM,CEM,M_reg);
assign M =~(~M_reg);
assign X_out=(OPMODE_reg[1:0]==0)?0:(OPMODE_reg[1:0]==1)?M_reg:(OPMODE_reg[1:0]==2)?P:concat_out;
assign Z_out=(OPMODE_reg[3:2]==0)?0:(OPMODE_reg[3:2]==1)?PCIN:(OPMODE_reg[3:2]==2)?P:C_reg;
//Post_adder/Subtracter
assign Post_add_sub_out =(OPMODE_reg[7])?(Z_out-(X_out+CARRYIN_reg)):(Z_out+X_out+CARRYIN_reg);
assign CYO = Post_add_sub_out[48];
Register_Mux #(1,CARRYOUTREG,RSTTYPE) CARRYOUT_register (CYO,CLK,RSTCARRYIN,CECARRYIN,CARRYOUT);
assign CARRYOUTF =CARRYOUT;
Register_Mux #(48,PREG,RSTTYPE) P_register (Post_add_sub_out[47:0],CLK,RSTP,CEP,P);
assign PCOUT=P;
endmodule
```

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Tb code:

Workspace Trust | P1.v | P1_tb.v | run_tb.do | basys_master.xdc

D: > new hard > Sessions Digital design and verification > mini project > P1_tb.v

```
module Project_tb ();
//Signal Declaration
reg CLK,CARRYIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE;
reg [7:0] OPMODE;
reg [17:0] A,B,D,BCIN;
reg [47:0] C,PCIN;
wire CARRYOUT,CARRYOUTF;
wire [17:0] BCOUT;
wire[35:0] M;
wire [47:0] PCOUT,P;
//DUT instantiation
DSP48A1_Project DUT (A,B,D,C,CLK,CARRYIN,OPMODE,BCIN,RSTA,RSTB,RSTM,RSTP,RSTC,RSTD,RSTCARRYIN,RSTOPMODE,
CEA,CEB,CEM,CEP,CEC,CED,CECARRYIN,CEOPMODE,PCIN,BCOUT,PCOUT,P,M,CARRYOUT,CARRYOUTF);
//CLOCK generation
initial begin
    CLK=0;
    forever begin
        #1 CLK=~CLK;
    end
end
initial begin
    //reset all
    CEA=1;CEB=1;CEM=1;CEP=1;CEC=1;CED=1;CECARRYIN=1;CEOPMODE=1;
    RSTA=1;RSTB=1;RSTM=1;RSTP=1;RSTC=1;RSTD=1;RSTCARRYIN=1;RSTOPMODE=1;
    #20;
    if(P!=0) begin
        $display("output is wrong");
        $stop;
    end
    RSTA=0;RSTB=0;RSTM=0;RSTP=0;RSTC=0;RSTD=0;RSTCARRYIN=0;RSTOPMODE=0;
    OPMODE='b00111101; //C+[([D+B].A)+OPMODE[5]]
    D=1000;B=2000;A=3;C=10; //Expected output = 3311
    #20;
    if(P!=9011) begin
        $display("output is wrong");
        $stop;
    end
    OPMODE='b01011101; //C+[(D-B).A]
    D=35;B=15;A=5;C=50;//Expected output =150
    #20
    if(P!=150) begin
        $display("output is wrong");
        $stop;
    end
    OPMODE='b11001101; //C-(A.B)
    B=15;A=5;C=250;    //Expected output =175
    #20
    if(P!=175) begin
        $display("output is wrong");
        $stop;
    end
$stop;
end
endmodule
```

Do file:

Workspace Trust | P1.v | P1_tb.v | run_tb.do

D: > new hard > Sessions Digital design and verification > mini project > run_tb.do

```
vlib work
vlog P1.v P1_tb.v
vsim -voptargs=+acc work.Project_tb
add wave *
add wave -position insertpoint  \
sim:/Project_tb/DUT/A0_reg \
sim:/Project_tb/DUT/A1_reg \
sim:/Project_tb/DUT/B0_reg \
sim:/Project_tb/DUT/B1_reg \
sim:/Project_tb/DUT/D_reg \
sim:/Project_tb/DUT/C_reg \
sim:/Project_tb/DUT/M_reg \
sim:/Project_tb/DUT/OPMODE_reg \
sim:/Project_tb/DUT/CARRYIN_reg
run -all
#quit -sim
```

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Constrain file:

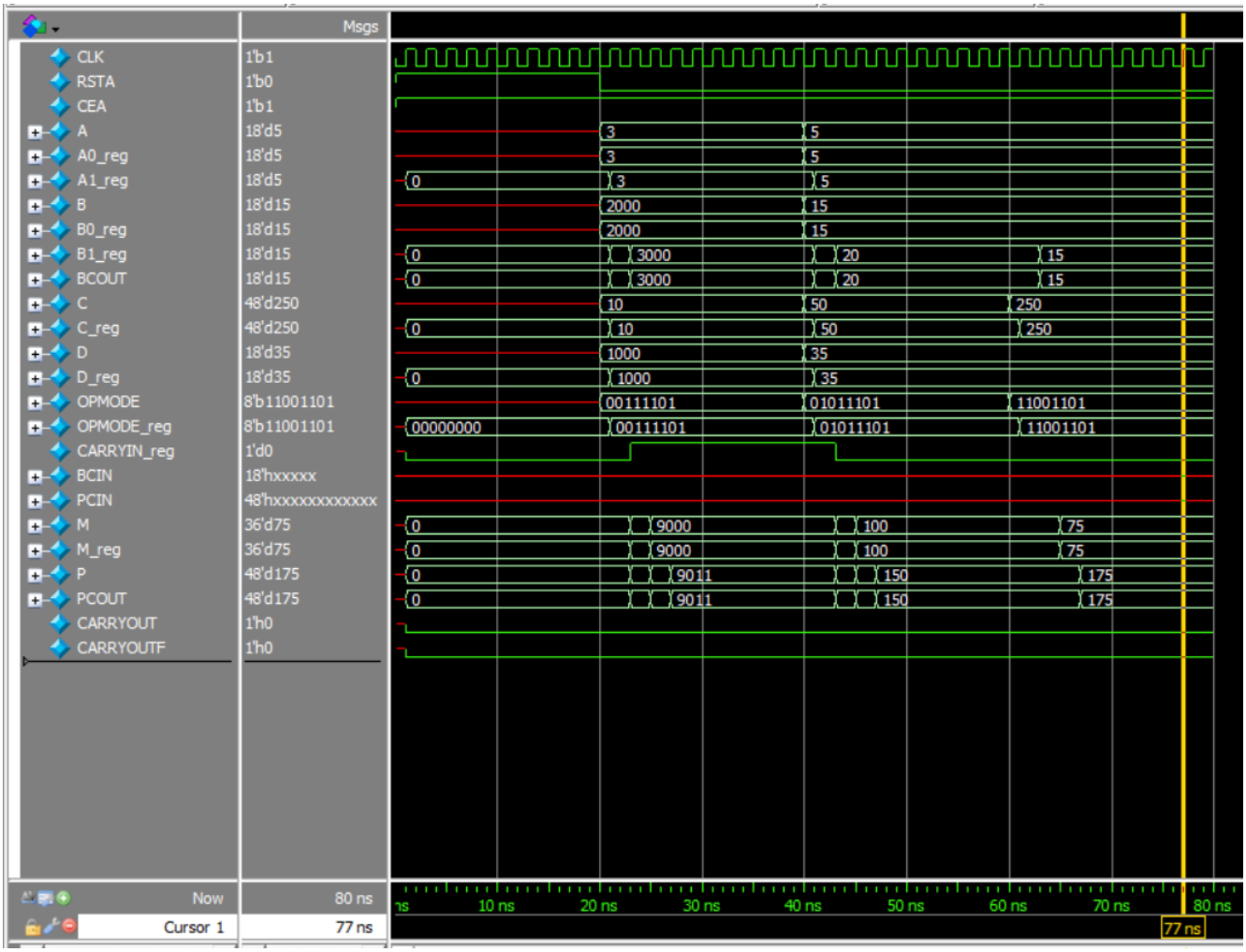
Workspace Trust | P1.v | basys_master.xdc

D: > new hard > Sessions Digital design and verification > mini project > basys_master.xdc

```
1   ## This file is a general .xdc for the Basys3 rev B board
2   ## To use it in a project:
3   ## - uncomment the lines corresponding to used pins
4   ## - rename the used ports (in each line, after get_ports) according to the top level signal names in the project
5
6   ## Clock signal
7   set_property -dict { PACKAGE_PIN W5   IOSTANDARD LVCMOS33 } [get_ports CLK]
8   create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports CLK]
```

```
152 ## Configuration options, can be used for all designs
153 set_property CONFIG_VOLTAGE 3.3 [current_design]
154 set_property CFGBVS VCCO [current_design]
155
156 ## SPI configuration mode options for QSPI boot, can be used for all designs
157 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
158 set_property BITSTREAM.CONFIG.CONFIGRATE 33 [current_design]
159 set_property CONFIG_MODE SPIx4 [current_design]
```

Test cases:



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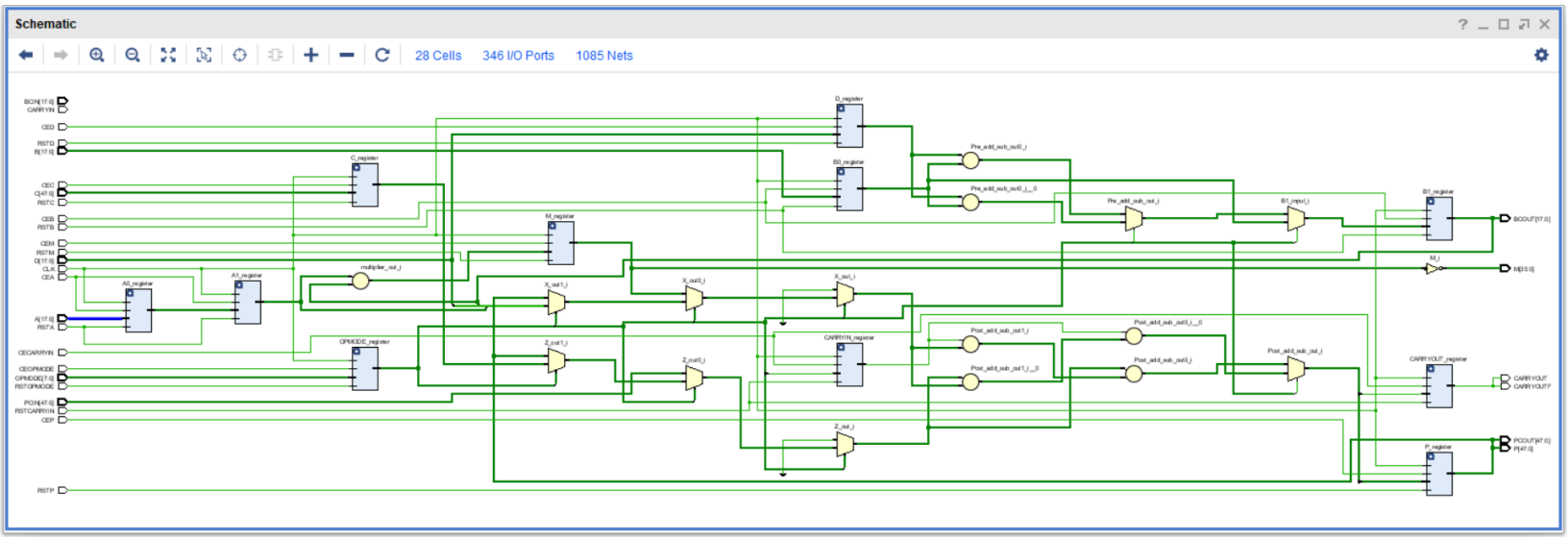
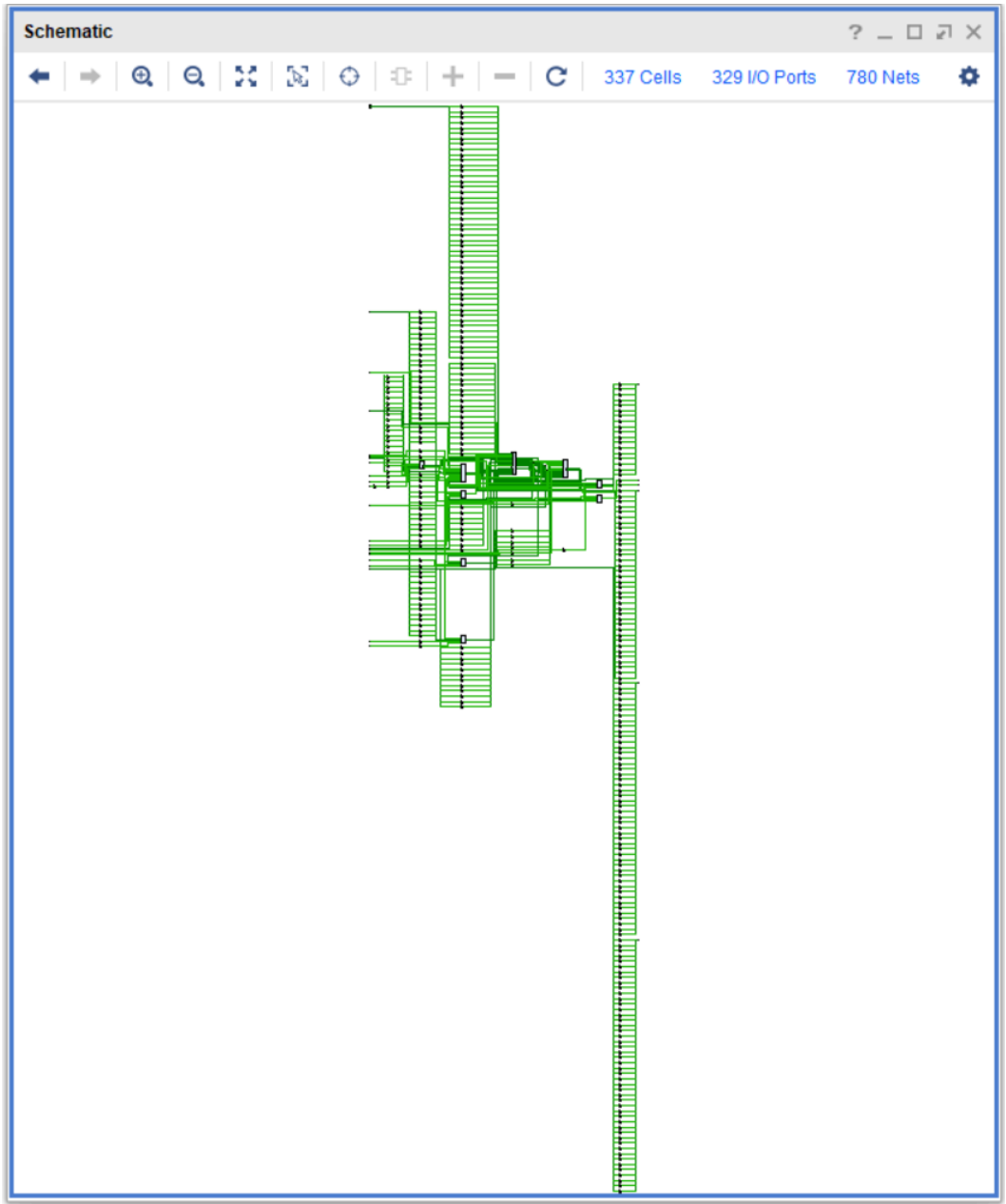
Elaborated design:



Synthesized design:



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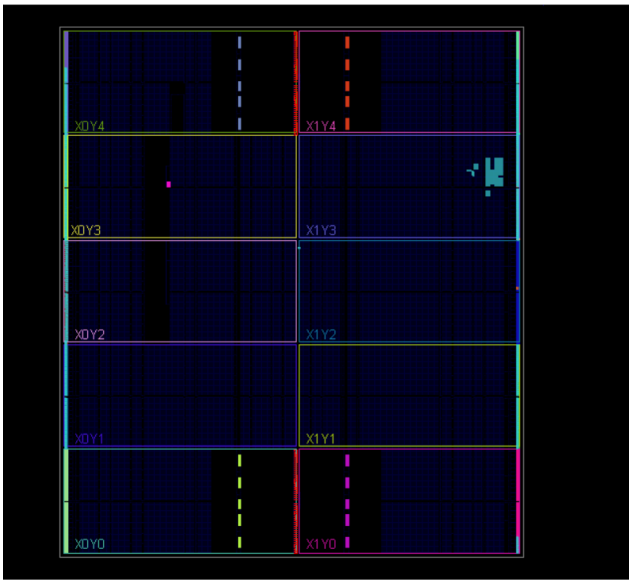
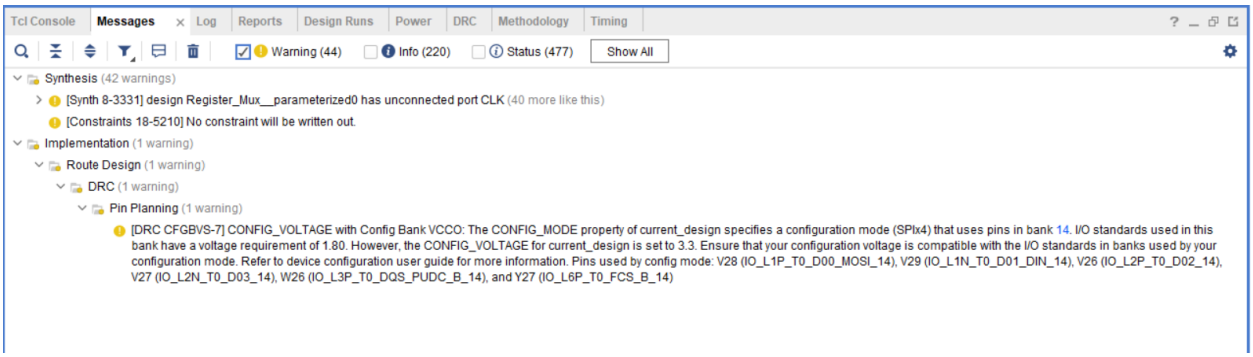
Implemented design:



Messages:



Utilization and timing reports: