Project

SPI-Slave with single port RAM

Team members:

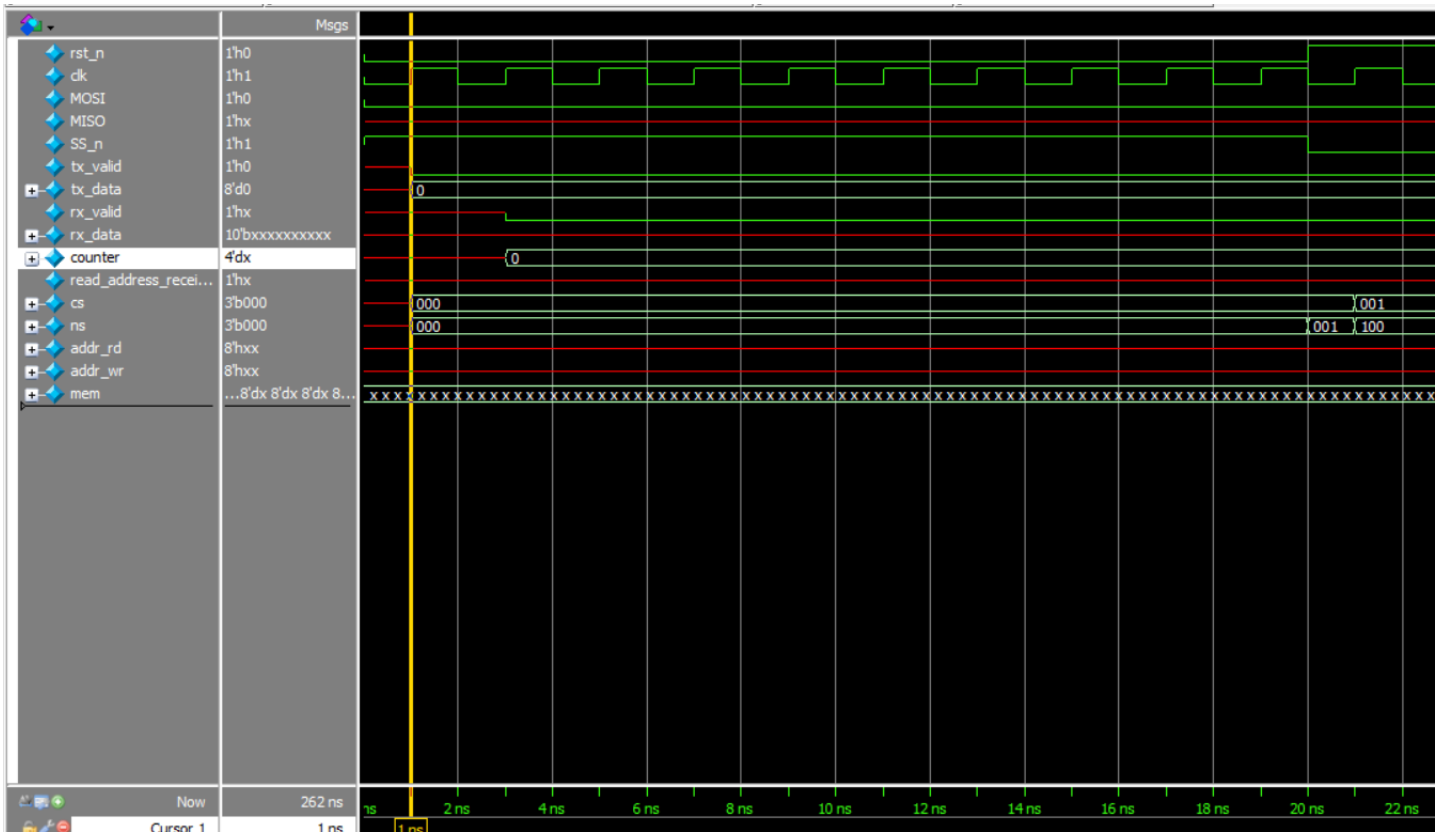
Ahmed Haitham Othman

Abdelrahman Khaled Fouad

Mohamed Adel Abdelrahem

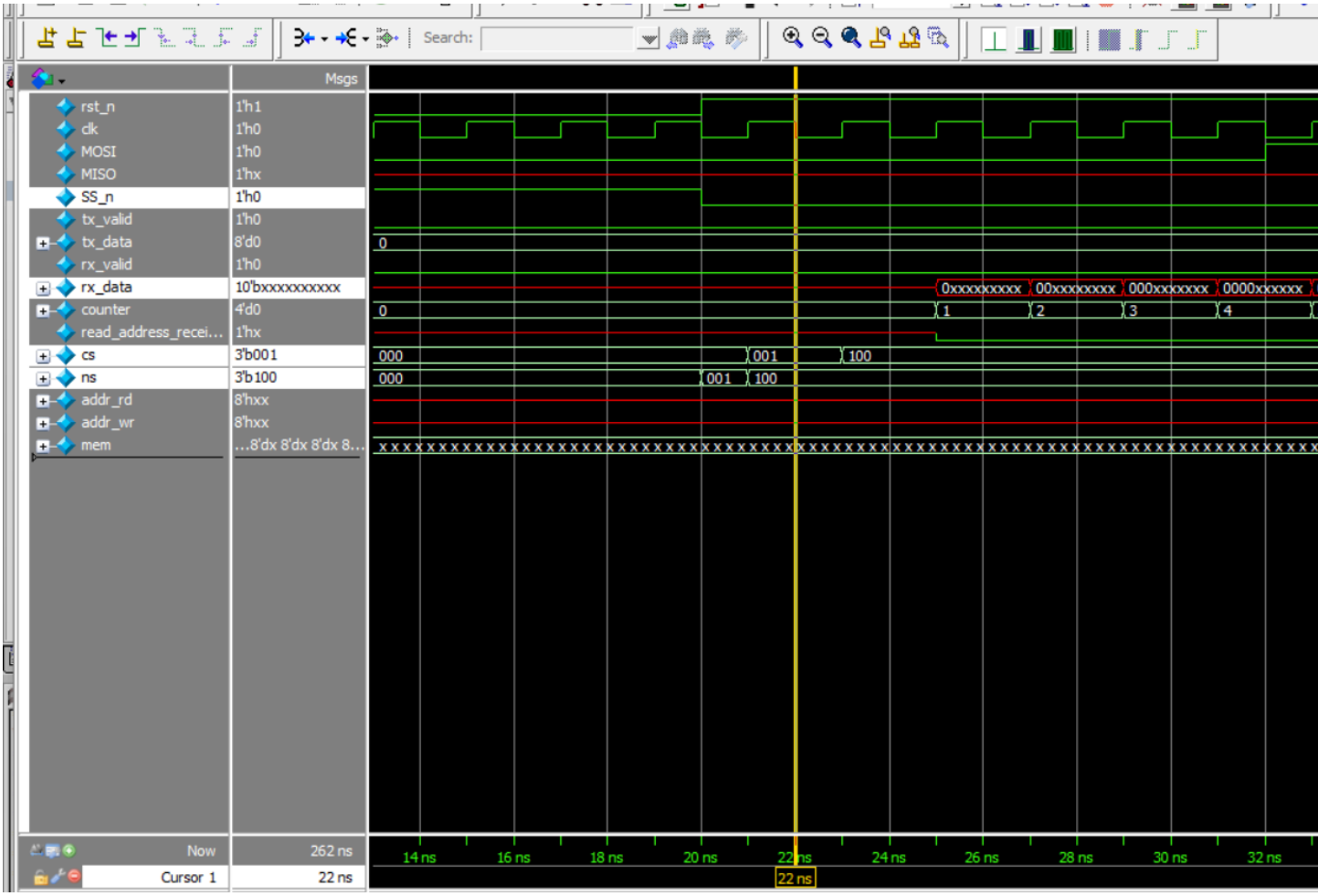
1) Snippets from the waveforms captured from QuestaSim for the design with inputs assigned values and output values visible.

1st test the reset



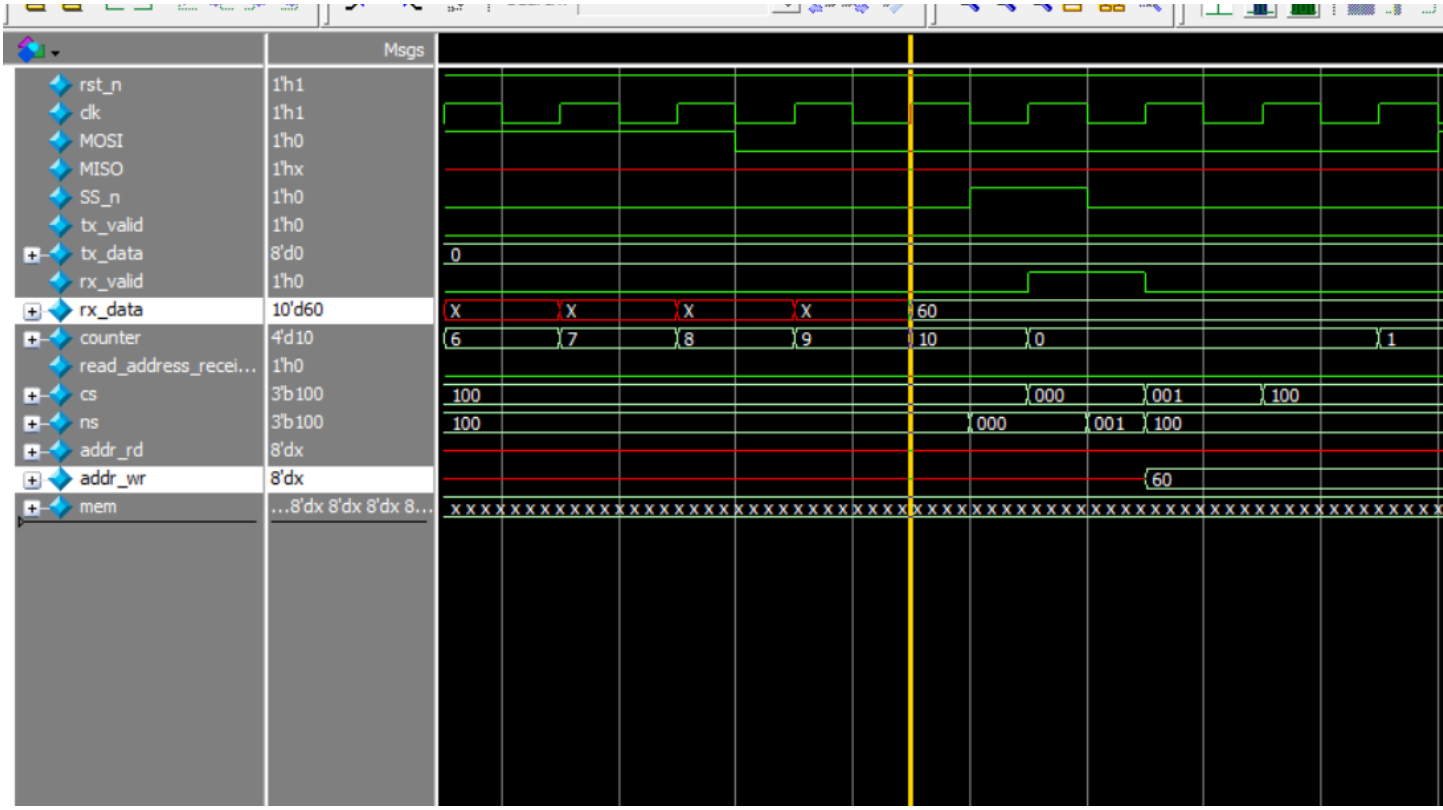
2nd test the write address the ns will be 100 which is WRITE state

And the rx_data will change every clk cycle with 1 bit input seril and after 10 clk cycle (counter==10) the rx_data is now full with the wr_address

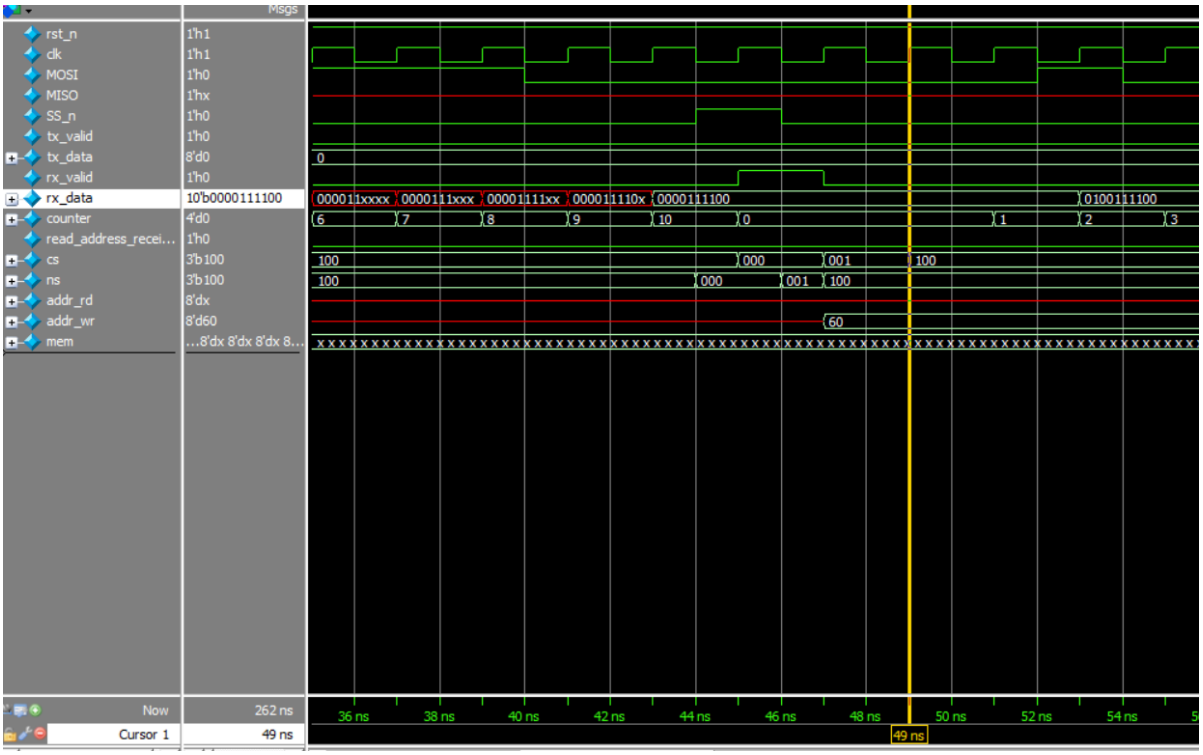


3rd now the rx_data is full and after 1 clk cycle the the rx_valid=1 .

And @ 2nd clk cycle the addr_wr=rx_data=60.

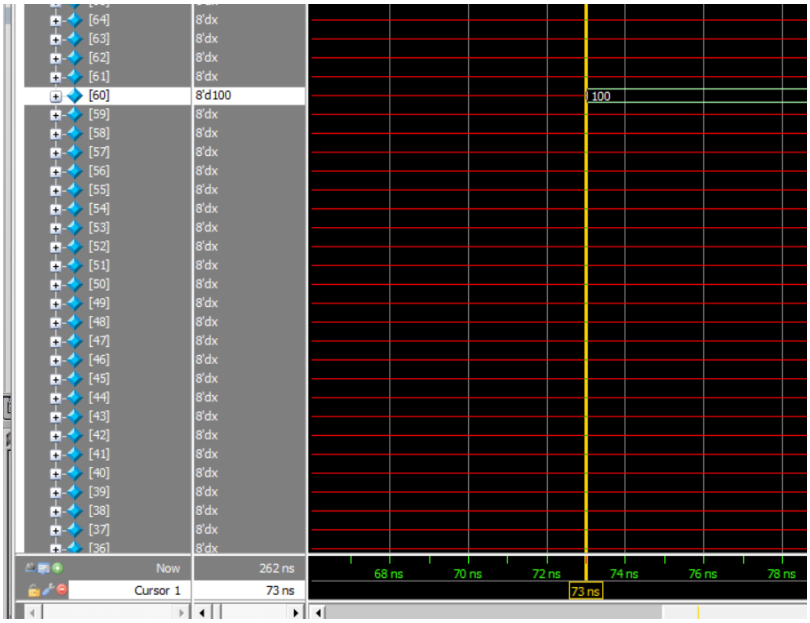


4th now write data begin



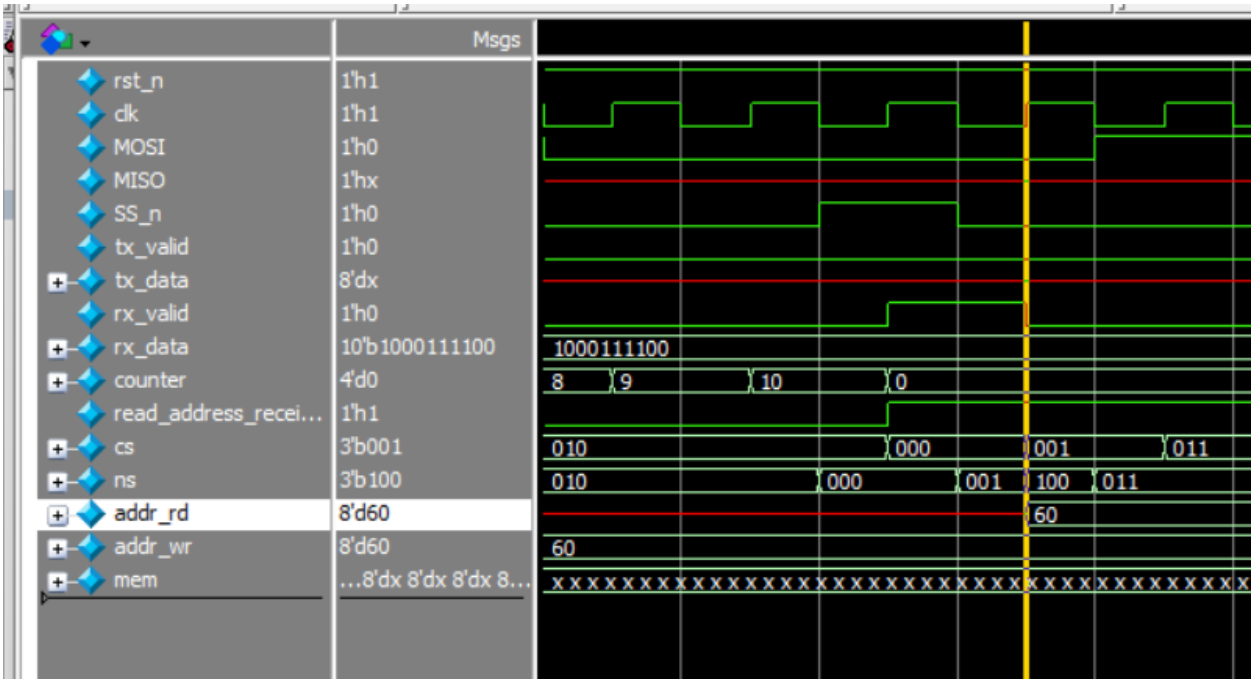
Here the bit control become zero and the next clk the rx[9]=0 so it's not changed and @53 ns the rx[8]=1 so it's changed to rx_data=01…… and so on the data in which is 100 decimal.

Here the rx_valid=1 and the next clk edge the mem changed @addr=60 to be 100 see next fig.

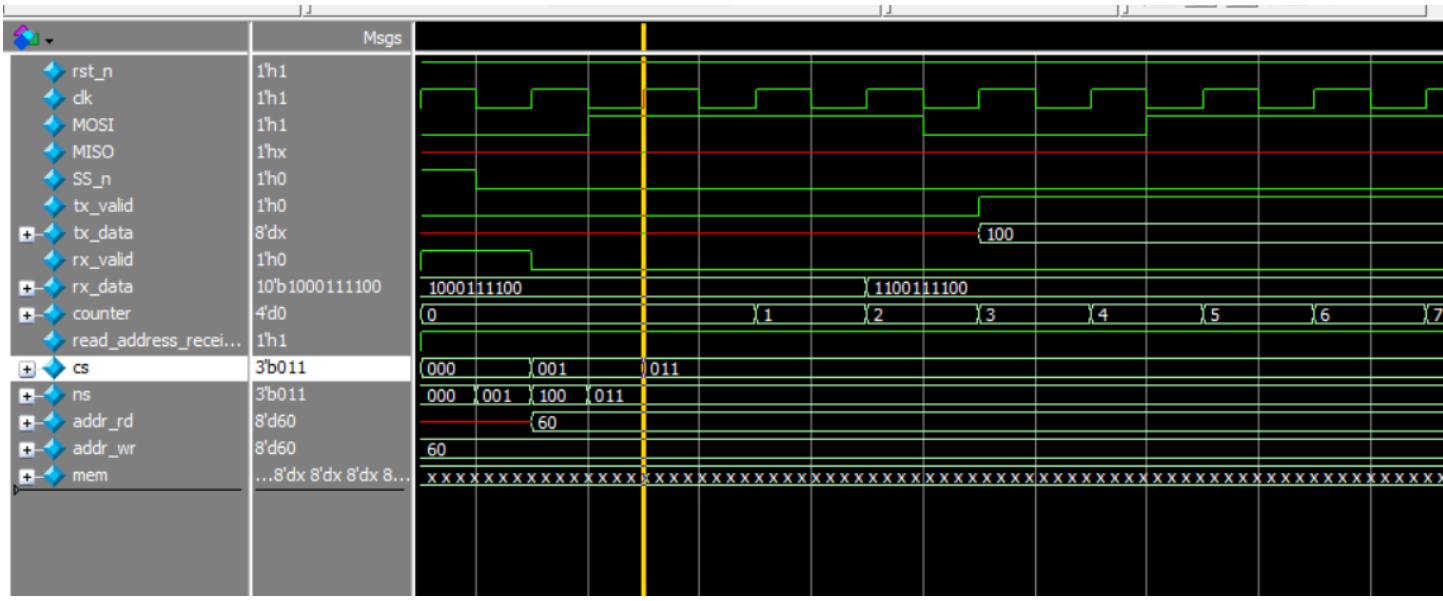


5th the read address test.

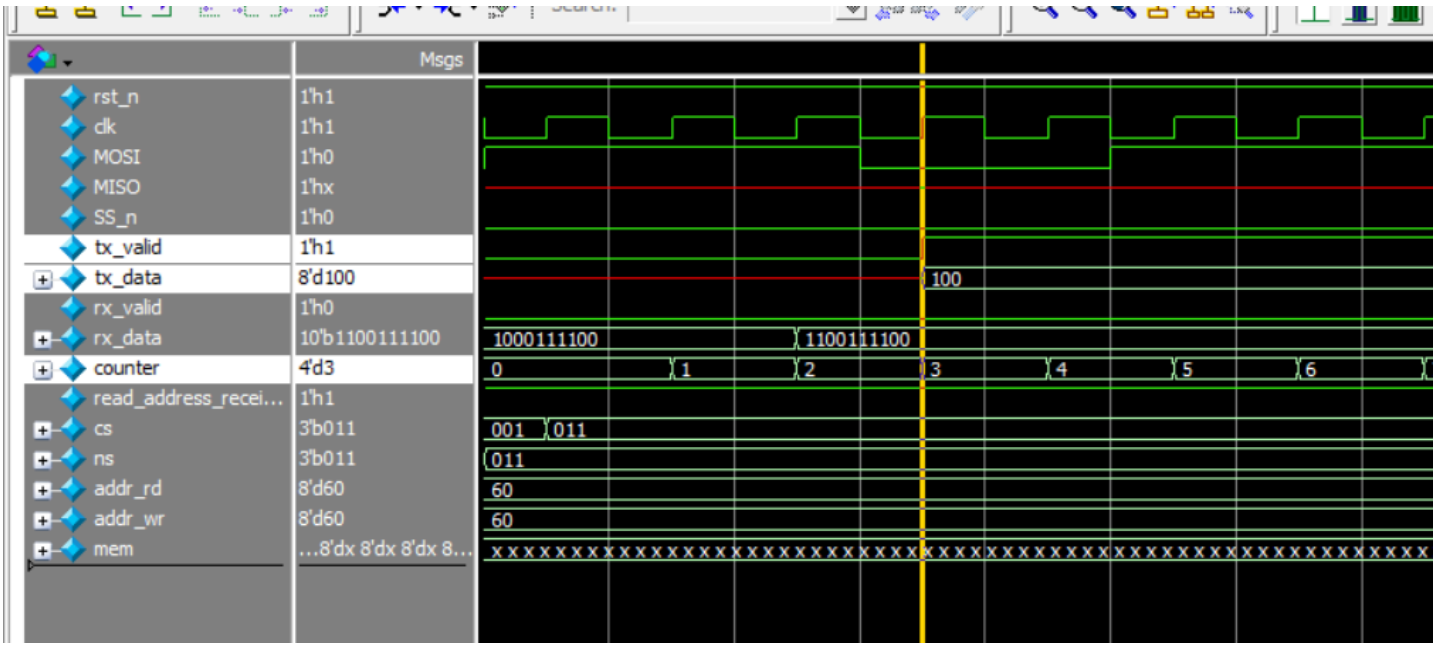
After we pass the address @rx_data the addr_rd changed to be 60



In next figure the cs changed to be 011 which is READ_DATA state

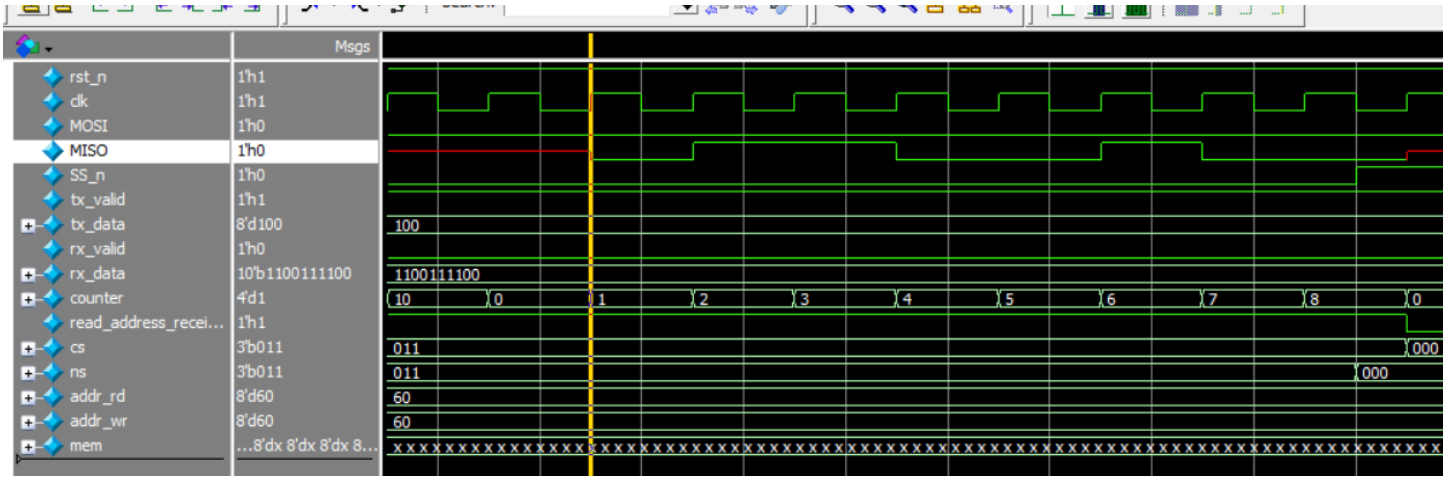


Now after 2 clk cycle the 2 bit is 11 which is read data so ram will read address 60 and send it to tx_data and the slave after that convert it into serial output MISO



Now the MISO started to change one by one

0 1 1 0 0 1 0 0 >> which is 100 in decimal that is the data in address 60 we wrote before .

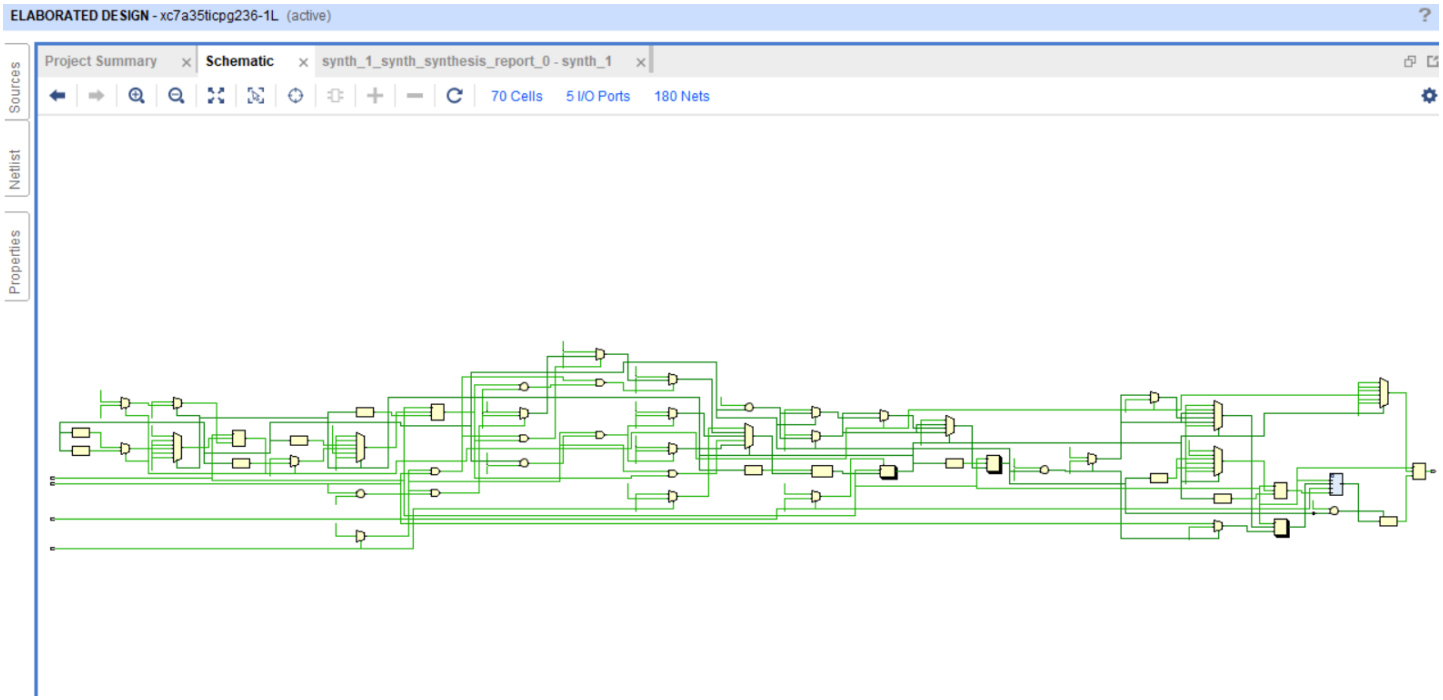


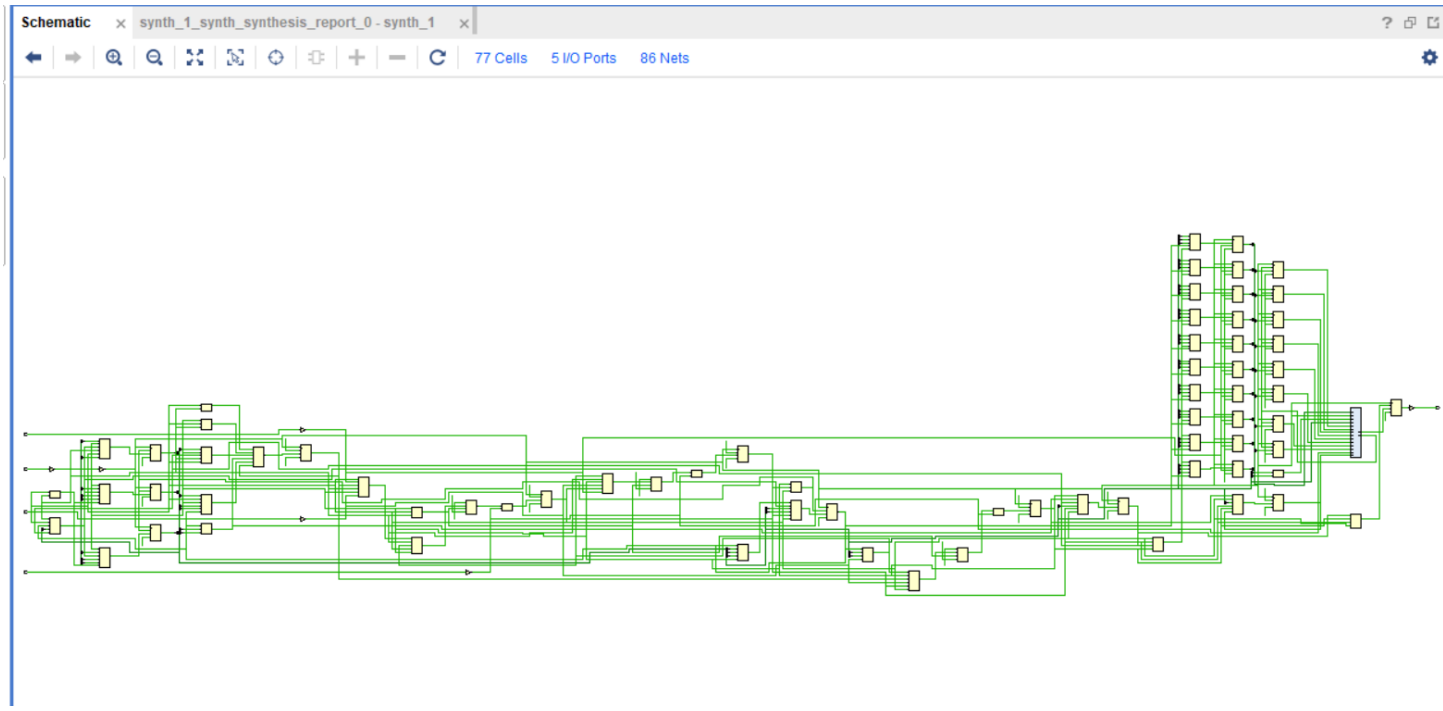
The remaining part of simulation is test with different numbers only but the same behavior .

2) Synthesis snippets for each encoding

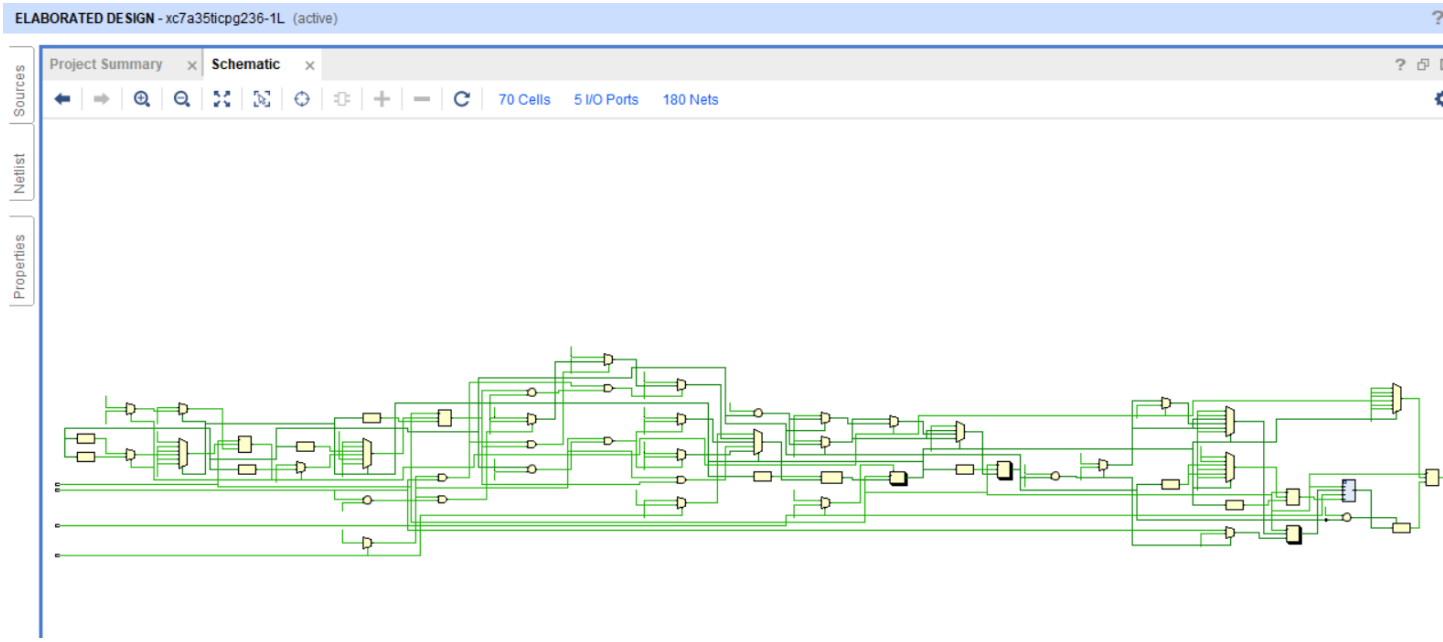
• Schematic after the elaboration & synthesis

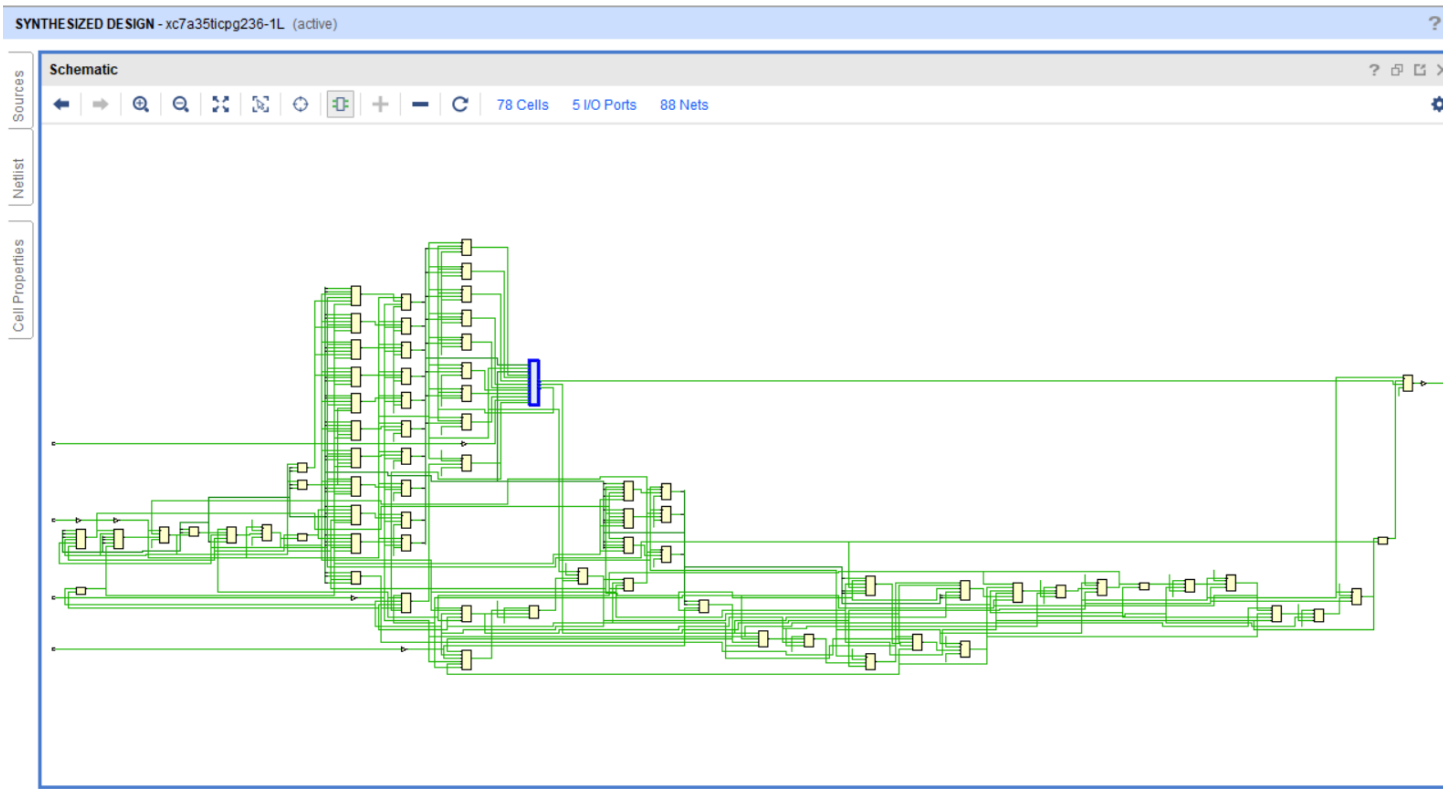
Gray encoding



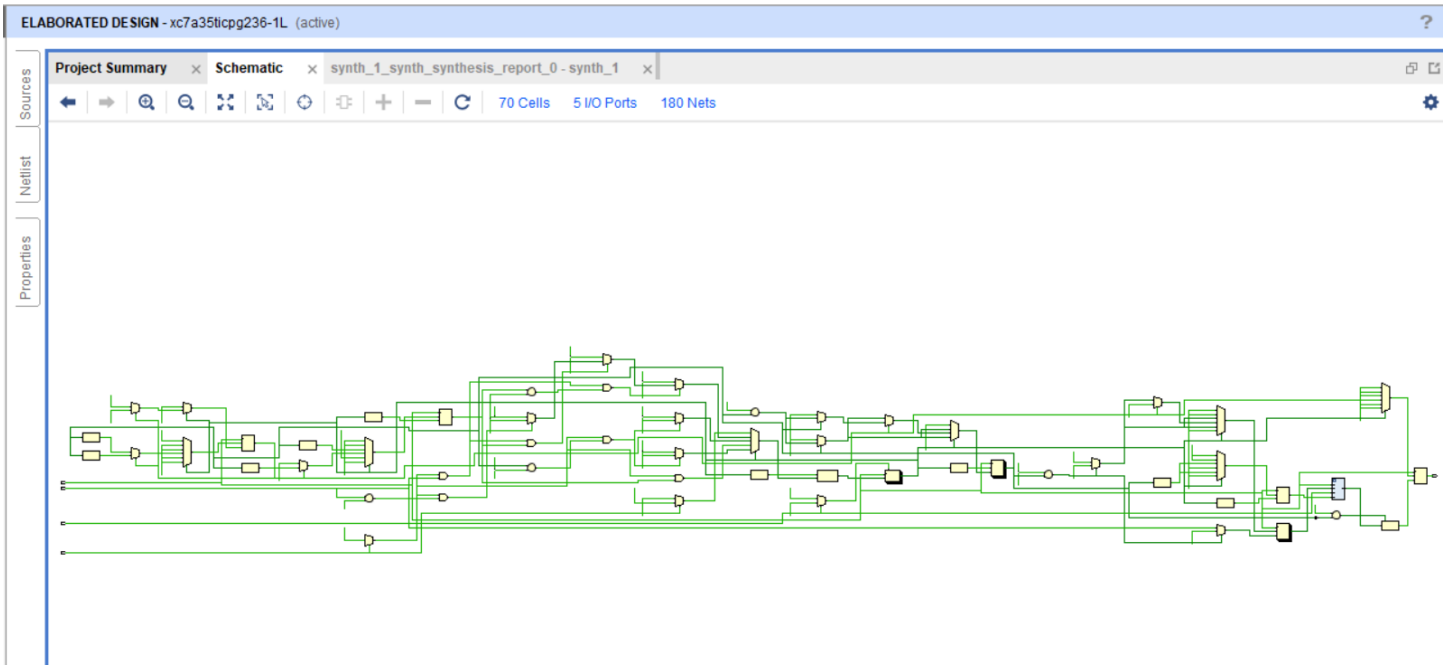


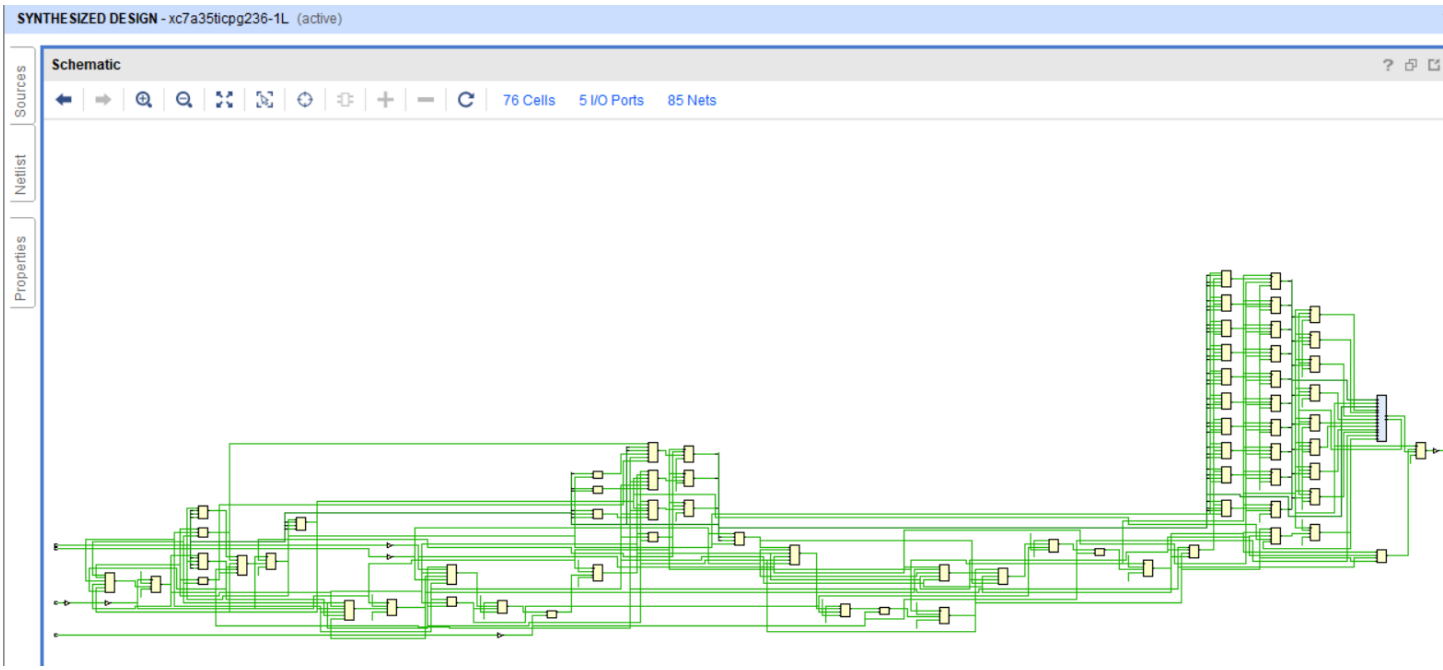
One_hot encoding





Sequential encoding





- **Synthesis report showing the encoding used**

Gray encoding

```
(* fsm_encoding = "gray" *)
```

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
READ_ADD	011	010
READ_DATA	010	011
WRITE	111	100

One_hot encoding

```
:e (* fsm_encoding = "one_hot" *) [
ile 'RAM_SPI' [E:/Digital course/pr
```

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
READ_ADD	00100	010
READ_DATA	01000	011
WRITE	10000	100

Sequential encoding

```
(* fsm_encoding = "sequential" *)
e 'RAM_SPI' [E:/Digital course/pro
```

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
READ_ADD	010	010
READ_DATA	011	011
WRITE	100	100

- **Timing report snippet**

Gray encoding

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.714 ns	Worst Hold Slack (WHS):	0.164 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	82	Total Number of Endpoints:	82	Total Number of Endpoints:	40

All user specified timing constraints are met.

One_hot encoding

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.714 ns	Worst Hold Slack (WHS):	0.164 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	82	Total Number of Endpoints:	82	Total Number of Endpoints:	42

All user specified timing constraints are met.

Sequential encoding

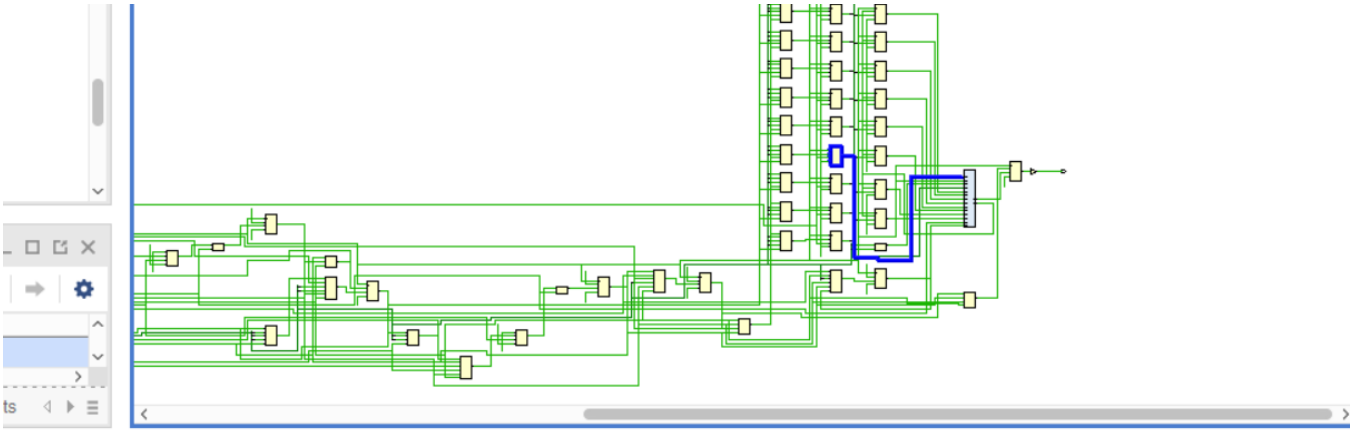
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.714 ns	Worst Hold Slack (WHS):	0.164 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	82	Total Number of Endpoints:	82	Total Number of Endpoints:	40

All user specified timing constraints are met.

• **Snippet of the critical path highlighted in the schematic**

Gray encoding

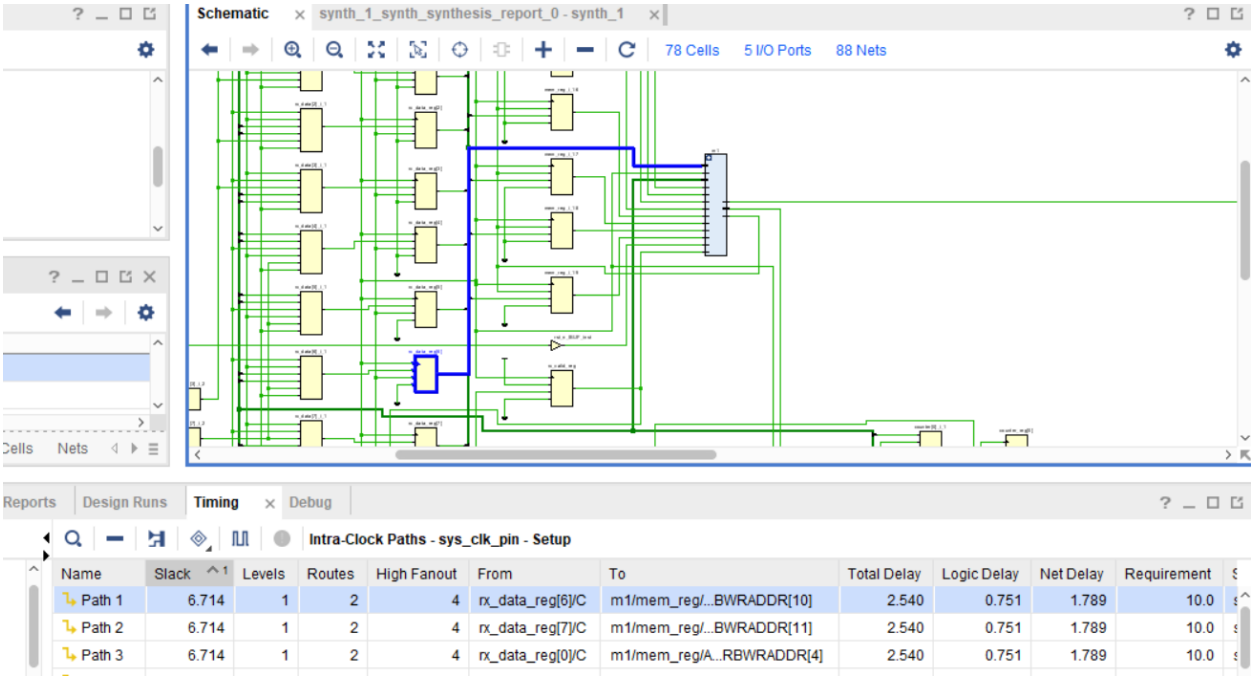


Design Runs | Timing | Debug

Intra-Clock Paths - sys_clk_pin - Setup

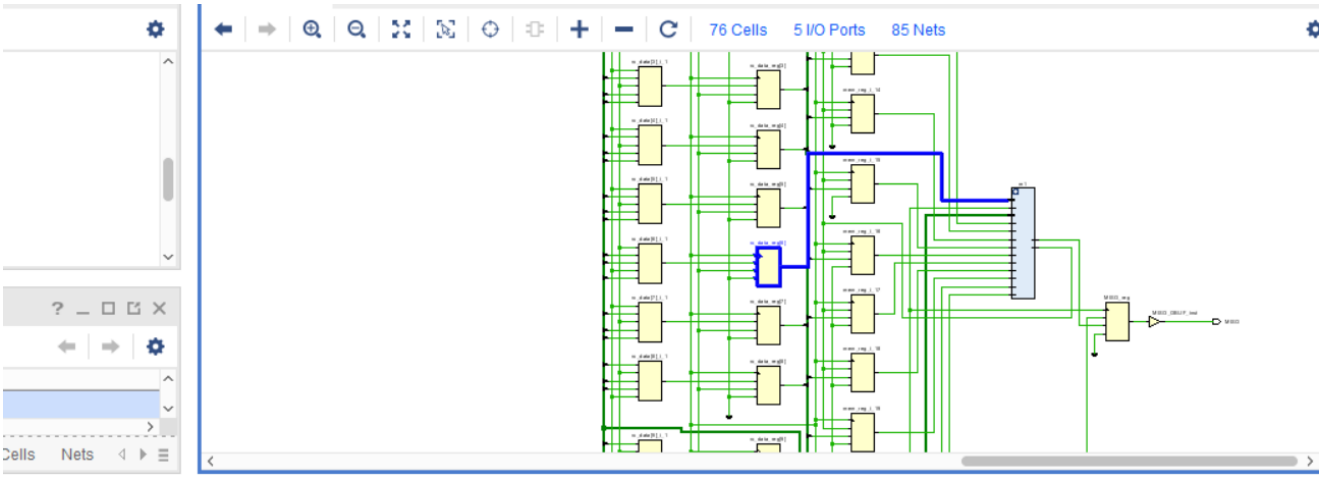
ame	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	6.714	1	2	4	rx_data_reg[6]/C	m1/mem_reg/...BWRADDR[10]	2.540	0.751	1.789	10.0
Path 2	6.714	1	2	4	rx_data_reg[7]/C	m1/mem_reg/...BWRADDR[11]	2.540	0.751	1.789	10.0
Path 3	6.714	1	2	4	rx_data_reg[0]/C	m1/mem_reg/A...RBWRADDR[4]	2.540	0.751	1.789	10.0
Path 4	6.714	1	2	4	rx_data_reg[1]/C	m1/mem_reg/A...RBWRADDR[5]	2.540	0.751	1.789	10.0
Path 5	6.714	1	2	4	rx_data_reg[2]/C	m1/mem_reg/A...RBWRADDR[6]	2.540	0.751	1.789	10.0
Path 6	6.714	1	2	4	rx_data_reg[3]/C	m1/mem_reg/A...RBWRADDR[7]	2.540	0.751	1.789	10.0

One_hot encoding



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	6.714	1	2	4	rx_data_reg[6]/C	m1/mem_reg/...BWRADDR[10]	2.540	0.751	1.789	10.0
Path 2	6.714	1	2	4	rx_data_reg[7]/C	m1/mem_reg/...BWRADDR[11]	2.540	0.751	1.789	10.0
Path 3	6.714	1	2	4	rx_data_reg[0]/C	m1/mem_reg/A...RBWRADDR[4]	2.540	0.751	1.789	10.0

Sequential encoding



Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	6.714	1	2	4	rx_data_reg[6]/C	m1/mem_reg/...BWRADDR[10]	2.540	0.751	1.789	10.0
Path 2	6.714	1	2	4	rx_data_reg[7]/C	m1/mem_reg/...BWRADDR[11]	2.540	0.751	1.789	10.0
Path 3	6.714	1	2	4	rx_data_reg[0]/C	m1/mem_reg/A...RBWRADDR[4]	2.540	0.751	1.789	10.0

3) Implementation snippets for each encoding

- **Utilization report**

Gray encoding

Name	Slice LUTs (20800)	Slice Registers (41600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI	53	40	0.5	5	1
m1 (RAM_SPI)	17	8	0.5	0	0

One_hot encoding

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI	47	44	1	20	47	8	0.5	5	1
m1 (RAM_SPI)	16	8	1	7	16	0	0.5	0	0

Sequential encoding

Hierarchy

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
SPI	48	40	1	21	48	13	0.5	5	1
m1 (RAM_SPI)	15	8	1	8	15	0	0.5	0	0

- **Timing report snippet**

Gray encoding

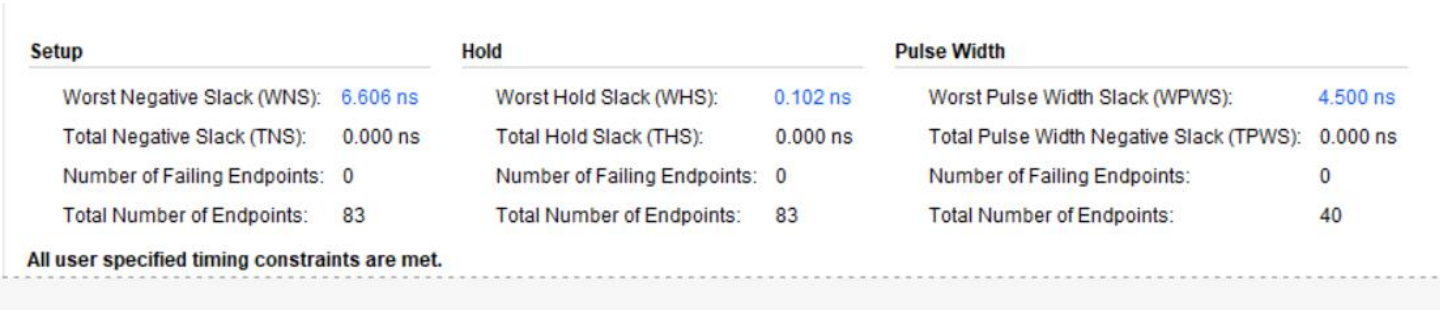
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.494 ns	Worst Hold Slack (WHS):	0.146 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	83	Total Number of Endpoints:	83	Total Number of Endpoints:	40

All user specified timing constraints are met.

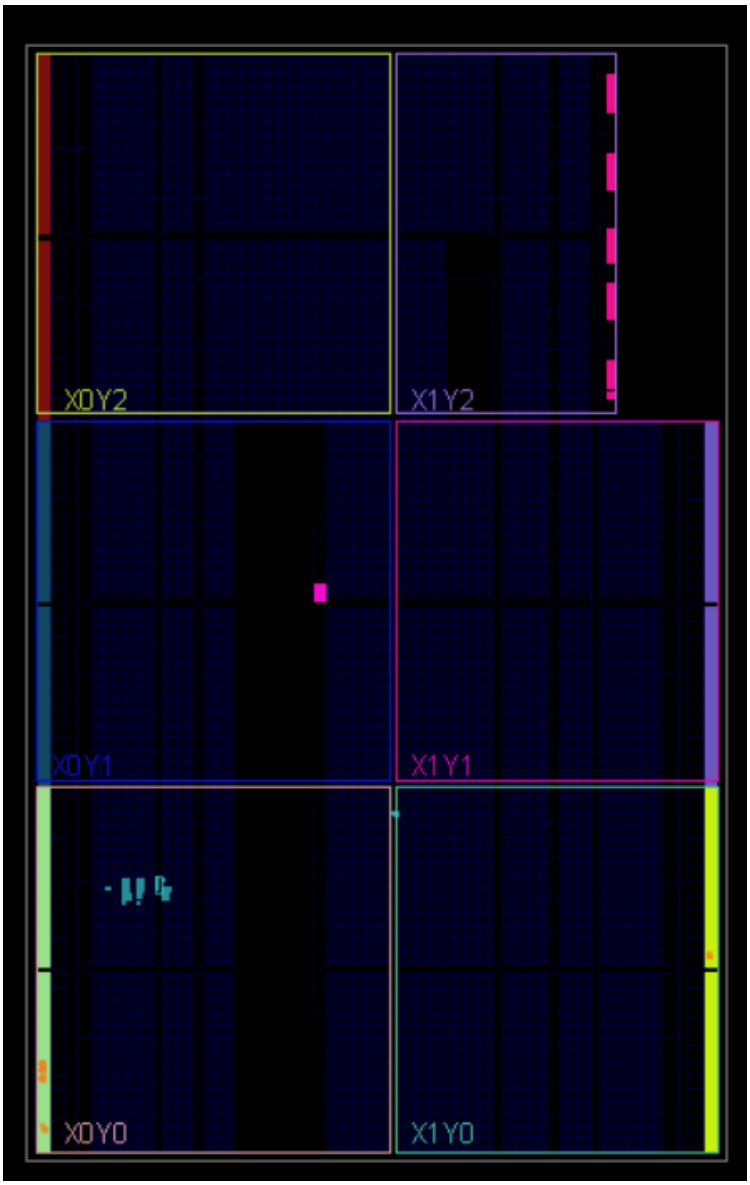
One_hot encoding

Sequential encoding

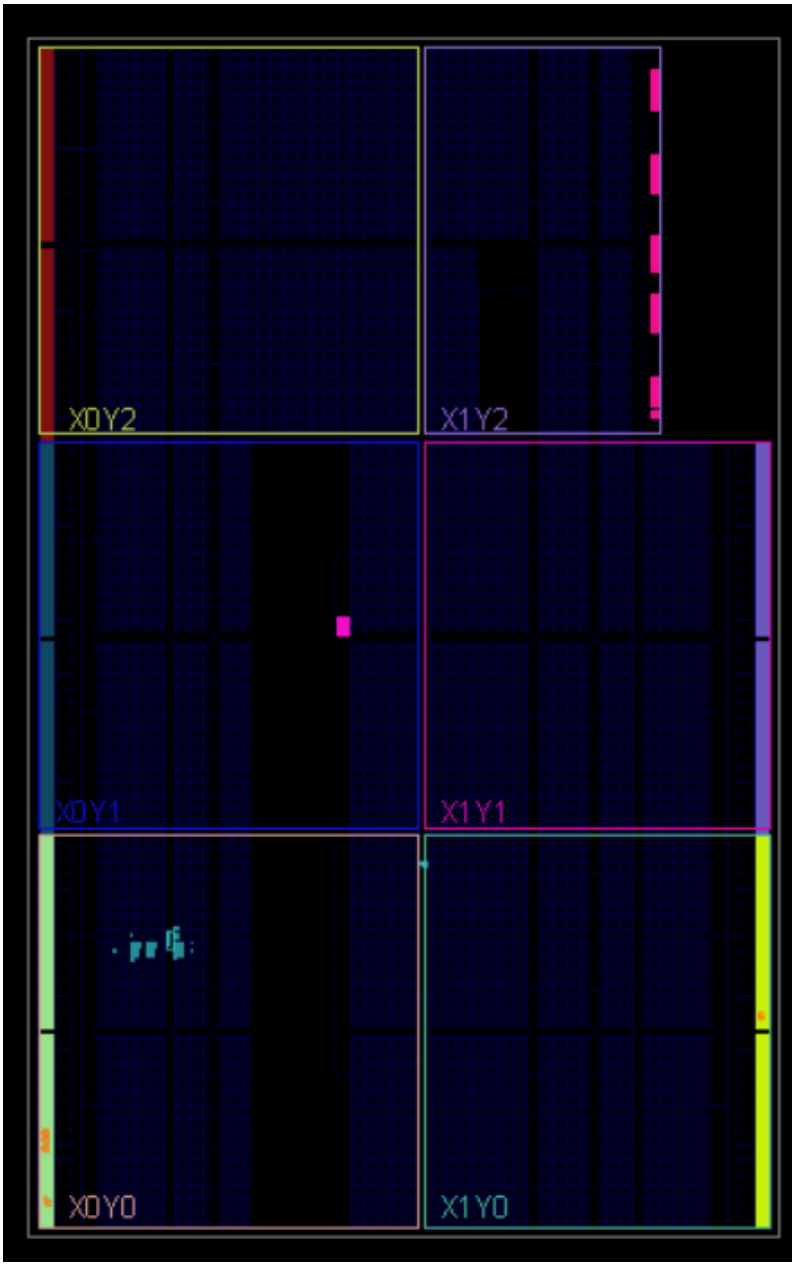


- **FPGA device snippet**

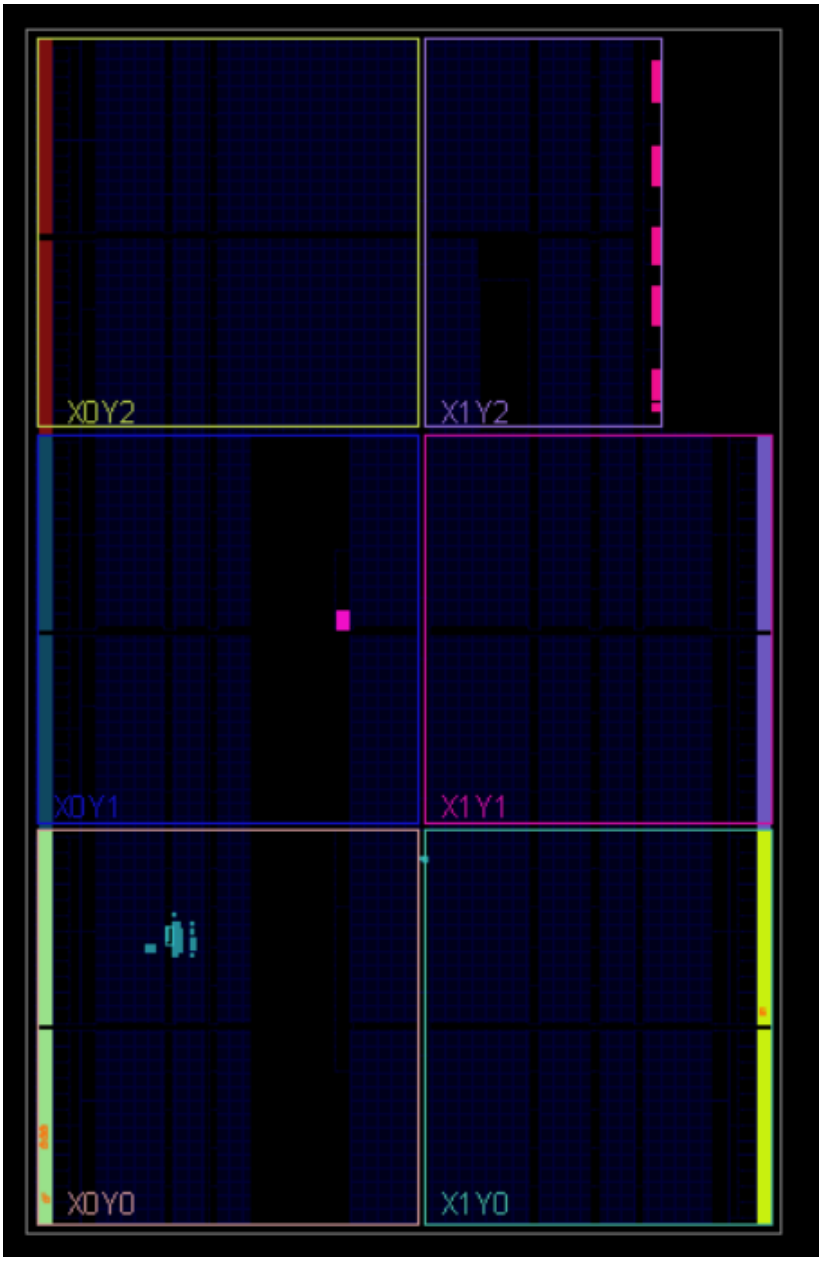
Gray encoding



One_hot encoding



Sequential encoding



4) Snippet of the “Messages” tab showing no critical warnings or errors after running elaboration,

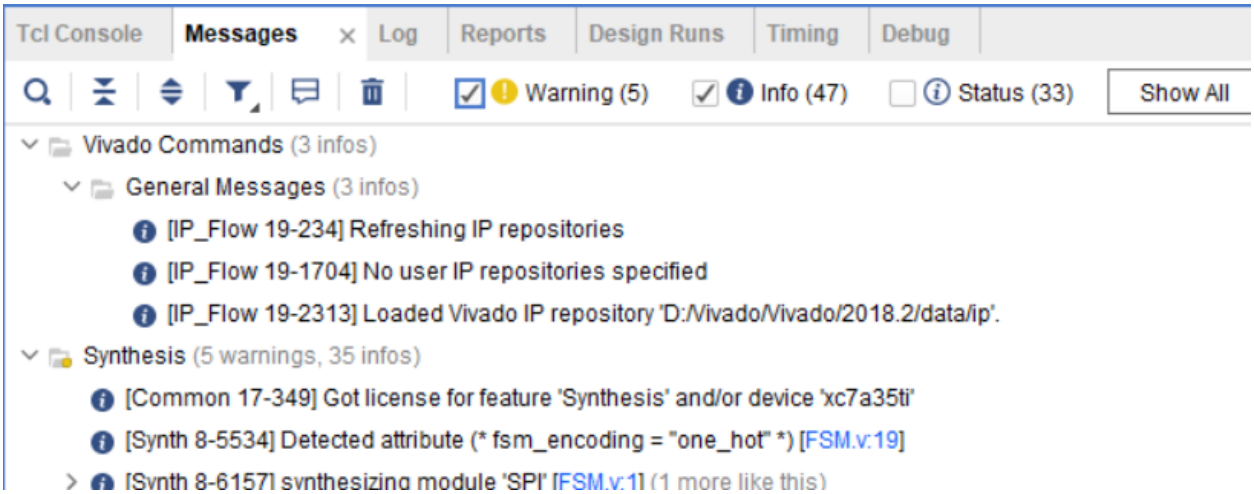
synthesis, implementation and a successful bitstream generation.

Elaboration

From sequential encoding

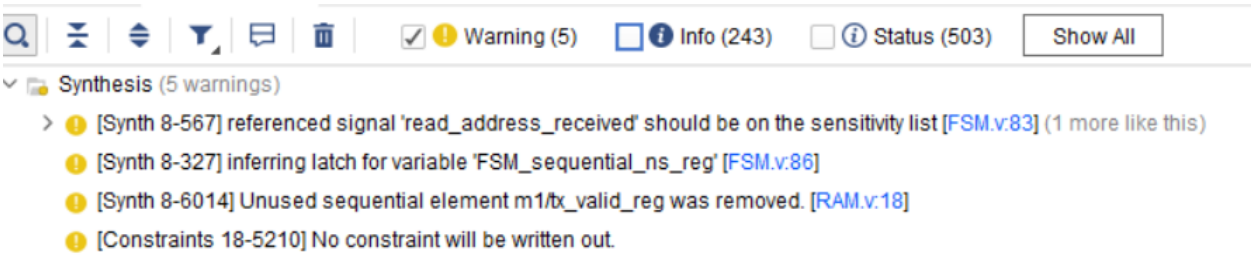
Synthesis

From one_hot encoding



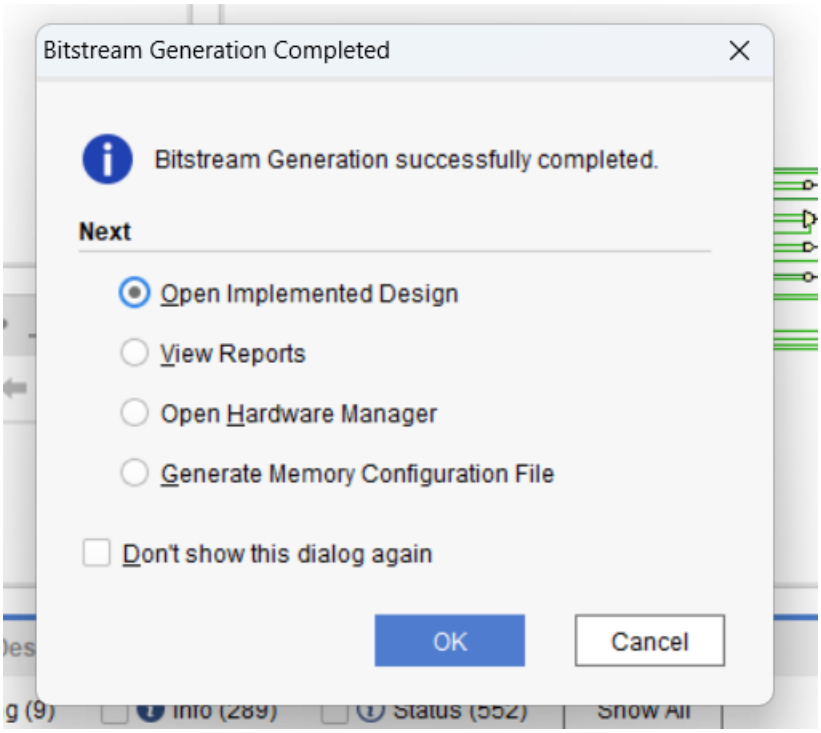
Implementation

From sequential encoding



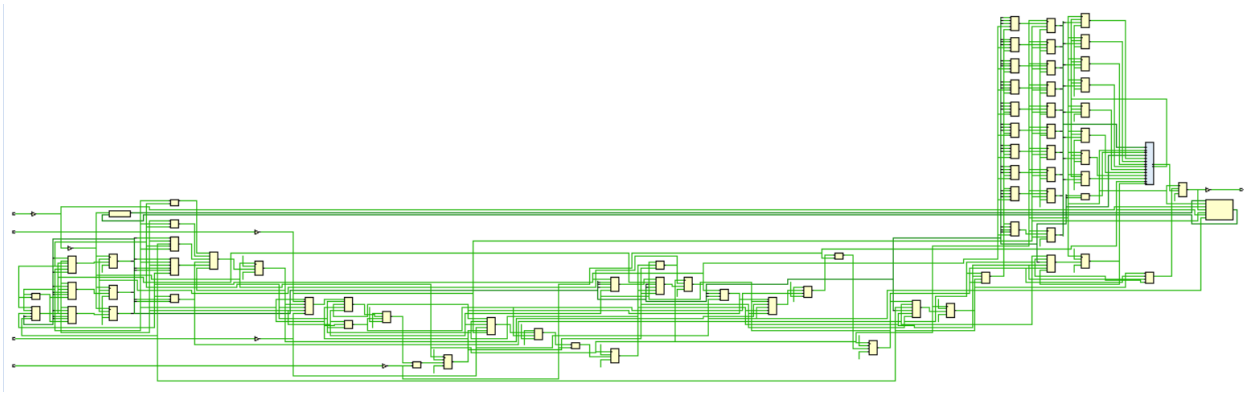
bitstream generation

from sequential encoding

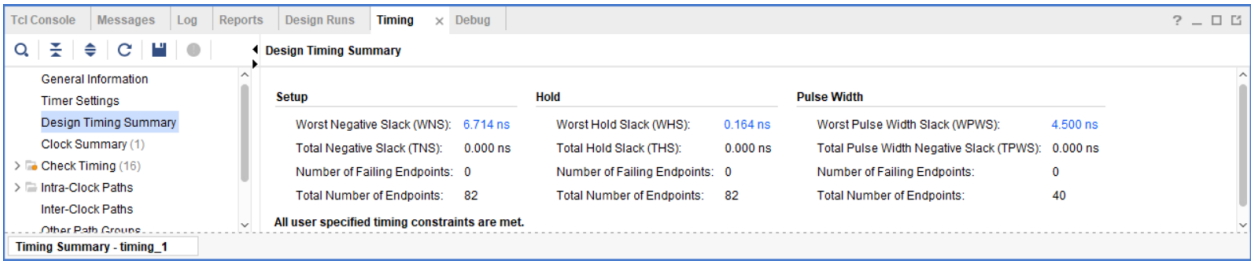


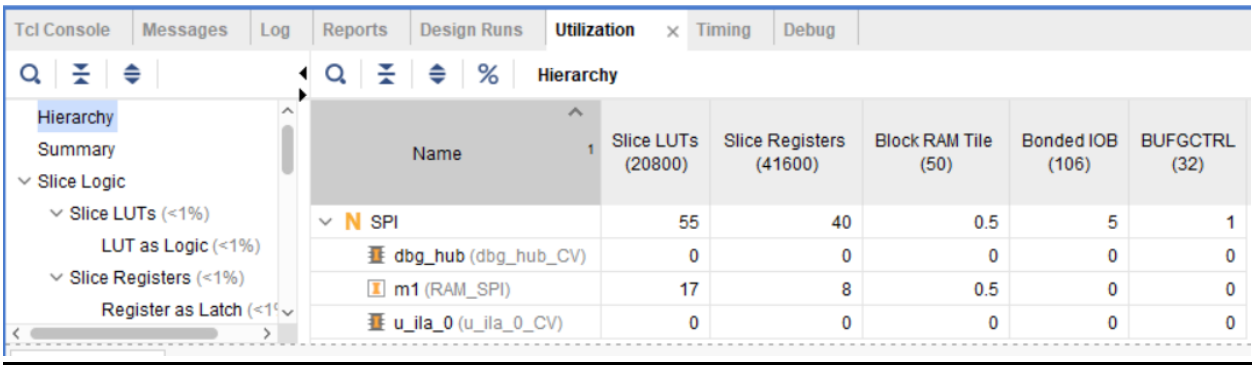
After debug choosing gray encoding:

Synthesis

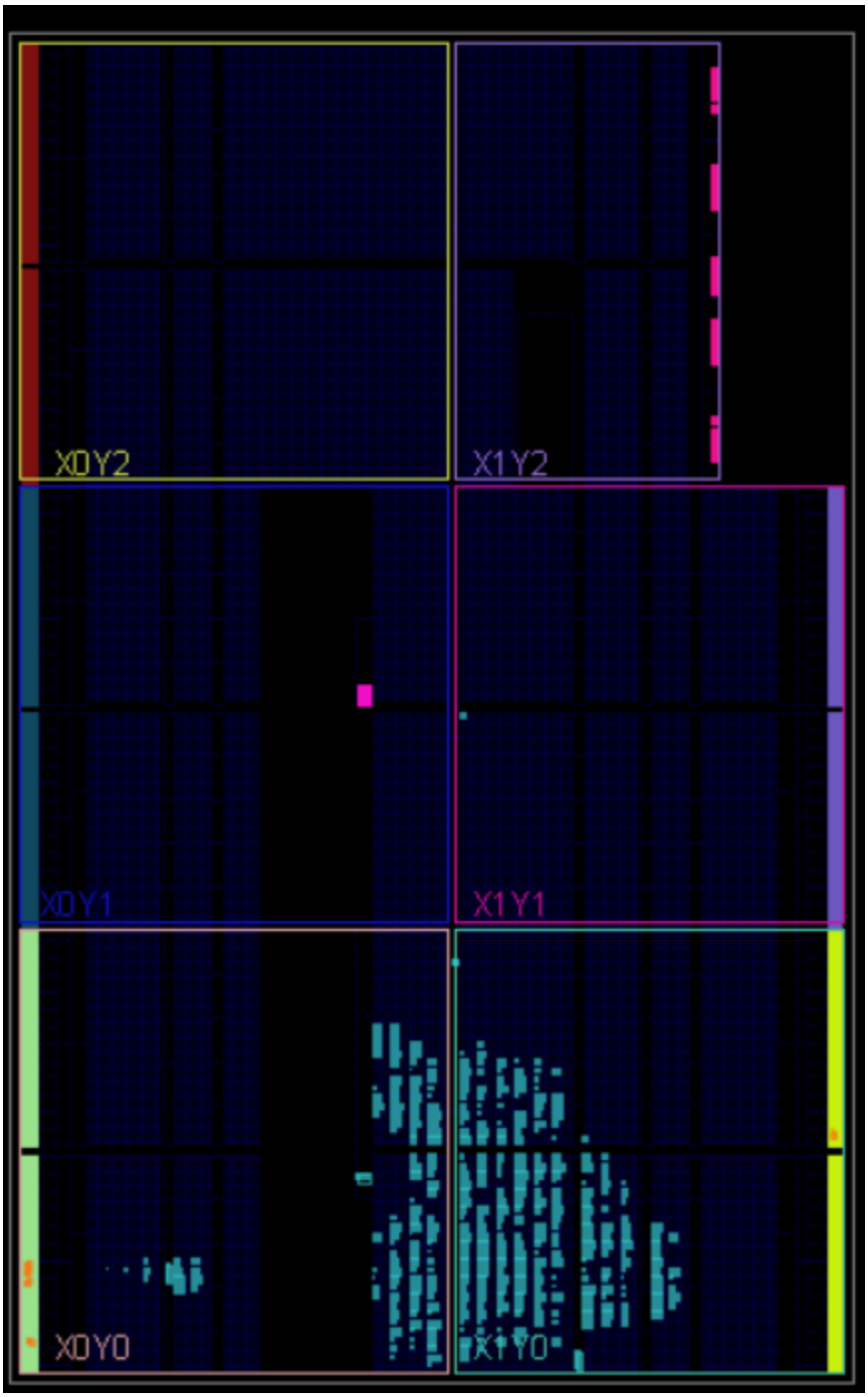


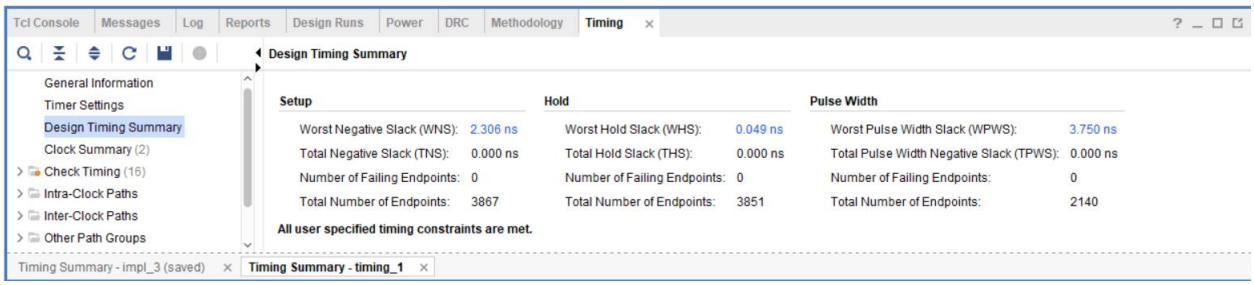
```
100 | ---------------------------------------------------------------------------------------------------
101 |                    State |                     New Encoding |                Previous Encoding
102 | ---------------------------------------------------------------------------------------------------
103 |                     IDLE |                              000 |                               000
104 |                  CHK_CMD |                              001 |                               001
105 |                 READ_ADD |                              011 |                               010
106 |                READ_DATA |                              010 |                               011
107 |                    WRITE |                              111 |                               100
108 | ---------------------------------------------------------------------------------------------------
109 | INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'
```





Implementation


X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0


Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (16)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
Setup
Worst Negative Slack (WNS): 2.306 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 3867
Hold
Worst Hold Slack (WHS): 0.049 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 3851
Pulse Width
Worst Pulse Width Slack (WPWS): 3.750 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 2140
All user specified timing constraints are met.
Timing Summary - impl_3 (saved)
Timing Summary - timing_1

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
N SPI	1293	1956	10	649	1185	108	740	1	5	2	1
> dbg_hub (dbg_hub)	475	727	0	237	451	24	302	0	0	1	1
m1 (RAM_SPI)	16	8	0	7	16	0	0	0.5	0	0	0
> u_ila_0 (u_ila_0)	764	1189	10	392	680	84	425	0.5	0	0	0