



Digital Implementation of digital transmitter system

Chapter 1

ASIC Flow

1.1 Synthesis

Synthesis is a step in the flow in which we convert the RTL along with physical libraries to netlist. Design compiler tool is used.

Basic synthesis flow:

- 1 Define libraries.
- 2 Reading design.
- 3 Reading constraints.
- 4 Check design.
- 5 Compile / Technology mapping & optimization.
- 6 Generate gate level netlist.
- 7 Generate reports

Define libraries:

is used as an input to synthesis tool with timing, area, power information, propagation delay and transition time of the output. specify multiple standard cell libraries to account for different voltage corners, threshold voltages (VTs), and process corners. For accurate timing analysis, I used the worst-case library for setup analysis (SS0P72VM40) and the worst-case library for hold analysis (FF0P88V125C) as shown in synthesis setup script. Also I'm using the clock gating library as shown in picture.

```
'#####
#set ROOT_DIR          "/home/svgasic25abkhaled/GP"
#set VERILOG_PATH      "${ROOT_DIR}/RTL"
#set CONSTRAIN_PATH    "${ROOT_DIR}/cons"

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH      "/home/tools/PDK/SAED14_EDK"
#####

# Library Setup Variables

set std_cell_lib      "${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/base/saed14slvt_base_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/base/saed14slvt_base_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/base/saed14slvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/cg/saed14lvt_cg_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/cg/saed14lvt_cg_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/cg/saed14lvt_cg_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/cg/saed14rvt_cg_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/cg/saed14rvt_cg_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/cg/saed14rvt_cg_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/cg/saed14hvt_cg_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/cg/saed14hvt_cg_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/cg/saed14hvt_cg_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/cg/saed14slvt_cg_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/cg/saed14slvt_cg_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/cg/saed14slvt_cg_tt0p8v25c.db "
```

Reading design files:

Analyze/elaborate analyze: reads HDL files. It informs the designer if there is any syntax error or non-synthesizable block.

elaborate: takes (.syn) if it passed the analyze command and translates the HDL to GTECH (technology independent cells). Also, it replaces operators and performs link command automatically. I'm write script for analyze and sourced it in my synthesis script.

```
analyze -library WORK -format sverilog " \
$VERILOG_PATH/dig_tx_clock_gating.sv \
$VERILOG_PATH/dig_tx_reg_file.sv\
$VERILOG_PATH/dig_tx_serializer.sv\
$VERILOG_PATH/dig_tx_rst_sync.sv\
$VERILOG_PATH/dig_tx_pulse_delayed.sv \
$VERILOG_PATH/dig_tx_pow_man_unit.sv \
$VERILOG_PATH/dig_tx_crc.sv \
$VERILOG_PATH/dig_tx_fifo_synchronizer.sv\
$VERILOG_PATH/dig_tx_fifo_wr_ptr_handler.sv \
$VERILOG_PATH/dig_tx_fifo_re_ptr_handler.sv \
$VERILOG_PATH/dig_tx_fifo_mem.sv \
$VERILOG_PATH/dig_tx_asyn_fifo.sv \
$VERILOG_PATH/dig_tx_control_unit.sv \
$VERILOG_PATH/spi_slave.sv\
$VERILOG_PATH/dig_tx_system.sv "
```

Reading constraints:

Original constraints

SYS_CLK	1 MHz
SPI_CLK	1 MHz
UNCERTAINTY SETUP	300ps
UNCERTAINTY HOLD	150ps
CLOCK TRANSITION	0.0ns
INPUT DELAY	400 ps
OUTPUT DELAY	400ps
Driving Cell	SAEDHVT14_BUF_1 from (saed14hvt_base_ss0p72vm40c)
Load	0.05 pf

Added constraints

```
#####
#Operating Condition #####
set_operating_conditions -min_library "saed14slvt_base_ff0p88v125c" -min "ff0p88v125c" -max_library "saed14hvt_base_ss0p72vm40c" -max "ss0p72vm40c"
#####
#wireload Model #####
set_wire_load_model -name 16000 -library saed14hvt_base_ss0p72vm40c
#####
#area #####
set_max_area 0
```

defines the operating conditions by assigning the worst-case (-max) and best-case (-min) process corners using two libraries: saed14hvt_base_ss0p72vm40c for slow-slow at 0.72V, -40°C, and saed14slvt_base_ff0p88v125c for fast-fast at 0.88V, 125°C. also specifies a wireload model named 16000 from the HVT library to estimate interconnect parasitics during early stages like synthesis. constrains the total cell area by setting a hard limit of zero with set_max_area 0, effectively disabling area growth .

Compile:

There are two different approaches to the ASIC physical implementation:

- **Hierarchical**
- **Flat**

1. Hierarchical flow

The hierarchical flow tries to do the opposite of the flat by keeping the hierarchy of the design intact. This allows the tools to optimize the logic within the modules but not on the boundaries. There are two topologies in hierarchical flow:

- **Top-down approach:** here we analyze all RTL design files including top module at the same time, the tool handles interdependencies between files automatically. This method is recommended most of the time but is hard in large designs; it needs large memory.
- **Bottom-up approach:** here each file is constrained and analyzed independently; at the end of the flow, they are assembled.

Hierarchical approach:

1.1 Top-down strategy:

First, reading synthesis setup script and define the top module

```
source /home/svgasic25abkhaled/GP/synthesis/common_setup.tcl
#####
##### Define Top Module #####
set DESIGN_NAME "dig_tx_system"
#####
##### Define Working Library Directory #####
sh rm -rf work
sh rm -rf outputs
sh rm -rf reports
sh rm -rf ./reports/compile
sh rm -rf ./reports/compile_incr_high

define_design_lib work -path ./work
sh mkdir ./outputs
sh mkdir ./reports
sh mkdir ./reports/compile
sh mkdir ./reports/compile_incr_high
```

Then specifying some options to Avoids using Verilog tri (tri-state) nets in the synthesized netlist and forces Design Compiler to map logic into standard cells only by Prevents DC from generating Verilog equations and also disables automatic phase inference for clocks.

```
#####
##### option #####
set verilogout_no_tri true
set verilogout_equation false
set compile_automatic_clock_phase_inference none
```

Then reading libraries and files and check design if there are no errors in this stage.

```
#####
##### Reading Libraries #####
#####

set target_library "$std_cell_lib"
set link_library "* $std_cell_lib"

#####
##### Reading files #####
#####

source /home/svgasic25abkhaled/GP/synthesis/analyze_script.tcl
elaborate $DESIGN_NAME -lib work

#####
##### Defining toplevel #####
#####

current_design $DESIGN_NAME

#####
##### fix multiple nets and buffer any constant net #####
#####

set_fix_multiple_port_nets -all -buffer_constants

#####
##### checking design consistency #####
#####

check_design > "./reports/check_design.rpt"
```

The I will prevent tool from using SLVT cells in first phase to force it to use HVT ,LVTand RVT.

```
#####
##### Prevent tool from using SLVT cells initially#####
#####

set_dont_use [get_lib_cells saed14slvt_base_ff0p88v125c/*]
set_dont_use [get_lib_cells saed14slvt_base_ss0p72vm40c/*]
set_dont_use [get_lib_cells saed14slvt_base_tt0p8v25c/*]
```

I used group_path strategy to prioritize timing optimization across different clock domains in the design. the sys_clock domain is assigned the highest priority with a weight of 40 and a wide critical range of 0.4 ns, ensuring that paths within 0.4 ns of the worst slack receive optimization effort. The sys_gated_clk domain is given moderate priority with a weight of 30 and a critical range of 0.3 ns, allowing it to optimize near-critical paths. The spi_gated_clk and spi_clock domains are assigned lower weights (2 and 1 respectively) and narrower or zero critical ranges, indicating that only the most critical or violating paths will be considered for optimization. This configuration effectively guides the synthesis tool to focus more resources on the sys_clock domain, which is the most timing-sensitive, while de-emphasizing less critical domains like SPI.

```
#####
##### Constraint #####
#####

source "$CONSTRAIN_PATH/cons_v2.tcl"

group_path -name SYS_CLK -weight 40 -critical_range 0.4 -to sys_clock
group_path -name SYS_GATED_CLK -weight 30 -critical_range 0.3 -to sys_gated_clk
group_path -name SPI_GATED_CLK -weight 2 -critical_range 0.1 -to spi_gated_clk
group_path -name SPI_CLK -weight 1 -critical_range 0.0 -to spi_clock
```

First phase by using The compile command to perform high-effort mapping (-map_effort high) to explore a broader range of logic synthesis optimizations. Clock gating is enabled using the -gate_clock option, allowing the tool to automatically insert clock gating cells to reduce unnecessary switching activity, which is important for power optimization. The area optimization effort is set to medium (-area_effort medium). Power optimization is explicitly disabled (-power_effort none), indicating that power consumption is not a primary concern in this synthesis run.

```
#####
##### Compile #####
compile -map_effort high -gate_clock -area_effort medium -power_effort none
```

Synthesis results of first run in Top-down strategy:

Total area	Total cell area:	Total power	Setup Violating Paths	Setup max (sys clk) Group path	Setup max (sys gated clk) Group path	Setup max (spi gated clk) Group path	Hold Violating Paths
2041.812555	875.612404	8.3778mw	2	+0.01ns	+0.00ns	-0.69ns	263

I'm run compile three phases again to get more optimization. and making power effort none to disable it effort and Concentrate on timing and area effort.

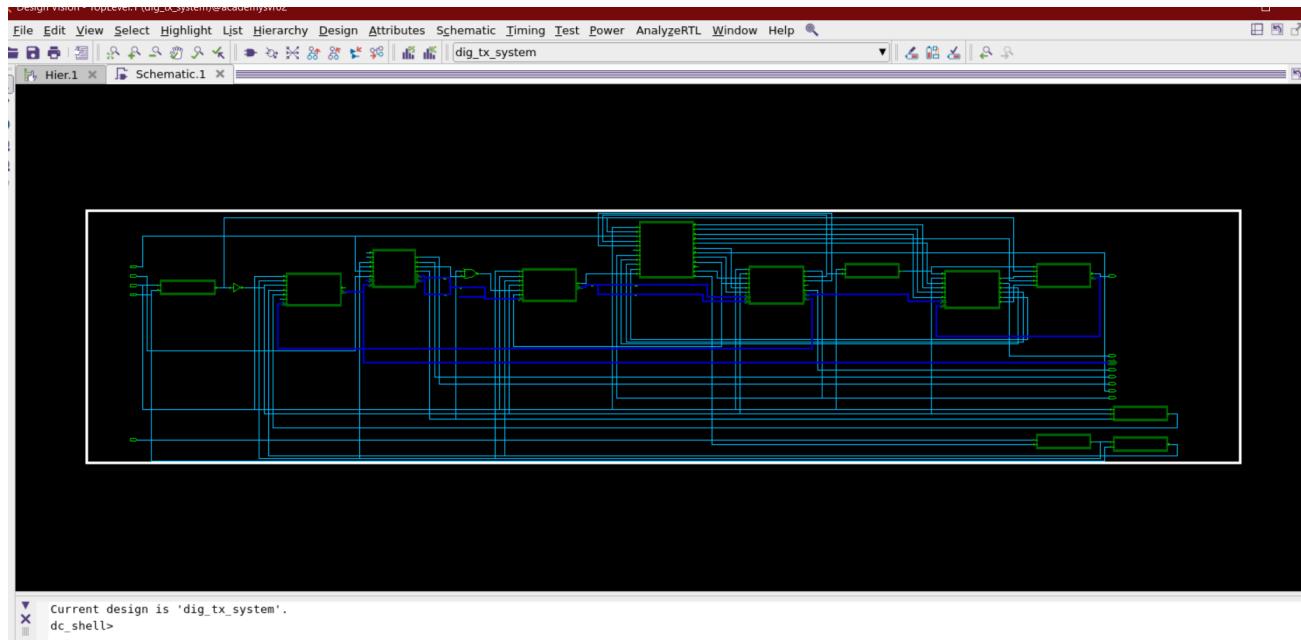
```
compile -exact_map -map_effort high -area_effort medium -power_effort none -incremental_mapping
compile -exact_map -map_effort high -area_effort medium -power_effort none -incremental_mapping
compile -exact_map -map_effort high -area_effort medium -power_effort none -incremental_mapping
```

Synthesis results of Top-down strategy:

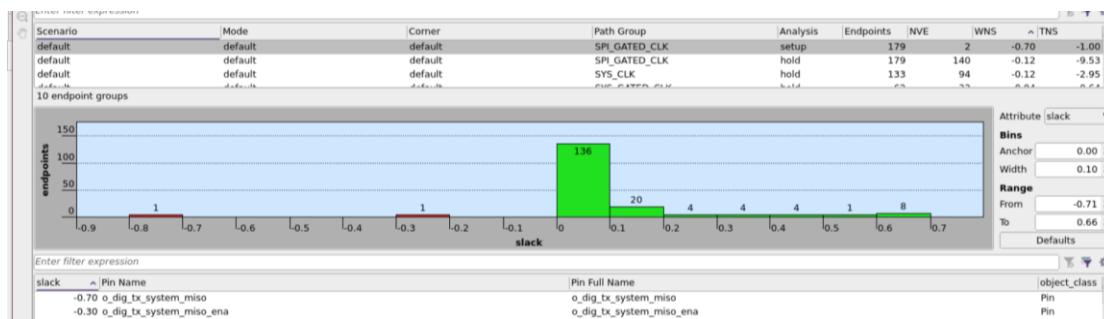
(green color mean enhancement & red color means it gets worse)

Total area	cell area:	Total power	Setup Violating Paths	Setup max (sys clk) Group path	Setup max (sys gated clk) Group path	Setup max (spi gated clk) Group path	Hold Violating Paths
2026.115424	853.767603	8.3589 mW	2	+0.00ns	+0.00ns	-0.70ns	264

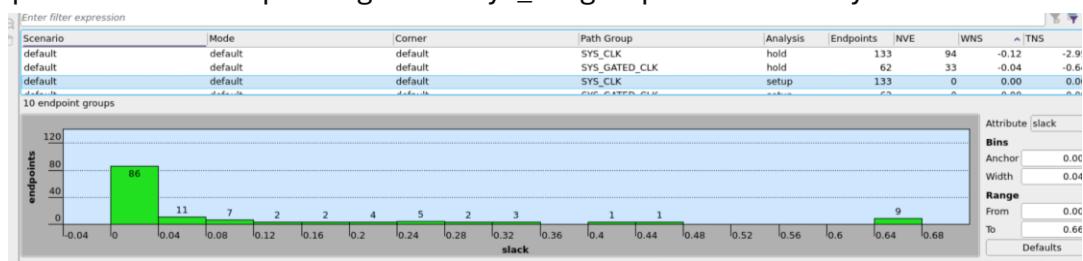
The gate level netlist schematic.



The next graph shows the setup timing on the spi_gated_clk group. As shown in figure , there are two violation paths at the output ports due to high output delay



The next graph shows the setup timing on the sys_clk group there is no any violation.



Synthesis reports

Power

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.8750	7.0423	1.2633e+06	7.9185	(94.73%)	i
register	6.5585e-03	1.4488e-02	5.7885e+07	7.8932e-02	(0.94%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	3.4453e-02	0.1708	1.5619e+08	0.3614	(4.32%)	
Total	0.9160 mW	7.2275 mW	2.1534e+08 pW	8.3589 mW		

Area

```
*****
Report : area
Design : dig_tx_system
Version: V-2023.12-SP5-1
Date   : Fri May 2 01:25:19 2025
*****
Library(s) Used:
    saed14lvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v125c.db)
    saed14hvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v125c.db)
    saed14rvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v125c.db)

Number of ports:          493
Number of nets:           2217
Number of cells:          1647
Number of combinational cells: 1244
Number of sequential cells: 378
Number of macros/black boxes: 0
Number of buf/inv:         366
Number of references:     21

Combinational area:      462.159598
Buf/Inv area:            118.681199
Noncombinational area:   391.608005
Macro/Black Box area:    0.000000
Net Interconnect area:   1172.347820

Total cell area:          853.767603
Total area:               2026.115424
```

QOR

Design Rules	
Total Number of Nets:	1758
Nets With Violations:	0
Max Trans Violations:	0
Max Cap Violations:	0
Hostname:	academysvr02
Compile CPU Statistics	
Resource Sharing:	0.15
Logic Optimization:	0.14
Mapping Optimization:	3.07
Overall Compile Time:	238.52
Overall Compile Wall Clock Time:	273.30
Design WNS:	0.70 TNS: 1.00 Number of Violating Paths: 2
Design (Hold) WNS:	0.12 TNS: 13.10 Number of Violating Paths: 264

1.2 bottom-up strategy:

A key modification in this strategy involves compiling each file separately and applying the uniquify command. This command plays a crucial role in hierarchical design by assigning unique names to instances that originally shared the same name across different parts of the design. This distinction is essential during optimization, as it ensures that modifications—such as resizing an instantiated cell—affect only the targeted instance. Without uniquify, changes to one instance would propagate to all identically named instances.

```
set my_blocks { "dig_tx_clock_gating" "dig_tx_reg_file" "dig_tx_serializer" "dig_tx_rst_sync" "dig_tx_pulse_delayed" "dig_tx_pow_man_unit" "dig_tx_crc" "dig_tx_fifo_synchronizer" "dig_tx_fifo_wr_ptr_handler" "dig_tx_fifo_re_ptr_handler" "dig_tx_fifo_mem" "dig_tx_asyn_fifo" "dig_tx_control_unit" "spi_slave" }

foreach block $my_blocks {
    analyze -library WORK -format sverilog "$block.sv"
    elaborate "$block" -lib work
    current_design $block
    link
    uniquify
}

compile -exact_map -gate_clock -map_effort high -area_effort medium -power_effort medium
}
```

In this step the first phase compile of the top design by using this arguments

- -exact_map :

It performs an exact mapping of the design's sequential elements. Under normal conditions, sequential units surrounded by logic elements may be used if their behaviour resembles the HDL. This argument specifies that an exact match must be used.

- -gate_clock :

It enables clock gating optimization by the automatic insertion and removal of the clock gates from the design.

- -map_effort :

It specifies the relative CPU computational time the tool spends in the mapping phase of the synthesis.

- -area_effort

It specifies the relative CPU computational time the tool spends in the area recovery phase of the synthesis.

- -power_effort

It specifies the relative CPU computational time the tool spends in the power recovery phase of the synthesis. Synthesis results of first run in bottom-up strategy:

Total area	cell area:	Total power	Setup Violating Paths	Setup max (sys clk) Group path	Setup max (sys gated clk) Group path	Setup max (spi gated clk) Group path	Hold Violating Paths
1489.277397	741.213606	3.1214 mW	2	+0ns	+0.0nss	-0.78ns	185

By Running more compile phases

```

compile -exact_map -gate_clock -map_effort high -area_effort medium -power_effort medium -incremental
compile -exact_map -gate_clock -map_effort high -area_effort medium -power_effort medium -incremental
compile -exact_map -gate_clock -map_effort high -area_effort medium -power_effort medium -incremental

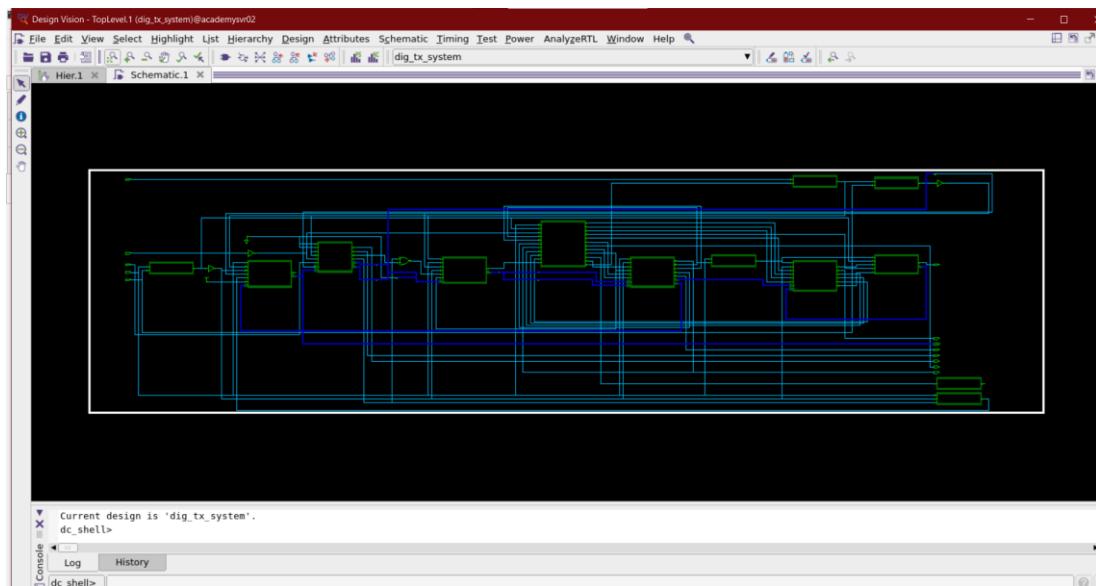
```

Synthesis results of fourth run in bottom up strategy by using compile:

Total area	cell area:	Total power	Setup Violating Paths	Setup max (sys clk) Group path	Setup max (sys gated clk) Group path	Setup max (spi gated clk) Group path	Hold Violating Paths
1484.216574	734.864406	3.1151 mW	2	+0.0ns	+0.0ns	-0.8ns	178

The green color shows that the value become enhancement and that due to making compile four times. More compile phases mean more optimization and good results but take more time.

The gate level netlist schematic:



Synthesis reports

Power

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
<hr/>						
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.4208	2.3012	1.6760e+06	2.7237	(87.43%)	i
register	5.4730e-03	1.8859e-02	7.4102e+07	9.8433e-02	(3.16%)	
sequential	0.0000	0.0000	0.0000	0.0000	(0.00%)	
combinational	3.6020e-02	0.1548	1.0216e+08	0.2930	(9.41%)	
<hr/>						
Total	0.4623 mW	2.4749 mW	1.7793e+08 pW	3.1151 mW		

Clock gating clock

Report : clock_gating		
Design : dig_tx_system		
Version: V-2023.12-SP5-1		
Date : Sat Apr 19 05:22:55 2025		

Clock Gating Summary		
Number of Clock gating elements	27	
Number of Gated registers	272 (77.49%)	
Number of Ungated registers	79 (22.51%)	
Total number of registers	351	
Clock Gating Report by Origin		
	Actual (%)	Count
Number of tool-inserted clock gating elements	27 (100.00%)	
Number of pre-existing clock gating elements	0 (0.00%)	
Number of gated registers	272 (77.49%)	
Number of tool-inserted gated registers	272 (77.49%)	
Number of pre-existing gated registers	0 (0.00%)	
Number of ungated registers	79 (22.51%)	
Number of registers	351	

QOR

Area	
Combinational Area:	316.927201
Noncombinational Area:	417.937206
Buf/Inv Area:	65.090400
Total Buffer Area:	34.54
Total Inverter Area:	36.81
Macro/Black Box Area:	0.000000
Net Area:	749.352167

Cell Area:	734.864406
Design Area:	1484.216574
Design Rules	

Total Number of Nets:	1195
Nets With Violations:	0
Max Trans Violations:	0
Max Cap Violations:	0

Hostname:	academysvr02
Compile CPU Statistics	

Resource Sharing:	0.15
Logic Optimization:	0.10
Mapping Optimization:	2.05

Overall Compile Time:	231.48
Overall Compile Wall Clock Time:	234.16

2. Flat approach:

The flat design flow is based on dissolving the boundaries between the different modules of the design. This allows for more logic optimization that wasn't previously possible at the boundaries. This flow results in the best-optimized logic for area, power and speed. This approach, however, suffers from long runtime as the tool's optimization algorithms run longer as space or optimization expands. First I compile each block separately as shown in picture:

```
foreach block $my_blocks {  
  
    analyze -library WORK -format sverilog "$block.sv"  
    elaborate "$block" -lib work  
    current_design $block  
    link  
    uniquify  
    compile -exact_map  
    #compile -exact_map -map_effort high -area_effort  
  
}
```

And then I'm using different ungrouping options as shown below.

- **-ungroup_all :**
It collapses all hierarchical levels and their boundaries
- **-auto_ungroup area | delay:**
If the delay option is specified, it performs automatic ungrouping for hierarchies which are more likely to improve the overall design timing.
- **-boundary_optimization :**
It optimizes across all hierarchical boundaries of the design as shown below.
- **incremental_mapping:**
Allows incremental optimization to the design constraints based on previous runs.

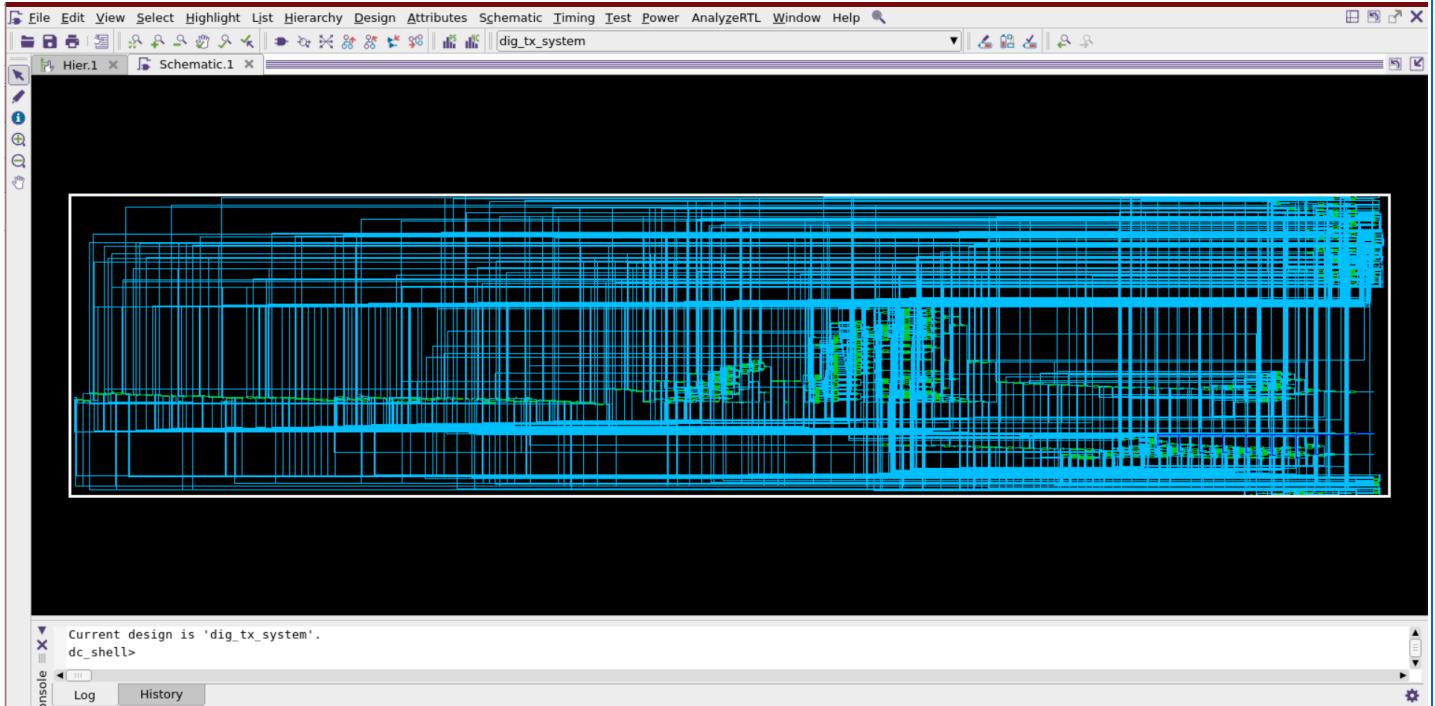
```
ungroup -all -flatten  
compile -exact_map -gate_clock -map_effort high -ungroup_all -area_effort medium -power_effort medium -boundary_optimization -auto_ungroup delay -incremental_mapping
```

Synthesis results of Flat Flow:

Total area	cell area:	Total power	Setup Violating Paths	Setup max (sys clk) Group path	Setup max (sys gated clk) Group path	Setup max (spi gated clk) Group path	Hold Violating Paths
1868.722896	803.196001	7.8266 mW	2	+0.00ns	+0.00ns	+0.00ns	244

I am currently unable to perform further optimization because each time I attempt to run the tool, it crashes due to heavy server load and user congestion, causing the compilation process to be stopped at this point.

The gate level netlist schematic:



Reports

1)power:

the high leakage power, shown as $2.10e+08$ pW (or $210 \mu\text{W}$), which dominates the total power . This is notable, especially given that the HVT library is being used, which should typically reduce leakage.

```
*****
Report : power
-hier
-analysis_effort low
Design : dig_tx_system
Version: V-2023.12-SP5-1
Date : Thu May 1 20:58:04 2025
*****

Library(s) Used:
    saed14lvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v125c.db)
    saed14hvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v125c.db)
    saed14rvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v125c.db)

Operating Conditions: ss0p72vm40c   Library: saed14hvt_base_ss0p72vm40c
Wire Load Model Mode: top

Design      Wire Load Model      Library
dig_tx_system      16000      saed14hvt_base_ss0p72vm40c

Global Operating Voltage = 0.72
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW      (derived from V,C,T units)
    Leakage Power Units = 1pW

-----
Hierarchy          Switch Power   Int Power   Leak Power   Total Power   %
dig_tx_system           6.740     0.876  2.10e+08     7.827  100.0
1
```

2) area:

Total area: 1868.72 ,Cell area is 803.20 μm^2 which about 43% of total area and Net interconnect area: ~1065.53 μm^2 (57%)

```
*****
Report : area
Design : dig_tx_system
Version: V-2023.12-SP5-1
Date  : Thu May 1 20:57:52 2025
*****


Library(s) Used:
  saed14lvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v125c.db)
  saed14hvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v125c.db)
  saed14rvt_base_ff0p88v125c (File: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v125c.db)

Number of ports:          20
Number of nets:           1563
Number of cells:          1530
Number of combinational cells: 1166
Number of sequential cells: 364
Number of macros/black boxes: 0
Number of buf/inv:         354
Number of references:     211

Combinational area:      436.540797
Buf/Inv area:            117.926399
Noncombinational area:   366.655204
Macro/Black Box area:    0.000000
Net Interconnect area:   1065.526895

Total cell area:          803.196001
Total area:               1868.722896
```

3) worst path setup:

The worst path is from register to output and this high value due to using high output delay.

```
Startpoint: u_spi_slave/state_tx_reg[1]
             (falling edge-triggered flip-flop clocked by spi_gated_clk)
Endpoint: o_dig_tx_system_miso
           (output port clocked by spi_gated_clk)
Path Group: ALL_VIOS
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----              -----                -----
dig_tx_system       16000                 saed14hvt_base_ss0p72vm40c

Point                           Incr      Path
-----                          -----
clock spi_gated_clk (fall edge)    0.50      0.50
clock network delay (ideal)       0.00      0.50
u_spi_slave/state_tx_reg[1]/CK (SAEDLVT14_FDNRBSBQ_V2_1) 0.00      0.50 f
u_spi_slave/state_tx_reg[1]/Q (SAEDLVT14_FDNRBSBQ_V2_1) 0.11      0.61 f
U437/X (SAEDLVT14_INV_1)          0.06      0.67 r
U108/X (SAEDLVT14_ND2_CDC_1)     0.10      0.77 f
U766/X (SAEDLVT14_NR2_MM_1)       0.07      0.85 r
U404/X (SAEDRVT14_DEL_L4D100_1)   0.15      1.00 r
U511/X (SAEDLVT14_ND2B_4)         0.04      1.04 f
U207/X (SAEDLVT14_INV_12)        0.01      1.05 r
U99/X (SAEDLVT14_INV_S_2)         0.07      1.12 f
U502/X (SAEDLVT14_OR2_MM_1)       0.03      1.15 f
U340/X (SAEDLVT14_AN2_MM_1)       0.03      1.18 f
U158/X (SAEDLVT14_ND2_5)          0.03      1.21 r
o_dig_tx_system_miso (out)        0.00      1.21 r
data arrival time                  0.00      1.21

clock spi_gated_clk (rise edge)    1.00      1.00
clock network delay (ideal)       0.00      1.00
clock uncertainty                 -0.30      0.70
output external delay             -0.40      0.30
data required time                 0.30

data required time                  0.30
data arrival time                   -1.21

slack (VIOLATED)                  -0.91
```

4) worst hold path in sys_clk group:

```
*****
Report : timing
  -path full
  -delay min
  -max_paths 10
Design : dig_tx_system
Version: V-2023.12-SP5-1
Date   : Thu May  1 20:57:52 2025
*****  

Operating Conditions: ff0p88v125c Library: saed14lvt_base_ff0p88v125c
Wire Load Model Mode: top  

Startpoint: u_dig_tx_asyn_fifo_write/sync_rptr/metastable_flop_reg[0]
(rising edge-triggered flip-flop clocked by sys_clock)
Endpoint: u_dig_tx_asyn_fifo_write/sync_rptr/o_dig_tx_fifo_synchronizer_d_out_reg[0]
(rising edge-triggered flip-flop clocked by sys_clock)
Path Group: SYS_CLK
Path Type: min  

Des/Clust/Port      Wire Load Model      Library
dig_tx_system       16000                  saed14hvt_base_ss0p72vm40c  

Point                Incr      Path
-----  

clock sys_clock (rise edge)          0.00      0.00
clock network delay (ideal)        0.00      0.00
u_dig_tx_asyn_fifo_write/sync_rptr/metastable_flop_reg[0]/CK (SAEDLVT14_FDPRBQ_V2LP_1)
0.00      0.00 r
u_dig_tx_asyn_fifo_write/sync_rptr/metastable_flop_reg[0]/Q (SAEDLVT14_FDPRBQ_V2LP_1)
0.03      0.03 f
u_dig_tx_asyn_fifo_write/sync_rptr/o_dig_tx_fifo_synchronizer_d_out_reg[0]/D (SAEDLVT14_FDPRBQ_V2LP_1)
0.00      0.03 f
data arrival time                   0.03  

clock sys_clock (rise edge)          0.00      0.00
clock network delay (ideal)        0.00      0.00
clock uncertainty                  0.15      0.15
u_dig_tx_asyn_fifo_write/sync_rptr/o_dig_tx_fifo_synchronizer_d_out_reg[0]/CK (SAEDLVT14_FDPRBQ_V2LP_1)
0.00      0.15 r
library hold time                  0.00      0.15
data required time                 0.15  

data required time                  0.15
data arrival time                  -0.03  

slack (VIOLATED)                  -0.12
```

5) quality of results:

<pre>***** Report : qor Design : dig_tx_system Version: V-2023.12-SP5-1 Date : Thu May 1 20:57:52 2025 ***** Timing Path Group 'SYS_CLK' ----- Levels of Logic: 14.00 Critical Path Length: 0.69 Critical Path Slack: 0.00 Critical Path Clk Period: 1.00 Total Negative Slack: 0.00 No. of Violating Paths: 0.00 Worst Hold Violation: -0.12 Total Hold Violation: -3.26 No. of Hold Violations: 85.00 ----- Cell Count ----- Hierarchical Cell Count: 0 Hierarchical Port Count: 0 Leaf Cell Count: 1530 Buf/Inv Cell Count: 354 Buf Cell Count: 115 Inv Cell Count: 255 CT Buf/Inv Cell Count: 0 Combinational Cell Count: 1166 Sequential Cell Count: 364 Macro Count: 0 ----- </pre>	<pre>Timing Path Group 'SYS_GATED_CLK' ----- Levels of Logic: 9.00 Critical Path Length: 0.69 Critical Path Slack: 0.00 Critical Path Clk Period: 1.00 Total Negative Slack: 0.00 No. of Violating Paths: 0.00 Worst Hold Violation: -0.04 Total Hold Violation: -0.60 No. of Hold Violations: 29.00 ----- Design Rules ----- Total Number of Nets: 1563 Nets With Violations: 0 Max Trans Violations: 0 Max Cap Violations: 0 ----- Hostname: academysvr02 Compile CPU Statistics ----- Resource Sharing: 0.69 Logic Optimization: 33.71 Mapping Optimization: 20.22 ----- Overall Compile Time: 84.48 Overall Compile Wall Clock Time: 88.06 ----- </pre>
--	---

3. Flat approach with old constraints but with more compile phases than the first:

I make same as the previous flat approach; fist I compile each module separately and then making ungroup and compile again as shown in script.

```

ungroup -all -flatten

compile -exact_map -gate_clock -map_effort high -ungroup_all -area_effort medium -power_effort medium -boundary_optimization -auto_ungroup delay -incremental_mapping

##### Reports_compile_incr #####
report_timing -max_paths 10 -delay_type max > "./reports/compile_incr_high/syn_setup.rpt"
report_timing -max_paths 10 -delay_type min > "./reports/compile_incr_high/syn_hold.rpt"
report_area > "./reports/compile_incr_high/syn_area.rpt"
report_qor > "./reports/compile_incr_high/syn_qor.rpt"
report_power > "./reports/compile_incr_high/syn_power.rpt"
report_constraint -all_violators > "./reports/compile_incr_high/syn_violators.rpt"
report_power -hierarchy > "./reports/compile_incr_high/power_reports.rpt"
report_cell > "./reports/compile_incr_high/cells_reports.rpt"
report_resources > "./reports/compile_incr_high/resources.rpt"
report_clock_gating > "./reports/compile_incr_high/clock_gating_reports.rpt"

##### Compile_ultra #####
compile_ultra -exact_map -gate_clock -timing_high_effort_script -retime -incremental

##### Reports_compile_ultra #####
report_timing -max_paths 10 -delay_type max > "./reports/compile_ultra/syn_setup.rpt"
report_timing -max_paths 10 -delay_type min > "./reports/compile_ultra/syn_hold.rpt"
report_area > "./reports/compile_ultra/syn_area.rpt"
report_qor > "./reports/compile_ultra/syn_qor.rpt"
report_power > "./reports/compile_ultra/syn_power.rpt"
report_constraint -all_violators > "./reports/compile_ultra/syn_violators.rpt"
report_power -hierarchy > "./reports/compile_ultra/power_reports.rpt"
report_cell > "./reports/compile_ultra/cells_reports.rpt"
report_resources > "./reports/compile_ultra/resources.rpt"
report_clock_gating > "./reports/compile_ultra/clock_gating_reports.rpt"

##### Compile_ultra_incr #####
compile_ultra -exact_map -gate_clock -timing_high_effort_script -retime -incremental

##### Close Formality Setup file #####
set_svf -off

##### Reports #####
report_timing -max_paths 10 -delay_type max > "./reports/compile_ultra_incr/syn_setup.rpt"
report_timing -max_paths 10 -delay_type min > "./reports/compile_ultra_incr/syn_hold.rpt"
report_area > "./reports/compile_ultra_incr/syn_area.rpt"
report_qor > "./reports/compile_ultra_incr/syn_qor.rpt"
report_power > "./reports/compile_ultra_incr/syn_power.rpt"
report_constraint -all_violators > "./reports/compile_ultra_incr/syn_violators.rpt"
report_power -hierarchy > "./reports/compile_ultra_incr/power_reports.rpt"
report_cell > "./reports/compile_ultra_incr/cells_reports.rpt"
report_resources > "./reports/compile_ultra_incr/resources.rpt"
report_clock_gating > "./reports/compile_ultra_incr/clock_gating_reports.rpt"
report_threshold_voltage_group > "./reports/compile_ultra_incr/threshold_voltage_reports.rpt"

```

Synthesis results of first compile ultra in Flat Flow

Total area	cell area:	Total power	Setup Violating Paths	Setup max (sys clk) Group path	Setup max (sys gated clk) Group path	Setup max (spliced clk) Group path	Hold Violating Paths
1264.497286	586.213207	0.1445 mW	0	+0.30ns	+0.73ns	+ 3.13ns	395

Synthesis results of forth run in Flat Flow

Total area	cell area:	Total power	Setup Violating Paths	Setup max (sys clk) Group path	Setup max (sys gated clk) Group path	Setup max (spi gated clk) Group path	Hold Violating Paths
1271.606712	586.080007	0.1442 mW	0	+ 0.26ns	0.60ns	+ 3.13ns	395

When I ran the same number of compile phases using compile, I observed that the results were better compared to compile_ultra. It appears that compile_ultra focused more on power optimization, while compile delivered better results in terms of timing and area.

Chapter 2

PNR

Place and route is the back-end flow in ASIC physical design. Here, we read the netlist generated from synthesis and constraints to arrange the generated cells, manage, fix timing and route them for physical system on chip.

At the start of PnR flow, we define the PDK that we use, and the TLU+ library which is used to estimate the parasitic, hence estimating the delays. IC Compiler tool is used.

Basic PnR flow:

- Floor planning
- Power planning
- Placement
- Clock tree network
- Routing
- Finishing

Setup or design preparation at the start of PnR flow: This section will explain in detail the commands and steps used in order to setup the design in order to proceed in the PnR steps correctly.

First, we need to define the library files with the (.db) file extension. It is possible to do that by setting the application variables link_library and target_library to the library files path.

```
#####
#REF_PATH

set DESIGN_REF_PATH "${DESIGN_REF_PATH}/SAED14nm_EDK_TECH_DATA"

#####
#Liberty
set Std_cell_lib      "${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/base/saed14slvt_base_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/base/saed14slvt_base_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/base/saed14slvt_base_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/cg/saed14lvt_cg_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/cg/saed14lvt_cg_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_LVT/liberty/nldm/cg/saed14lvt_cg_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/cg/saed14rvt_cg_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_RVT/liberty/nldm/cg/saed14rvt_cg_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/cg/saed14hvt_cg_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/cg/saed14hvt_cg_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_HVT/liberty/nldm/cg/saed14hvt_cg_tt0p8v25c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/cg/saed14slvt_cg_ff0p88v125c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/cg/saed14slvt_cg_ss0p72vm40c.db \
${DESIGN_REF_PATH}/SAED14nm_EDK_STD_SLVT/liberty/nldm/cg/saed14slvt_cg_tt0p8v25c.db "
```

Also define paths of inputs like netlist and .scd and paths of outputs

```
#####
#Main_PATH
set ROOT_DIR      "/home/svgasic25abkhaled/GP"
set DESIGN_REF_PATH "/home/tools/PDK/SAED14_EDK"
set VERILOG_DIR   "/home/svgasic25abkhaled/GP/synthesis/syn_new_cons/syn_hier_top_down_2/outputs"

#####
#inputs
set DESIGN_NAME    "dig_tx_system"
set Constraints_file  "${ROOT_DIR}/synthesis/syn_new_cons/syn_hier_top_down_2/outputs/${DESIGN_NAME}.scd"
set Core_compile   "${ROOT_DIR}/synthesis/syn_new_cons/syn_hier_top_down_2/outputs/${DESIGN_NAME}.v"

#####
#outputs
set Svf_file       "${ROOT_DIR}/pnr/hier_top_down2/results/${DESIGN_NAME}.svf"
set ARC_TOP        "${ROOT_DIR}/pnr/hier_top_down2/results/${DESIGN_NAME}.ndm"
set Top_design_pt  "${ROOT_DIR}/pnr/hier_top_down2/results/${DESIGN_NAME}_pt.v"
```

```

#####
set REFERENCE_LIB "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/ndm/saed14lvt_frame_only.ndm \
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_SLVT/ndm/saed14slvt_frame_only.ndm \
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_HVT/ndm/saed14hvt_frame_only.ndm \
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_RVT/ndm/saed14rvt_frame_only.ndm "

set Std_cell_gds      "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_RVT/gds/saed14rvt.gds \
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_SLVT/gds/saed14slvt.gds \
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_HVT/gds/saed14hvt.gds \
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/gds/saed14lvt.gds "

set Tech_file          "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/tf/saed14nm_ip9m.tf"
set Map_file            "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/map/saed14nm_tf_itf_tluplus.map"
#set Gds_map_file      "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/map/saed14nm_ip9m_gdsout.map"
set Gds_map_file       "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/map/saed14nm_ip9m_gdsin_gdsout.map"

set Tlup_max_file     "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/tlup/saed14nm_ip9m_Cmax.tlup"
set Tlup_min_file     "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/tlup/saed14nm_ip9m_Cmin.tlup"
set Nxtgrd_max_file   "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/nxtgrd/saed14nm_ip9m_Cmax.nxtgrd"
set Nxtgrd_min_file   "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/nxtgrd/saed14nm_ip9m_Cmin.nxtgrd"

set icv_drc_runset    "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/icv_drc/saed14nm_ip9m_drc_rules.rs"
set icv_mfill_runset   "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/icv_drc/saed14nm_ip9m_mfill_rules.rs"
#####

```

After that, we create the library that holds all the design files. This is done using the command:

```

#####
sh rm -fr $ARC_TOP
create_lib $ARC_TOP \
-technology $Tech_file \
-ref_libs $REFERENCE_LIB

#####
read_parasitic.tech -tlup "$Tlup_max_file $Tlup_min_file" \
-layermap $Map_file

#####
read_verilog "$Core_compile"
current_design ${DESIGN_NAME}
source $Constraints_file

#####
report_ports -drive > "../reports/floorplanning/driving_cells.rpt"

#####
save_block -as ${DESIGN_NAME}_1_data_setup
save_lib

close_block
close_lib

```

Chapter 3

PNR in Flat flow

1) Floorplan

At first I'm overwriting the constrain to make tool work hard

```
#####
#####overwrite constrains

remove_clock_uncertainty -setup [all_clocks]
remove_clock_uncertainty -hold [all_clocks]
remove_clock_transition [all_clocks]
remove_input_delay [all_inputs]
remove_output_delay [all_outputs]

set_input_delay -clock [get_clocks spi_gated_clk] 0.42 [remove_from_collection [all_inputs] [get_ports "i_dig_tx_system_clk32 i_dig_tx_system_clk26"]]

set_output_delay -clock [get_clocks sys_gated_clk] 0.42 [get_ports o_dig_tx_system_data_out]
set_output_delay -clock [get_clocks sys_gated_clk] 0.42 [get_ports o_dig_tx_system_crc_valid]
set_output_delay -clock [get_clocks sys_clock] 0.42 [get_ports o_dig_tx_system_regfile_valid]
set_output_delay -clock [get_clocks sys_clock] 0.42 [get_ports o_dig_tx_system_output_valid]
set_output_delay -clock [get_clocks spi_gated_clk] 0.42 [get_ports o_dig_tx_system_data_slave_out]
set_output_delay -clock [get_clocks sys_clock] 0.42 [get_ports o_dig_tx_system_done]
set_output_delay -clock [get_clocks spi_gated_clk] 0.42 [get_ports o_dig_tx_system_miso_ena]
set_output_delay -clock [get_clocks spi_gated_clk] 0.42 [get_ports o_dig_tx_system_miso]

set_clock_uncertainty -setup 0.350 [all_clocks]
set_clock_uncertainty -hold 0.160 [all_clocks]

set_clock_transition 0.0 [get_clocks sys_clock]
```

I used a floorplan with 25% core utilization. An Incremental floorplan placement was needed to decrease the congestion. This means only 25% of the core area will be occupied by standard cells, leaving 75% for routing.

```
initialize_floorplan -core_utilization 0.25 -flip_first_row true \
                     -core_offset {10 10 10 10}
```

Then added boundary cell and tie. Insert boundary cells at boundaries to prevent latch-up and ensure proper isolation. Also Insert tap cells to maintain substrate biasing and avoid floating well issues.

```
#####
##### Boundary cells insertion

set_boundary_cell_rules -prefix boundary -insert_into_blocks -at_va_boundary -left_boundary_cell */SAEDLVT14_CAPB2 -right_boundary_cell */SAEDLVT14_CAPB2
compile_boundary_cells

check_boundary_cells > "../reports/floorplanning/boundary_cell_check.rpt"

create_tap_cells -lib_cell [get_lib_cells saed14rvt_base_ff0p88v125c/SAEDRVT14_TAPDS] -distance 30 -pattern stagger
```

Report check boundary cells to check any error :

```
*****
Report : check_boundary_cells
Design : temp_data_setup
Version: V-2023.12-SP5
Date   : Thu May  1 23:09:08 2025
*****
Collecting design data...

Continuity report
=====
For design temp_data_setup:
Information: No continuity violation. (CHF-024)
Continuity violations in design temp_data_setup: 0
-----
Total continuity violations: 0

Redundant extra boundary cells report
=====
For design temp_data_setup:
Information: No redundant extra boundary cells violation. (CHF-024)
Redundant extra boundary cell in design temp_data_setup: 0
-----
Total redundant extra boundary cells: 0

Corner and boundary cell report
=====
For design temp_data_setup:
Information: No corner and boundary cell violation. (CHF-024)
Corner and boundary cell violations in design temp_data_setup: 0
-----
Total corner and boundary cell violations: 0

Orientation report
=====
For design temp_data_setup:
Information: No orientation violation. (CHF-024)
Orientation violations in design temp_data_setup: 0
-----
Total orientation violations: 0
```

Then create placement and global routing. The initial placement was performed using create_placement in floorplan-aware mode with high effort and timing-driven optimization to achieve quality cell distribution.

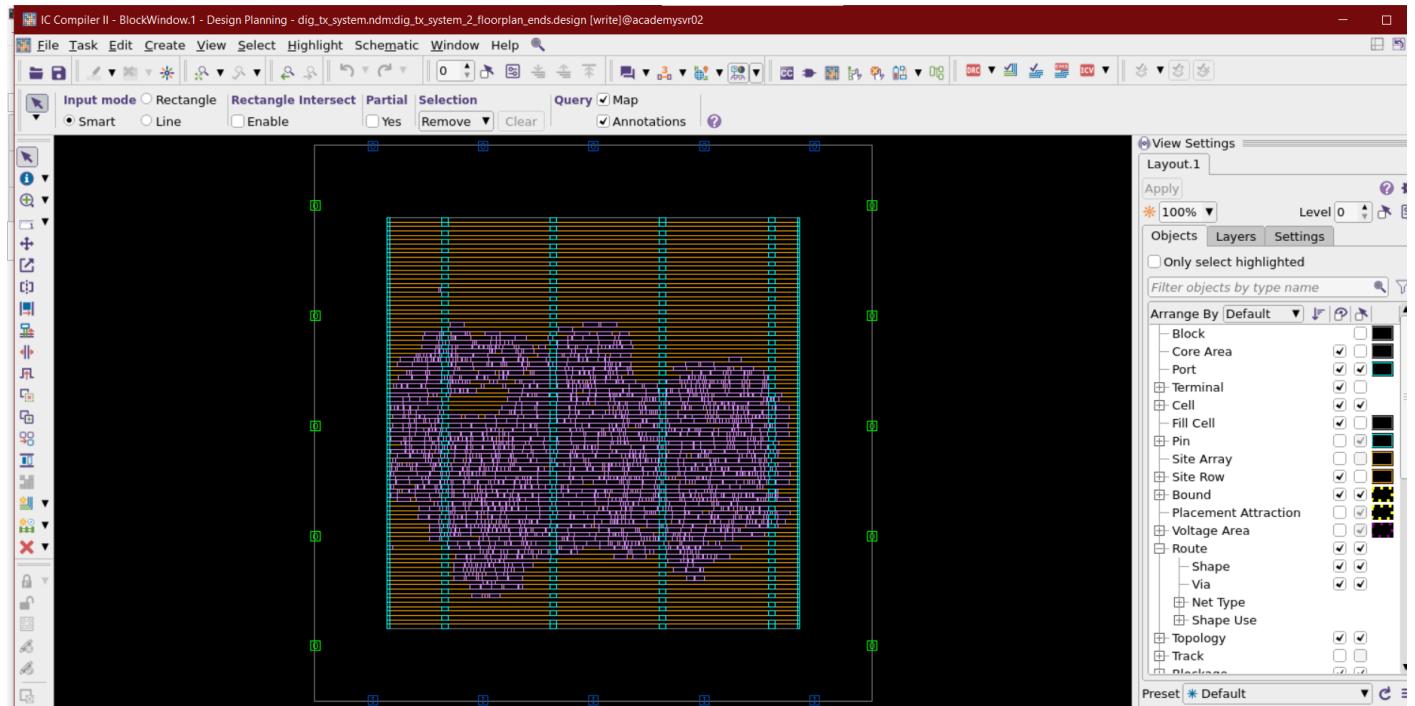
```
create_placement -floorplan -timing_driven -effort high -incremental
legalize_placement
route_global -floorplan true -congestion_map_only true -effort_level high

report_placement > "../reports/floorplanning/floorplacement.rpt"
report_utilization > "../reports/floorplanning/utilization.rpt"
report_qor_summary > "../reports/floorplanning/qor.rpt"
report_timing -delay_type max -max_paths 5 > "../reports/floorplanning/setup_delay.rpt"
report_global_timing > "../reports/floorplanning/global_timing.rpt"

set_app_option -name time.snapshot_storage_location -value "./"
create_qor_snapshot -name floor_qor_snp -significant_digits 4

report_qor_snapshot -name floor_qor_snp > "../reports/floorplanning/floor.qor_snapshot.rpt"
```

The floor planning shown in next figure:



Floorplaning reports

report placement: no error

```
*****
Report : report_placement
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Thu May  1 23:09:19 2025
*****  
=====
Note: Including violations of fixed cells or between fixed pairs of cells.
      To ignore violations of / between fixed cells, enable -ignore_fixed.
=====

Wire length report (all)
=====
wire length in design temp_data_setup: 8101.482 microns.
wire length in design temp_data_setup (see through blk pins): 8101.482 microns.

Physical hierarchy violations report
=====
Violations in design temp_data_setup:
  0 cells have placement violation.

Voltage area violations report
=====
Voltage area placement violations in design temp_data_setup:
  0 cells placed outside the voltage area which they belong to.
```

utilization

```
*****
Report : report_utilization
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Thu May  1 23:09:19 2025
*****
Utilization Ratio:          0.2513
Utilization options:
  - Area calculation based on: site_row of block temp_data_setup
  - Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                3196.9776
Total Capacity Area:        3196.9776
Total Area of cells:        803.4624
Area of excluded objects:
  - hard_macros      : 0.0000
  - macro_keepouts   : 0.0000
  - soft_macros       : 0.0000
  - io_cells          : 0.0000
  - hard_blockages   : 0.0000
Total Area of excluded objects: 0.0000
Ratio of excluded objects:    0.0000

Utilization of site-rows with:
  - Site 'unit': 0.2513
```

The total area available for placement (site row capacity) is 3196.98 units, and the total cell area used is 803.46 units. There are no excluded objects like hard macros, keepouts, or IO cells in this block.

QOR: no DRC violation

Timing			
Context		WNS	TNS
default	(Setup)	-0.51	-13.39
default::estimated_corner	(Setup)	-0.51	-13.39
Design	(Setup)	-0.51	-13.39
default	(Hold)	-0.18	-68.79
default::estimated_corner	(Hold)	-0.18	-68.79
Design	(Hold)	-0.18	-68.79

Miscellaneous			
Cell Area (netlist):		803.46	
Cell Area (netlist and physical only):		939.15	
Nets with DRC Violations:	0		
	1		

The timing report for the design shows violations in both setup and hold paths. The Worst Negative Slack (WNS) is -0.51 ns for setup and -0.18 ns for hold. These indicate the most timing-critical paths in the design are currently violating timing requirements.

The Total Negative Slack (TNS) is -13.39 ns for setup and -68.79 ns for hold. This reflects the cumulative slack across all failing paths, showing a higher volume of violations on the hold side.

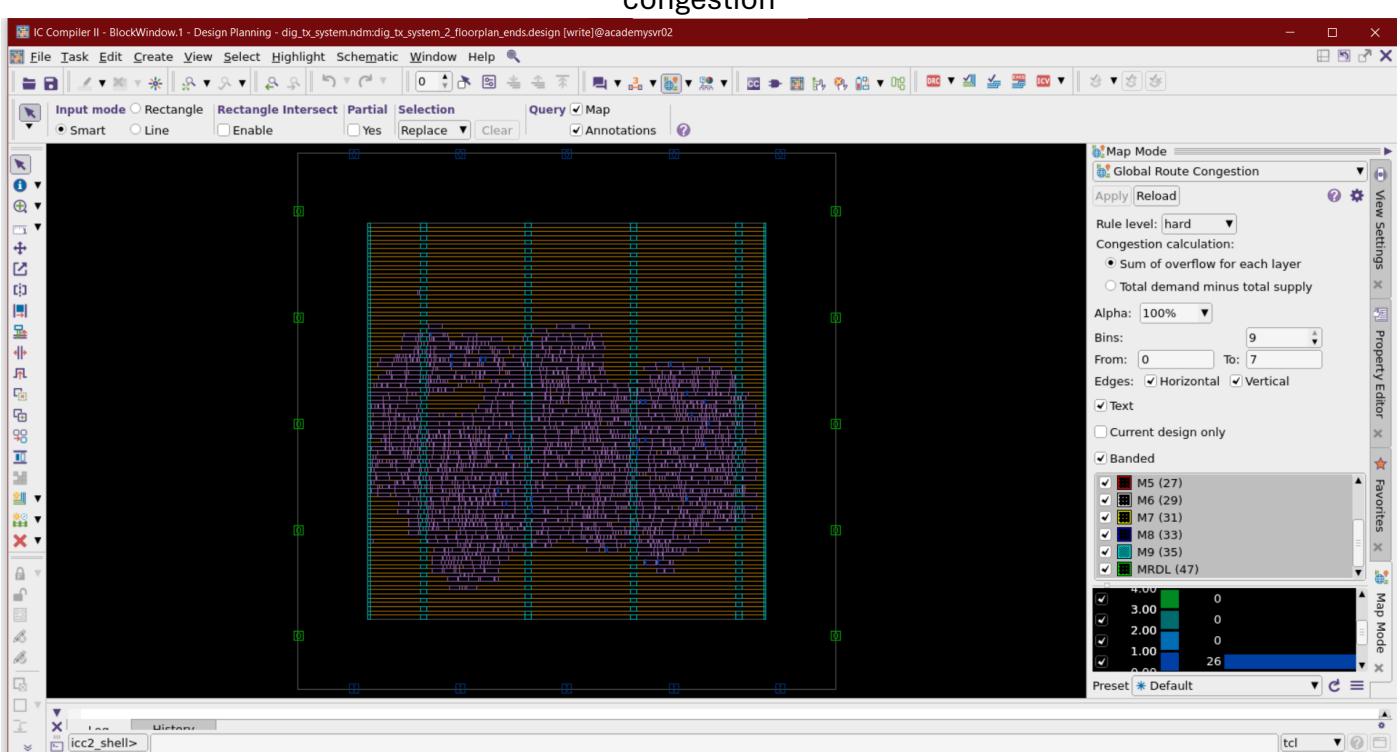
There are 38 setup and 549 hold violating endpoints (NVE).

QOR Snapshot

```
*****
Report      : create_qor_snapshot (floor_qor_snp)
Design      : dig_tx_system
Version     : V-2023.12-SP5
Date        : Thu May  1 23:09:25 2025
Time unit   : 1.00ns
Resistance unit : 1.00kOhm
Capacitance unit: 1.00pF
Voltage unit  : 1.00V
Current unit  : 1.00uA
Power unit   : 1.00pW
Location     : /home/svgasic25abkhaled/GP/pnr/flat/work/./
*****
No. of scenario = 2
s1 = default
s2 = default::estimated_corner
-----
WNS of each timing group:           s1      s2
-----
INPUT                           -0.4859  -0.4859
COMBO                          -0.3080  -0.3080
REG2REG                        -0.0583  -0.0583
OUTPUT                          -0.5099  -0.5099
SPI_CLK                         0.1188  0.1188
SYS_CLK                         0.0889  0.0889
-----
Setup WNS:                      -0.5099  -0.5099  -0.5099
Setup TNS:                      -13.3856 -13.3856 -13.3856
Number of setup violations:       38      38      38
Hold WNS:                       -0.1762  -0.1762  -0.1762
Hold TNS:                       -68.7882 -68.7882 -68.7882
Number of hold violations:       549    549    549
Number of max trans violations:  0      0      0
Number of max cap violations:   0      0      0
Number of min pulse width violations: 0      0      0
-----
Area:                            939.149
Cell count:                     1530
Buf/inv cell count:             354
Std cell utilization:          0.2513
CPU(s):                          52
Mem(Mb):                        1272
Host name:                      academysvr02
-----
Histogram:           s1      s2
-----
Max violations:                38      38
  above ~ -0.7    ---    0      0
  -0.6 ~ -0.7    ---    0      0
  -0.5 ~ -0.6    ---    1      1
  -0.4 ~ -0.5    ---   26     26
  -0.3 ~ -0.4    ---    1      1
  -0.2 ~ -0.3    ---    0      0
  -0.1 ~ -0.2    ---    0      0
  0 ~ -0.1      ---   10     10
-----
Min violations:                549    549
  -0.06 ~ above  ---    4      4
```

Global timing

```
*****
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Thu May  1 23:09:19 2025
*****
-----
Setup violations
-----
      Total  reg->reg  in->reg  reg->out  in->out
-----
WNS   -0.51    -0.06    -0.49    -0.51    -0.31
TNS   -13.39   -0.15   -12.31   -0.62    -0.31
NUM    38      7       26      4       1
-----
Hold violations
-----
      Total  reg->reg  in->reg  reg->out  in->out
-----
WNS   -0.18    -0.18    0.00    0.00    0.00
TNS   -68.79   -68.79   0.00    0.00    0.00
NUM    549    549      0       0       0
```



I don't have any errors in this stage, so I go to next stage to create power mesh.

2) power planning

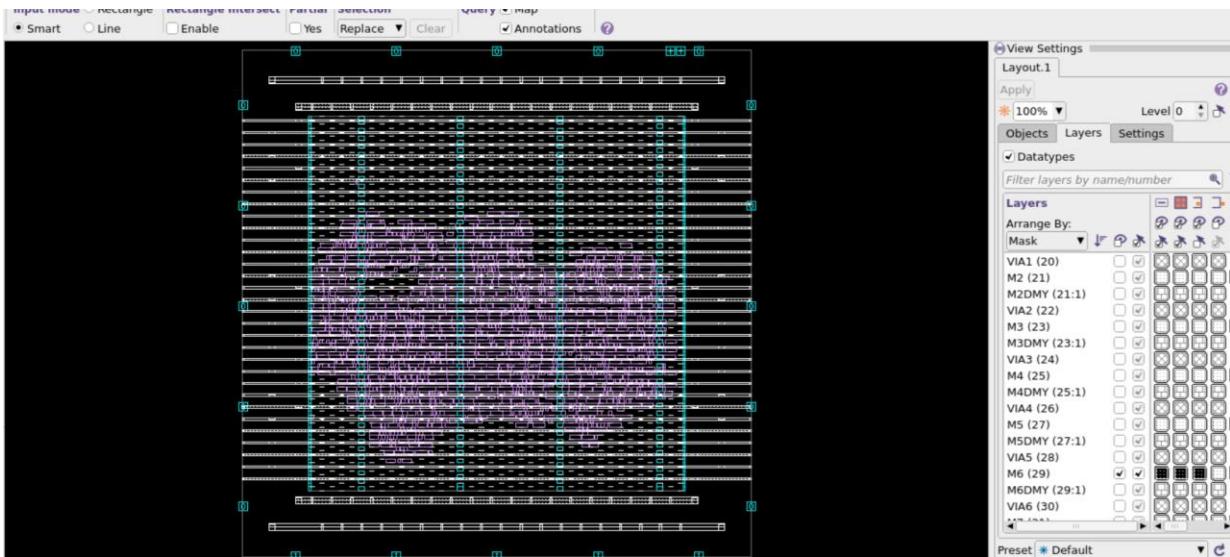
There is no strategy before this step:

```
[svgasic25abkhaled@academysvr02 scripts]$ cat ..../reports/powerplanning/strategies_before_pg.rpt
Cannot find any strategy.
```

Creating two mesh. The first on M6 with pitch 3.6 and the second on M7 with pitch 3 and offset 0.5 . this strategy solve each DRC error that generated before.

```
#####
#####Create_Top_horizontal_Mesh
create_pg_mesh_pattern TOP_MESH_HORIZONTAL \
    -layers " \
        { {horizontal_layer: M6} {width: 0.3} {spacing: interleaving} {pitch: 3.6} {offset: 0.0} {trim : true} } \
    "
set_pg_strategy VDDVSS_TOP_MESH_HORIZONTAL \
    -core \
    -pattern { {name: TOP_MESH_HORIZONTAL} {nets:{VDD VSS}} } \
    -extension { {{stop:design_boundary_and_generate_pin}} }
```

```
compile_pg -strategies {VDDVSS_TOP_MESH_HORIZONTAL}
```

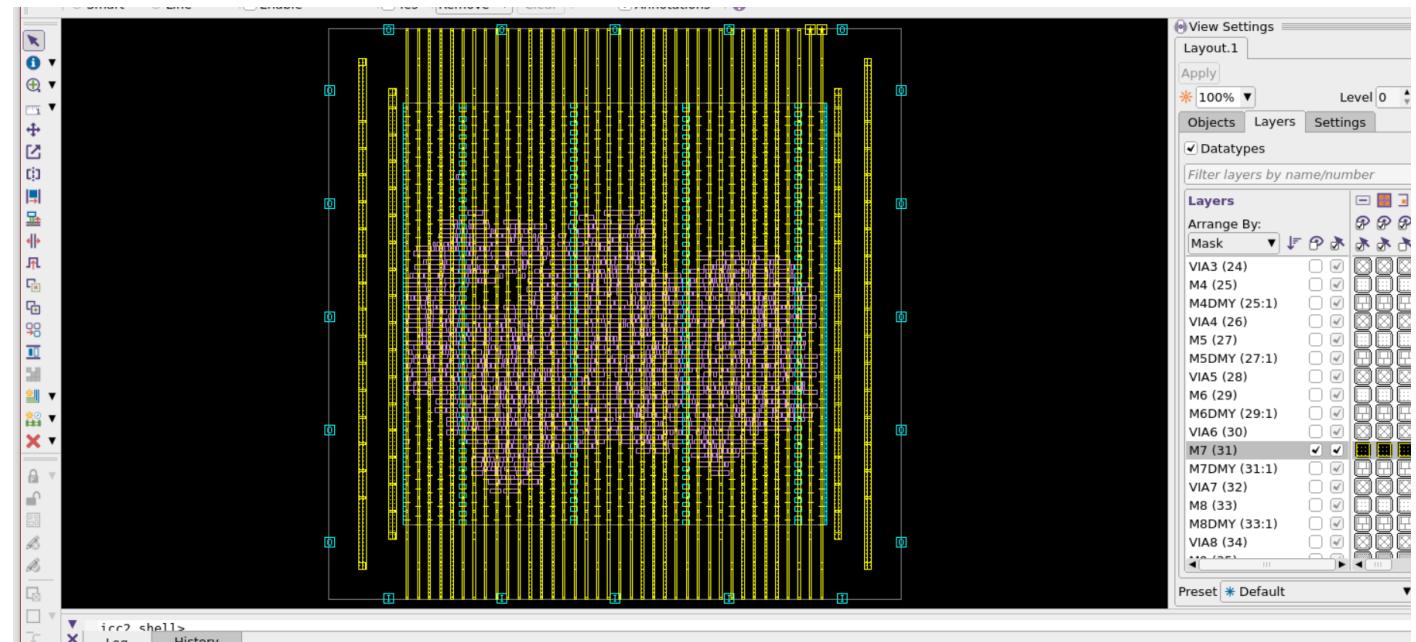


The vertical mesh

```
#####
#####Create_Top_vertical_Mesh
create_pg_mesh_pattern TOP_MESH_VERTICAL \
-layers " \
    {vertical_layer: M7} {width: 0.3} {spacing: interleaving} {pitch: 3} {offset: 0.5} {trim : true} } \
"

set_pg_strategy VDDVSS_TOP_MESH_VERTICAL \
-core \
-pattern { {name: TOP_MESH_VERTICAL} {nets:{VSS VDD}} } \
-extension { {stop:design_boundary_and_generate_pin} }

compile_pg -strategies {VDDVSS_TOP_MESH_VERTICAL}
```



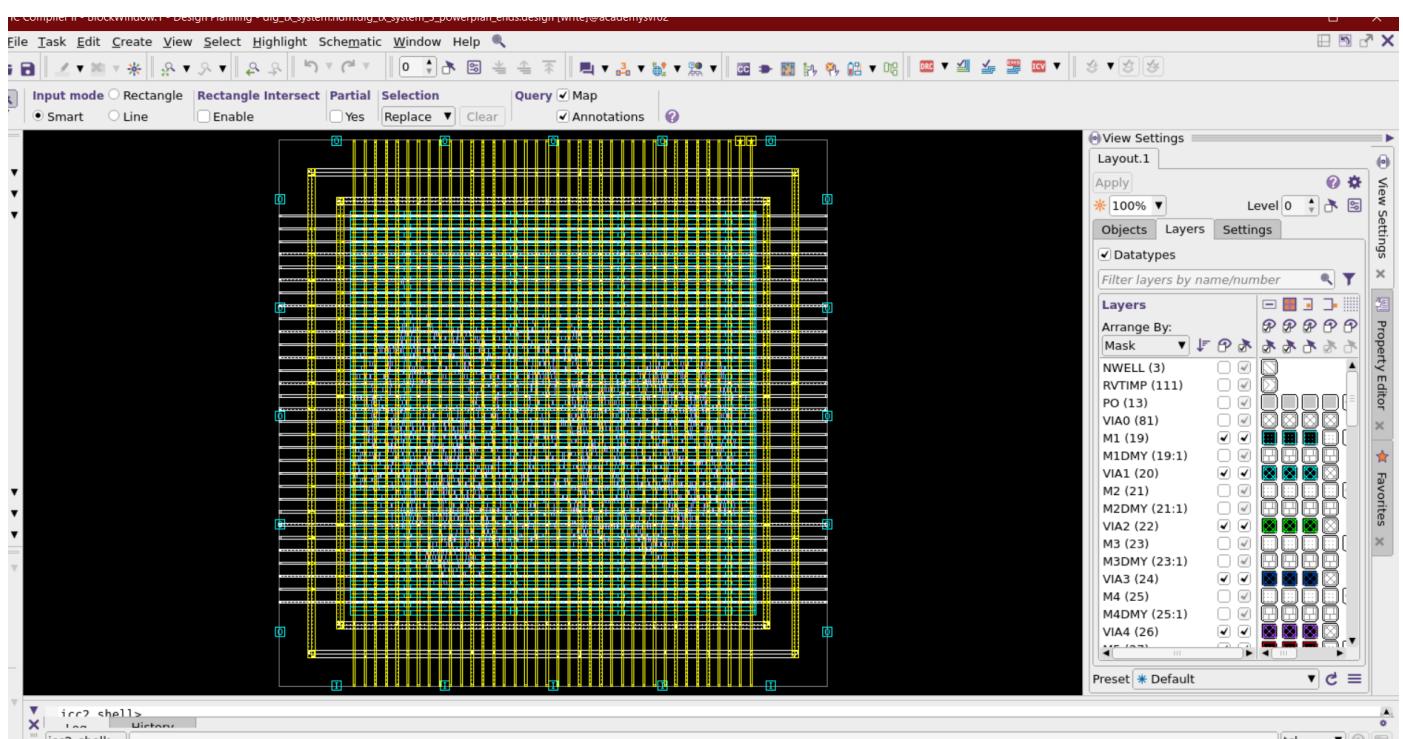
Then Creating ring on layer M6,M7

```
#####
#Create_Recursive_Rings
create_pg_ring_pattern \
    ring_pattern \
    -horizontal_layer M6 -vertical_layer M7 \
    -horizontal_width 1 -vertical_width 1 \
    -horizontal_spacing 3 -vertical_spacing 3

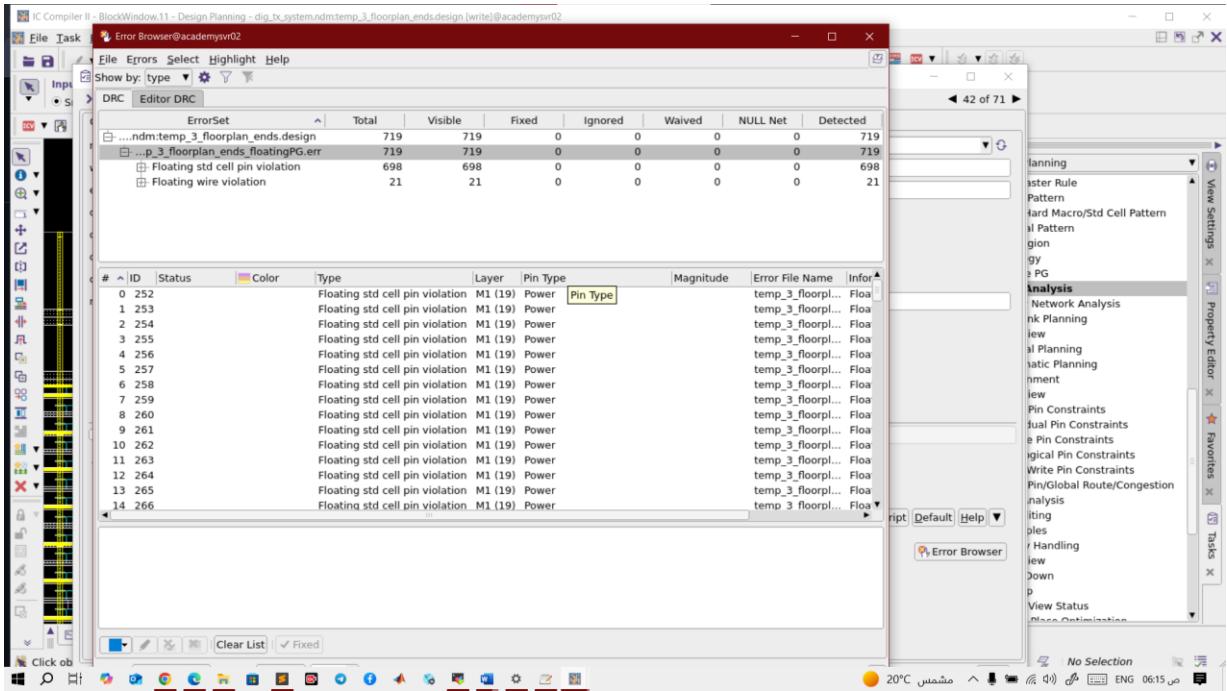
set_pg_strategy RING -core -pattern {{ name: ring_pattern } { nets: "VSS VDD" } { offset:{1 1}}}

compile_pg -strategies RING

check_pg_connectivity -nets "VDD VSS"
```



Because there is no direct via from M7 to rails, this problem will lead the floating stander cell without connected to VDD or VSS and will make drcs as shown in next figure.



I solved the floating point DRC by creating via from layer M7 to M1

```
set_pg_via_master_rule PG_VIA_3x1 -cut_spacing 0.25 -via_array_dimension {3 1}
create_pg_vias -to_layers M7 -from_layers M1 -via_masters PG_VIA_3x1 -nets VDD
create_pg_vias -to_layers M7 -from_layers M1 -via_masters PG_VIA_3x1 -nets VSS
```

Power planning reports:

check pg connectivity:

```
Checking secondary net through power switch is enabled.
Secondary net will be checked together from primary net. They will be treated as the same net
Primary Net : VDD Secondary Net:
Primary Net : VSS Secondary Net:
Loading cell instances...
Number of Standard Cells: 1910
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 86
Number of VDD Vias: 5544
Number of VDD Terminals: 68
*****Verify net VDD connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 86
Number of VSS Vias: 5432
Number of VSS Terminals: 70
*****Verify net VSS connectivity*****
Number of floating wires: 0
Number of floating vias: 0
Number of floating std cells: 0
Number of floating hard macros: 0
Number of floating I/O pads: 0
Number of floating terminals: 0
Number of floating hierarchical blocks: 0
*****
Overall runtime: 0 seconds.
```

No floating wires, vias, cells, macros, IO pads, or terminals were found.

checking DRC:

```
Command check_pg_drc started at Thu May 1 23:10:32 2025
Command check_pg_drc finished at Thu May 1 23:10:34 2025
CPU usage for check_pg_drc: 0.72 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 2.85 seconds ( 0.00 hours)
No errors found.
```

checking any missing via

```
Check net VDD vias...
Number of missing vias: 0
Checking net VDD vias took 0 seconds.
Check net VSS vias...
Number of missing vias: 0
Checking net VSS vias took 0 seconds.
Overall runtime: 0 seconds.
```

QOR

```
*****
Report : qor
      -summary
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Thu May 1 23:10:35 2025
*****
```

Timing

Context	WNS	TNS	NVE
default (Setup)	-0.51	-13.39	38
default::estimated_corner (Setup)	-0.51	-13.39	38
Design (Setup)	-0.51	-13.39	38
default (Hold)	-0.18	-68.79	549
default::estimated_corner (Hold)	-0.18	-68.79	549
Design (Hold)	-0.18	-68.79	549

Miscellaneous

Cell Area (netlist):	803.46
Cell Area (netlist and physical only):	939.15
Nets with DRC Violations:	0

1

qor snapshot

```
*****
Report      : create_qor_snapshot (power_qor_snp)
Design       : dig_tx_system
Version      : V-2023.12-SP5
Date         : Thu May  1 23:10:31 2025
Time unit    : 1.00ns
Resistance unit : 1.00kOhm
Capacitance unit: 1.00pF
Voltage unit   : 1.00V
Current unit    : 1.00uA
Power unit     : 1.00pW
Location       : /home/svgasic25abkhaled/GP/pnr/flat/work/..
*****
No. of scenario = 2
s1 = default
s2 = default::estimated_corner
-----
WNS of each timing group:           s1      s2
-----
INPUT                           -0.4859  -0.4859
COMBO                          -0.3080  -0.3080
REG2REG                        -0.0583  -0.0583
OUTPUT                         -0.5099  -0.5099
SPI_CLK                         0.1188  0.1188
SYS_CLK                         0.0889  0.0889
-----
Setup WNS:                      -0.5099  -0.5099  -0.5099
Setup TNS:                      -13.3856 -13.3856 -13.3856
Number of setup violations:      38       38       38
Hold WNS:                       -0.1762  -0.1762  -0.1762
Hold TNS:                       -68.7882 -68.7882 -68.7882
Number of hold violations:      549      549      549
Number of max trans violations:  0        0        0
Number of max cap violations:   0        0        0
Number of min pulse width violations: 0        0        0
-----
Area:                            939.149
Cell count:                     1530
Buf/inv cell count:             354
Std cell utilization:          0.2513
CPU(s):                          73
Mem(Mb):                        1272
Host name:                      academysvr02
```

Majority of violations are in the -0.4 to -0.5 ns range. There are 26 violations in this range for both s1 and s2. And the Hold Violations The majority of violations are between -0.05 to -0.06 ns, with 14 violations in this range for both corners.

3) Placement

The main goal of the placement step was to reach a legalized detailed placement for the cells that achieve the minimum congestion while maintaining good timing. To achieve this goal several incremental placements focused on fixing the congestion was needed as initial placement had some congestion problems.

First, I will generate some option to help tool in this step These settings focus on improving both timing and placement while enhancing efforts to handle hold violations.:

```
#####
General Optimization
set_app_options -name time.disable_recovery_removal_checks -value false
set_app_options -name time.disable_case_analysis -value false
set_app_options -name place.coarse.continue_on_missing_scandef -value true
set_app_options -name place.coarse.congestion_analysis_effort -value high
set_app_options -name opt.common.hold_effort -value high

set_app_options -name opt.timing.effort -value high
```

The source the multi-mode muti corner script, I'm working in one mode (fun) and two corner fast and slow

```
source ./../scripts/mcmm.tcl
```

Then change the constraints and overwriting on it after power plane stage. No changing in the value of input and output delay but change the uncertainty and reduces it .

```
#####
#####overwrite constraints#####
remove_clock_uncertainty -setup [all_clocks]
remove_clock_uncertainty -hold [all_clocks]
remove_clock_transition [all_clocks]
remove_input_delay [all_inputs]
remove_output_delay [all_outputs]

set_input_delay -clock [get_clocks spi_gated_clk] 0.40 [remove_from_collection [all_inputs] [get_ports "i_dig_tx_system_clk32 i_dig_tx_system_clk26"]]

set_output_delay -clock [get_clocks sys_gated_clk] 0.40 [get_ports o_dig_tx_system_data_out]
set_output_delay -clock [get_clocks sys_gated_clk] 0.40 [get_ports o_dig_tx_system_crc_valid]
set_output_delay -clock [get_clocks sys_clock] 0.40 [get_ports o_dig_tx_system_regfile_valid]
set_output_delay -clock [get_clocks sys_clock] 0.40 [get_ports o_dig_tx_system_output_valid]
set_output_delay -clock [get_clocks spi_gated_clk] 0.40 [get_ports o_dig_tx_system_data_slave_out]
set_output_delay -clock [get_clocks sys_clock] 0.40 [get_ports o_dig_tx_system_done]
set_output_delay -clock [get_clocks spi_gated_clk] 0.40 [get_ports o_dig_tx_system_miso_ena]
set_output_delay -clock [get_clocks spi_gated_clk] 0.40 [get_ports o_dig_tx_system_miso]

set_clock_uncertainty -setup 0.310 [all_clocks]
set_clock_uncertainty -hold 0.155 [all_clocks]

set_clock_transition 0.0 [get_clocks sys_clock]
```

I create placement and making effort high in timing. Multiple incremental placement steps are performed with the same high-effort, timing-driven approach. This allows for adjustments while retaining previous placement optimization

```
#####
#####Placement Optimization #####
create_placement -effort high -timing_driven
create_placement -effort high -timing_driven -incremental
create_placement -effort high -timing_driven -incremental
create_placement -effort high -timing_driven -incremental

place_opt

legalize_placement
```

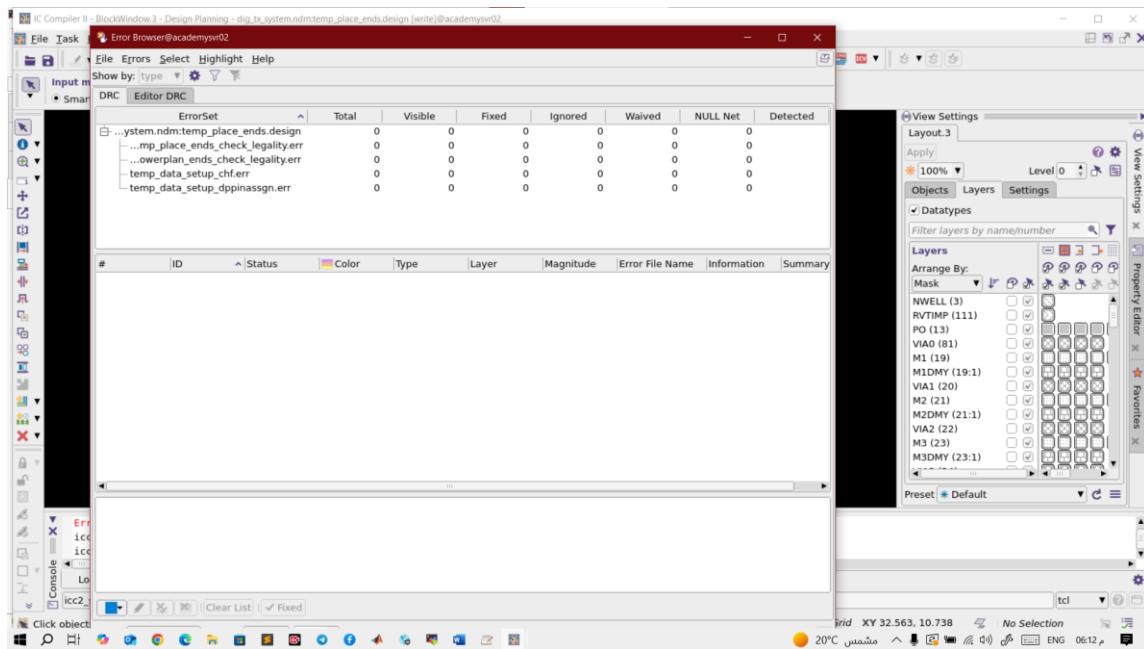
Then added tie cells. to insert tie cells (e.g., tie-high or tie-low cells) into the design. These cells are essential for ensuring proper logic functionality in cases where certain nets need to be fixed at a constant value (high or low).

```
#####
#####insert tie cells#####
add_tie_cells

legalize_placement -incremental
```

Placement reports:

Check DRC in GUI:



As shown in the figure, there are no reported errors in the design.

Legality check

```
*****
Report : Legality
*****  
  
VIOLATIONS BY CATEGORY:  
MOVABLE APP-FIXED USER-FIXED DESCRIPTION  
0 0 0 Two objects overlap.  
0 0 0 A cell violates a net.  
0 0 0 A cell is illegal at a site.  
0 0 0 A cell is not aligned with a site.  
0 0 0 A cell has an illegal orientation.  
0 0 0 A cell spacing rule is violated.  
0 0 0 A layer rule is violated.  
0 0 0 A cell is in the wrong region.  
0 0 0 Two cells violate cts margins.  
0 0 0 Two cells violate coloring.  
  
0 0 0 TOTAL  
  
TOTAL 0 Violations.
```

```

VIOLATIONS BY SUBCATEGORY:
    MOVABLE APP-FIXED USER-FIXED DESCRIPTION

        0      0      0  Two objects overlap.
        0      0      0  Two cells overlap.
        0      0      0  Two cells have overlapping keepout margins.
        0      0      0  A cell overlaps a blockage.
        0      0      0  A cell keepout margin overlaps a blockage.

        0      0      0  A cell violates a pnet.

        0      0      0  A cell is illegal at a site.
        0      0      0  A cell violates pin-track alignment rules.
        0      0      0  A cell is illegal at a site.
        0      0      0  A cell violates legal index rule.
        0      0      0  A cell has the wrong variant for its location.

        0      0      0  A cell is not aligned with a site.
        0      0      0  A cell is not aligned with the base site.
        0      0      0  A cell is not aligned with an overlaid site.

        0      0      0  A cell has an illegal orientation.

        0      0      0  A cell spacing rule is violated.
        0      0      0  A spacing rule is violated in a row.
        0      0      0  A spacing rule is violated between adjacent rows.
        0      0      0  A cell violates vertical abutment rule.
        0      0      0  A cell violates metal spacing rule.

        0      0      0  A layer rule is violated.
        0      0      0  A layer VTH rule is violated.
        0      0      0  A layer OD rule is violated.
        0      0      0  A layer OD max-width rule is violated.
        0      0      0  A layer ALL_OD corner rule is violated.
        0      0      0  A layer max-vertical-length rule is violated.
        0      0      0  A layer TPO rule is violated.
        0      0      0  Filler cell insertion cannot satisfy layer rules.

        0      0      0  A cell is in the wrong region.
        0      0      0  A cell is outside its hard bound.
        0      0      0  A cell is in the wrong voltage area.
        0      0      0  A cell violates an exclusive movebound.

        0      0      0  Two cells violate cts margins.

        0      0      0  Two cells violate coloring.

check_legality for block design dig_tx_system succeeded!

check_legality succeeded.

```

Don't have any violations, all cell legalized correctly.

Utilization

```

*****
Report : report_utilization
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Thu May 1 23:49:06 2025
*****
Utilization Ratio:          0.2184
Utilization options:
- Area calculation based on: site_row_of block temp_1_powerplan_ends
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                3196.9776
Total Capacity Area:       3196.9776
Total Area of cells:       698.3676
Area of excluded objects:
- hard_macros           : 0.0000
- macro_keepouts         : 0.0000
- soft_macros            : 0.0000
- io_cells               : 0.0000
- hard_blockages         : 0.0000
Total Area of excluded objects: 0.0000
Ratio of excluded objects:   0.0000

Utilization of site-rows with:
- Site 'unit':           0.2184

```

Qor snapshot

```
*****
Report      : create_qor_snapshot (place_qor_snp)
Design      : dig_tx_system
Version     : V-2023.12-SP5
Date        : Thu May  1 23:49:04 2025
Time unit   : 1.00ns
Resistance unit : 1.00kOhm
Capacitance unit: 1.00pF
Voltage unit  : 1.00V
Current unit   : 1.00uA
Power unit    : 1.00pW
Location      : /home/svgpasic25abkhaled/GP/pnr/flat/work/..
*****
No. of scenario = 2
s1 = func_fast
s2 = func_slow
-----
WNS of each timing group:           s1      s2
-----
SYS_GATED_CLK                      0.0784   0.0523
SPI_GATED_CLK                      -0.2210  -0.2320
ALL_VIOS                           -0.3027  -0.3137
SPI_CLK                            0.1442   0.1343
SYS_CLK                            0.0623   0.0358
-----
Setup WNS:                          -0.3027  -0.3137  -0.3137
Setup TNS:                          -2.8952  -2.9540  -2.9905
Number of setup violations:         28       28       28
Hold WNS:                           -0.2816  -0.2980  -0.2980
Hold TNS:                           -50.7484 -52.1894 -52.6215
Number of hold violations:          496      496      496
Number of max trans violations:    0         0         0
Number of max cap violations:      0         0         0
Number of min pulse width violations: 0         0         0
-----
Area:                               834.054
Cell count:                         1427
Buf/inv cell count:                 280
Std cell utilization:              0.2184
CPU(s):                             549
Mem(Mb):                            2112
Host name:                          academysvr02
```

Qor

```
Area
-----
Combinational Area:                332.56
Noncombinational Area:             365.81
Buf/Inv Area:                     67.13
Total Buffer Area:                24.55
Total Inverter Area:              42.58
Macro/Black Box Area:              0.00
Net Area:                          0
Net XLength:                       4259.53
Net YLength:                        3814.01
-----
Cell Area (netlist):               698.37
Cell Area (netlist and physical only): 834.05
Net Length:                        8073.54
```

Design Rules

```
-----
Total Number of Nets:              1455
Nets with Violations:             566
Max Trans Violations:              0
Max Cap Violations:                0
-----
```

There are 566 min capacitance DRC violation on nets because the require capacitance 0.0001 but there are 566 nets have capacitance less than required value.

Global timing

```
*****
Report : global timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Thu May 1 23:49:05 2025
*****  
  
Setup violations
-----  


|     | Total  | reg->reg | in->reg | reg->out | in->out |
|-----|--------|----------|---------|----------|---------|
| WNS | -0.314 | 0.000    | -0.232  | -0.314   | -0.162  |
| TNS | -2.990 | 0.000    | -2.515  | -0.314   | -0.162  |
| NUM | 28     | 0        | 26      | 1        | 1       |

  
Hold violations
-----  


|     | Total   | reg->reg | in->reg | reg->out | in->out |
|-----|---------|----------|---------|----------|---------|
| WNS | -0.298  | -0.298   | 0.000   | 0.000    | 0.000   |
| TNS | -52.622 | -52.622  | 0.000   | 0.000    | 0.000   |
| NUM | 496     | 496      | 0       | 0        | 0       |


```

The number of violations has decreased significantly (38 → 28), and WNS is less negative, indicating improved setup timing performance in the new report.

Both the number of violations (549 → 496) and the total negative slack (TNS) have improved in the new report, suggesting better hold timing closure.

4)CTS

Clock tree synthesis is a very important and critical stage. It involves checking the design readiness for CTS, specifying the CTS options, compiling the clock tree and optimizing it. The first step is performed using the command `check_design-stage pre_clock_opt`.

Not contain any errors

```
Running mega-check 'pre_clock_tree_stage':
  Running atomic-check 'design_mismatch'
  Running atomic-check 'scan_chain'
  Running atomic-check 'mv_design'
  Running atomic-check 'legality'
  Running atomic-check 'timing'
  Running atomic-check 'clock_trees'
  Running atomic-check 'hier_pre_clock_tree'

*** EMS Message summary ***
-----

| Rule    | Type | Count | Message                                                              |
|---------|------|-------|----------------------------------------------------------------------|
| DFT-011 | Info | 1     | The design has no scan chain defined in the scandef.                 |
| TCK-001 | Warn | 47    | The reported endpoint '%endpoint' is unconstrained. Reason: '%re ... |


Total 48 EMS messages : 0 errors, 47 warnings, 1 info.

*** Non-EMS message summary ***
-----

| Rule    | Type | Count | Message                                                              |
|---------|------|-------|----------------------------------------------------------------------|
| CTS-101 | Info | 1     | %s will work on the following scenarios.                             |
| CTS-107 | Info | 1     | %s will work on all clocks in active scenarios, including %d mas ... |
| CTS-973 | Info | 1     | The value of option cts.compile.enable_cell_relocation has been ...  |
| NEX-001 | Warn | 1     | Technology layer '%s' setting '%s' is not valid                      |
| PDC-003 | Warn | 4     | Routing direction of metal layer %s is neither "horizontal" nor ...  |
| PVT-032 | Info | 2     | Corner %s: <b>no</b> PVT mismatches.                                 |
| TIM-124 | Info | 1     | RDE mode is turned %s.                                               |


Total 11 non-EMS messages : 0 errors, 5 warnings, 6 info.

Warning: EMS database "check_design.ems" already exists, over-writing it. (EMS-040)
Information: EMS database is saved to file 'check_design.ems'.
Information: Non-EMS messages are saved into file 'check_design2025May01235433.log'.
```

Then I set some option to guide the tool in building the clock tree synthesis . These settings focus on improving timing and hold violations by enhancing the clock network and optimizing cell relocation and skew management

```
set_app_options -name cts.compile.enable_cell_relocation -value all
set_app_options -name cts.compile.size_pre_existing_cell_to_cts_references -value true
set_app_options -name cts.compile.timing_driven_sink_transition -value true
set_app_options -name clock_opt.flow.enable_ccd -value true
set_app_options -name ccd.timing_effort -value high
set_app_options -name cts.compile.enable_local_skew -value true
set_app_options -name ccd.hold_control_effort -value ultra
set_app_options -name opt.common.hold_effort -value high
set_app_options -name cts.compile.enable_global_route -value true
```

Then overwrite constrain again and reduce uncertainty.

```
#####
#####overwrite constraints
remove_clock_uncertainty -setup [all_clocks]
remove_clock_uncertainty -hold [all_clocks]
remove_clock_transition [all_clocks]
remove_input_delay [all_inputs]
remove_output_delay [all_outputs]

set_input_delay -clock [get_clocks spi_gated_clk] 0.41 [remove_from_collection [all_inputs] [get_ports "i_dig_tx_system_clk32 i_dig_tx_system_clk26"]]

set_output_delay -clock [get_clocks sys_gated_clk] 0.41 [get_ports o_dig_tx_system_data_out]
set_output_delay -clock [get_clocks sys_gated_clk] 0.41 [get_ports o_dig_tx_system_crc_valid]
set_output_delay -clock [get_clocks sys_clock] 0.41 [get_ports o_dig_tx_system_regfile_valid]
set_output_delay -clock [get_clocks sys_clock] 0.41 [get_ports o_dig_tx_system_output_valid]
set_output_delay -clock [get_clocks spi_gated_clk] 0.41 [get_ports o_dig_tx_system_data_slave_out]
set_output_delay -clock [get_clocks sys_clock] 0.41 [get_ports o_dig_tx_system_done]
set_output_delay -clock [get_clocks spi_gated_clk] 0.41 [get_ports o_dig_tx_system_miso_ena]
set_output_delay -clock [get_clocks spi_gated_clk] 0.41 [get_ports o_dig_tx_system_miso]

set_clock_uncertainty -setup 0.305 [all_clocks]
set_clock_uncertainty -hold 0.151 [all_clocks]
```

I give buffer and inverter to tool with flavor SLVT and LVT.

```
#####
#####Set_Clock_Tree_References
set_lib_cell_purpose -include cts {*/SAEDLVT14_INV_S_1 */SAEDLVT14_INV_S_2 */SAEDLVT14_INV_S_4 */SAEDLVT14_INV_S_8 */SAEDLVT14_INV_S_16 */SAEDLVT14_INV_S_20 \
*/SAEDLVT14 BUF_S_2 */SAEDLVT14_BUF_S_4 */SAEDLVT14_BUF_S_6 */SAEDLVT14_BUF_S_8 */SAEDLVT14_BUF_S_16 */SAEDLVT14_BUF_S_20 \
*/SAEDSLVT14_INV_S_1 */SAEDSLVT14_INV_S_2 */SAEDSLVT14_INV_S_4 */SAEDSLVT14_INV_S_8 */SAEDSLVT14_INV_S_16 */SAEDSLVT14_INV_S_20 \
*/SAEDSLVT14_BUF_S_2 */SAEDSLVT14_BUF_S_4 */SAEDSLVT14_BUF_S_6 */SAEDSLVT14_BUF_S_8 */SAEDSLVT14_BUF_S_16 */SAEDSLVT14_BUF_S_20 }
```

CTS reports:

Checking DRC

ErrorSet	Total	Visible	Fixed	Ignored	Waived	NULL Net	Detected
/home/svgasic25abkhaled/GP/pnr/flat/results/dig_tx_system.nndm:dig_tx_system_5_clock_ends.design	0	0	0	0	0	0	0
- DRC_report_by_check_pg.drc	0	0	0	0	0	0	0
- _temp_place_ends_check_legality.err	0	0	0	0	0	0	0
- _temp_1_powerplan_ends_check_legality.err	0	0	0	0	0	0	0
- temp_data_setup_chf.err	0	0	0	0	0	0	0
- temp_data_setup_dppinassgn.err	0	0	0	0	0	0	0
- temp_data_setup_dpplace.err	0	0	0	0	0	0	0
- temp_floorplan_ends_floating.err	0	0	0	0	0	0	0
- temp_floorplan_ends_missingVia.err	0	0	0	0	0	0	0
- temp_place_ends_floatingPG.err	0	0	0	0	0	0	0
- temp_1_powerplan_ends_floatingPG.err	0	0	0	0	0	0	0

Don't have any DRC errors in CTS stage

Checking legality after place CTS

```

TOTAL 0 Violations.

VIOLATIONS BY SUBCATEGORY:
    MOVABLE   APP-FIXED   USER-FIXED   DESCRIPTION
        0       0       0   Two objects overlap.
        0       0       0   Two cells overlap.
        0       0       0   Two cells have overlapping keepout margins.
        0       0       0   A cell overlaps a blockage.
        0       0       0   A cell keepout margin overlaps a blockage.

        0       0       0   A cell violates a pnet.

        0       0       0   A cell is illegal at a site.
        0       0       0   A cell violates pin-track alignment rules.
        0       0       0   A cell is illegal at a site.
        0       0       0   A cell violates legal index rule.
        0       0       0   A cell has the wrong variant for its location.

        0       0       0   A cell is not aligned with a site.
        0       0       0   A cell is not aligned with the base site.
        0       0       0   A cell is not aligned with an overlaid site.

        0       0       0   A cell has an illegal orientation.

        0       0       0   A cell spacing rule is violated.
        0       0       0   A spacing rule is violated in a row.
        0       0       0   A spacing rule is violated between adjacent rows.
        0       0       0   A cell violates vertical abutment rule.
        0       0       0   A cell violates metal spacing rule.

        0       0       0   A layer rule is violated.
        0       0       0   A layer VTH rule is violated.
        0       0       0   A layer OD rule is violated.
        0       0       0   A layer OD max-width rule is violated.
        0       0       0   A layer ALL_OD corner rule is violated.
        0       0       0   A layer max-vertical-length rule is violated.
        0       0       0   A layer TPO rule is violated.
        0       0       0   Filler cell insertion cannot satisfy layer rules.

        0       0       0   A cell is in the wrong region.
        0       0       0   A cell is outside its hard bound.
        0       0       0   A cell is in the wrong voltage area.
        0       0       0   A cell violates an exclusive movebound.

        0       0       0   Two cells violate cts margins.

        0       0       0   Two cells violate coloring.

check_legality for block design dig_tx_system succeeded!

```

Qor

```

*****
Report : qor
          -summary
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May 2 00:15:19 2025
*****  

Timing
-----
Context           WNS      TNS      NVE
func_fast        (Setup)  -0.37   -6.71     28
func_slow        (Setup)  -0.38   -6.93     78
Design           (Setup)  -0.38   -6.93     78  

func_fast        (Hold)   -0.17   -1.47     60
func_slow        (Hold)   -0.17   -1.42     35
Design           (Hold)   -0.17   -1.48     61  

-----  

Miscellaneous
-----
Cell Area (netlist):          1754.29
Cell Area (netlist and physical only): 1889.97
Nets with DRC Violations: 1436
1

```

Report constrains

```

Mode: func Corner: slow
Scenario: func_slow
-----
Number of max_transition violation(s): 0

Mode: func Corner: slow
Scenario: func_slow
max_capacitance
Net           Required Capacitance   Actual Capacitance   Slack   Violation
-----          0.04                  0.00            0.04 (MET)

-----
Number of max_capacitance violation(s): 0

Mode: func Corner: slow
Scenario: func_slow
min_capacitance
Net           Required Capacitance   Actual Capacitance   Slack   Violation
-----          0.00                  0.00            0.00 (MET)

-----
Number of min_capacitance violation(s): 0

Mode: func
Corner: slow
Scenario: func_slow

-----
Number of min_pulse_width violation(s): 0
Total number of violation(s): 0

```

Qor snapshot

```

*****
No. of scenario = 2
s1 = func_fast
s2 = func_slow
-----
WNS of each timing group:           s1      s2
-----
SYS_GATED_CLK                      -       -0.0040
SPI_GATED_CLK                      -0.2437 -0.2462
ALL_VIOS                           -0.3740 -0.3772
SPI_CLK                            0.1642  0.1631
SYS_CLK                            -       -0.0036
-----
Setup WNS:                          -0.3740 -0.3772 -0.3772
Setup TNS:                          -6.7130 -6.9273 -6.9273
Number of setup violations:         28      78      78
Hold WNS:                           -0.1660 -0.1677 -0.1677
Hold TNS:                           -1.4671 -1.4198 -1.4774
Number of hold violations:          60      35      61
Number of max trans violations:    0       0       0
Number of max cap violations:     0       0       0
Number of min pulse width violations: 0       0       0
-----
Area:                               1889.975
Cell count:                         4349
Buf/inv cell count:                 3204
Std cell utilization:               0.5487
CPU(s):                             1483
Mem(Mb):                            2788
Host name:                          academysvr02
-----
Histogram:                         s1      s2
-----
Max violations:                    28      78
  above ~ -0.7 --- 0 0
  -0.6 ~ -0.7 --- 0 0
  -0.5 ~ -0.6 --- 0 0
  -0.4 ~ -0.5 --- 0 0
  -0.3 ~ -0.4 --- 1 1
  -0.2 ~ -0.3 --- 26 26
  -0.1 ~ -0.2 --- 1 1
  0 ~ -0.1 --- 0 50
-----
Min violations:                    60      35
  -0.06 ~ above --- 3 3
  -0.05 ~ -0.06 --- 2 2
  -0.04 ~ -0.05 --- 1 1
  -0.03 ~ -0.04 --- 6 6
  -0.02 ~ -0.03 --- 4 4
  -0.01 ~ -0.02 --- 1 1
  0 ~ -0.01 --- 38 13

```

Global timing

```
*****
Report : global timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Fri May 2 00:15:20 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.377	-0.011	-0.246	-0.377	-0.184
TNS	-6.927	-0.143	-6.224	-0.377	-0.184
NUM	78	50	26	1	1

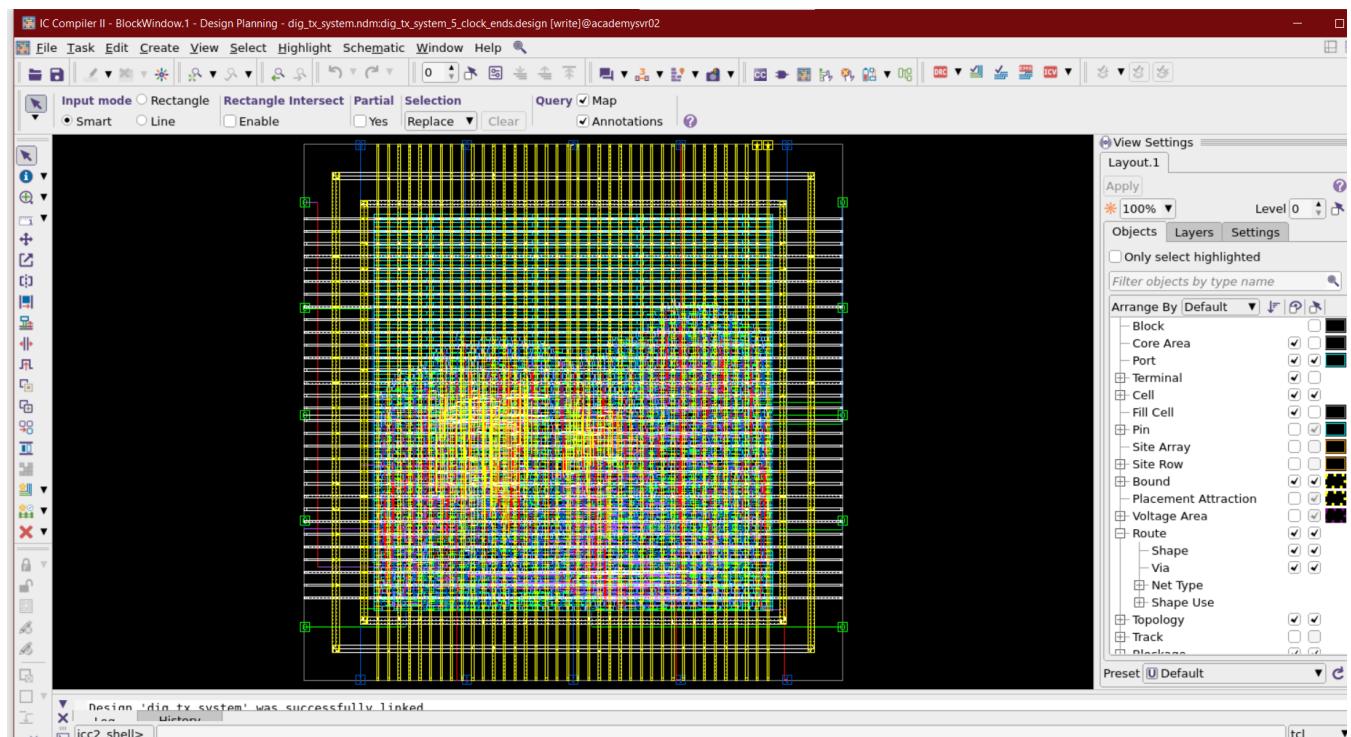
Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.168	-0.168	0.000	0.000	0.000
TNS	-1.477	-1.477	0.000	0.000	0.000
NUM	61	61	0	0	0

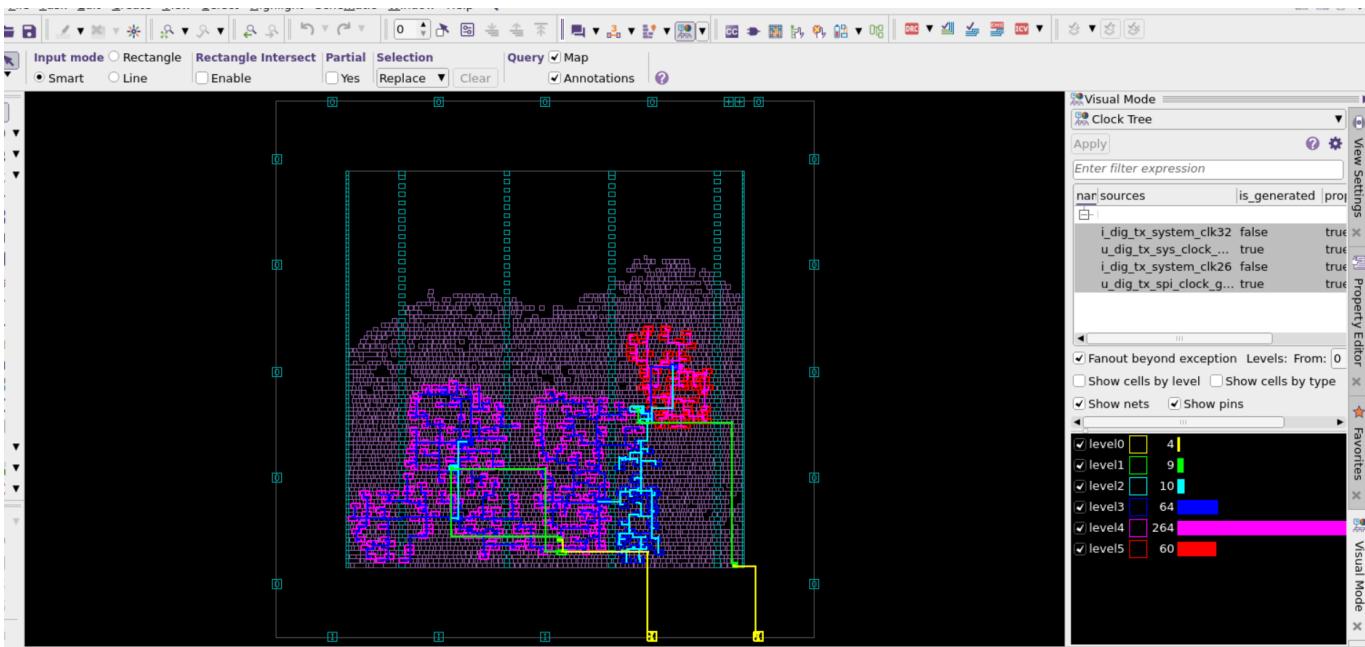
Setup Timing has shown considerable improvement after optimization, reducing both violations and negative slack. Hold Timing has improved significantly in terms of negative slack (TNS), though the number of violations has increased. The increased effort on hold optimization (via ultra hold control effort) likely contributed to this result.

There are a lot of violations because I'm overwriting constraints with high inputs and outputs delays and uncertainty. This violation will be solved in primetime and routing.

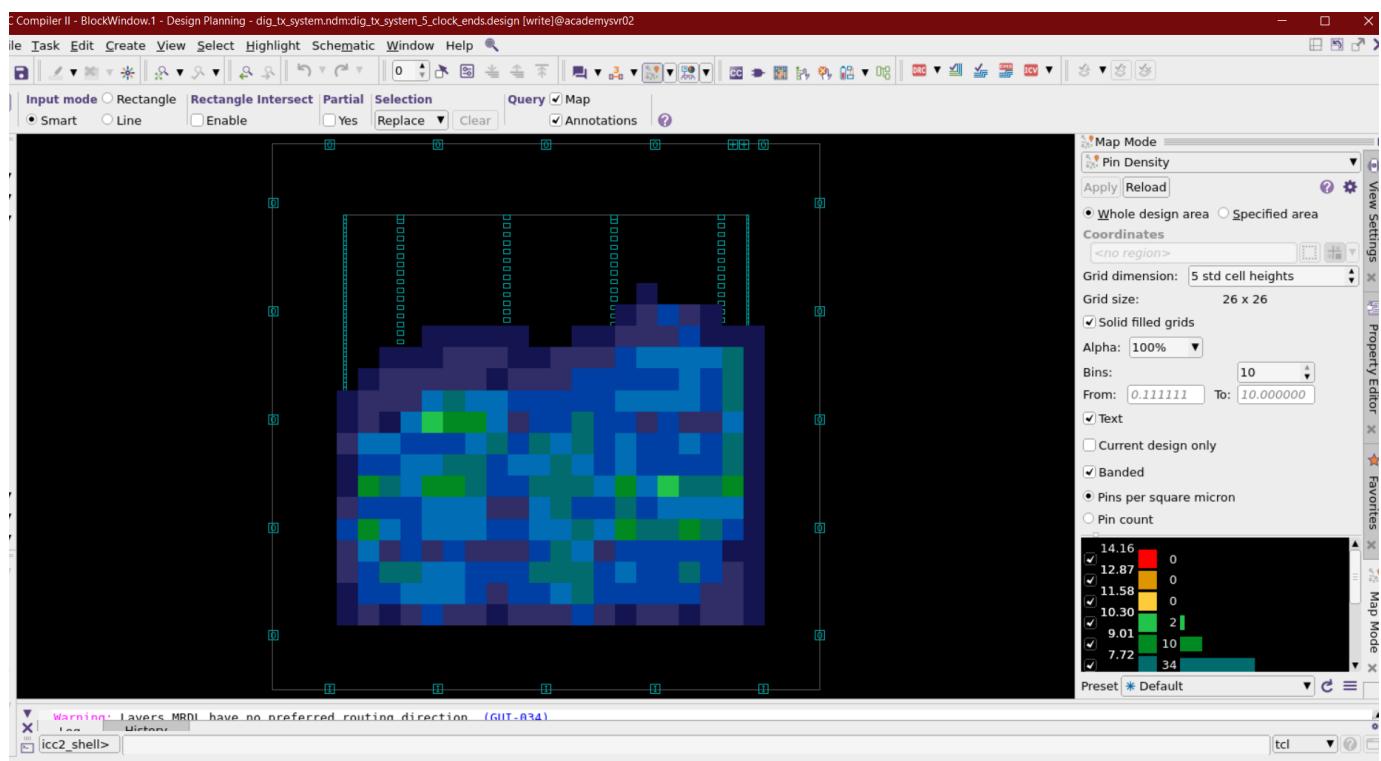
The clock ends design block shown in the next figure.



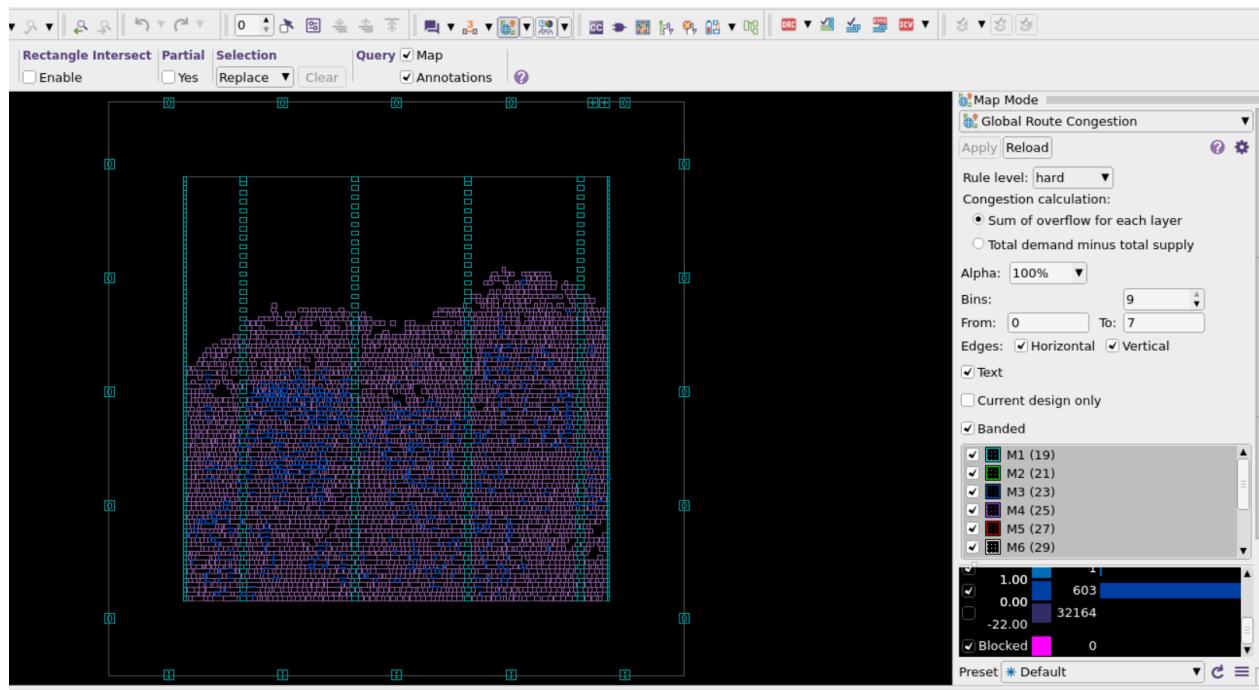
the clock tree in next figure



Pin density



The global routing Congestion which is not high



5)routing

The physical design is now ready to be routed after completing the core clock network without any timing or DRC violations. However, before proceeding to the routing stage, we must first check for congestion so that the tool can route efficiently. In the post-CTS stage, the resultant congestion is nearly 0% in both vertical and horizontal directions.

First, check design in stage before routing to ensure that I don't have any errors.

```
*****  
Report : check_design  
Options: { pre_route_stage }  
Design : dig_tx_system  
Version: V-2023.12-SP5  
Date  : Fri May 2 00:20:43 2025  
*****  
  
Running mega-check 'pre_route_stage':  
  Running atomic-check 'design_mismatch'  
  Running atomic-check 'scan_chain'  
  Running atomic-check 'my_design'  
  Running atomic-check 'timing'  
  Running atomic-check 'routability'  
  Running atomic-check 'hier_pre_route'  
  
*** EMS Message summary ***  
  
Rule      Type   Count   Message  
-----  
DFT-011  Info    1       The design has no scan chain defined in the scandef.  
TCK-001  Warn   47      The reported endpoint '%endpoint' is unconstrained. Reason: '%re ...  
  
Total 48 EMS messages : 0 errors, 47 warnings, 1 info.  
  
*** Non-EMS message summary ***  
  
Rule      Type   Count   Message  
-----  
CSTR-407  Warn  2260    Constrained %s '%s' is not in the design.  
NEX-001  Warn    1       Technology layer '%s' setting '%s' is not valid  
PVT-032  Info    2       Corner %s: no PVT mismatches.  
TIM-124  Info    1       RDE mode is turned %s.  
ZRT-022  Warn    1       Cannot find a default contact code for layer %s.  
ZRT-025  Warn    1       Layer %s does not have a preferred direction, assigning to %s.  
ZRT-026  Warn    7       Layer %s default pitch %.3f may be too small to handle up/down v ...  
ZRT-044  Warn    1       Standard cell pin %s/%s has no valid via regions.  
ZRT-619  Info    1       Via ladder engine would be activated for pattern must join conne ...  
ZRT-703  Info    1       Option route.detail.force_end_on_preferred_grid will be ignored ...  
ZRT-706  Info    1       When applicable layer based tapering will taper up to %.2f in di ...  
ZRT-707  Info    1       When applicable Min-max layer allow_pin_connection mode will all ...  
ZRT-718  Info    1       When applicable Min-max layer allow_pin_connection mode will all ...  
ZRT-761  Warn    1       pin is off track in the region (%.4f %.4f) (%.4f %.4f) on layer %s.  
  
Total 2280 non-EMS messages : 0 errors, 2272 warnings, 8 info.
```

Now I return constrains to it's original value as synthesis

```
remove_clock_uncertainty -setup [all_clocks]  
remove_clock_uncertainty -hold [all_clocks]  
remove_clock_transition [all_clocks]  
remove_input_delay [all_inputs]  
remove_output_delay [all_outputs]  
  
set_input_delay -clock [get_clocks spi_gated_clk] 0.40 [remove_from_collection [all_inputs] [get_ports "i_dig_tx_system_clk32 i_dig_tx_system_clk26"]]  
set_output_delay -clock [get_clocks sys_gated_clk] 0.40 [get_ports o_dig_tx_system_data_out]  
set_output_delay -clock [get_clocks sys_gated_clk] 0.40 [get_ports o_dig_tx_system_crc_valid]  
set_output_delay -clock [get_clocks sys_clock] 0.40 [get_ports o_dig_tx_system_regfile_valid]  
set_output_delay -clock [get_clocks sys_clock] 0.40 [get_ports o_dig_tx_system_output_valid]  
set_output_delay -clock [get_clocks spi_gated_clk] 0.40 [get_ports o_dig_tx_system_data_slave_out]  
set_output_delay -clock [get_clocks sys_clock] 0.40 [get_ports o_dig_tx_system_done]  
set_output_delay -clock [get_clocks spi_gated_clk] 0.40 [get_ports o_dig_tx_system_miso_ena]  
set_output_delay -clock [get_clocks spi_gated_clk] 0.40 [get_ports o_dig_tx_system_miso]  
  
set_clock_uncertainty -setup 0.300 [all_clocks]  
set_clock_uncertainty -hold 0.150 [all_clocks]
```

I performed routing using route_opt with up to 1000 optimization iterations. After routing, I checked the routability and evaluated DRCs. If any violations were detected, I re-optimized the design. In cases where DRCs persisted, I reverted to the placement stage to address the issues before re-routing. I followed this iterative loop to systematically resolve all DRCs and ensure clean routing.

```

route_opt
#route_opt
#####
#####Connecting_power/Ground_Nets_And_Pins
connect_pg_net -net VDD [get_pins -physical_context */VDD]
connect_pg_net -net VSS [get_pins -physical_context */VSS]

optimize_routes -max_detail_route_iterations 10000

check_lvs -max_errors 10000 > "../reports/routing/check_lvs.rpt"

```

The most frequent DRC encountered was "pin off track." To address this, I applied several methods. First, I disabled crosstalk optimization during global routing by setting the global route crosstalk option to false. After that, I re-ran pin placement to align the pins properly with the routing tracks.

```

set_app_options -name route.global.effort_level -value ultra
set_app_options -name route.global.timing_driven -value true
set_app_options -name route.global.timing_driven_effort_level -value high
#set_app_options -name route.global.crosstalk_driven -value true

```

routing reports

Check LVS

```

=====
Maximum number of violations is set to 10000
Abort checking when more than 10000 violations are found
All violations might not be found.
=====
Total number of input nets is 3287.
Total number of short violations is 0.
Total number of open nets is 0.
Total number of floating route violations is 0.

Elapsed = 0:00:02, CPU = 0:00:01

```

Check_routability

```

=====
== Check for design ==
=====

>>> No net contains a large number of ports
>>> No port contains a large number of pins

=====
== Check for PG DPT on Track ==
=====
>>>> Number of PG rails cross even number of track: 0

=====
== Check for PG PreRoute setting ==
=====
No number_of_secondary_pg_pin_connections setting and skip checking

=====
== Check for pins ==
=====

>>>> No pin violations found

=====
== Check for the Cut Metal not on Preferred Grid ==
=====

=====
== Check for overlap of standard cells ==
=====

>>>> No overlap of standard cells found

```

```

=====
== Check for min-grid violations ==
=====

>>> No Library min-grid violations found
>>> No Design min-grid violations found
>>>> No min-grid violations found

=====
== Check for out-of-boundary ports ==
=====

>>>> No out-of-boundary error found

=====
== Check for blocked ports ==
=====

>>>> Port might be blocked by layer constraints - min/max and freeze layer settings
>>>> Port might be blocked by check port access
>>>> No blocked ports found
>>>> Net blocked by layer constraints - min/max and freeze layer settings
>>>> No blocked nets found

=====
== Check for shielding violations ==
=====

>>>> The following Non-PG net has a shape with shape_use_shield_route
>> No non-PG net has a shape with shape_use_shield_route.

```

Check routes

```

Total number of nets = 3287, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
          0 ports without pins of 0 cells connected to 0 nets
          0 ports of 0 cover cells connected to 0 non-pg nets
Total number of DRCs = 0
Total number of antenna violations = no antenna rules defined
Total number of tie to rail violations = not checked
Total number of tie to rail directly violations = not checked

```

DRC

Error Set								
	Total	Visible	Fixed	Ignored	Waived	NULL Net	Detected	
/home/svgasic25abkhaled/GP/pnr/flat/results/dig_tx_system.ndm:dig_tx_system_6_complete.design	0	0	0	0	0	0	0	
- DRC_report_by_check_pg_drc	0	0	0	0	0	0	0	
- _temp_place_ends_check_legality.err	0	0	0	0	0	0	0	
- _temp_1_powerplan_ends_check_legality.err	0	0	0	0	0	0	0	
- check_routability.err	0	0	0	0	0	0	0	
- temp_clock_ends_lvs.err	0	0	0	0	0	0	0	
- temp_data_setup_chf.err	0	0	0	0	0	0	0	
- temp_data_setup_dppinassgn.err	0	0	0	0	0	0	0	
- temp_data_setup_dpplace.err	0	0	0	0	0	0	0	
- temp_floorplan_ends_floatingPG.err	0	0	0	0	0	0	0	
- temp_floorplan_ends_missingVia.err	0	0	0	0	0	0	0	
- temp_place_ends_floatingPG.err	0	0	0	0	0	0	0	
- temp_1_powerplan_ends_floatingPG.err	0	0	0	0	0	0	0	
- zroute.err	0	0	0	0	0	0	0	

#	ID	Status	Color	Type	Layer	Magnitude	Error File Name	Information	Summary

Qor snapshot

WNS of each timing group:	s1	s2
SYS_GATED_CLK	0.0128	0.0013
SPI_GATED_CLK	-0.2228	-0.2236
ALL_VIOS	-0.3026	-0.3038
SPI_CLK	0.1746	0.1743
SYS_CLK	0.0156	0.0025
Setup WNS:	-0.3026	-0.3038
Setup TNS:	-6.1421	-6.1639
Number of setup violations:	28	29
Hold WNS:	-0.1366	-0.1364
Hold TNS:	-0.4129	-0.4015
Number of hold violations:	36	4
Number of max trans violations:	0	0
Number of max cap violations:	0	0
Number of min pulse width violations:	0	0
Area:	1517.814	
Cell count:	3259	
Buf/inv cell count:	2114	
Std cell utilization:	0.4323	
CPU(s):	1813	
Mem(Mb):	2788	
Host name:	academysvr02	
Histogram:	s1	s2
Max violations:	28	29
above ~ -0.7	---	0 0
-0.6 ~ -0.7	---	0 0
-0.5 ~ -0.6	---	0 0
-0.4 ~ -0.5	---	0 0
-0.3 ~ -0.4	---	1 1
-0.2 ~ -0.3	---	26 26
-0.1 ~ -0.2	---	1 1
0 ~ -0.1	---	0 1
Min violations:	36	4
-0.06 ~ above	---	0 0
-0.05 ~ -0.06	---	0 0
-0.04 ~ -0.05	---	0 0
-0.03 ~ -0.04	---	0 0
-0.02 ~ -0.03	---	0 0
-0.01 ~ -0.02	---	0 0
0 ~ -0.01	---	33 1

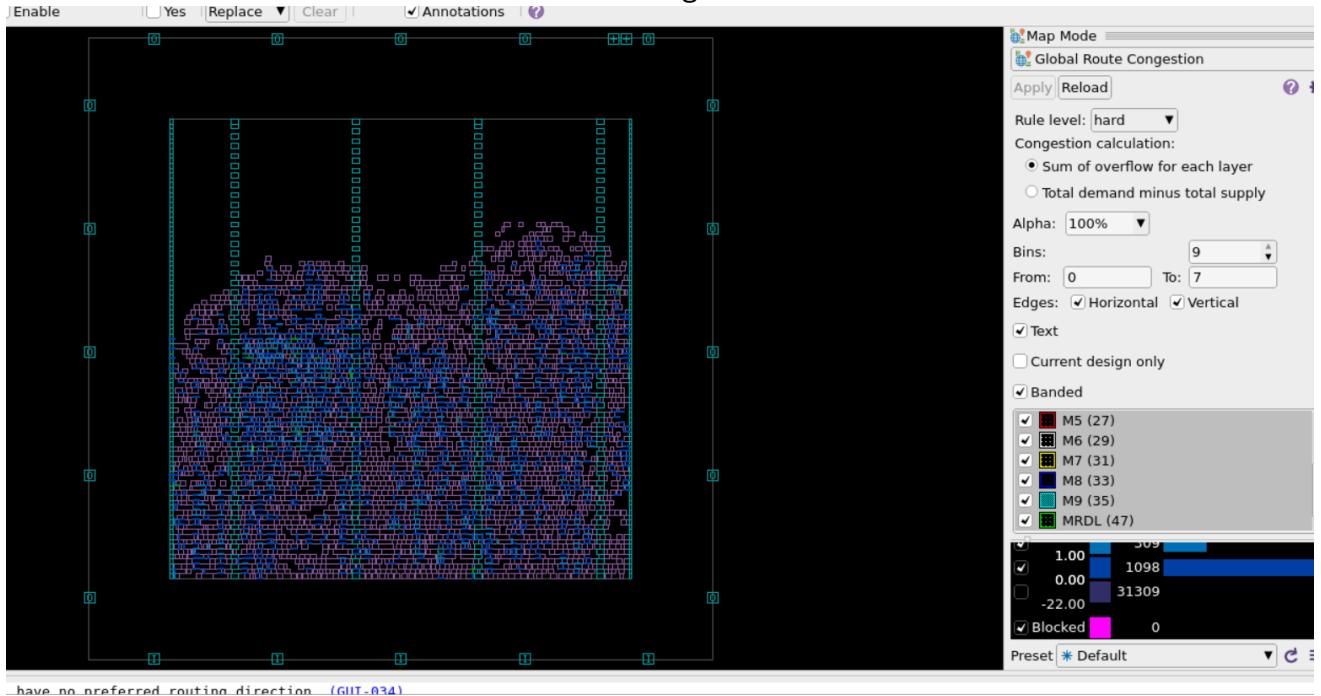
Global timing

Report : global timing					
=format { narrow }					
Design : dig_tx_system					
Version: V-2023.12-SP5					
Date : Fri May 2 00:54:19 2025					

Setup violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.304	-0.000	-0.224	-0.304	-0.144
TNS	-6.164	-0.000	-5.716	-0.304	-0.144
NUM	29	1	26	1	1

Hold violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.137	-0.137	0.000	0.000	0.000
TNS	-0.413	-0.413	0.000	0.000	0.000
NUM	36	36	0	0	0

Congestion



Acceptable value.

```
*****
Report : congestion
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May  2 00:54:11 2025
*****
```

Layer Name	overflow total	max	# GRCs has overflow (%)	max overflow
Both Dirs	1157	6	(2.63%)	1
H routing	234	6	(1.03%)	1
V routing	923	5	(4.24%)	1

6)primetime

In these steps, I take the output netlist from ICC2 along with the constraint file and proceed to run StarRC to generate the SPEF file. The extraction is performed for two operating corners: first, the slow corner at -40°C, and then the fast corner at 125°C.

```
CORNER_NAME: slow  
OPERATING_TEMPERATURE: -40  
TCAD_GRD_FILE: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/nxtgrd/saed14nm_1p9m_Cmax.nxtgrd  
  
CORNER_NAME: fast  
OPERATING_TEMPERATURE: 125  
TCAD_GRD_FILE: /home/tools/PDK/SAED14_EDK/SAED14nm_EDK_TECH_DATA/nxtgrd/saed14nm_1p9m_Cmin.nxtgrd
```

After generating the SPEF, I use it in PrimeTime for timing analysis, applying input and output delays of 200ps. Based on the timing violations, I perform ECO fixes and save the changes. These ECO changes are then brought back into ICC2 for legalization and routing. After completing the routing, I re-check timing and repeat the loop back to PrimeTime. I typically perform this loop four times to progressively close timing and ensure convergence.

I'm Starting with slow corner then save eco cell changes and source it in fast corner then source two scripts in icc2.

First Reading all slow libraries and netlist .

```
set Std_cell_lib "/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_HVT/liberty/nldm/base/saed14hvt_base_ss0p72vm40c.db \  
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_RVT/liberty/nldm/base/saed14rvt_base_ss0p72vm40c.db \  
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/base/saed14lvt_base_ss0p72vm40c.db \  
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_SLVT/liberty/nldm/base/saed14slvt_base_ss0p72vm40c.db \  
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_SLVT/liberty/nldm/cg/saed14slvt_cg_ss0p72vm40c.db \  
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_LVT/liberty/nldm/cg/saed14lvt_cg_ss0p72vm40c.db \  
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_HVT/liberty/nldm/cg/saed14hvt_cg_ss0p72vm40c.db \  
/home/tools/PDK/SAED14_EDK/SAED14nm_EDK_STD_RVT/liberty/nldm/cg/saed14rvt_cg_ss0p72vm40c.db "  
  
set link_path ** $Std_cell_lib  
  
#read_verilog "/home/svgasic25abkhaled/GP/pnr/flat/outputs/dig_tx_system_pt.v"  
read_verilog "/home/svgasic25abkhaled/GP/pnr/flat/outputs/dig_tx_system_pt_apt.v"  
  
current_design dig_tx_system  
link  
read_parasitics "/home/svgasic25abkhaled/GP/primetime/starrc/results/dig_tx_system.spef.slow"
```

The Global timing report in primetime before fixing

```
pt_shell> report_global_timing  
*****  
Report : global_timing  
      -format { narrow }  
Design : dig_tx_system  
Version: V-2023.12-SP5  
Date  : Fri May 2 22:38:57 2025  
*****  
  
Setup violations  
-----  
          Total  reg->reg  in->reg  reg->out  in->out  
-----  
WNS    -0.10    -0.00    -0.02    -0.10     0.00  
TNS    -0.22    -0.00    -0.11    -0.10     0.00  
NUM      10        2         7         1         0  
-----  
  
Hold violations  
-----  
          Total  reg->reg  in->reg  reg->out  in->out  
-----  
WNS    -0.12    -0.12     0.00     0.00     0.00  
TNS    -0.12    -0.12     0.00     0.00     0.00  
NUM      1         1         0         0         0  
-----
```

After run fixing setup by :

```
#Setup  
fix_eco_timing -type setup -methods {size_cell size_cell_side_load} -cell_type {combinational sequential}
```

The 20% of violation paths solved and Then the global timing report become as shown

```
Report : global_timing  
          -format { narrow }  
Design : dig_tx_system  
Version: V-2023.12-SP5  
Date   : Fri May 2 22:49:57 2025  
*****  
  
Setup violations  
-----  
      Total  reg->reg  in->reg  reg->out  in->out  
-----  
WNS    -0.10    0.00    -0.01    -0.10    0.00  
TNS    -0.20    0.00    -0.10    -0.10    0.00  
NUM      8        0        7        1        0  
-----  
  
Hold violations  
-----  
      Total  reg->reg  in->reg  reg->out  in->out  
-----  
WNS    -0.12    -0.12    0.00    0.00    0.00  
TNS    -0.12    -0.12    0.00    0.00    0.00  
NUM      1        1        0        0        0  
-----
```

The Worst hold path not solved by prime time so I solved it manually by inserting buffer.

The path before fixing

```
*****  
Report : timing  
          -path_type full  
          -delay_type min  
          -max_paths 1  
          -sort_by slack  
Design : dig_tx_system  
Version: V-2023.12-SP5  
Date   : Fri May 2 22:51:56 2025  
*****  
  
Startpoint: u_dig_tx_reg_file/reg_file_reg[0][0]  
           (rising edge-triggered flip-flop clocked by sys_clock)  
Endpoint: u_dig_tx_sys_clock_gating/enable_latch_reg  
           (negative level-sensitive latch clocked by sys_clock)  
Path Group: SYS_CLK  
Path Type: min  
  
Point                      Incr      Path  
-----  
clock sys_clock (rise edge)      1.00      1.00  
clock network delay (ideal)    0.00      1.00  
u_dig_tx_reg_file/reg_file_reg[0][0]/CK (SAEDSLVT14_FDPRBQ_V2_1)  
           0.00      1.00 r  
u_dig_tx_reg_file/reg_file_reg[0][0]/Q (SAEDSLVT14_FDPRBQ_V2_1)  
           0.03 &  1.03 f  
u_dig_tx_sys_clock_gating/enable_latch_reg/D (SAEDSLVT14_LDNQ_3)  
           0.00 &  1.03 f  
data arrival time                1.03  
  
clock sys_clock (rise edge)      1.00      1.00  
clock network delay (ideal)    0.00      1.00  
clock reconvergence pessimism  0.00      1.00  
clock uncertainty               0.15      1.15  
u_dig_tx_sys_clock_gating/enable_latch_reg/G (SAEDSLVT14_LDNQ_3)  
           1.15 r  
library hold time                -0.00     1.15  
data required time              1.15  
-----  
data required time              1.15  
data arrival time                -1.03  
-----  
slack (VIOLATED)                -0.12
```

After fixing

Startpoint: u_dig_tx_reg_file/reg_file_reg[0][0]		
	(rising edge-triggered flip-flop clocked by sys_clock)	
Endpoint: u_dig_tx_sys_clock_gating/enable_latch_reg		
	(negative level-sensitive latch clocked by sys_clock)	
Path Group: SYS_CLK		
Path Type: min		
Point	Incr	Path
clock sys_clock (rise edge)	1.00	1.00
clock network delay (ideal)	0.00	1.00
u_dig_tx_reg_file/reg_file_reg[0][0]/CK (SAEDSLVT14_FDPRBQ_V2_1)	0.00	1.00 r
u_dig_tx_reg_file/reg_file_reg[0][0]/Q (SAEDSLVT14_FDPRBQ_V2_1) ←	0.03 &	1.03 f
U1/X (SAEDHVT14_BUF_1)	0.03 H	1.06 f
U2/X (SAEDHVT14_BUF_4)	0.04	1.10 f
U3/X (SAEDHVT14_BUF_4)	0.02	1.12 f
U4/X (SAEDHVT14_BUF_1)	0.03	1.16 f
u_dig_tx_sys_clock_gating/enable_latch_reg/D (SAEDSLVT14_LDNO_3)	0.00	1.16 f
data arrival time		1.16
clock sys_clock (rise edge)	1.00	1.00
clock network delay (ideal)	0.00	1.00
clock reconvergence pessimism	0.00	1.00
clock uncertainty	0.15	1.15
u_dig_tx_sys_clock_gating/enable_latch_reg/G (SAEDSLVT14_LDNO_3)		1.15 r
library hold time	-0.01	1.14
data required time		1.14
data required time		1.14
data arrival time		-1.16
slack (MET)		0.02

Then the global timing report

Setup violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.10	0.00	-0.01	-0.10	0.00
TNS	-0.20	0.00	-0.10	-0.10	0.00
NUM	8	0	7	1	0

No hold violations found.

Making the same in the minimum corner. Take the netlist from icc2 and constrains and take SPEF fast. Then try to solve the hold and setup violations.

the global timing report in prime time Before solving any paths

```
*****  
Report : global_timing  
    -format { narrow }  
Design : dig_tx_system  
Version: V-2023.12-SP5  
Date   : Fri May  2 07:22:00 2025  
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.07	0.00	-0.00	-0.07	0.00
TNS	-0.08	0.00	-0.01	-0.07	0.00
NUM	7	0	6	1	0

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.14	-0.14	0.00	0.00	0.00
TNS	-0.45	-0.45	0.00	0.00	0.00
NUM	47	47	0	0	0

The global time After solving hold paths

```
* pt_shell> report_global_timing  
*****  
Report : global_timing  
    -format { narrow }  
Design : dig_tx_system  
Version: V-2023.12-SP5  
Date   : Fri May  2 23:41:08 2025  
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.07	0.00	-0.00	-0.07	0.00
TNS	-0.08	0.00	-0.02	-0.07	0.00
NUM	9	0	8	1	0

No hold violations found.

After applying ECO changes for both fast and slow corners in PrimeTime, I return to ICC2 to place and route the ECO cells. Once the routing is complete, I generate a new SPEF and run another timing analysis in PrimeTime to verify the updates and ensure timing closure.

The global timing report in prime time in round 2 before fixing

```
pt_shell> report_global_timing
*****
Report : global_timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Sat May  3 01:33:28 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.16	0.00	0.00	-0.16	0.00
TNS	-0.16	0.00	0.00	-0.16	0.00
NUM	1	0	0	1	0

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.12	-0.12	0.00	0.00	0.00
TNS	-4.46	-4.46	0.00	0.00	0.00
NUM	64	64	0	0	0

After fixing some paths manually:

```
pt_shell> report_global_timing
*****
Report : global_timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Sat May  3 01:38:35 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.16	0.00	0.00	-0.16	0.00
TNS	-0.16	0.00	0.00	-0.16	0.00
NUM	1	0	0	1	0

No hold violations found.

And in fast corner the timing report after fixing

```
pt_shell> report_global_timing
*****
Report : global_timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Sat May  3 01:49:59 2025
*****  
  
Setup violations
-----
      Total  reg->reg  in->reg  reg->out  in->out
-----
WNS      -0.11      0.00      0.00      -0.11      0.00
TNS      -0.11      0.00      0.00      -0.11      0.00
NUM        1          0          0          1          0
-----  
  
No hold violations found.
```

I return to ICC2 to place and route the new ECO cells. I repeated this loop four times — transferring ECO changes between ICC2 and PrimeTime, updating placement and routing, regenerating SPEF, and re-running timing — until I achieved global timing closure in Primetime.

```
Lib dig_tx_system.ndm /home/svpgasic25abkhaled/GP/pnr/flat/results/dig
→ 0 dig_tx_system.design May-01-23:08
→ 0 dig_tx_system_1_data_setup.design May-01-23:08
→ 0 temp_data_setup.design May-01-23:09
→ 0 temp_floorplan_init.design May-01-23:08
→ 0 temp_floorplane.design May-01-23:08
→ 0 dig_tx_system_2_floorplan_ends.design May-03-12:11
→ 0 temp_floorplan_ends.design May-01-23:23
→ 0 dig_tx_system_3_powerplan_ends.design May-03-12:22
→ 0 temp_1_powerplan_ends.design May-01-23:51
→ 0 dig_tx_system_4_place_ends.design May-01-23:49
→ 0 temp_place_ends.design May-02-00:15
→ 0 dig_tx_system_5_clock_ends.design May-03-11:26
→ 0 temp_clock_ends.design May-02-00:54
→ 0 dig_tx_system_6_complete.design May-03-12:01
→ 0 temp_pt_route.design May-02-08:49
→ 0 dig_tx_system_7_complete_after_pt.design May-02-08:49
→ 0 dig_tx_system_8_complete_after_pt.design May-02-09:20
→ 0 temp_pt_route_round_2.design May-02-09:36
→ 0 dig_tx_system_9_complete_after_pt.design May-02-09:36
→ 0 temp_pt_1.design May-03-01:26
→ 0 dig_tx_system_7_complete_pt.design May-03-01:26
```

This is the final global timing report that I reached to it .

```
pt_shell> report_global_timing
*****
Report : global_timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May 2 09:28:20 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.31	0.00	0.00	-0.31	0.00
TNS	-0.31	0.00	0.00	-0.31	0.00
NUM	1	0	0	1	0

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.02	-0.02	0.00	0.00	0.00
TNS	-0.02	-0.02	0.00	0.00	0.00
NUM	1	1	0	0	0

All constrains:

Constraint	Cost
max_delay/setup	0.17 (VIOLATED)
min_delay/hold	0.00 (MET)
sequential_clock_pulse_width	0.00 (MET)
clock_tree_pulse_width	0.00 (MET)
max_capacitance	0.00 (MET)
min_capacitance	0.41 (VIOLATED)
max_transition	0.00 (MET)
max_fanout	0.00 (MET)

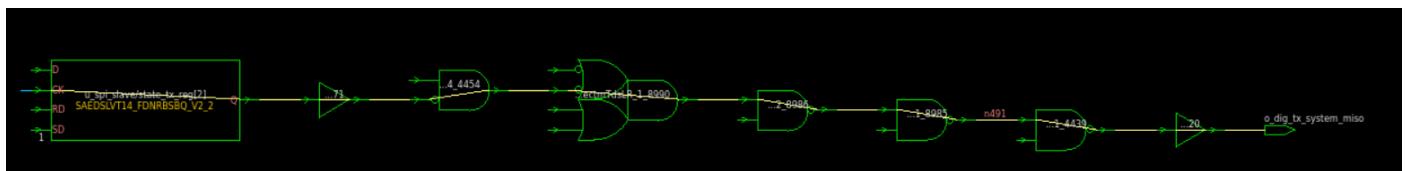
- 1) All constrains met except min capacitance due to actual capacitance is less than 0.001 but I will ignore this violation

```
pt_shell> report_constraints -all_violators -min_capacitance -significant_digits 5
*****
Report : constraint
    -all_violators
    -min_capacitance
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May  2 22:57:38 2025
*****
```

Pin	Required Capacitance	Actual Capacitance	Slack	
clockkopt_h_inst_21764/X	0.00100	0.00031	-0.00069	(VIOLATED)
clockkopt_gre_h_inst_21377/X	0.00100	0.00031	-0.00069	(VIOLATED)
clockkopt_h_inst_21744/X	0.00100	0.00033	-0.00067	(VIOLATED)
clockkopt_gre_h_inst_21010/X	0.00100	0.00034	-0.00066	(VIOLATED)
clockkopt_gre_h_inst_21293/X	0.00100	0.00035	-0.00065	(VIOLATED)
clockkopt_gre_h_inst_21253/X	0.00100	0.00036	-0.00064	(VIOLATED)
clockkopt_h_inst_21739/X	0.00100	0.00036	-0.00064	(VIOLATED)
clockkopt_gre_h_inst_21389/X	0.00100	0.00036	-0.00064	(VIOLATED)
clockkopt_gre_h_inst_21017/X	0.00100	0.00036	-0.00064	(VIOLATED)
clockkopt_gre_h_inst_21460/X	0.00100	0.00037	-0.00063	(VIOLATED)
clockkopt_gre_h_inst_21387/X	0.00100	0.00037	-0.00063	(VIOLATED)
clockkopt_h_inst_18148/X	0.00100	0.00038	-0.00062	(VIOLATED)
u_spi_slave/miso_reg_reg[6]/Q	0.00100	0.00038	-0.00062	(VIOLATED)
clockkopt_h_inst_21712/X	0.00100	0.00038	-0.00062	(VIOLATED)
clockkopt_h_inst_17689/X	0.00100	0.00038	-0.00062	(VIOLATED)
clockkopt_h_inst_18251/X	0.00100	0.00038	-0.00062	(VIOLATED)
clockkopt_h_inst_19916/X	0.00100	0.00038	-0.00062	(VIOLATED)
clockkopt_h_inst_21770/X	0.00100	0.00038	-0.00062	(VIOLATED)

- 2) There are 8 paths violation due to high input and output delay and uncertainty

The worst path slack



This path can't be solved due to large logic gate and output delay

- The design can work without any violation at input and output delay equal to 0.19999 ns without needing to fix it.

```
spt_shell> spt_shell> set_input_delay -clock [get_clocks spi_gated_clk] 0.19999 [remove_from_collection [all_inputs] [get_ports "i_dig_tx_system_clk32 i_dig_tx_system_clk26"]]
pt_shell> set_output_delay -clock [get_clocks sys_gated_clk] 0.19999 [get_ports o_dig_tx_system_data_out]
et_output_delay -clock [get_clocks sys_gated_clk] 0.19999 [get_ports o_dig_tx_system_crc_valid]
set_output_delay -clock [get_clocks sys_clock] 0.19999 [get_ports o_dig_tx_system_regfile_valid]
set_output_delay -clock [get_clocks sys_clock] 0.19999 [get_ports o_dig_tx_system_output_valid]
set_output_delay -clock [get_clocks spi_gated_clk] 0.19999 [get_ports o_dig_tx_system_data_slave_out]
set_output_delay -clock [get_clocks sys_clock] 0.19999 [get_ports o_dig_tx_system_done]
set_output_delay -clock [get_clocks spi_gated_clk] 0.19999 [get_ports o_dig_tx_system_miso_ena]
set_output_delay -clock [get_clocks spi_gated_clk] 0.19999 [get_ports o_dig_tx_system_miso]
```

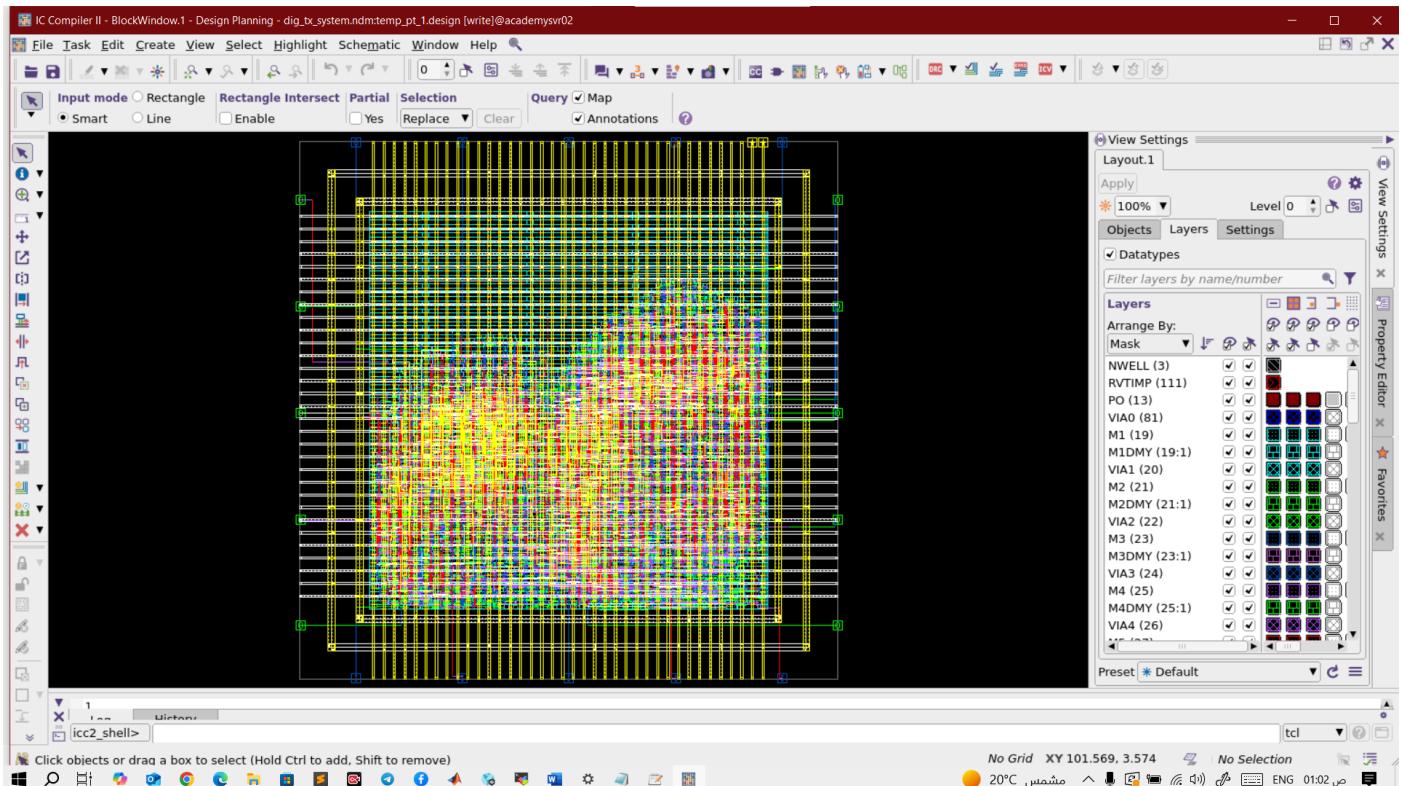
After making input and output delay 0.19999 ns the global timing report before any fixing is:

```
*****
Report : global_timing
        -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May 2 23:18:37 2025
*****  
  

No setup violations found.  
  

No hold violations found.  
1
```

The final chip is



No DRC as shown in the picture.

#	ID	Status	Color	Type	Layer	Magnitude	Error File Name	Information	Summary
1									

Chapter 4

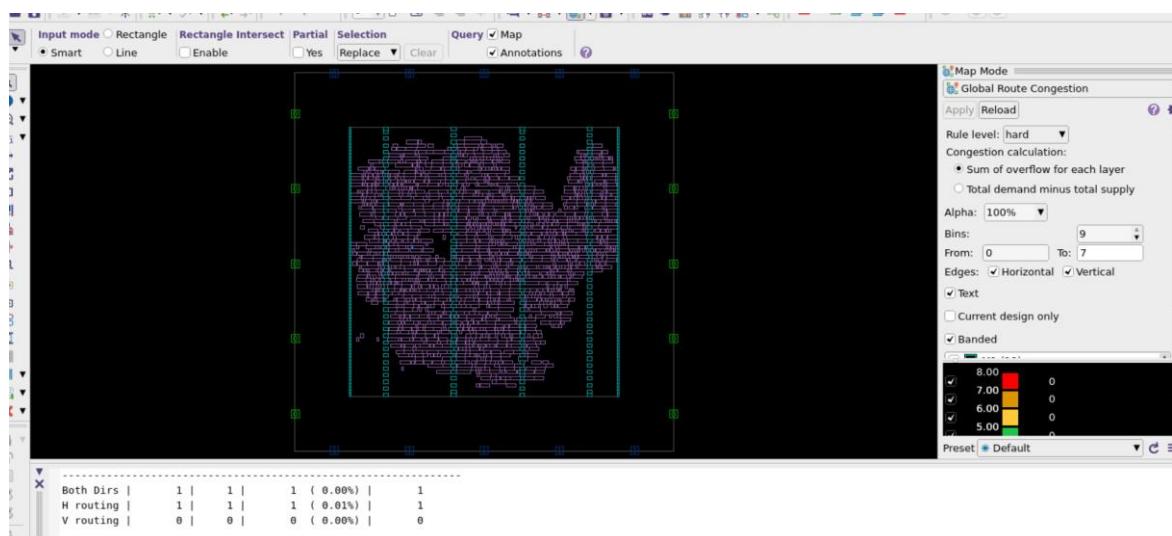
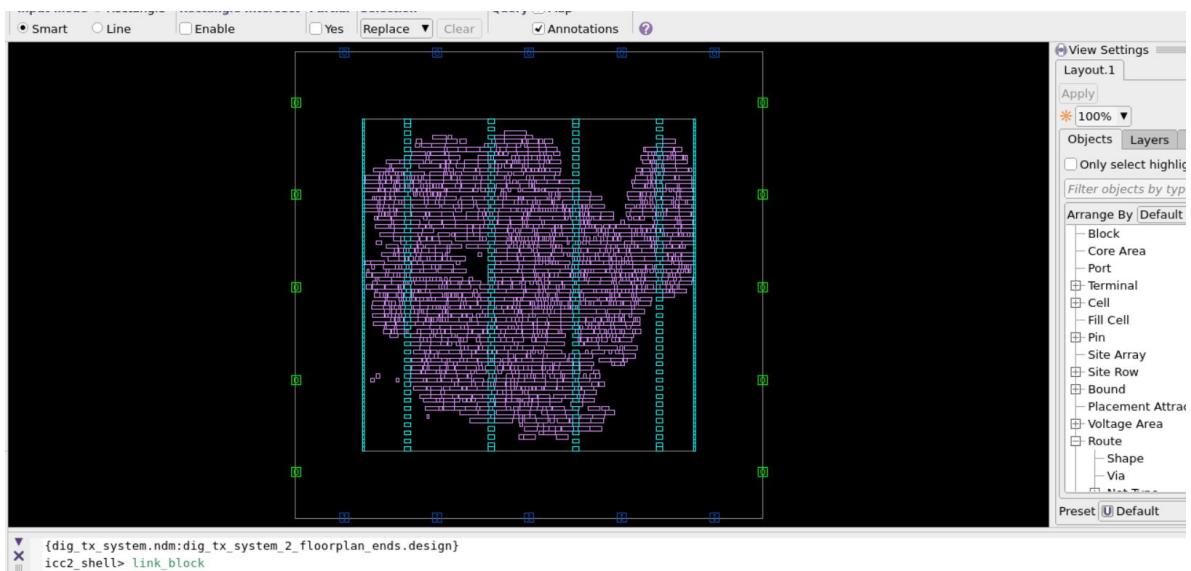
PNR in Hierarchical top down flow

1) floor planning

In this flow I will change the core utilization to 0.35 instead of 0.25

```
initialize_floorplan -core_utilization 0.35 -flip_first_row true \
                      -core_offset {10 10 10 10}
```

Following are figures for the floorplan , the QOR and the congestion map after this stage.



As shown in QOR report the worst setup slack is less than that in flat flow due to increase the utilization .

Timing				
Context		WNS	TNS	NVE
default	(Setup)	-0.43	-10.27	37
default::estimated_corner	(Setup)	-0.43	-10.27	37
Design	(Setup)	-0.43	-10.27	37
default	(Hold)	-0.18	-74.27	563
default::estimated_corner	(Hold)	-0.18	-74.27	563
Design	(Hold)	-0.18	-74.27	563

Miscellaneous			
Cell Area (netlist):		853.81	
Cell Area (netlist and physical only):		972.45	
Nets with DRC Violations:	0		
1			

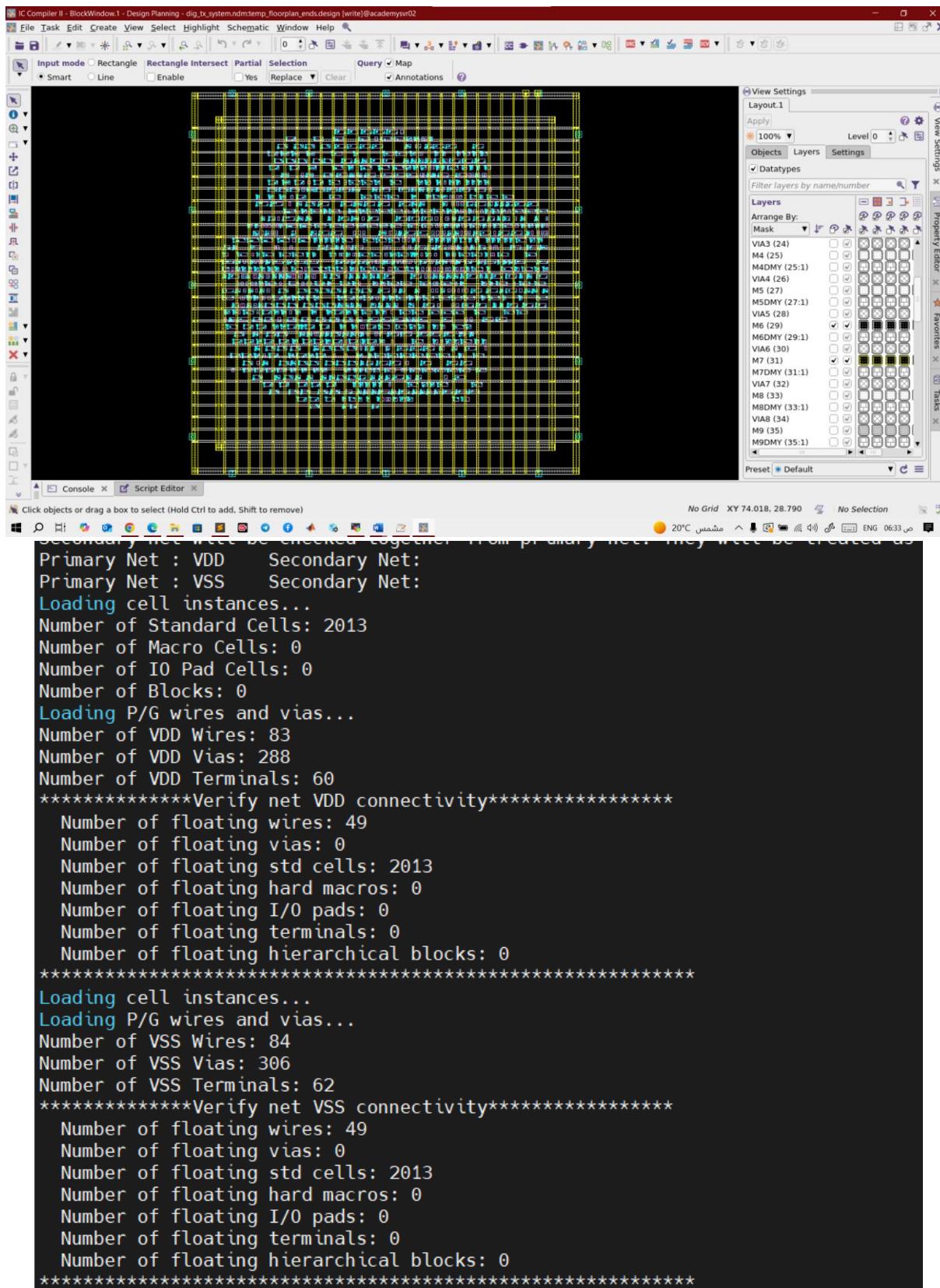
QOR.snapshot

WNS of each timing group:	s1	s2
INPUT	-0.3555	-0.3555
COMBO	-0.3191	-0.3191
OUTPUT	-0.4268	-0.4268
SPI_CLK	0.1185	0.1185
SYS_CLK	0.1175	0.1175
REG	-0.0143	-0.0143
Setup WNS:	-0.4268	-0.4268
Setup TNS:	-10.2675	-10.2675
Number of setup violations:	37	37
Hold WNS:	-0.1776	-0.1776
Hold TNS:	-74.2672	-74.2672
Number of hold violations:	563	563
Number of max trans violations:	0	0
Number of max cap violations:	0	0
Number of min pulse width violations:	0	0
Area:		972.449
Cell count:		1622
Buf/inv cell count:		366
Std cell utilization:		0.3516
CPU(s):		48
Mem(Mb):		1282
Host name:		academyvr02
Histogram:	s1	s2
Max violations:	37	37
above ~ -0.7	0	0
-0.6 ~ -0.7	0	0
-0.5 ~ -0.6	0	0
-0.4 ~ -0.5	1	1
-0.3 ~ -0.4	28	28
-0.2 ~ -0.3	0	0
-0.1 ~ -0.2	0	0
0 ~ -0.1	8	8
Min violations:	563	563
-0.06 ~ above	0	0
-0.05 ~ -0.06	0	0
-0.04 ~ -0.05	0	0
-0.03 ~ -0.04	0	0
-0.02 ~ -0.03	0	0
-0.01 ~ -0.02	0	0
0 ~ -0.01	0	0

2) power planning

For creating the power network, I used the top two metal layers to create the power straps then we connected the cells to the power rails. Using metals M6,M7. Create power mesh with different pitch to solve the new generated error.

Before solve floating nets and stander cells:



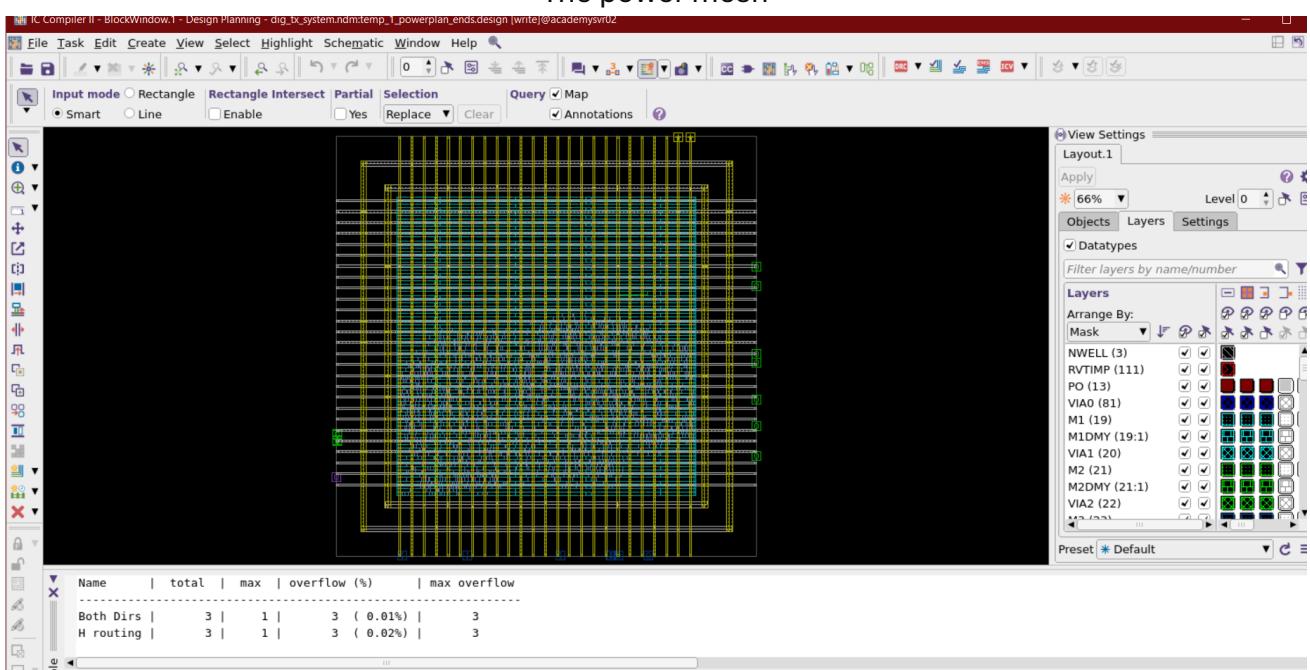
After adding vias and solve errors

```

icc2_shell> check_pg_connectivity
Checking secondary net through power switch is enabled.
Secondary net will be checked together from primary net. They will be treated as the same net
Primary Net : VDD      Secondary Net:
Primary Net : VSS      Secondary Net:
Loading cell instances...
Number of Standard Cells: 1830
Number of Macro Cells: 0
Number of IO Pad Cells: 0
Number of Blocks: 0
Loading P/G wires and vias...
Number of VDD Wires: 71
Number of VDD Vias: 3078
Number of VDD Terminals: 50
*****Verify net VDD connectivity*****
    Number of floating wires: 0
    Number of floating vias: 0
    Number of floating std cells: 0
    Number of floating hard macros: 0
    Number of floating I/O pads: 0
    Number of floating terminals: 0
    Number of floating hierarchical blocks: 0
*****
Loading cell instances...
Loading P/G wires and vias...
Number of VSS Wires: 72
Number of VSS Vias: 3256
Number of VSS Terminals: 54
*****Verify net VSS connectivity*****
    Number of floating wires: 0
    Number of floating vias: 0
    Number of floating std cells: 0
    Number of floating hard macros: 0
    Number of floating I/O pads: 0
    Number of floating terminals: 0
    Number of floating hierarchical blocks: 0
*****
Overall runtime: 0 seconds.
icc2_shell> check_pg_drc
Command check_pg_drc started at Sat May 3 14:48:09 2025
Command check_pg_drc finished at Sat May 3 14:48:09 2025
CPU usage for check_pg_drc: 0.45 seconds ( 0.00 hours)
Elapsed time for check_pg_drc: 0.45 seconds ( 0.00 hours)
No errors found.
icc2_shell>

```

The power mesh



QOR.snapshot

```
WNS of each timing group:          s1      s2
-----
INPUT                           -0.3555  -0.3555
COMBO                          -0.3191  -0.3191
OUTPUT                         -0.4268  -0.4268
SPI_CLK                        0.1185  0.1185
SYS_CLK                        0.1175  0.1175
REG                            -0.0143  -0.0143
-----
Setup WNS:                      -0.4268  -0.4268  -0.4268
Setup TNS:                      -10.2675 -10.2675 -10.2675
Number of setup violations:      37       37       37
Hold WNS:                       -0.1776  -0.1776  -0.1776
Hold TNS:                       -74.2672 -74.2672 -74.2672
Number of hold violations:      563     563     563
Number of max trans violations: 0        0        0
Number of max cap violations:   0        0        0
Number of min pulse width violations: 0        0        0
-----
Area:                           972.449
Cell count:                     1622
Buf/inv cell count:             366
Std cell utilization:           0.3516
CPU(s):                         85
Mem(Mb):                        1545
Host name:                      academysvr02
-----
Histogram:          s1    s2
-----
Max violations:      37    37
  above ~ -0.7    ---  0  0
  -0.6 ~ -0.7    ---  0  0
  -0.5 ~ -0.6    ---  0  0
  -0.4 ~ -0.5    ---  1  1
  -0.3 ~ -0.4    --- 28  28
  -0.2 ~ -0.3    ---  0  0
  -0.1 ~ -0.2    ---  0  0
  0 ~ -0.1      ---  8  8
-----
Min violations:      563   563
  -0.06 ~ above   ---  0  0
  -0.05 ~ -0.06   ---  0  0
  -0.04 ~ -0.05   ---  0  0
  -0.03 ~ -0.04   ---  0  0
  -0.02 ~ -0.03   ---  0  0
  -0.01 ~ -0.02   ---  0  0
  0 ~ -0.01      ---  0  0
```

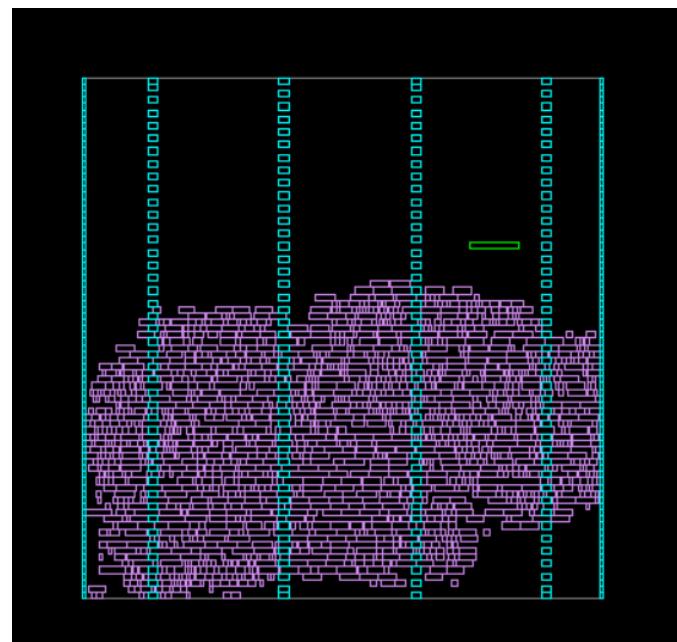
3)placement

After completing the placement stage, I ran a routability check and found six pins that were off-track on the M1 layer.

```
=====
=          Check for pins          =
=====
>>>> found 6 off track pins
```

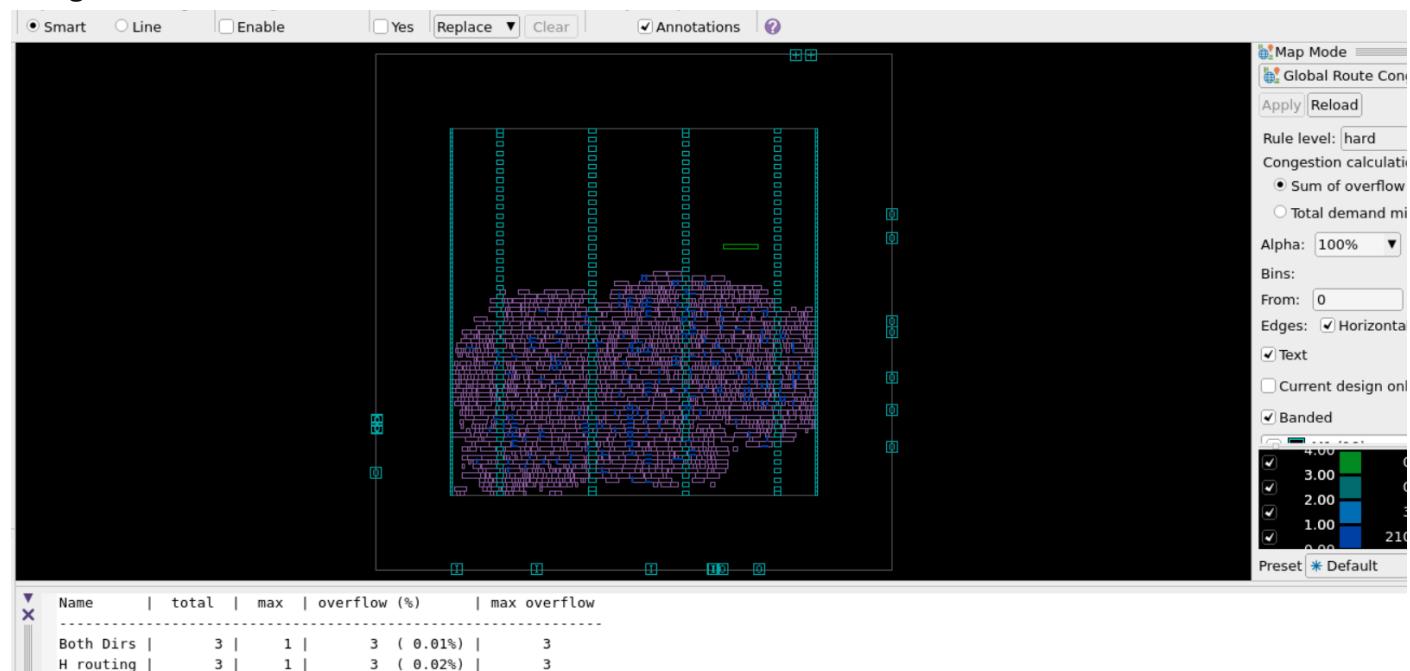
To resolve this, I first attempted to fix the issue by removing the affected tracks and regenerating them, followed by re-routing. This approach successfully corrected two of the pins. However, the remaining four pins continued to show errors. To fully resolve the issue, I created a placement blockage in that region and reran the placement, which successfully fixed the problem.

After solving by placement blockages



```
=====
Check for pins
=====
>>>>> No pin violations found
```

Congestion:



The utilization reduce to 0.31

```
*****  
Report : report_utilization  
Design : dig_tx_system  
Version: V-2023.12-SP5  
Date  : Fri May  2 08:27:43 2025  
*****  
Utilization Ratio: 0.3150  
Utilization options:  
- Area calculation based on: site_row of block temp_1_powerplan_ends  
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages  
Total Area: 2428.4136  
Total Capacity Area: 2428.4136  
Total Area of cells: 765.0564  
Area of excluded objects:  
- hard_macros : 0.0000  
- macro_keepouts : 0.0000  
- soft_macros : 0.0000  
- io_cells : 0.0000  
- hard_blockages : 0.0000  
Total Area of excluded objects: 0.0000  
Ratio of excluded objects: 0.0000  
Utilization of site-rows with:  
- Site 'unit': 0.3150
```

NO Logical DRC

```
Mode: func Corner: slow  
Scenario: func_slow  
-----  
Number of max_transition violation(s): 0  
  
Mode: func Corner: slow  
Scenario: func_slow  
-----  
Number of max_capacitance violation(s): 0  
  
Mode: func Corner: slow  
Scenario: func_slow  
-----  
Number of min_capacitance violation(s): 0  
  
Mode: func  
Corner: slow  
Scenario: func_slow  
-----  
Number of min_pulse_width violation(s): 0  
Total number of violation(s): 0
```

QOR.snapshot

WNS of each timing group:	s1	s2
SYS_GATED_CLK	0.0236	0.0105
SPI_GATED_CLK	-0.3068	-0.3171
SPI_CLK	0.1442	0.1342
SYS_CLK	0.0236	0.0005
Setup WNS:	-0.3068	-0.3171
Setup TNS:	-2.6994	-2.8181
Number of setup violations:	32	33
Hold WNS:	-0.2674	-0.2847
Hold TNS:	-54.0017	-55.5743
Number of hold violations:	558	526
Number of max trans violations:	0	0
Number of max cap violations:	0	0
Number of min pulse width violations:	0	0
Area:		883.693
Cell count:		1498
Buf/inv cell count:		292
Std cell utilization:		0.3150
CPU(s):		1928
Mem(Mb):		2405
Host name:		academysvr02
Histogram:	s1	s2
Max violations:	32	33
above ~ -0.7	---	0
-0.6 ~ -0.7	---	0
-0.5 ~ -0.6	---	0
-0.4 ~ -0.5	---	0
-0.3 ~ -0.4	---	1
-0.2 ~ -0.3	---	6
-0.1 ~ -0.2	---	2
0 ~ -0.1	---	23
	24	
Min violations:	558	526
-0.06 ~ above	---	2
-0.05 ~ -0.06	---	32
-0.04 ~ -0.05	---	0
-0.03 ~ -0.04	---	7
-0.02 ~ -0.03	---	25
-0.01 ~ -0.02	---	33
0 ~ -0.01	---	50
	39	31

4)CTS

Clock tree qor

```
*****
Report : clock qor
-type summary
Design : dig_tx_system
Version: V-2023.12-SP5
Date : Fri May 2 08:47:32 2025
*****  
  
Attributes  
=====  
M Master Clock  
G Generated Clock  
& Internal Generated Clock  
U User Defined Skew Group  
D Default Skew Group  
* Generated Clock Balanced Separately  
  
==== Summary Reporting for Corner fast ====  
  
===== Summary Table for Corner fast =====  


| Clock / Skew Group                 | Attrs | Sinks | Levels | Clock Repeater Count | Clock Repeater Area | Clock Stdcell Area | Max Latency | Global Skew | Trans Count | DRC Count | Cap DRC Count | Wire Length |
|------------------------------------|-------|-------|--------|----------------------|---------------------|--------------------|-------------|-------------|-------------|-----------|---------------|-------------|
| ## Mode: func, Scenario: func_fast |       |       |        |                      |                     |                    |             |             |             |           |               |             |
| sys_clock                          | M,D   | 197   | 5      | 6                    | 2.84                | 5.37               | 0.10        | 0.06        | 0           | 0         | 0             | 423.32      |
| sys_gated_clk                      | G     | 60    | 1      | 0                    | 0.00                | 0.00               | 0.00        | 0.00        | 0           | 0         | 0             | 0.00        |
| spi_clock                          | M,D   | 178   | 4      | 5                    | 2.80                | 4.00               | 0.08        | 0.03        | 0           | 0         | 0             | 402.12      |
| spi_gated_clk                      | G     | 178   | 2      | 4                    | 2.53                | 2.53               | 0.03        | 0.01        | 0           | 0         | 0             | 348.40      |
| All Clocks                         |       | 375   | 5      | 11                   | 5.64                | 9.37               | 0.10        | 0.06        | 0           | 0         | 0             | 825.44      |

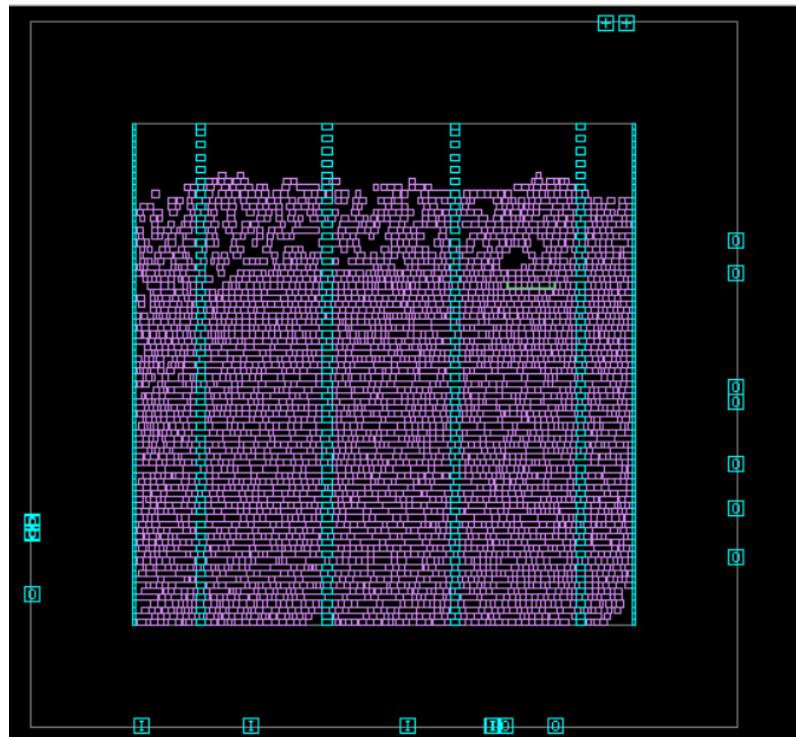

Warning: Please use -largest / -smallest / -all switches with -show_verbose_paths / -show_paths to report the clock paths. (CTS-956)

  
==== Summary Reporting for Corner slow ====  
  
===== Summary Table for Corner slow =====  


| Clock / Skew Group                 | Attrs | Sinks | Levels | Clock Repeater Count | Clock Repeater Area | Clock Stdcell Area | Max Latency | Global Skew | Trans Count | DRC Count | Cap DRC Count | Wire Length |
|------------------------------------|-------|-------|--------|----------------------|---------------------|--------------------|-------------|-------------|-------------|-----------|---------------|-------------|
| ## Mode: func, Scenario: func_slow |       |       |        |                      |                     |                    |             |             |             |           |               |             |
| sys_clock                          | M,D   | 197   | 5      | 6                    | 2.84                | 5.37               | 0.10        | 0.06        | 0           | 0         | 0             | 423.32      |
| sys_gated_clk                      | G     | 60    | 1      | 0                    | 0.00                | 0.00               | 0.00        | 0.00        | 0           | 0         | 0             | 0.00        |
| spi_clock                          | M,D   | 178   | 4      | 5                    | 2.80                | 4.00               | 0.09        | 0.03        | 0           | 0         | 0             | 402.12      |
| spi_gated_clk                      | G     | 178   | 2      | 4                    | 2.53                | 2.53               | 0.03        | 0.01        | 0           | 0         | 0             | 348.40      |
| All Clocks                         |       | 375   | 5      | 11                   | 5.64                | 9.37               | 0.10        | 0.06        | 0           | 0         | 0             | 825.44      |


```

The chip after cts and adding buffer



The utilization become 0.7

```
*****
Report : report_utilization
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Sat May  3 15:27:13 2025
*****
Utilization Ratio:          0.7408
Utilization options:
- Area calculation based on: site_row_of_block dig_tx_system_5_clock_ends
- Categories of objects excluded: hard_macros macro_keepouts soft_macros io_cells hard_blockages
Total Area:                2428.4136
Total Capacity Area:       2428.4136
Total Area of cells:       1798.9992
Area of excluded objects:
- hard_macros      : 0.0000
- macro_keepouts   : 0.0000
- soft_macros      : 0.0000
- io_cells         : 0.0000
- hard_blockages   : 0.0000
Total Area of excluded objects: 0.0000
Ratio of excluded objects:    0.0000

Utilization of site-rows with:
- Site 'unit':           0.7408
```

Global timing path

```
*****
Report : global_timing
        -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May  2 08:47:32 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.387	-0.008	-0.232	-0.387	-0.180
TNS	-6.703	-0.064	-6.072	-0.387	-0.180
NUM	55	26	27	1	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.164	-0.164	0.000	0.000	0.000
TNS	-5.676	-5.676	0.000	0.000	0.000
NUM	157	157	0	0	0

Qor snapshot:

```
No. of scenario = 2
s1 = func_fast
s2 = func_slow

WNS of each timing group:          s1      s2
-----
SYS_GATED_CLK                      -       -0.0037
SPI_GATED_CLK                     -0.3835  -0.3869
SPI_CLK                            0.1665   0.1658
SYS_CLK                           -       -0.0049

Setup WNS:                         -0.3835  -0.3869  -0.3869
Setup TNS:                         -6.6053  -6.7033  -6.7033
Number of setup violations:        29       55       55
Hold WNS:                          -0.1624  -0.1638  -0.1638
Hold TNS:                          -5.6692  -5.3239  -5.6760
Number of hold violations:         157      128      157
Number of max trans violations:    0        0        0
Number of max cap violations:     0        0        0
Number of min pulse width violations: 0        0        0

Area:                             1917.636
Cell count:                       4400
Buf/inv cell count:                3191
Std cell utilization:              0.7408
CPU(s):                           3065
Mem(Mb):                          2805
Host name:                        academysvr02

Histogram:             s1      s2
-----
Max violations:      29      55
  above ~ -0.7     ---     0      0
  -0.6 ~ -0.7     ---     0      0
  -0.5 ~ -0.6     ---     0      0
  -0.4 ~ -0.5     ---     0      0
  -0.3 ~ -0.4     ---     1      1
  -0.2 ~ -0.3     ---    27     27
  -0.1 ~ -0.2     ---     1      1
  0 ~ -0.1        ---     0     26

Min violations:      157     128
  -0.06 ~ above    ---     5      6
  -0.05 ~ -0.06    ---    14     11
  -0.04 ~ -0.05    ---    17     17
  -0.03 ~ -0.04    ---    25     22
  -0.02 ~ -0.03    ---    14     13
  -0.01 ~ -0.02    ---    14     18
  0 ~ -0.01        ---    46     20
```

6)routing

Pre routing check:

```
Printing options for 'route.auto_via_ladder.*'

=====
== Check for design ==
=====

>>> No net contains a large number of ports
>>> No port contains a large number of pins

=====
== Check for PG DPT on Track ==
=====

>>>> Number of PG rails cross even number of track: 0

=====
== Check for PG PreRoute setting ==
=====

No number_of_secondary_pg_pin_connections setting and skip checking

=====
== Check for pins ==
=====

>>>> No pin violations found

=====
== Check for the Cut Metal not on Preferred Grid ==
=====

=====
== Check for overlap of standard cells ==
=====

>>>> No overlap of standard cells found

=====
== Check for overlap of standard cells ==
=====

>>>> No overlap of standard cells found

=====
== Check for min-grid violations ==
=====

>>>> No Library min-grid violations found
>>>> No Design min-grid violations found
>>>> No min-grid violations found

=====
== Check for out-of-boundary ports ==
=====

>>>> No out-of-boundary error found

=====
== Check for blocked ports ==
=====

>>>> Port might be blocked by layer constraints - min/max and freeze layer settings
>>>> Port might be blocked by check port access
>>>> Port u_spi_slave/U262 D0 at (10.9840 10.7760)_|(11.0180 11.0240) on layer M1 might be blocked (refer
>>>> The design might not be cleanly routed because it has 1 possibly blocked ports
>>>> Net blocked by layer constraints - min/max and freeze layer settings
>>>> No blocked nets found

=====
== Check for shielding violations ==
=====

>>>> The following Non-PG net has a shape with shape_use shield_route
>>> No non-PG net has a shape with shape_use shield_route.
>>>> The following PG net has shape with shape_use detail_route and shape length is too long.
>>> No PG net has shape with shape_use detail_route and shape length is too long.
>>>> The following nets with shield non-default rule has no internal data representation in Zroute.
>>> No nets with shield non-default rule has no internal data representation in Zroute.
```

There is no error.

ErrorSet	Total	Visible	Fixed	Ignored	Waived	NULL Net	Detected
/home/svgbasic25abkhaled/GP/pnr/hier_top_down2/results/dig_tx_system.ndm:dig_tx_system_6_complete.design	0	0	0	0	0	0	0
DRC_report_by_check_pg_drc	0	0	0	0	0	0	0
_temp_place_ends_check_legality.err	0	0	0	0	0	0	0
_temp_1_powerplan_ends_check_legality.err	0	0	0	0	0	0	0
check_routability.err	0	0	0	0	0	0	0
dig_tx_system_6_complete_floatingPG.err	0	0	0	0	0	0	0
temp_clock_ends_lvs.err	0	0	0	0	0	0	0
temp_data_setup_chf.err	0	0	0	0	0	0	0
temp_data_setup_dppinassgn.err	0	0	0	0	0	0	0
temp_data_setup_dpplace.err	0	0	0	0	0	0	0
temp_floorplan_ends_floatingPG.err	0	0	0	0	0	0	0
temp_floorplan_ends_missingVia.err	0	0	0	0	0	0	0
temp_1_powerplan_ends_dppinassgn.err	0	0	0	0	0	0	0
temp_1_powerplan_ends_floatingPG.err	0	0	0	0	0	0	0
zroute.err	0	0	0	0	0	0	0

Check routes

```
Total number of nets = 3657, of which 0 are not extracted
Total number of open nets = 0, of which 0 are frozen
Total number of excluded ports = 0 ports of 0 unplaced cells connected to 0 nets
          0 ports without pins of 0 cells connected to 0 nets
          0 ports of 0 cover cells connected to 0 non-pg nets
```

Qor.snapshot

WNS of each timing group:	s1	s2
SYS_GATED_CLK	-	-0.0041
SPI_GATED_CLK	-0.3091	-0.3095
SPI_CLK	0.1736	0.1735
SYS_CLK	-	-0.0071
-----	-----	-----
Setup WNS:	-0.3091	-0.3095
Setup TNS:	-6.3319	-6.3735
Number of setup violations:	29	34
Hold WNS:	-0.1365	-0.1364
Hold TNS:	-0.4501	-0.4377
Number of hold violations:	24	4
Number of max trans violations:	0	0
Number of max cap violations:	0	0
Number of min pulse width violations:	0	0
-----	-----	-----
Area:		1626.461
Cell count:		3520
Buf/inv cell count:		2311
Std cell utilization:		0.6209
CPU(s):		3427
Mem(Mb):		2805
Host name:		academysvr02
-----	-----	-----
Histogram:	s1	s2
Max violations:	29	34
above ~ -0.7	---	0
-0.6 ~ -0.7	---	0
-0.5 ~ -0.6	---	0
-0.4 ~ -0.5	---	0
-0.3 ~ -0.4	---	1
-0.2 ~ -0.3	---	27
-0.1 ~ -0.2	---	1
0 ~ -0.1	---	0
		5
-----	-----	-----
Min violations:	24	4
-0.06 ~ above	---	0
-0.05 ~ -0.06	---	0
-0.04 ~ -0.05	---	0
-0.03 ~ -0.04	---	1
-0.02 ~ -0.03	---	0
-0.01 ~ -0.02	---	0
0 ~ -0.01	---	20
		0
-----	-----	-----

The global timing after routing

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.309	-0.007	-0.224	-0.309	-0.148
TNS	-6.374	-0.022	-5.894	-0.309	-0.148
NUM	34	5	27	1	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.137	-0.137	0.000	0.000	0.000
TNS	-0.450	-0.450	0.000	0.000	0.000
NUM	24	24	0	0	0

7)primetime

the timing reported from icc2 in primetime before any solving is:

```
pt_shell> report_global_timing
*****
Report : global_timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May 2 09:47:25 2025
*****  
  
Setup violations
-----  
      Total  reg->reg  in->reg  reg->out  in->out  
-----  
WNS    -0.11     -0.01     -0.01     -0.11     0.00  
TNS    -0.21     -0.02     -0.09     -0.11     0.00  
NUM      9         2         6         1         0  
-----  
  
Hold violations
-----  
      Total  reg->reg  in->reg  reg->out  in->out  
-----  
WNS    -0.13     -0.13     0.00     0.00     0.00  
TNS    -0.38     -0.38     0.00     0.00     0.00  
NUM      3         3         0         0         0  
-----
```

I disabled the two timing paths because they are not actual clock gating paths. These paths were mistakenly treated by the tool as gating paths, which prevented proper optimization. Ideally, the tool should have replaced them using Integrated Clock Gating (ICG) logic, but in this case, it did not. As a result, I manually intervened to ensure these paths were excluded from gating consideration, which helped in resolving unnecessary timing constraints and improved overall timing convergence.

```
pt_shell> set_false_path -from u_dig_tx_sys_clock_gating/enable_latch_reg -to u_dig_tx_sys_clock_gating/U2
1
pt_shell> set_false_path -from u_dig_tx_spi_clock_gating/enable_latch_reg -to u_dig_tx_spi_clock_gating/U2
1
pt_shell> report_global_timing
*****
Report : global_timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May 2 16:11:55 2025
*****  
  
Setup violations
-----  
      Total  reg->reg  in->reg  reg->out  in->out  
-----  
WNS    -0.15     0.00     0.00     -0.15     0.00  
TNS    -0.15     0.00     0.00     -0.15     0.00  
NUM      1         0         0         1         0  
-----  
  
Hold violations
-----  
      Total  reg->reg  in->reg  reg->out  in->out  
-----  
WNS    -0.14     -0.14     0.00     0.00     0.00  
TNS    -0.14     -0.14     0.00     0.00     0.00  
NUM      1         1         0         0         0  
-----
```

After solution

```
*****
Report : global_timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May  2 16:25:47 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.15	0.00	0.00	-0.15	0.00
TNS	-0.15	0.00	0.00	-0.15	0.00
NUM	1	0	0	1	0

No hold violations found.

In Fast corner check the timing reported from icc2 in primetime is

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.11	0.00	0.00	-0.11	0.00
TNS	-0.11	0.00	0.00	-0.11	0.00
NUM	1	0	0	1	0

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.01	-0.01	0.00	0.00	0.00
TNS	-0.03	-0.03	0.00	0.00	0.00
NUM	10	10	0	0	0

After fixing by inserting buffer.

```
*****
Report : global_timing
    -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May  2 17:35:32 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.11	0.00	0.00	-0.11	0.00
TNS	-0.11	0.00	0.00	-0.11	0.00
NUM	1	0	0	1	0

No hold violations found.

This is the timing output from icc2 after route eco changes

```
*****
Report : global_timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May  2 19:12:57 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.38	-0.09	-0.23	-0.38	-0.26
TNS	-6.98	-0.29	-5.97	-0.46	-0.26
NUM	45	11	27	6	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.04	-0.02	-0.04	0.00	0.00
TNS	-0.17	-0.03	-0.13	0.00	0.00
NUM	21	15	6	0	0

The following timing report reflects the results obtained from PrimeTime after exporting the netlist and SPEF from ICC2, following the latest routing and ECO steps.

```
pt_shell> report_global_timing
*****
Report : global_timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Fri May  2 21:47:52 2025
*****
```

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.10	0.00	0.00	-0.10	0.00
TNS	-0.10	0.00	0.00	-0.10	0.00
NUM	1	0	0	1	0

No hold violations found.

The remain path can't solve due to output delay also the path contain more logic as shown in figure.

