Design of Direct Sequence-Spread Spectrum System

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1.INTRODUCTION

Direct Sequence-Spread Spectrum (DS-SS) is a transmission technique in which a pseudo-noise code, independent of the information data is employed as a modulation waveform to "spread" the signal energy over a bandwidth much greater than the signal information bandwidth. At the receiver the signal is de-spread using a synchronized replica of the pseudo-noise code. The spreading sequence in DS-SS is often called as PN sequence.

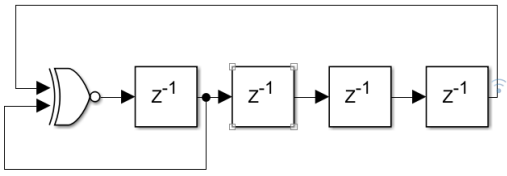
the spread signal is modulated using Binary Phase Shift keying (BPSK) modulation technique in the transmitter and on the receiver side the modulated signal is recovered using BPSK demodulation technique.

2.PN Sequence Generator

A Pseudo-random Noise (PN) sequence/code is a binary sequence that exhibits randomness properties but has a finite length and is therefore deterministic. PN generators are based on Linear Feedback Shift Registers (LFSR). The contents of the registers are shifted right by one position at each clock cycle. The feedback from predetermined registers or taps to the left most register are XNOR-ed together.

A maximum length sequence (L) for a shift register of length N is referred to as m-sequence and is defined as

$$L = 2^N - 1$$

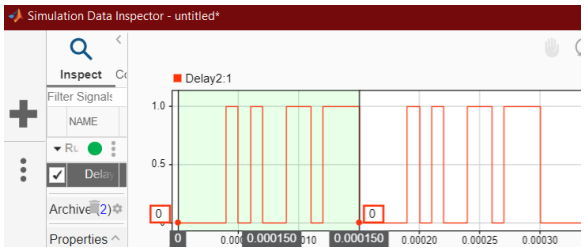


2.1 Design of PN Sequence Generator

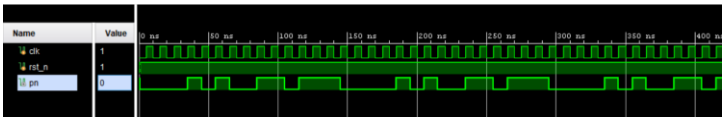
Specifications:

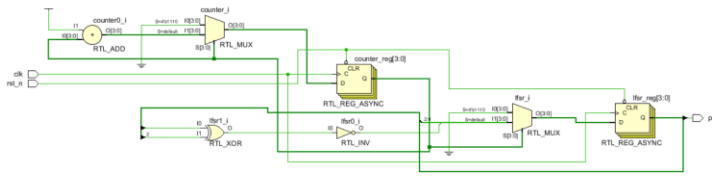
Clock frequency for PN	Fpn=100 KHz
LFSR length	N=4
LFSRs	D-FF type
FPGA board clock frequency	Fb=50 MHz

- A clock frequency of 100 KHz for PN Sequence generator is designed using a divider of 500 clock cycles of Fb . Clock divider=Fb /Fpn=50 MHz/100 KHz=500
- Maximum length sequence, N=4 corresponds to 4 D-FF to realize LFSRs of the PN generator system. Since N=4, the maximum sequence length L=24−1=15. Hence the sequence repeats every 15 clock cycles.
- The Chip rate for the PN sequence generator system is calculated as follows: Chip period, Tc=1/100 KHz=10 us Chip rate,Fc=100 KHz
- The bit period for the input data signal is calculated as follows: Data bit period, Td=Max. sequence Length (L)×Chip period (Tc) For the system, Td=15×10 us



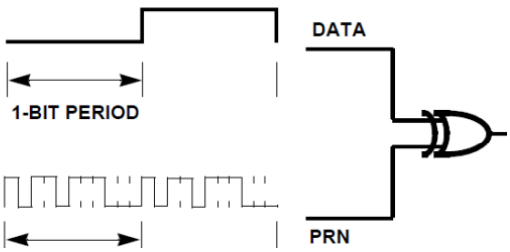
The next figures shown the waveform of PN sequence and netlist.





3. Overview of DS-SS Transmitter System

DS-SS transmitter, the input data bits are spread by PN sequence generator. The spreading is actually done by multiplying the data bits with that of the PN sequence code generated.



Specifications:

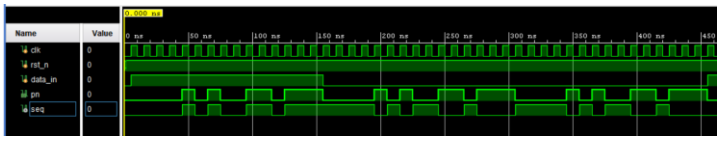
- PN sequence Chip rate, Tc=10 us.
- Data signal Bit rate, Tb=150 us.

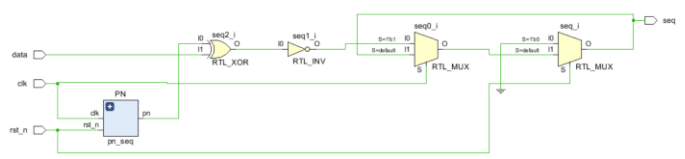
Let the data signal be m(t) and PN sequence p(t). The two signals are multiplied and the multiplied output is the spread signal. it can be inferred that an XNOR gate can act as a multiplier to spread the data signal with the PN signal

m(t)	p(t)	s(t)
0	0	1
0	1	0
1	0	0
1	1	1

The output from MATLAB is shown in next figure.

The next figures shown the waveform of PN sequence and netlist.





Oscillator Design

Specification:

- PN sequence Chip rate, Tc=10 us.
- The carrier frequency Fc should be at least 5 times the inverse of the chip rate.
- The sampling rate Fs=25 MHz.
- N=36 is the number of samples used to represent one full cycle of the sine wave.

The carrier frequency is determined by how often the oscillator completes one full cycle of the sine wave using the given number of samples at the specified sampling rate. Fc=FS/N=25M/36 ~= 700KHZ

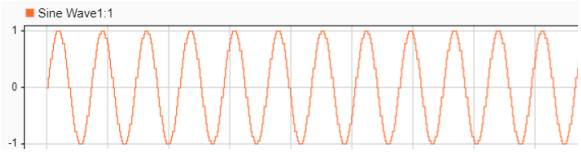
Steps to Design a LUT for Sine Wave Generation:

The sine wave ranges from 0 to 2pi radians over one complete cycle. For each sample i, the corresponding angle θi is:

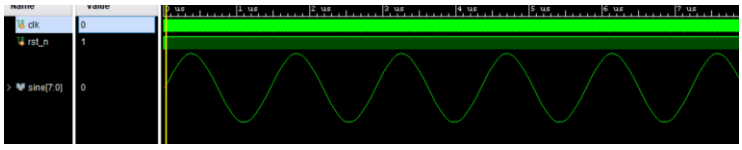
$$\theta_i = \frac{2\pi i}{N} \quad \text{for } i = 0, 1, 2, \ldots, N-1$$

The samples can generate from MATLAB sin(i*2*pi/N) and then convert it from floating point to fixed by using function FI with word length 8 bits and fraction 6 bits

```
i=zeros(1,36);
f=zeros(1,36);
i(1)=0;
for v = 1:1:35
  i(v+1)=sin(v*10*pi/180);

end

for v = 1:1:36

  f(v)=fi(i(v),1,8,6);
end
```



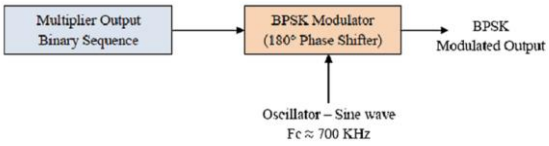
After getting fixed point, convert it to binary and store it in look up table



BPSK Modulator Design:

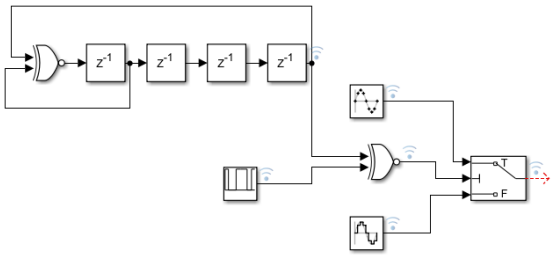
Specification:

- Spread binary sequence is the input to the system
- Oscillator carrier sine wave of frequency, Fc ~=700 KHz



The BPSK modulator is designed using the spread binary sequence as the input to the system and the carrier frequency Fc . The logic is implemented in such a way that the phase of the sine wave is shifted by 180° whenever the input binary bit changes.

The modeling of DSSS transmitter shown in figure



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depending on value of spread sequence the sine wave will be shifted.

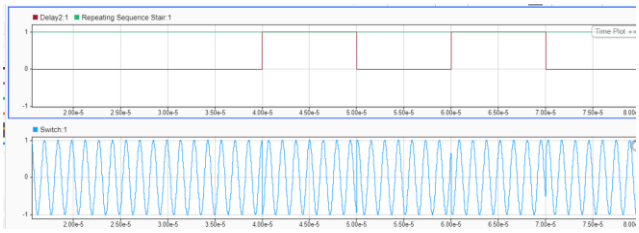
In a Binary Phase Shift Keying (BPSK) modulator, the input binary sequence modulates the phase of a carrier signal, typically a sine wave. Here's how it works:

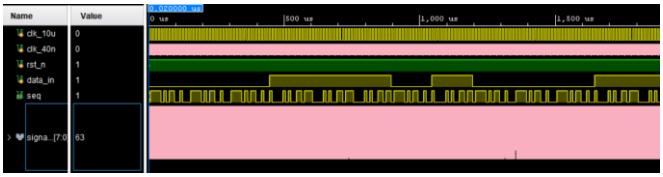
Carrier Signal: A sinusoidal carrier signal with frequency Fc is used, represented as:

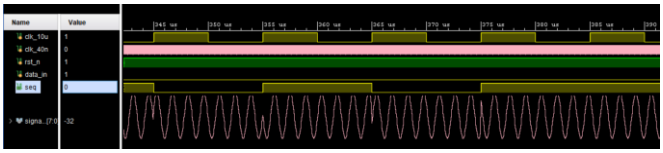
$$s(t) = A\cos(2\pi F_c t)$$

- When the input bit is **'1'**, the carrier signal is transmitted without a phase shift, The signal remains.
- When the input bit is **'0'**, the carrier signal is shifted by 180°. The signal becomes

$$A\cos(2\pi F_c t + \pi) = -A\cos(2\pi F_c t).$$







The netlist of transmitter.