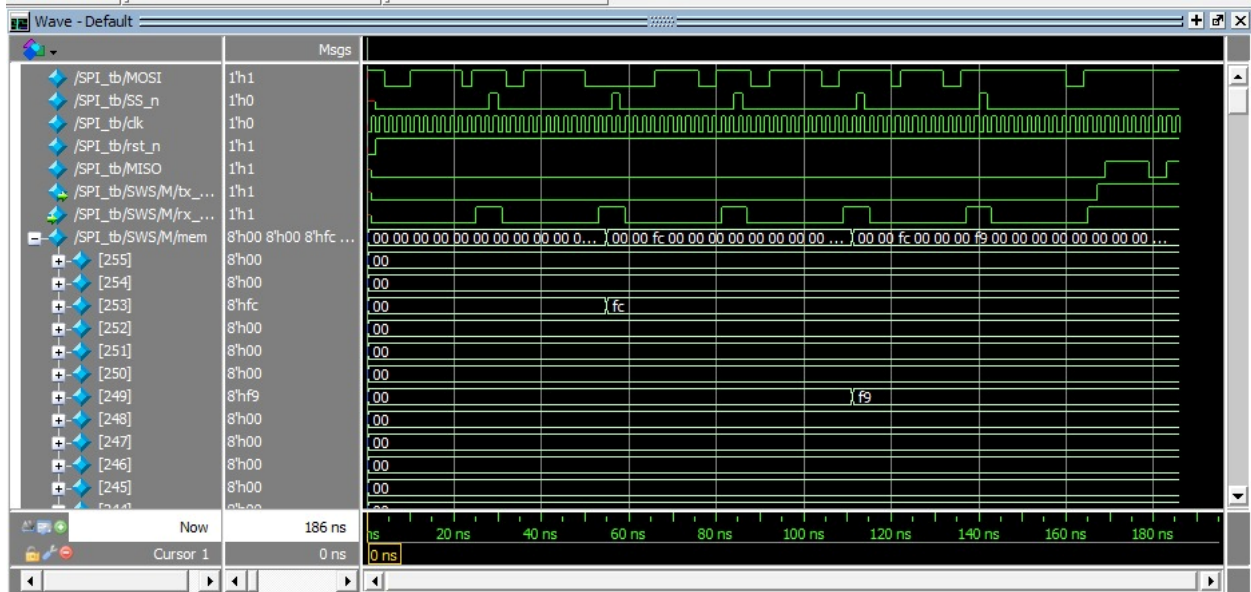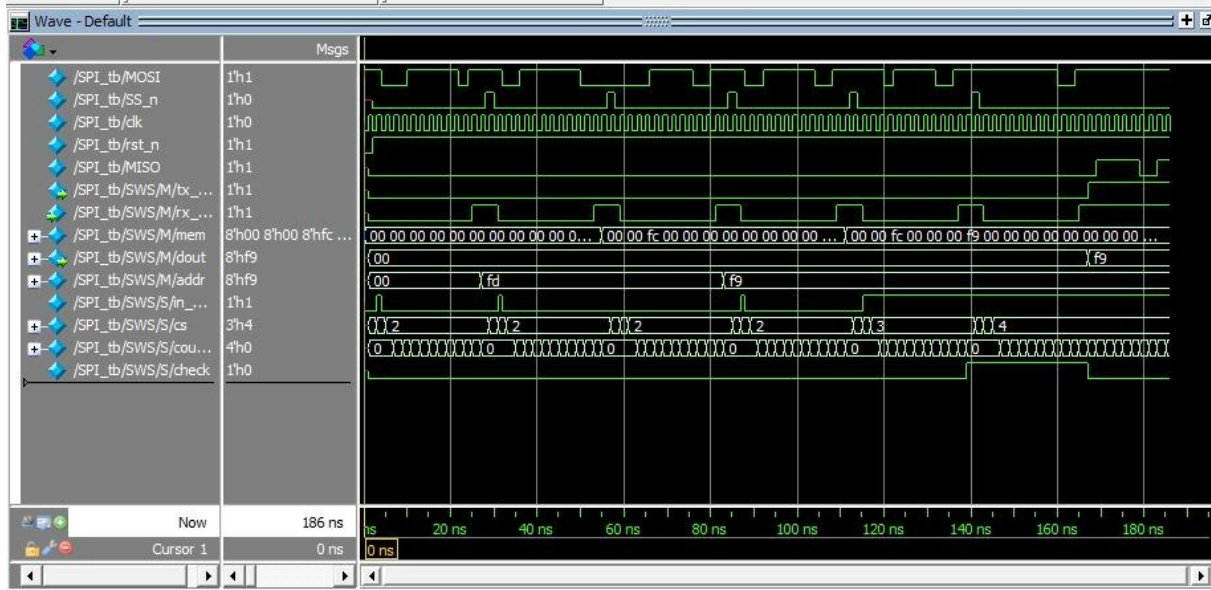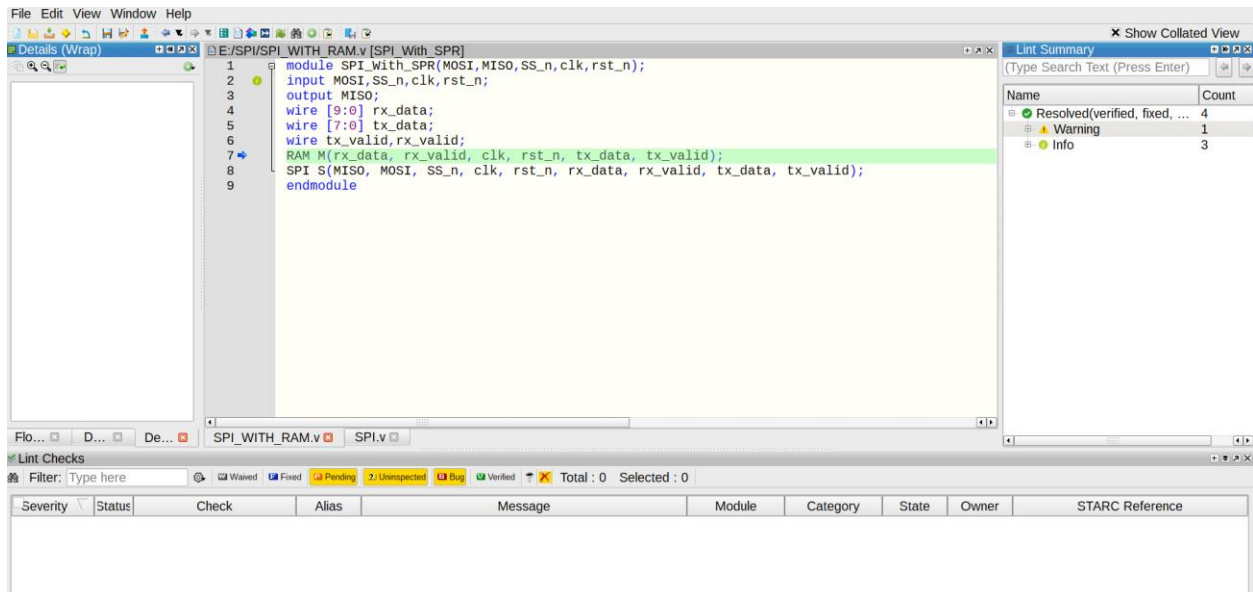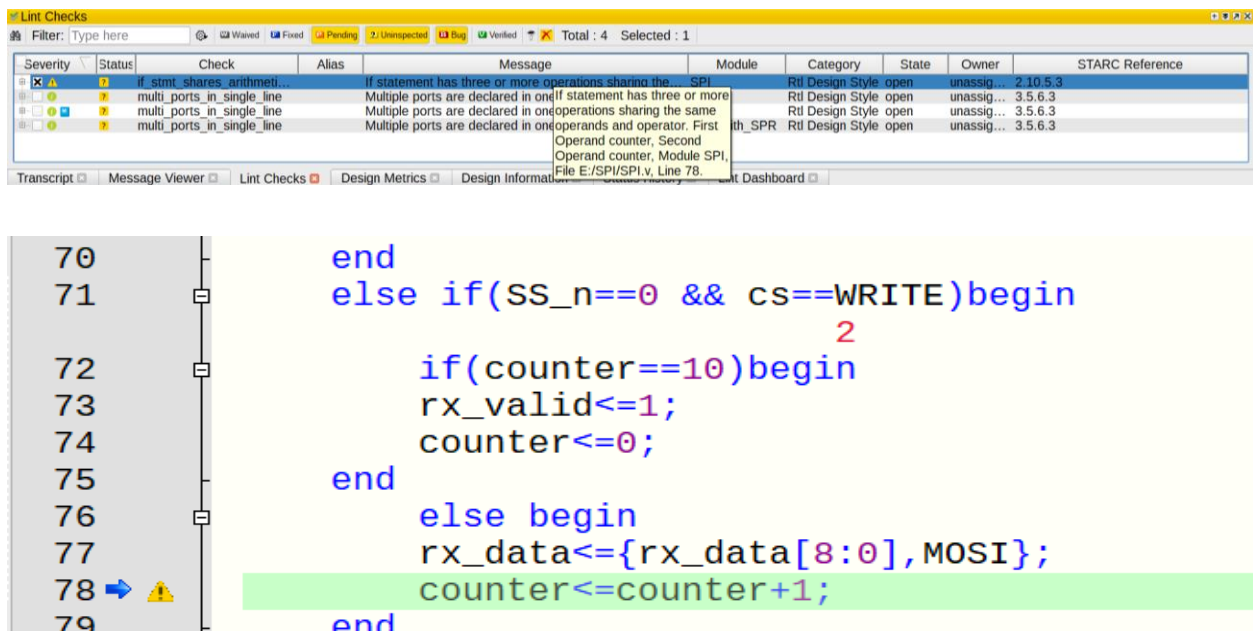# 1-Waveform snippets:

2-QuestaLint snippets:

Figure 1: snippet from QuestaLint showing no linting Errors

Lint checks had only one warning as shown below:

There was no problem with this warning so we just waived it and the design now has no Errors as shown in figure 1.

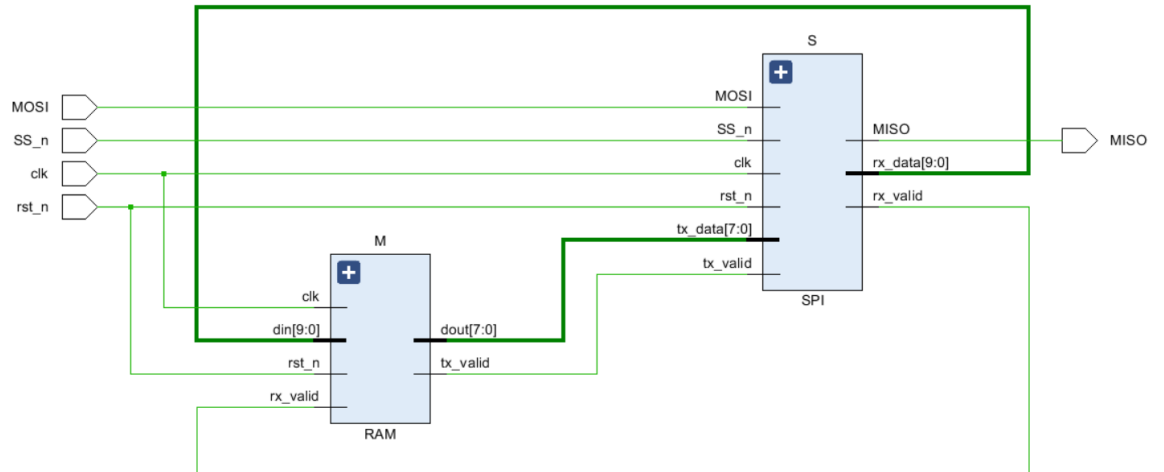# 3-Synthesis snippets for each encoding:

1- Sequential :

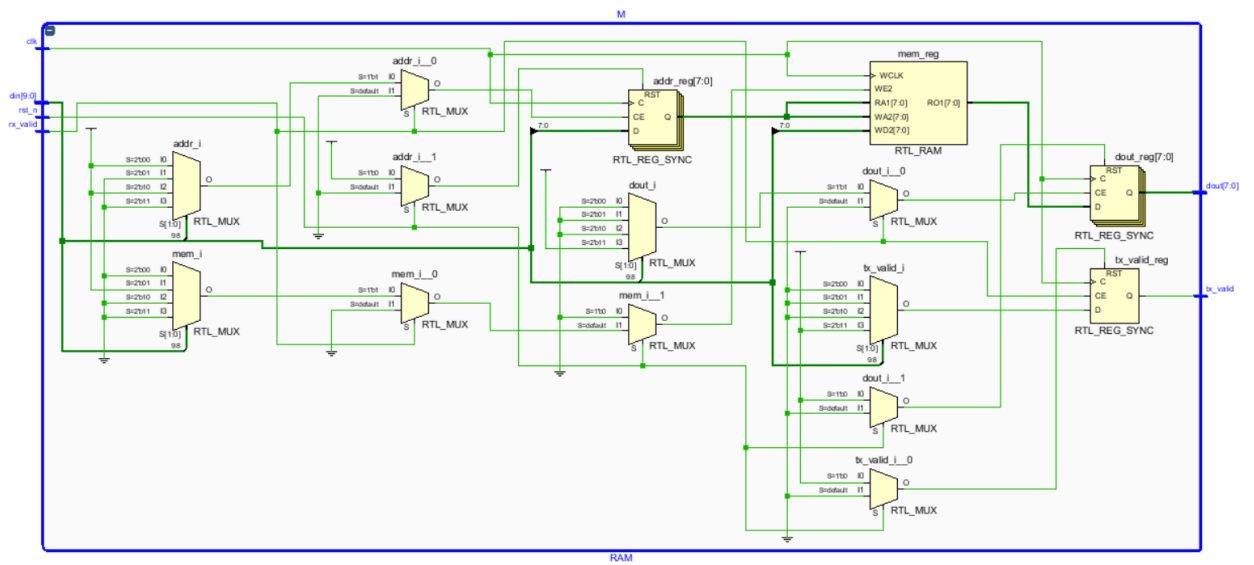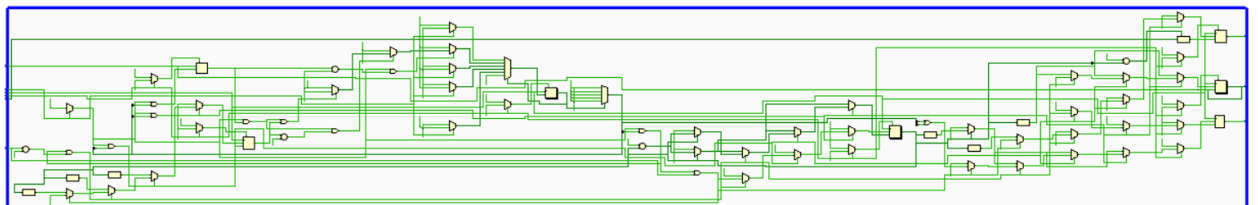

Figure 2: Schematic after the elaboration
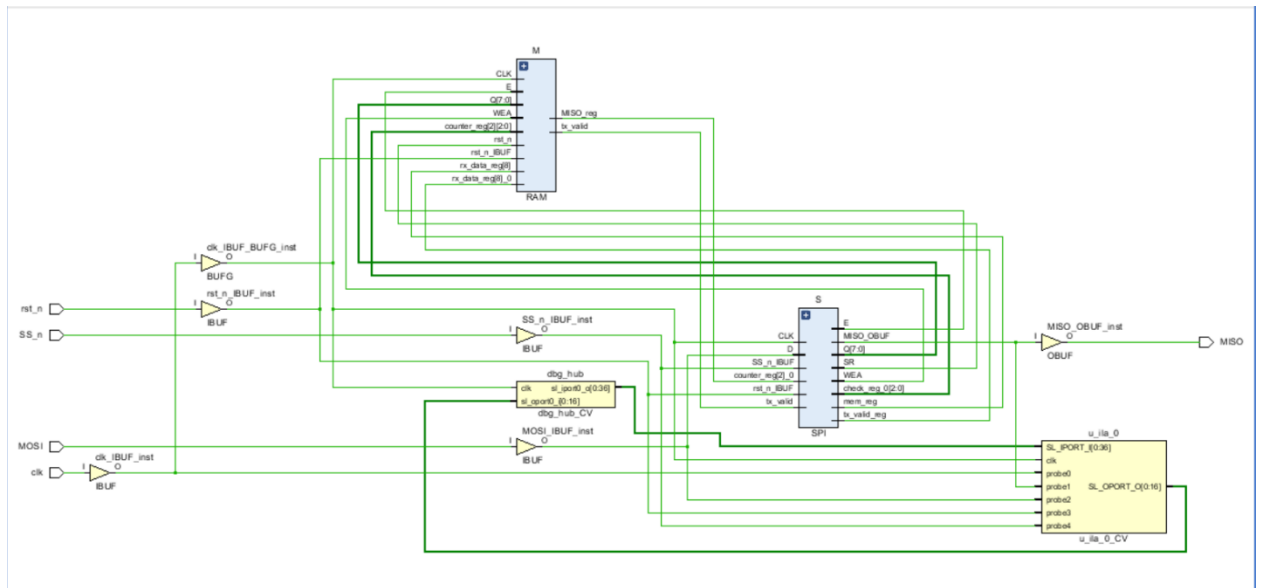

Figure 3: RAM

Figure 4: SPI

Figure 5: Schematic after synthesis
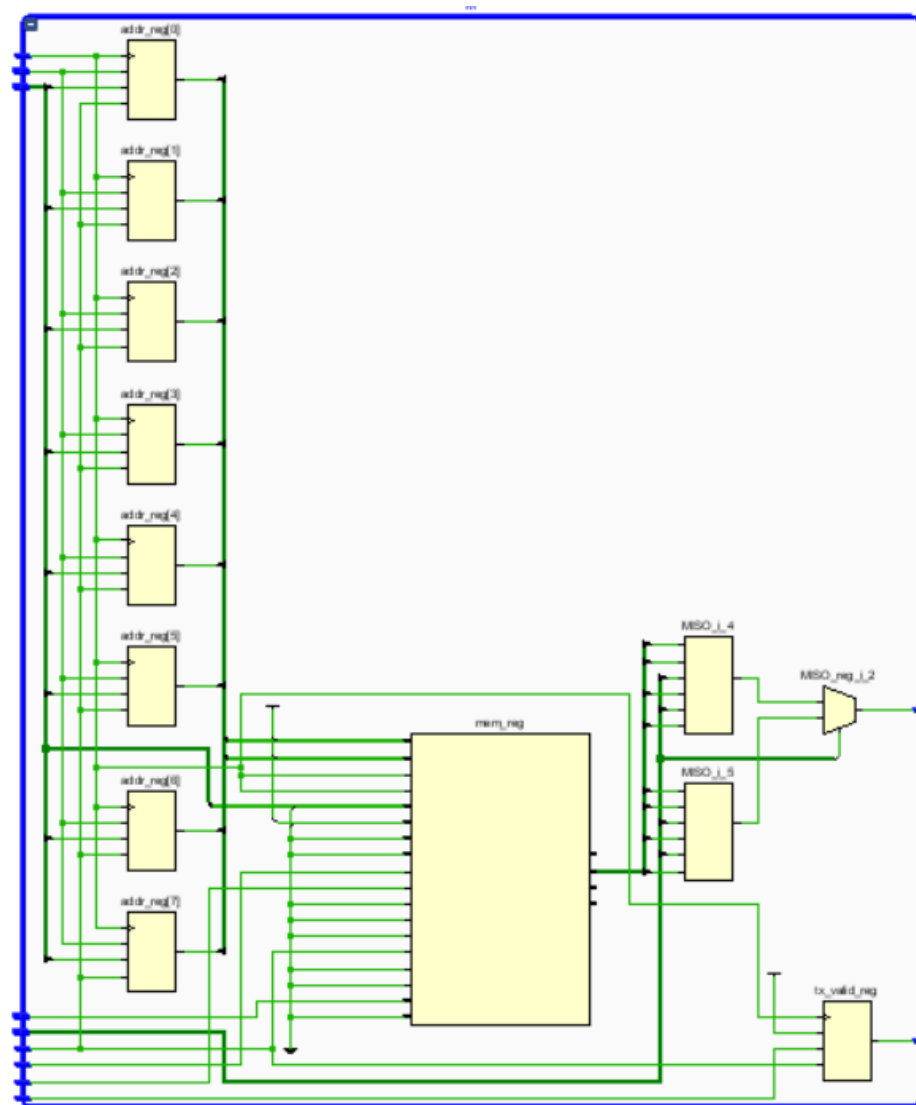
Figure 6: RAM after synthesis

Figure 7: SPI after synthesis

Figure 8: Report showing type of encoding used (sequential)

Figure 9: Timing Report

Figure 10: Snippet of the critical path highlighted in the schematic

2- One_hot:
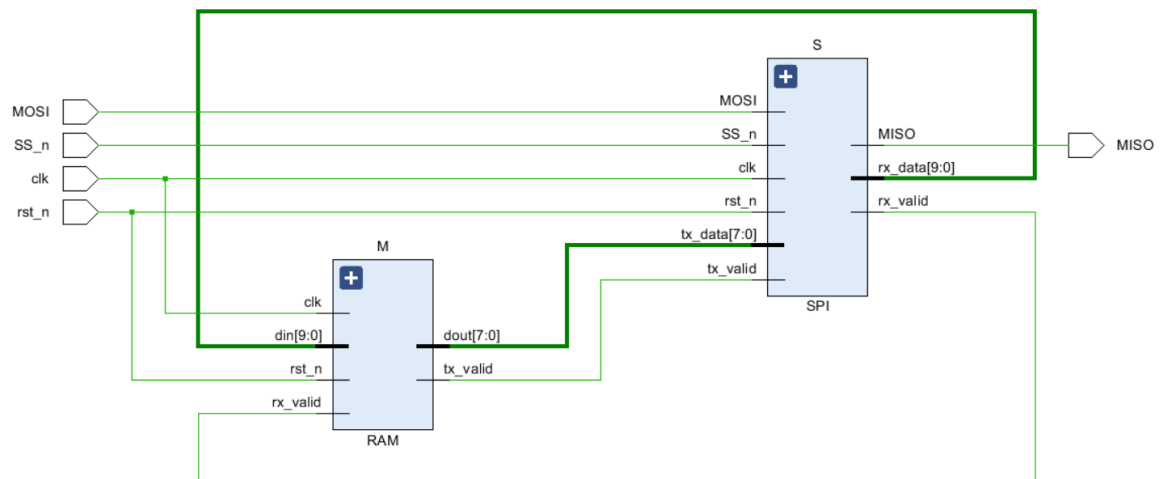
Figure 11:Schematic after the elaboration
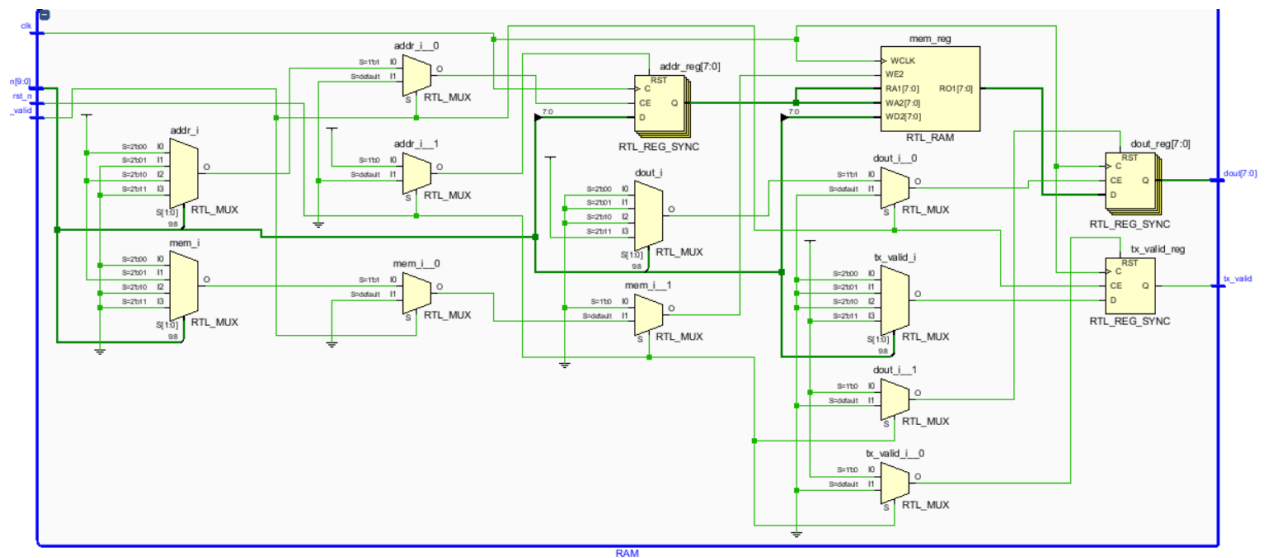
Figure 12: RAM
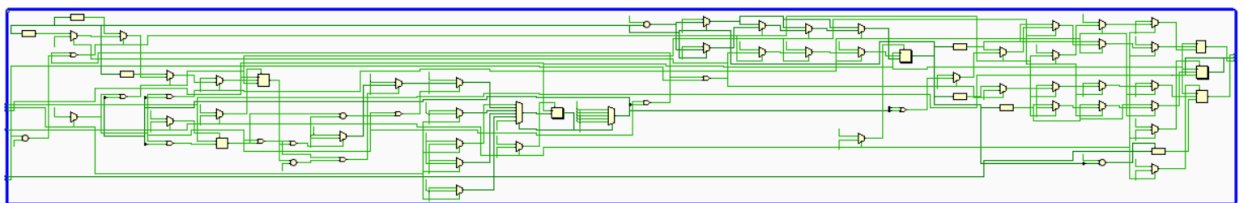
Figure 13: SPI
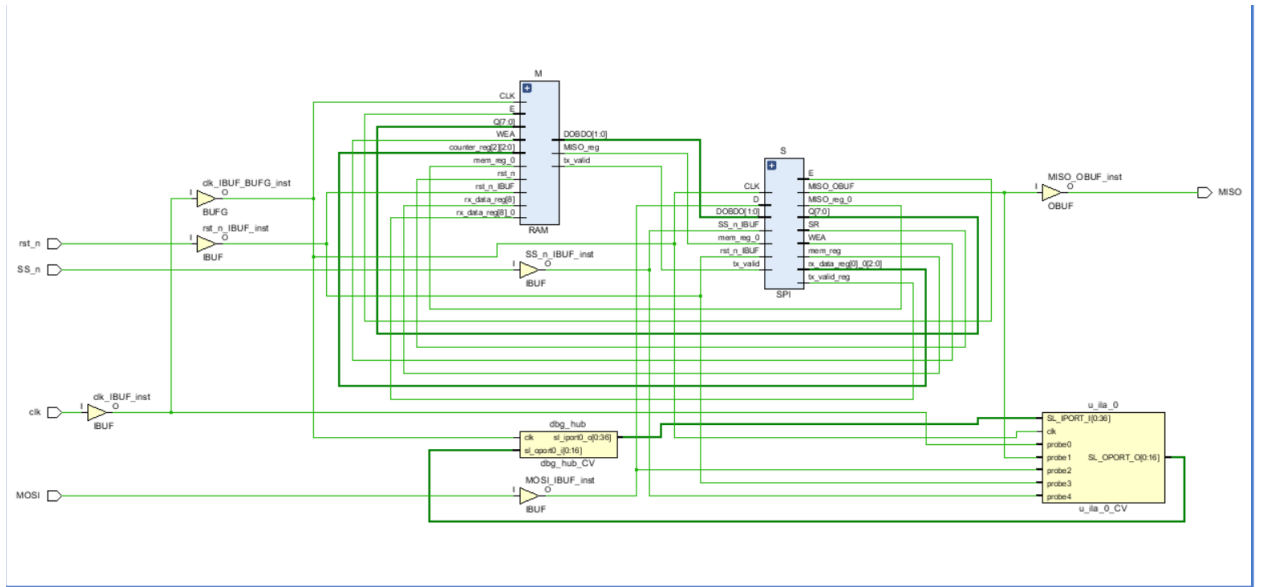
Figure 14:Schematic after synthesis
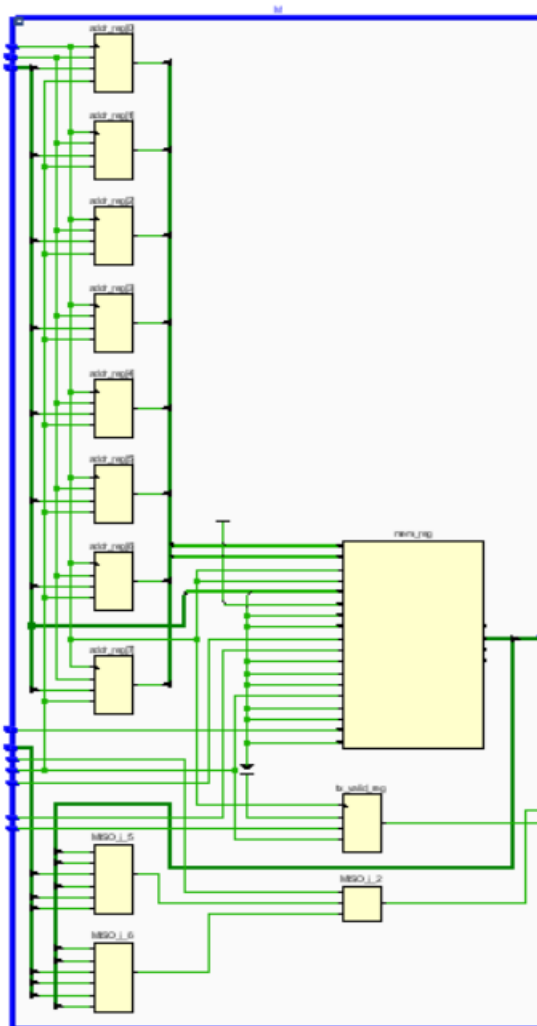
Figure 15: RAM after synthesis
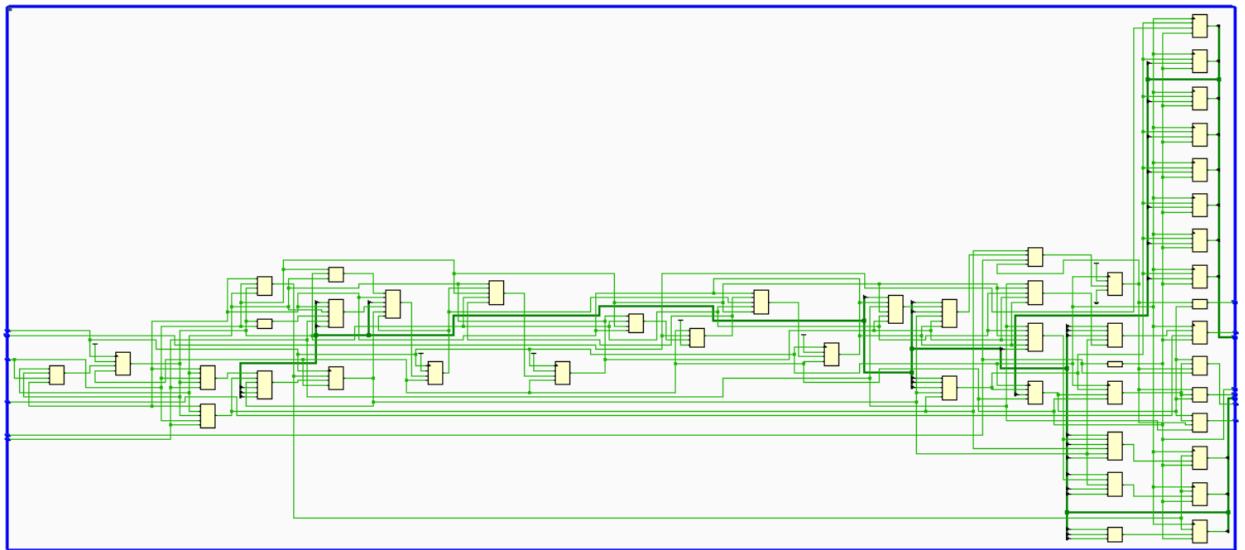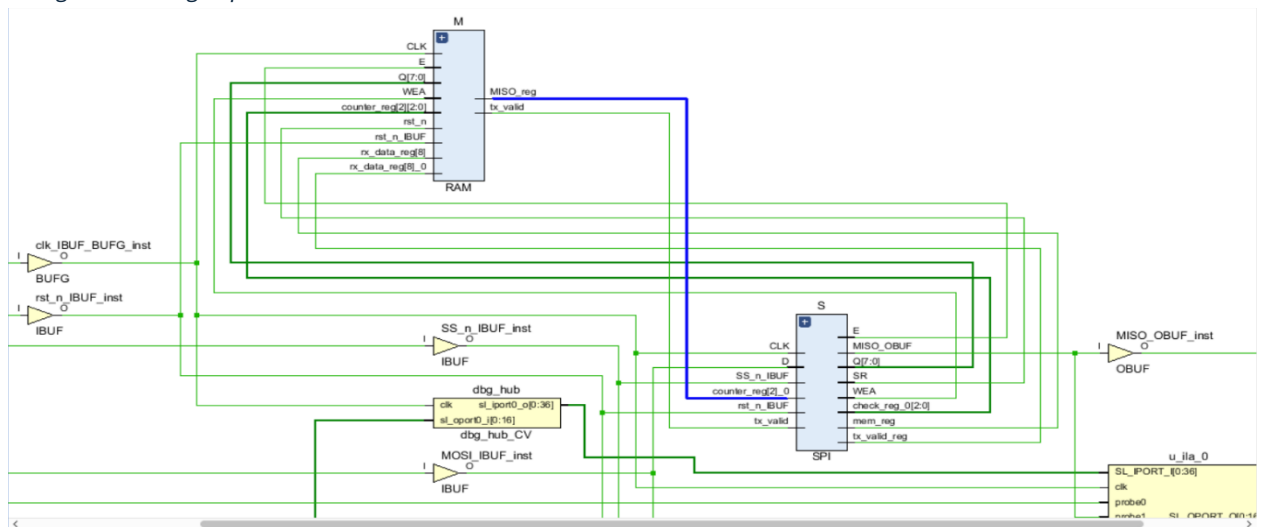
7
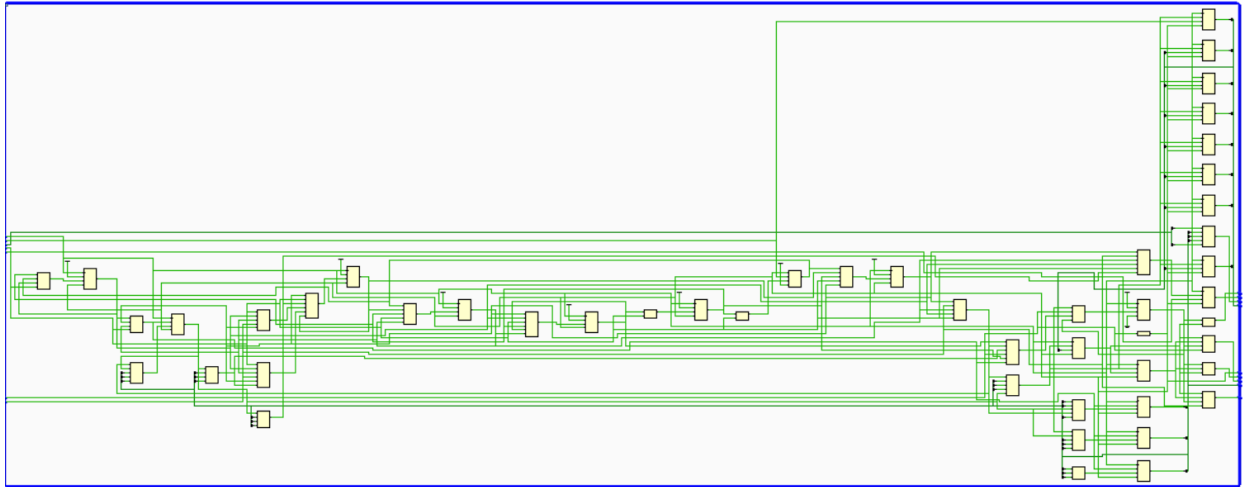
Figure 16: SPI after synthesis

```
-----------------------------------------------------------------------------------
          State |               New Encoding |              Previous Encoding
-----------------------------------------------------------------------------------
           IDLE |                     00001 |                              000
        CHK_CMD |                     10000 |                              001
          WRITE |                     01000 |                              010
       READ_ADD |                     00100 |                              011
      READ_DATA |                     00010 |                              100
-----------------------------------------------------------------------------------

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI'
WARNING: [Synth 8-327] inferring latch for variable 'in_MOSI_reg' [E:/digital design projects/Team_project
```

Figure 17:Report showing type of encoding used (one_hot)

Figure 18: Timing Report


Figure 19: Critical Path

8

3- gray:

Figure 20: Schematic after the elaboration

Figure 21: RAM

Figure 22: SPI

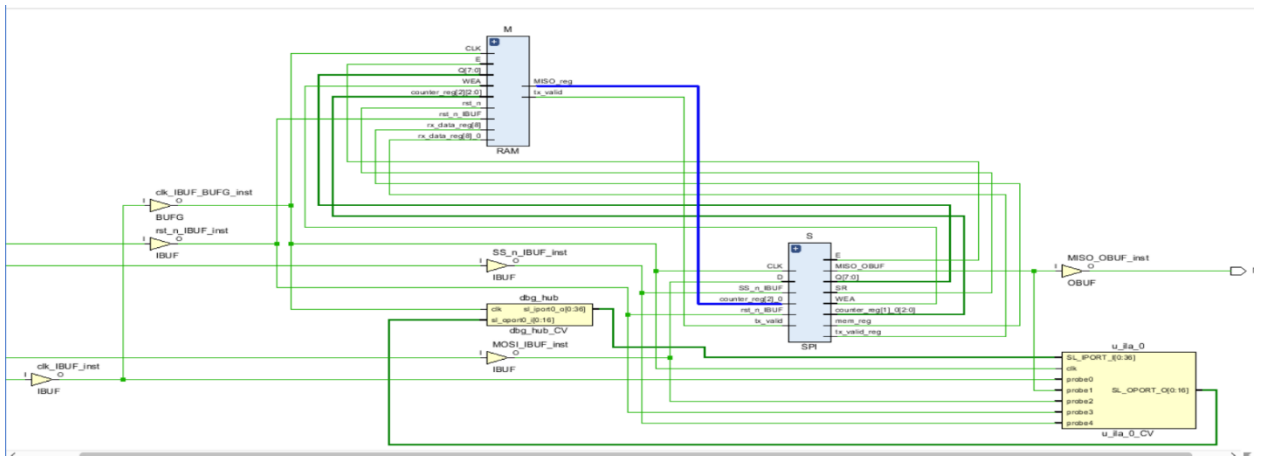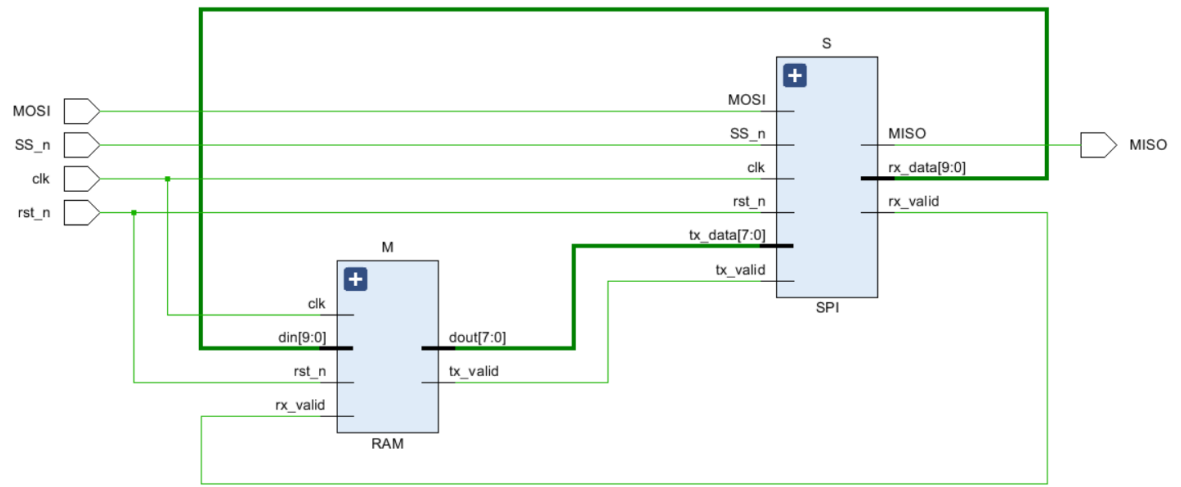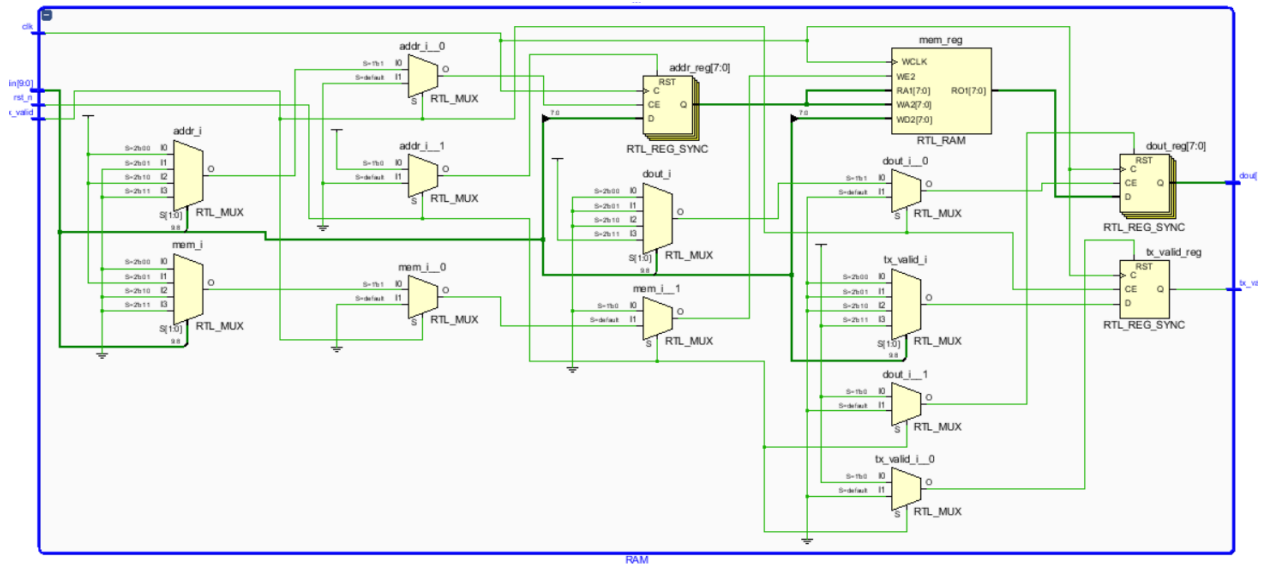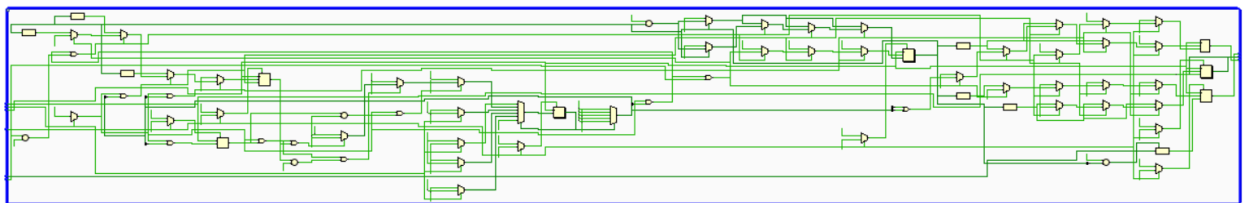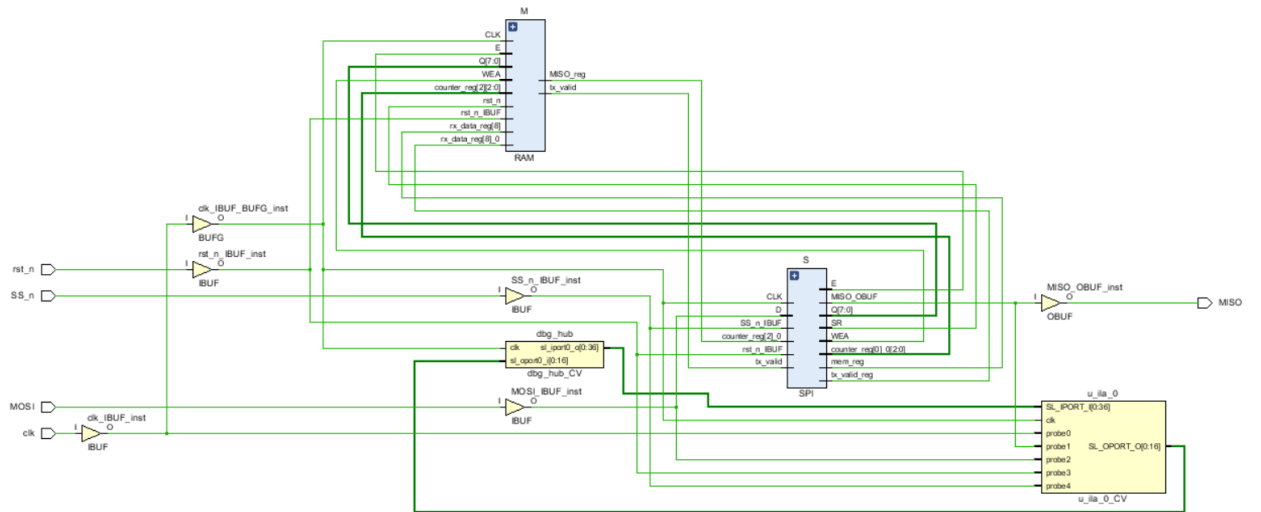*Figure 23: Schematic after synthesis*
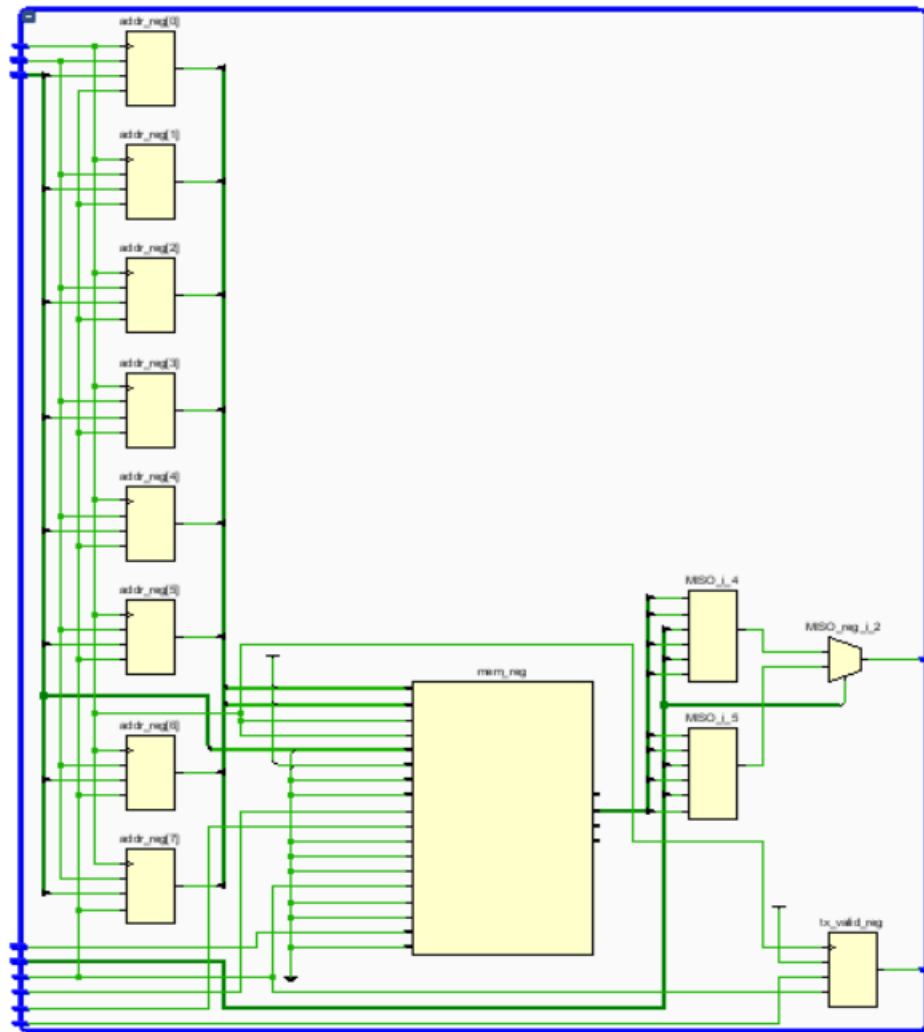
Figure 24: RAM after synthesis
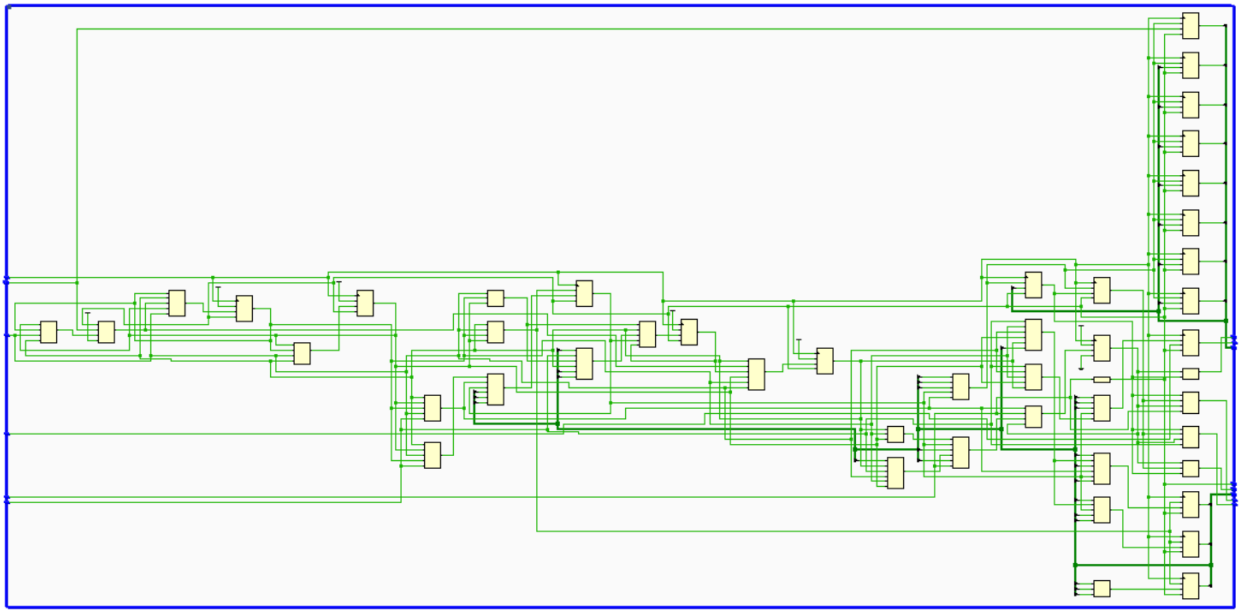
Figure 25: SPI after synthesis

```
-------------------------------------------------------------------------------------
          State |                  New Encoding |              Previous Encoding
-------------------------------------------------------------------------------------
           IDLE |                           000 |                              000
        CHK_CMD |                           111 |                              001
          WRITE |                           010 |                              010
       READ_ADD |                           011 |                              011
      READ_DATA |                           001 |                              100
-------------------------------------------------------------------------------------

INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI'
```

Figure 26: Report showing type of encoding used (gray)

Figure 27: Timing Report

Figure 28: Critical path

4-Implementation snippets for each encoding:

1- Sequential:

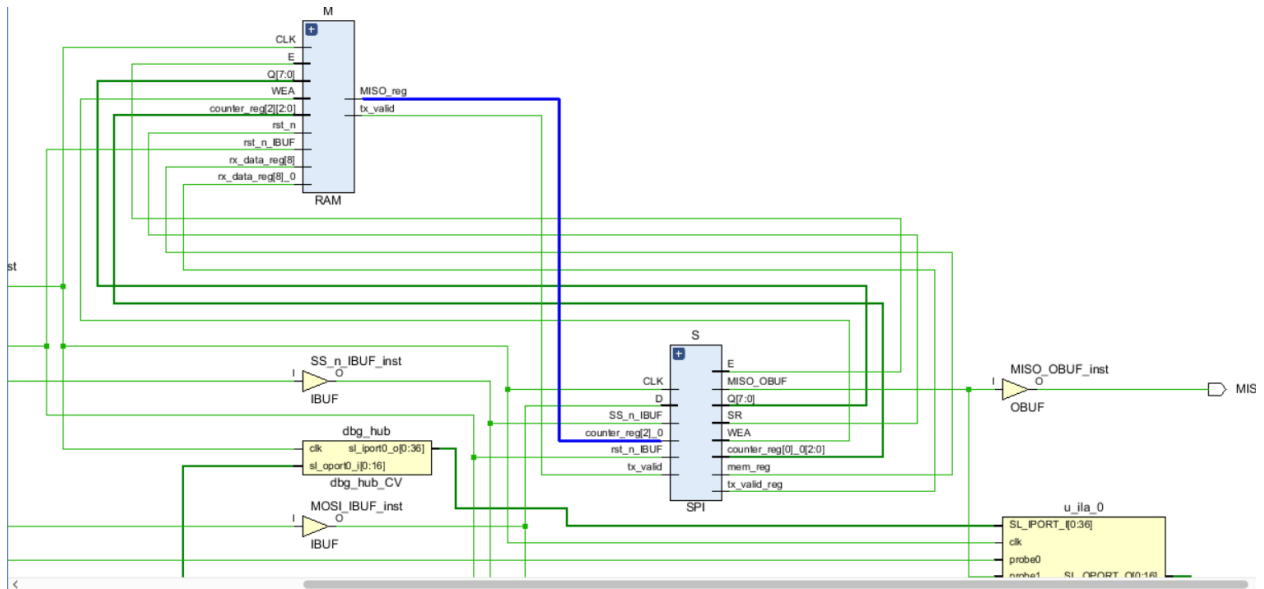| Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
∨ N SPI_With_SPR	1274	1946	11	605	1166	108	743	1	5	2	1
> ⬚ dbg_hub (dbg_hub)	481	727	0	230	457	24	309	0	0	1	1
⬚ M (RAM)	2	9	1	3	2	0	0	0.5	0	0	0
⬚ S (SPI)	25	21	0	10	25	0	9	0	0	0	0
> ⬚ u_ila_0 (u_ila_0)	766	1189	10	370	682	84	422	0.5	0	0	0

Figure 29: Utilization report

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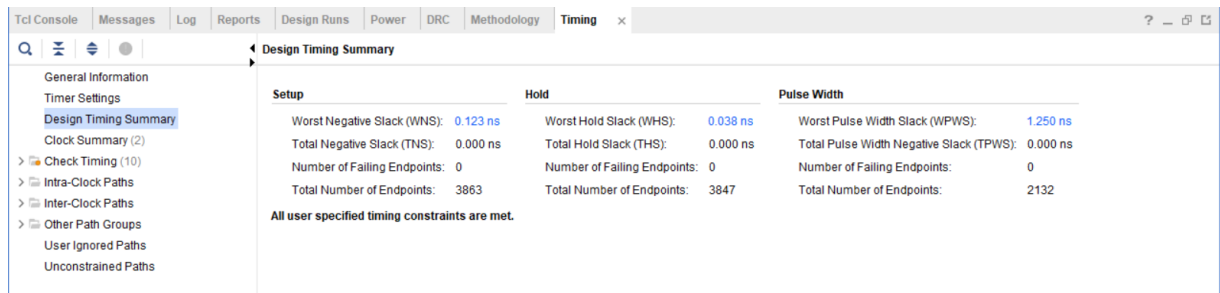
Figure 30: Timing Report
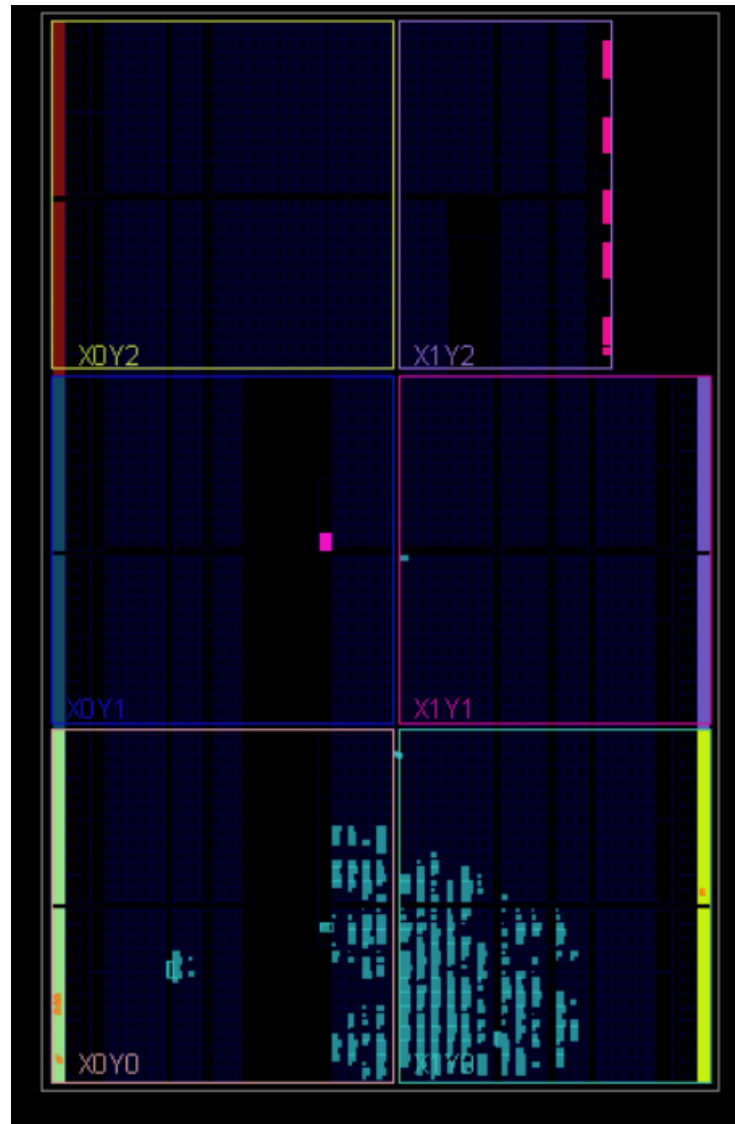
Figure 31: device

2- One_hot:

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
SPI_With_SPR	1270	1948	11	653	1162	108	742	1	5	2	1
dbg_hub (dbg_hub)	480	727	0	245	456	24	313	0	0	1	1
M (RAM)	2	9	1	3	2	0	0	0.5	0	0	0
S (SPI)	24	23	0	13	24	0	10	0	0	0	0
u_ila_0 (u_ila_0)	764	1189	10	402	680	84	417	0.5	0	0	0

Figure 32: Utilization report
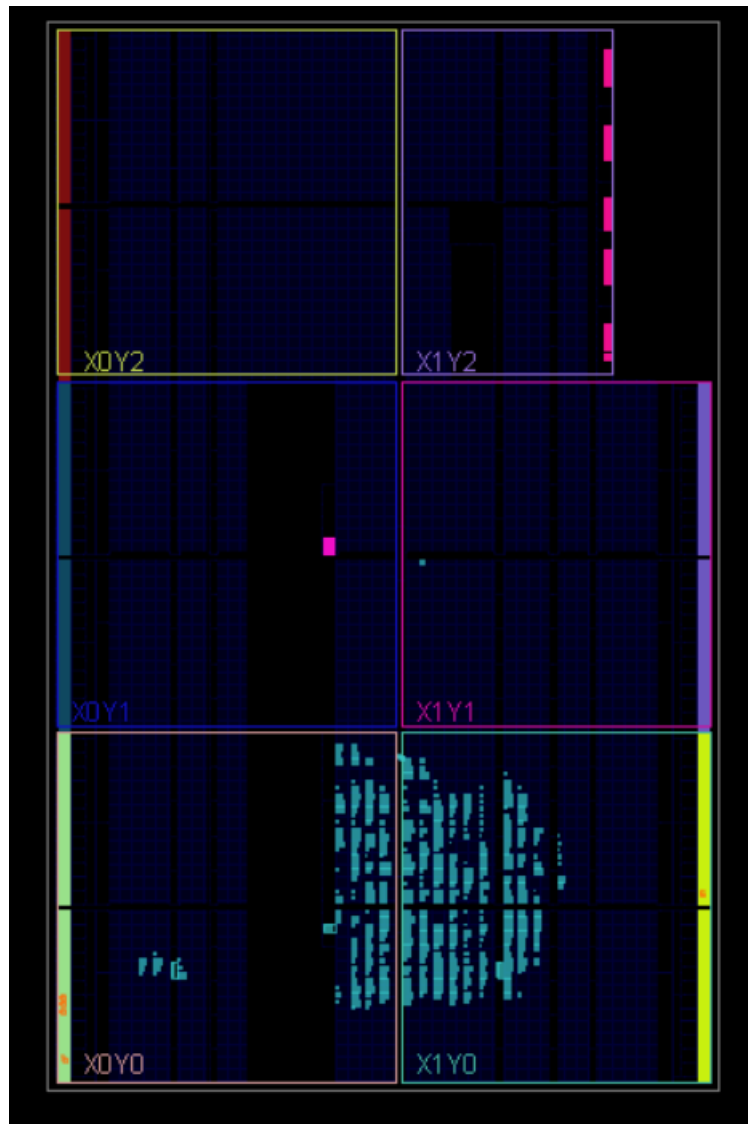

Figure 33: Timing Report

Figure 34: device

3- gray:

| Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (815 0)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
∨ N SPI_With_SPR	1267	1946	11	611	1159	108	744	1	5	2	1
> ∃E dbg_hub (dbg_hub)	480	727	0	234	456	24	309	0	0	1	1
☐ M (RAM)	2	9	1	3	2	0	0	0.5	0	0	0
☐ S (SPI)	22	21	0	10	22	0	8	0	0	0	0
> ∃E u_ila_0 (u_ila_0)	763	1189	10	369	679	84	423	0.5	0	0	0

Figure 35: Utilization report
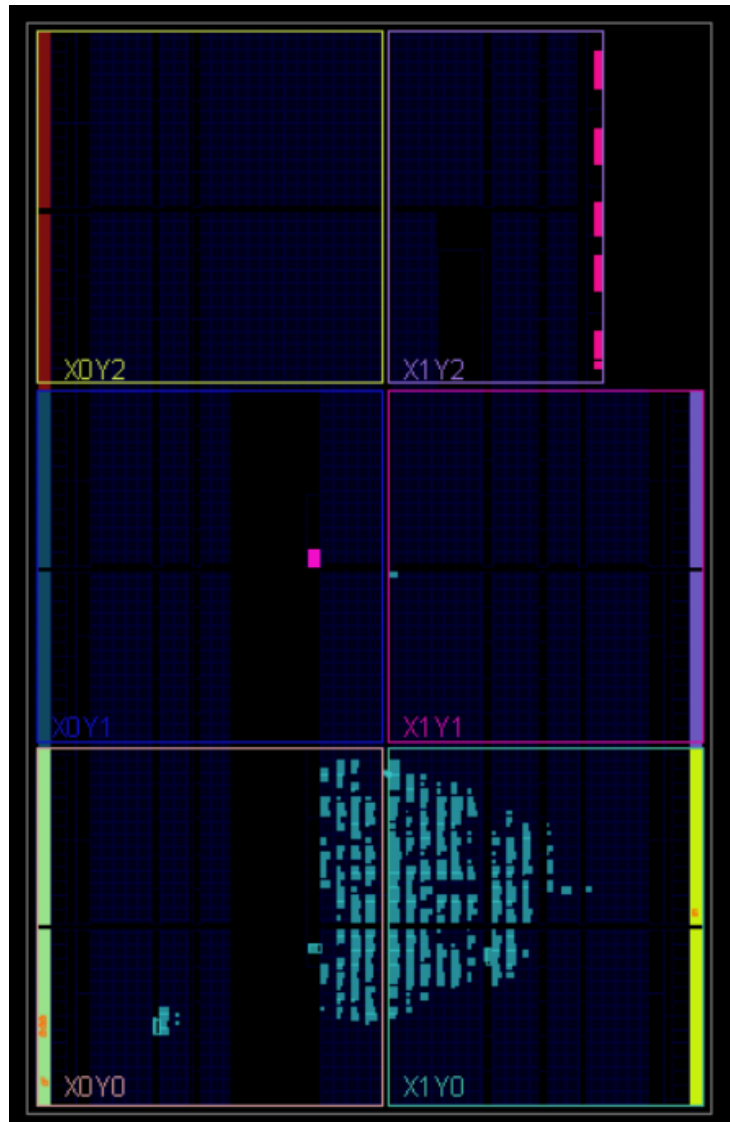
15
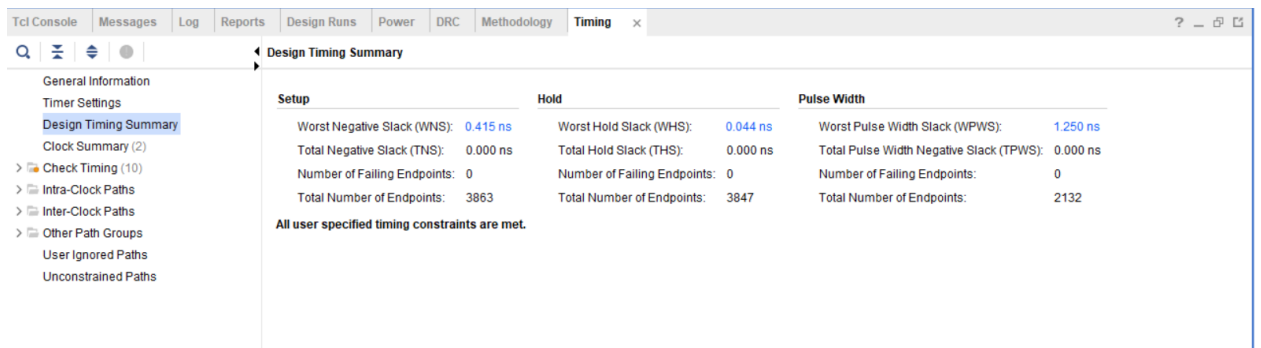
Figure 36: Timing report

Figure 37: device

➢ Since we wish to operate at the highest frequency possible so we will choose the encoding based on the encoding type that gives us highest setup time slack

- **Sequential = 0.123 ns**
- **One_hot =0.372 ns**
- **gray = 0.415 ns**

➢ So, we will choose gray encoding and now we will add a debug core such that all internals can be analyzed and generate bitstream file.

5- <u>Snippet of messages tab:</u>

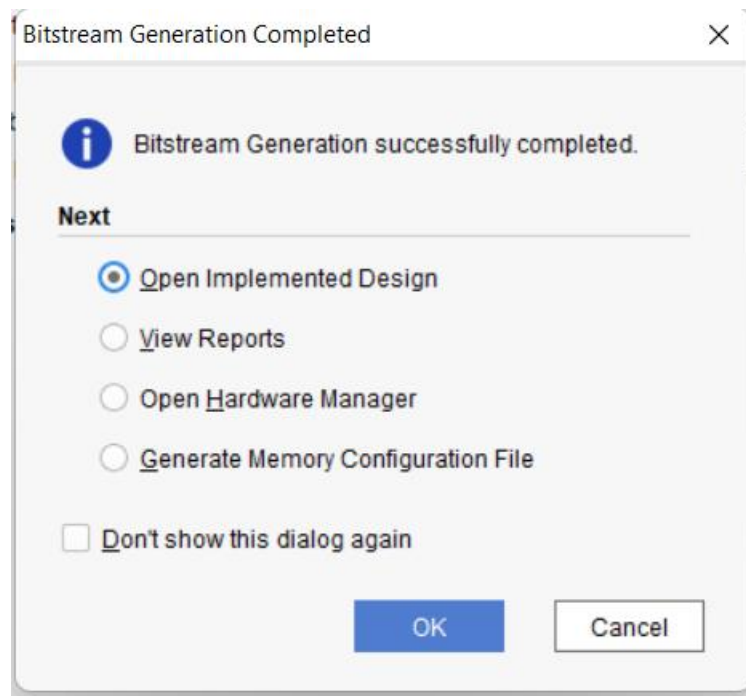*Figure 38: Snippets of messages tab showing no errors after running (elaboration, synthesis and implementation)*

Figure 39: successful bitstream