

APPENDIX B: Cycle accurate Simulator

Cycle Accurate Simulator

The Cycle-Accurate Simulator (CAS) was developed as a specialized tool for verifying the design and functionality of a 5-stage pipelined MIPS processor. Unlike traditional simulation tools like ModelSim, which rely heavily on waveform-based debugging, the CAS provides a clock-by-clock visualization of the processor's internal state. This includes tracking data transfers between pipeline stages, instruction progression, and the values of key control signals, offering a clearer and more structured view of the processor's operation.

The primary motivation behind creating this simulator was to enhance the verification process by closely mimicking the hardware design implemented in Verilog. The CAS reproduces the behavior of the pipelined processor cycle-by-cycle, ensuring that the simulated execution aligns with the intended hardware implementation. This alignment allows engineers to quickly identify discrepancies between the hardware design and its expected behavior, particularly in scenarios involving data hazards, control hazards, or branch mispredictions.

By visualizing the data flow through the pipeline and the changes in pipeline registers at each clock cycle, the CAS provides insights that are difficult to extract from waveform simulations alone. This makes it easier to debug complex behaviors and validate the correctness of the design under various operating conditions. The simulator also allows users to verify the impact of design decisions, such as branch prediction strategies or hazard detection mechanisms, in a highly detailed and precise manner.

In summary, the CAS serves as a robust verification tool that complements traditional simulation workflows by providing a more intuitive, cycle-accurate representation of the hardware's operation.

How to Operate

1. **Download the Simulator:**

Begin by downloading the zip folder containing the Cycle-Accurate Simulator (CAS).

2. **Open the Command Prompt:**

Press **Windows + R** to open the *Run* dialog box. Type `cmd` and press **Enter** to launch the terminal.

3. **Navigate to the Simulator Path:**

In the terminal, use the `cd` command to navigate to the folder where the simulator executable is located. For example:

```
cd path\to\simulator\folder
```

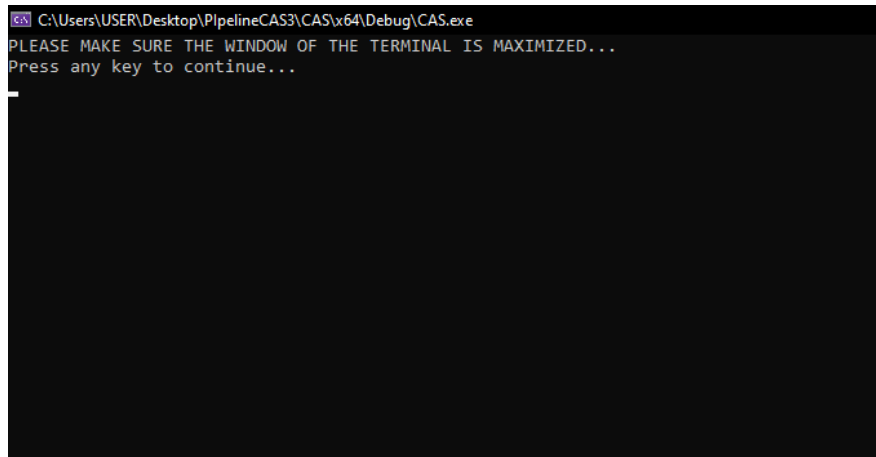
4. **Run the Simulator:**

Once in the correct directory, type the following command to launch the simulator:

```
CAS
```

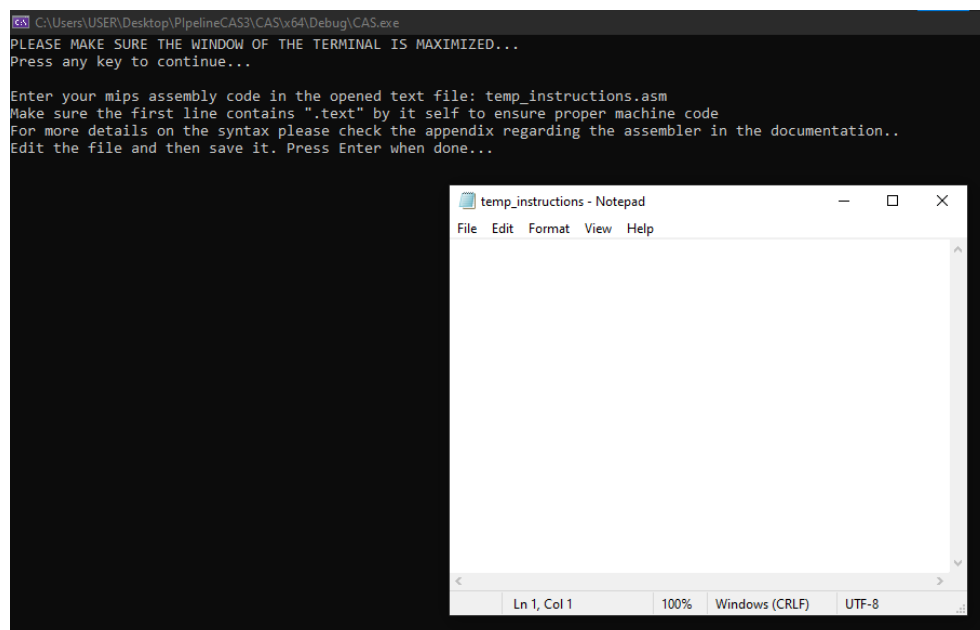
5. The simulator will start, and you can follow the on-screen instructions to interact with it.

For correct screen printing make sure that you maximize the window of the terminal.

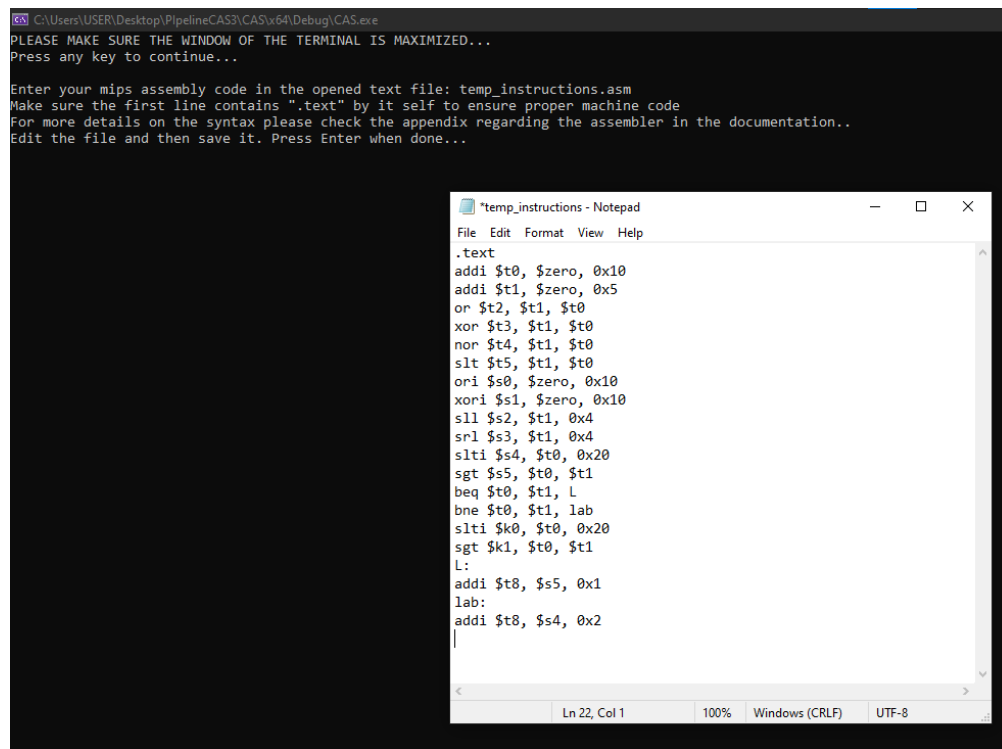


```
C:\Users\USER\Desktop\PipelineCAS3\CAS\x64\Debug\CAS.exe
PLEASE MAKE SURE THE WINDOW OF THE TERMINAL IS MAXIMIZED...
Press any key to continue...
```

A temporary text file will appear on the screen, here you can input your assembly code



Please make sure that the file starts with .text as shown,



The terminal window shows the following text:

```
C:\Users\USER\Desktop\PipelineCAS3\CASv64\Debug\CAS.exe
PLEASE MAKE SURE THE WINDOW OF THE TERMINAL IS MAXIMIZED...
Press any key to continue...

Enter your mips assembly code in the opened text file: temp_instructions.asm
Make sure the first line contains ".text" by it self to ensure proper machine code
For more details on the syntax please check the appendix regarding the assembler in the documentation..
Edit the file and then save it. Press Enter when done...
```

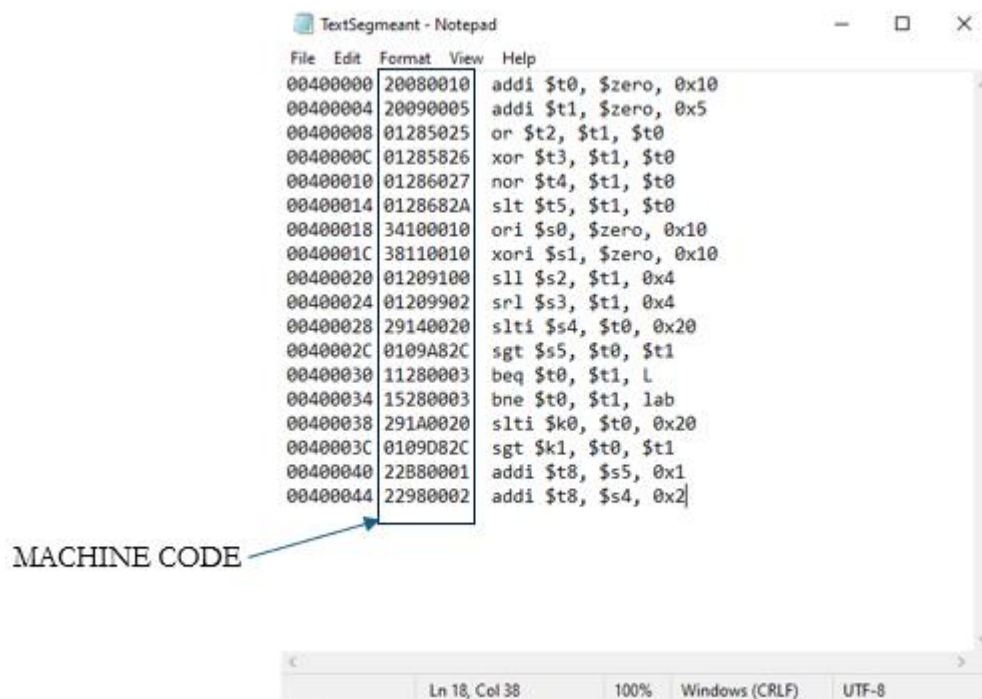
The Notepad window, titled "temp_instructions - Notepad", contains the following MIPS assembly code:

```
.text
addi $t0, $zero, 0x10
addi $t1, $zero, 0x5
or $t2, $t1, $t0
xor $t3, $t1, $t0
nor $t4, $t1, $t0
slt $t5, $t1, $t0
ori $s0, $zero, 0x10
xori $s1, $zero, 0x10
sll $s2, $t1, 0x4
srl $s3, $t1, 0x4
slli $s4, $t0, 0x20
sgt $s5, $t0, $t1
beq $t0, $t1, L
bne $t0, $t1, lab
slti $k0, $t0, 0x20
sgt $k1, $t0, $t1
L:
addi $t8, $s5, 0x1
lab:
addi $t8, $s4, 0x2
```

Refer to the assembler appendix for more details on the syntax.

When done save the file and press enter to activate the simulator

A file containing the instructions and their machine code will appear in the same directory as the executable for the Cycle accurate simulator.



The Notepad window, titled "TextSegmeant - Notepad", displays the machine code for the MIPS instructions from the previous block. The code is organized into three columns: the instruction address, the instruction, and the machine code. An arrow points to the machine code column with the label "MACHINE CODE".

| Address | Instruction | Machine Code |
|----------|-------------------------|--------------|
| 00400000 | addi \$t0, \$zero, 0x10 | 20080010 |
| 00400004 | addi \$t1, \$zero, 0x5 | 20090005 |
| 00400008 | or \$t2, \$t1, \$t0 | 01285025 |
| 0040000C | xor \$t3, \$t1, \$t0 | 01285026 |
| 00400010 | nor \$t4, \$t1, \$t0 | 01286027 |
| 00400014 | slt \$t5, \$t1, \$t0 | 0128682A |
| 00400018 | ori \$s0, \$zero, 0x10 | 34100010 |
| 0040001C | xori \$s1, \$zero, 0x10 | 38110010 |
| 00400020 | sll \$s2, \$t1, 0x4 | 01209100 |
| 00400024 | srl \$s3, \$t1, 0x4 | 01209902 |
| 00400028 | slli \$s4, \$t0, 0x20 | 29140020 |
| 0040002C | sgt \$s5, \$t0, \$t1 | 0109A82C |
| 00400030 | beq \$t0, \$t1, L | 11280003 |
| 00400034 | bne \$t0, \$t1, lab | 15280003 |
| 00400038 | slti \$k0, \$t0, 0x20 | 291A0020 |
| 0040003C | sgt \$k1, \$t0, \$t1 | 0109D82C |
| 00400040 | addi \$t8, \$s5, 0x1 | 22B80001 |
| 00400044 | addi \$t8, \$s4, 0x2 | 22980002 |

Memory Addressing in the Simulator

In the simulator, the values displayed on the left represent the addresses of the machine code in memory. However, it's important to note that these addresses are primarily for **visualization purposes** and do not reflect how memory addresses are actually indexed in the hardware or the CycleAccurateSimulator.

For comparison with tools like MARS, which use byte-addressable memory, these values are shown as byte addresses. In contrast, our hardware design and the cycle-accurate simulator both use **word-addressable memory**, starting at index 0. This means that in the actual design, each address corresponds to a word (typically 4 bytes), while the simulator's memory visualization shows addresses in byte units for easier alignment with MARS.

This distinction ensures that the design is properly validated, as we can directly compare our word-addressable memory implementation with the byte-addressable system in MARS, making sure our word alignment and addressing are correct.

Simulator Visualization

In our simulator, we visualized the data flow as follows

| Fetchthread waiting for clock tick | Decodethread waiting for clock tick | Executethread waiting for clock tick | MemoryThread waiting for clock tick | WBthread waiting for clock tick |
|--|-------------------------------------|--------------------------------------|-------------------------------------|---------------------------------|
| ----- | ----- | ----- | ----- | ----- |
| Clock Cycle count = 1 | | | | |
| Fetchthread starting new clock | Decodethread starting new clock | Executethread starting new clock | MemoryThread starting new clock | WBthread starting new clock |
| IMuxSel for current Cycle =0 | Reading data... | ReadOutg data... | ReadOutg data... | ReadOutg data... |
| ReadData for current Cycle =0 | PC=0 | PCOut=0 | PCOut=0 | PCOut=0 |
| UnitAddressOutput for current Cycle =0 | MC=0 | MCOut=0 | MCOut=0 | MCOut=0 |
| Fetch Instruction (PC = 0): 20080010 | PredictionOut=0 | RegWriteEnOut=0 | RegWriteEnOut=0 | RegWriteEnOut=0 |
| Is Flush = 0 | ##### | MemWriteEnOut=0 | MemWriteEnOut=0 | MemWriteEnOut=0 |
| IMuxSel after exe inp=0 | Writing data... | MemtoRegOut=0 | MemtoRegOut=0 | MemtoRegOut=0 |
| Writing data... | MC=0 | MemReadEnOut=0 | MemReadEnOut=0 | MemReadEnOut=0 |
| fPC = 00000001 fMC = 20080010 | PCin=0 | FCOut=0 | resultOut=0 | AddressOut=0 |
| PredictionIn=0 | RegWriteEnIn=1 | JrSignalOut=0 | MemreaddataOut=0 | WriteRegisterOut=0 |
| Fetchthread waiting for clock tick | MemWriteEnIn=0 | BranchOut=0 | WriteDataOut=0 | ##### |
| | MemtoRegIn=0 | ZeroSignalOut=0 | WriteRegisterOut=0 | mPC = 00000000 mMC = 0 |
| | MemReadEnIn=0 | ALUOpOut=0 | ##### | WBthread waiting for clock tick |
| | FCIn=0 | RegDstOut=0 | mPC = 00000000 mMC = 0 | |
| | FDIn=1 | readdata1Out=0 | Writing data... | |
| | JrSignalIn=0 | readdata2Out=0 | mPC = 00000000 mMC = 0 | |
| | BranchIn=0 | immediateOut=0 | PCIn=0 | |
| | ZeroSignalIn=0 | rsOut=0 | PCIn=0 | |
| | ALUOpIn=7 | rtOut=0 | RegWriteEnIn=0 | |
| | RegDstIn=1 | rdOut=0 | RegWriteEnIn=0 | |
| | readdata1In=0 | PredictionOut=0 | MemtoRegIn=0 | |
| | readdata2In=0 | ##### | ReadDataIn=0 | |
| | immediateIn=0 | is_Hit= 1 | AddressIn=0 | |
| | rsIn=0 | EXEdata.Branch= 0 | WriteRegisterIn=0 | |
| | rcrIn=0 | Writing data... | MemoryThread waiting for clock tick | |
| | rdIn=0 | PCIn=0 | | |
| | Prediction=0 | MCIn=0 | | |
| | Decoding logic done... | RegWriteEnIn=0 | | |
| | Decodethread waiting for clock tick | MemtoRegIn=0 | | |
| | | MemWriteEnIn=0 | | |
| | | MemReadEnIn=0 | | |
| | | resultIn=0 | | |
| | | WriteDataIn=0 | | |
| | | MemreaddataIn=0 | | |
| | | WriteRegisterIn=0 | | |
| | | ##### | | |
| | | mPC = 00000000 mMC = 0 | | |
| | | READDATA MEM after execute= ffffffff | | |
| | | Executethread waiting for clock tick | | |

Where each stage is represented by a column.

Each stage displays the values its reading from the previous pipe, and after it processes it displays what it is about to write to the next pipe in the next clock cycle.

Mind that the implicit write back stage here is shown in the simulator, but it behaves as expected and explain in the pipeline design chapter.

When the execution is done the simulator runs for some extra clock cycles to make sure that the pipeline is drained.

```
=====
Clock Cycle count = 21
Fetchthread starting new clock
No more instructions to fetch. Halt inserted
Wuxsel after exe inp=0
Writing data...
fPC = 00000000 fNC = 0
PredictionIn=0
Fetchthread waiting for clock tick

Decodethread starting new clock
Reading data...
PC=0
MC=0
PredictionOut=0
#####
Writing data...
PCin=0
RegWriteEnIn=1
MemWriteEnIn=0
MentoRegIn=0
MemReadEnIn=0
FCIn=0
FDir=1
JrSingalIn=0
BranchIn=0
ZeroSignalIn=0
ALUOpIn=7
RegDstIn=1
RegDstOut=0
readdata1Out=0
readdata2In=0
immediateIn=0
rsIn=0
rdIn=0
rdIn=0
Prediction=0
Decoding logic done...
Decodethread waiting for clock tick

Executethread starting new clock
ReadOutg data...
PCOut=0
MCOut=0
RegWriteEnOut=1
MemWriteEnOut=0
MentoRegOut=0
MemReadEnOut=0
FCOut=0
JrSingalOut=0
BranchOut=0
ZeroSignalOut=0
ALUOpOut=7
RegDstOut=1
readdata1Out=0
readdata2Out=0
immediateOut=0
rsOut=0
rtOut=0
rdOut=0
PredictionOut=0
#####
is_Hit= 1
EXEdata.Branch= 0
Writing data...
PCIn=0
MCIn=0
RegWriteEnIn=1
MentoRegIn=0
MemWriteEnIn=0
MemReadEnIn=0
resultIn=0
WriteDataIn=0
MemreaddataIn=ffffff
WriteRegisterIn=0
ePC = 00000000 eNC = 0
READDATA MEM after execute= fffffff
Executethread waiting for clock tick

MemoryThread starting new clock
ReadOutg data...
PCOut=0
MCOut=0
RegWriteEnOut=1
MentoRegOut=0
MemWriteEnOut=0
MemReadEnOut=0
resultOut=0
MemreaddataOut=ffffff
Writing data...
mPC = 00000000 mNC = 0
mPC = 00000000 mNC = 0
PCIn=0
MCIn=0
RegWriteEnIn=1
RegWriteEnIn=1
MentoRegIn=0
ReadDataIn=ffffff
AddressIn=0
WriteRegisterIn=0
MemoryThread waiting for clock tick

WBthread starting new clock
ReadOutg data...
PCOut=12
MCOut=22980002
RegWriteEnOut=1
MentoRegOut=0
ReaddataOut=ffffff
AddressOut=3
WriteRegisterOut=18
#####
wPC = 00000012 wNC = 22980002
WBthread waiting for clock tick
=====

Clock Cycle count = 22
Fetchthread starting new clock
No more instructions to fetch. Halt inserted
Wuxsel after exe inp=0
Writing data...
fPC = 00000000 fNC = 0
PredictionIn=0
Fetchthread waiting for clock tick

Decodethread starting new clock
Reading data...
PC=0
MC=0
PredictionOut=0
#####
Writing data...
PCin=0
RegWriteEnIn=1
MemWriteEnIn=0
MentoRegIn=0
MemReadEnIn=0
FCIn=0
FDir=1
JrSingalIn=0
BranchIn=0
ZeroSignalIn=0
ALUOpIn=7
RegDstIn=1
RegDstOut=0
readdata1Out=0
readdata2Out=0
immediateOut=0
rsOut=0
rtOut=0
rdOut=0
PredictionOut=0
#####
is_Hit= 1
EXEdata.Branch= 0
Writing data...
PCIn=0
MCIn=0
RegWriteEnIn=1
MentoRegIn=0
MemWriteEnIn=0
MemReadEnIn=0
resultIn=0
WriteDataIn=0
MemreaddataIn=ffffff
WriteRegisterIn=0
ePC = 00000000 eNC = 0
READDATA MEM after execute= fffffff
Executethread waiting for clock tick

MemoryThread starting new clock
ReadOutg data...
PCOut=0
MCOut=0
RegWriteEnOut=1
MentoRegOut=0
MemWriteEnOut=0
MemReadEnOut=0
resultOut=0
MemreaddataOut=ffffff
Writing data...
mPC = 00000000 mNC = 0
mPC = 00000000 mNC = 0
PCIn=0
MCIn=0
RegWriteEnIn=1
RegWriteEnIn=1
MentoRegIn=0
ReadDataIn=ffffff
AddressIn=0
WriteRegisterIn=0
MemoryThread waiting for clock tick

WBthread starting new clock
ReadOutg data...
PCOut=0
MCOut=0
RegWriteEnOut=1
MentoRegOut=0
ReaddataOut=ffffff
AddressOut=0
WriteRegisterOut=0
#####
wPC = 00000000 wNC = 0
WBthread waiting for clock tick
=====
```

And when the execution of the given program is finished, we dump the values of the register.

```
=====
Clock Cycle count = 24
Fetchthread starting new clock
No more instructions to fetch. Halt inserted
JMUXSel after exe inp=0
Writing data...
  fPC = 00000000 fMC = 0
PredictionInF=0
Register File Contents:
R0: 0
R1: 0
R2: 0
R3: 0
R4: 0
R5: 0
R6: 0
R7: 0
R8: 10
R9: 5
R10: 15
R11: 15
R12: fffffffea
R13: 1
R14: 0
R15: 0
R16: 10
R17: 10
R18: 50
R19: 0
R20: 1
R21: 1
R22: 0
R23: 0
R24: 3
R25: 0
R26: 0
R27: 0
R28: 0
R29: 7fffffffcc
R30: 0
R31: 0

Decodethread starting new clock
Reading data...
PC=0
MC=0
PredictionOutD=0
#####
Writing data...
MC=0
PCIn=0
RegWriteEnin=1
MemWriteEnin=0
MemtoRegin=0
MemReadEnin=0
FCin=0
FDin=1
JrSignalin=0
Branchin=0
ZeroSignalin=0
ALUOpin=7
RegDstin=1
readdata1in=0
readdata2in=0
immediatein=0
rsin=0
rtin=0
rdin=0
Prediction=0
Decoding logic done...

C:\Users\USER\Desktop\PIipelineCAS3\CAS\x64\Debug\CAS.exe (process 34924) exited
To automatically close the console when debugging stops, enable Tools->Options-
Press any key to close this window . . .
```

If there was memory access in the program, a file containing the memory elements after execution

Our simulator is yet to support, memory initialization. The User must use SW instruction to store data in the memory.

