SPI Test Plan

- Test reset value.

- Begin a certain number of a write (write address then write data) communication protocol, by creating two dynamic arrays to store random address/data and insert them via MOSI pin.
- Create two dynamic arrays to store address/data and an associative array to compare the data retrieved from MISO pin with it.

- Retrieve the random data (read address then read data) that stored in the random addresses via MISO port.

- Finally, Test reset value again.

Cover Points:

- Input pin SS_n: Transition from 1 ➔ 0 and from 0 ➔ 1 (Cover both start and end CMDs)

- **Input pin MOSI:** Check that all commands have been executed, this done by creating a signal called REQ_COMM which start sampling directly after asserted SS_n to begin communication and stop sampling it right after receiving three bits of MOSI which detect the command from master.
- Cover all transitions from state to IDLE , and from IDLE to CHK_CMD by creating enum for FSM states.

Bug Report

No bugs detected.

SPI SLAVE Sequences

Feature	Assertion
Whenever the rst_n is asserted, it checks if the MISO is equal to 0	@(posedge clk_sva) $fell(rst_n_sva) |-> (!MISO_sva);

WAVEFORM