Project 2

- *Code:*

```
module SPI_Slave (
    MOSI,
    MISO,
    SS_n,
    SCK,
    rst_n,
    rx_data,
    rx_valid,
    tx_data,
    tx_valid
);

  parameter IDLE = 3'b000;
  parameter CHK_CMD = 3'b001;
  parameter READ_ADD = 3'b010;
  parameter READ_DATA = 3'b011;
  parameter WRITE = 3'b100;

  input MOSI, SS_n;
  input SCK, rst_n;
  output reg MISO;

  input [7:0] tx_data;
  input tx_valid;
  output reg [9:0] rx_data;
  output reg rx_valid;

  reg [3:0] wr_counter;
  reg [2:0] rd_counter;
  reg read_addr_received;
  wire invalid_wr, invalid_rd_addr, invalid_rd_data;
```

```
  (* fsm_encoding = "gray"*)
  reg [2:0] cs, ns;


  //handle invalid cases
  assign invalid_wr = (cs == WRITE) && (wr_counter == 7) &&
(rx_data[9:8] != 2'b00) && (rx_data[9:8] != 2'b01);
  assign invalid_rd_addr = (cs == READ_ADD) && (wr_counter ==
7) && (rx_data[9:8] != 2'b10);
  assign invalid_rd_data = (cs == READ_DATA) && (wr_counter ==
7) && (rx_data[9:8] != 2'b11);

  // next state logic
  always @(*) begin
    case (cs)
      IDLE: begin
        if (~SS_n) begin
          ns = CHK_CMD;
        end else begin
          ns = IDLE;
        end
      end
      CHK_CMD: begin
        if (~SS_n && MOSI && read_addr_received) begin
          ns = READ_DATA;
        end else if (~SS_n && MOSI && ~read_addr_received)
begin
          ns = READ_ADD;
        end else if (~SS_n && ~MOSI) begin
          ns = WRITE;
        end else begin
          ns = IDLE;
        end
      end
      WRITE: begin
        if (SS_n || wr_counter == 0 || invalid_wr) begin
```

```
        ns = IDLE;
      end else begin
        ns = WRITE;
      end
    end
    READ_ADD: begin
      if (SS_n || wr_counter == 0 || invalid_rd_addr) begin
        ns = IDLE;
      end else begin
        ns = READ_ADD;
      end
    end
    READ_DATA: begin
      if (SS_n || rd_counter == 0 || invalid_rd_data) begin
        ns = IDLE;
      end else begin
        ns = READ_DATA;
      end
    end
    default: ns = IDLE;
  endcase
end

// state memory
always @(posedge SCK) begin
  if (~rst_n) begin
    cs <= IDLE;
  end else begin
    cs <= ns;
  end
end

// output logic
always @(posedge SCK) begin
  if (~rst_n) begin
    wr_counter <= 0;
```

```
      rd_counter <= 0;
      rx_data <= 0;
      read_addr_received <= 0;
      MISO <= 0;
      rx_valid <= 0;
    end else begin
      case (cs)
        IDLE: begin
          wr_counter <= 9;
          rd_counter <= 7;
          rx_data <= 0;
          rx_valid <= 0;
          MISO <= 0;
        end
        WRITE: begin
          // drive rx_data bus with parallel write address /
data
          rx_data[wr_counter] <= MOSI;
          wr_counter <= (wr_counter > 0) ? wr_counter - 1 : 0;
          // check data is valid or not
          rx_valid <= (wr_counter == 0) ? 1 : 0;
        end
        READ_ADD: begin
          // drive rx_data bus with parallel read address
          rx_data[wr_counter] <= MOSI;
          wr_counter <= (wr_counter > 0) ? wr_counter - 1 : 0;
          // check data is valid or not
          rx_valid <= (wr_counter == 0) ? 1 : 0;
          // indicate address is received
          read_addr_received <= (wr_counter == 0) ? 1 : 0;
        end
        READ_DATA: begin
          // indicate received address is used and waiting for
new address
          read_addr_received <= 0;
          // check data is valid or not
```

```
          rx_valid <= (wr_counter == 0) ? 1 : 0;
          if (wr_counter != 0) begin
            // drive rx_data bus with parallel read command &
dummy data
            rx_data[wr_counter] <= MOSI;
            wr_counter <= (wr_counter > 0) ? wr_counter - 1 :
0;
          end else if (tx_valid) begin
            // receive parallel data and convert it to serial
on MISO port
            MISO <= tx_data[rd_counter];
            rd_counter <= rd_counter - 1;
          end
        end
      endcase
    end
  end

endmodule
```

```
module RAM (
    din,
    clk,
    rst_n,
    rx_valid,
    dout,
    tx_valid
);

  parameter MEM_DEPTH = 256;
  parameter ADDR_SIZE = 8;

  input [9:0] din;
  input clk, rst_n, rx_valid;
  output reg [7:0] dout;
```

```
output reg tx_valid;

reg [7:0] mem[MEM_DEPTH-1:0];
reg [ADDR_SIZE-1:0] addr;


// memory read and write operations
always @(posedge clk) begin
  if (~rst_n) begin
    dout <= 0;
    addr <= 0;
    tx_valid <= 0;
  end else begin
    casex ({
      din[9:8], rx_valid
    })
      3'b001: begin
        addr <= din[7:0];
      end
      3'b011: begin
        mem[addr] <= din[7:0];
      end
      3'b101: begin
        addr <= din[7:0];
      end
      3'b111: begin
        dout <= mem[addr];
        tx_valid <= 1;
      end
      default: begin
        dout <= 0;
        tx_valid <= 0;
      end
    endcase
  end
end
```

```
endmodule
```

- *Testbench:*

```
module tb ();
  reg MOSI, SS_n, clk, rst_n;
  wire MISO;

  SPI_wrapper wrapper (
      MOSI,
      MISO,
      SS_n,
      clk,
      rst_n
  );

  initial begin
    clk = 0;
    forever begin
      #20 clk = ~clk;
    end
  end

  initial begin
    ////////////////////////////////////////
    // Test reset and memory initialization
    ////////////////////////////////////////
    rst_n = 0;
    $readmemb("mem.dat", wrapper.ram.mem, 0, 255);
    repeat (5) begin
      MOSI = $random;
      SS_n = $random;
      @(negedge clk);
    end

    ////////////////////////////////////////
    // Test writing
```

```
    ////////////////////////////////////
    // deactivate reset & activate slave select
    rst_n = 1;
    SS_n  = 0;

    // test write-address command
    MOSI  = 0;
    @(negedge clk);
    MOSI = 0;
    @(negedge clk);
    MOSI = 0;
    @(negedge clk);
    repeat (9) begin
      MOSI = $random;
      @(negedge clk);
    end

    // test write data
    MOSI = $random;
    @(negedge clk);
    MOSI = 0;
    @(negedge clk);
    MOSI = 0;
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    repeat (8) begin
      MOSI = $random;
      @(negedge clk);
    end

    ////////////////////////////////
    // Test memory read functionality
    ////////////////////////////////
    // test read-address holding command
    MOSI = $random;
```

```
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    MOSI = 0;
    @(negedge clk);
    repeat (8) begin
      MOSI = $random;
      @(negedge clk);
    end

    // test read data
    MOSI = $random;
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    MOSI = 1;
    repeat (20) begin
      MOSI = $random;
      @(negedge clk);
    end

    ////////////////////////
    // Test invalid cases
    ////////////////////////
    // test write-address command
    MOSI = 0;
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    MOSI = 0;
    @(negedge clk);
    repeat (9) begin
```

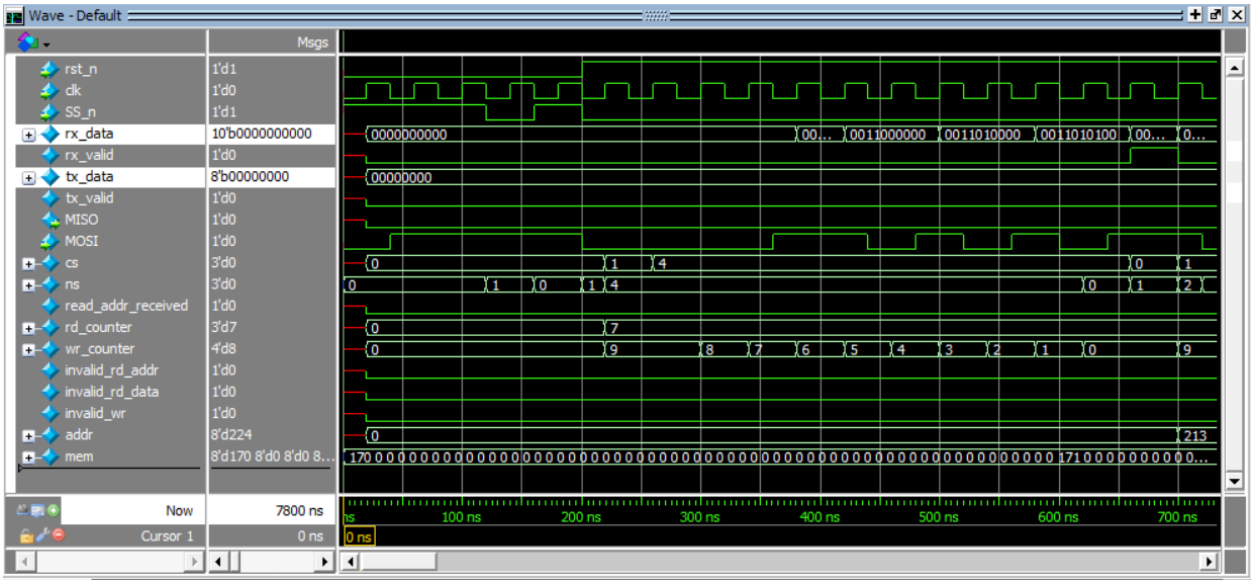
```
    MOSI = $random;
    @(negedge clk);
  end

  // test write data
  MOSI = $random;
  @(negedge clk);
  MOSI = 0;
  @(negedge clk);
  MOSI = 0;
  @(negedge clk);
  MOSI = 1;
  @(negedge clk);
  repeat (8) begin
    MOSI = $random;
    @(negedge clk);
  end

  // test invalid read-address holding command
  MOSI = $random;
  @(negedge clk);
  MOSI = 1;
  @(negedge clk);
  MOSI = 1;
  @(negedge clk);
  MOSI = 1;
  @(negedge clk);
  repeat (8) begin
    MOSI = $random;
    @(negedge clk);
  end

  // test read-address holding command
  MOSI = $random;
  @(negedge clk);
  MOSI = 1;
```

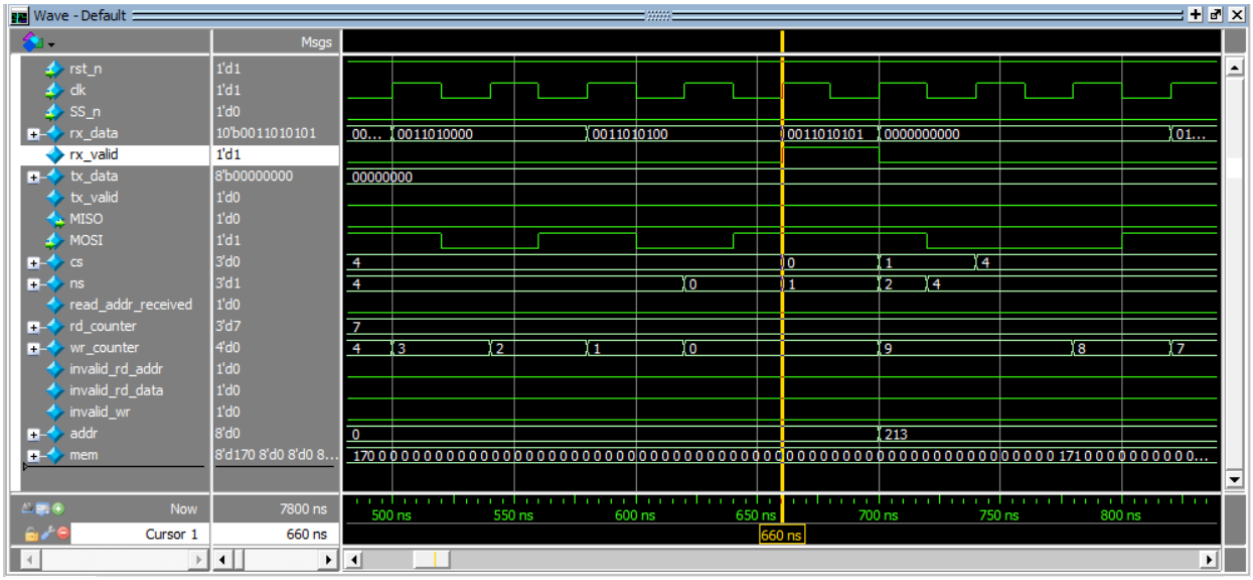
```
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    MOSI = 0;
    @(negedge clk);
    repeat (8) begin
      MOSI = $random;
      @(negedge clk);
    end

    // test read data
    MOSI = $random;
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    MOSI = 1;
    @(negedge clk);
    MOSI = 0;
    repeat (30) begin
      MOSI = $random;
      @(negedge clk);
    end

    ////////////////////////////////////////////////
    // test randomized data/address writing & reading
    ////////////////////////////////////////////////
    // randomized slave select
    repeat (50) begin
      MOSI = $random;
      SS_n = $random;
      @(negedge clk);
    end
    $stop;
  end
endmodule
```

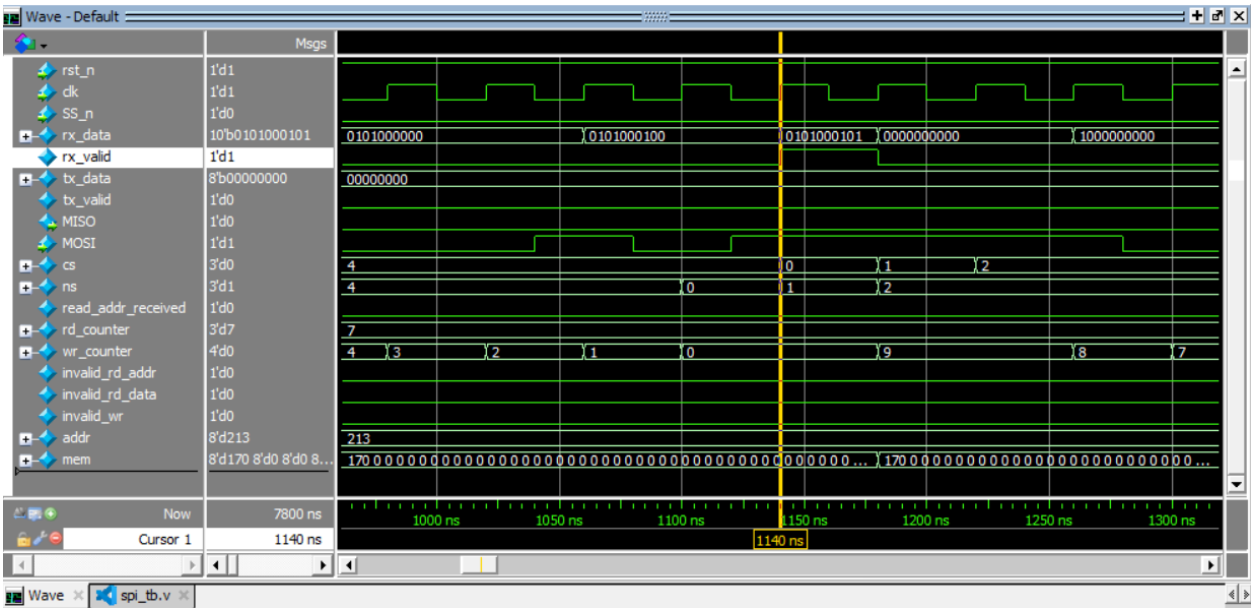
- *Do file:*

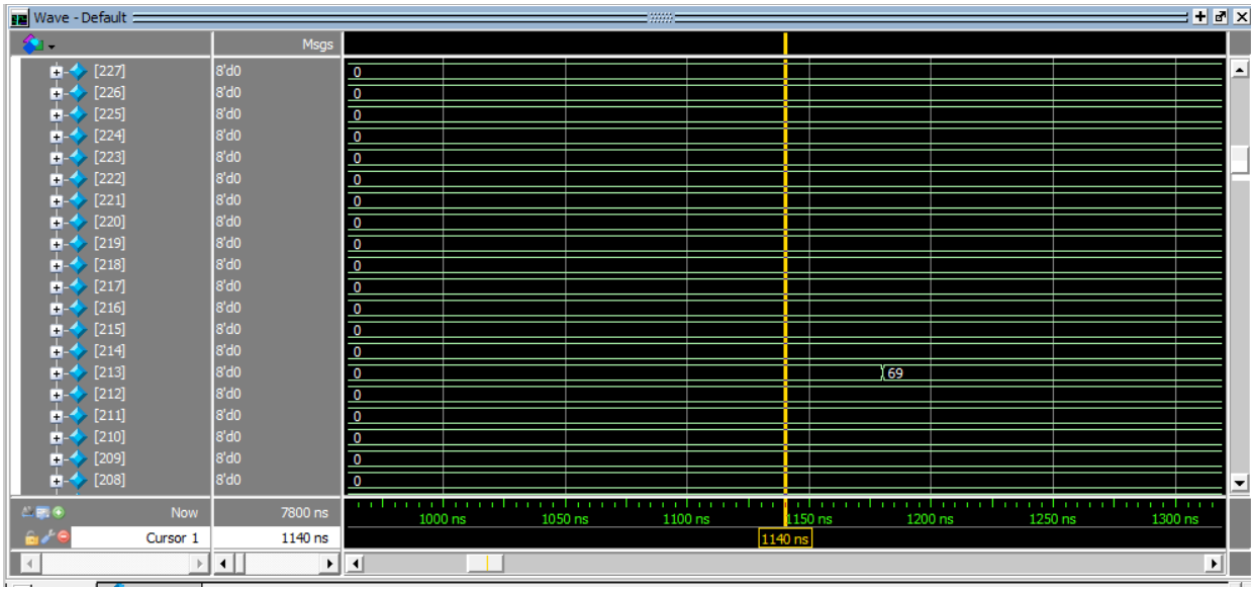
```
vlib work
vlog ram.v spi_slave.v wrapper.v spi_tb.v
vsim -voptargs=+acc work.tb

add wave -position insertpoint  \
sim:/tb/wrapper/rst_n \
sim:/tb/wrapper/clk \
sim:/tb/wrapper/SS_n \
sim:/tb/wrapper/rx_data \
sim:/tb/wrapper/rx_valid \
sim:/tb/wrapper/tx_data \
sim:/tb/wrapper/tx_valid \
sim:/tb/wrapper/MISO \
sim:/tb/wrapper/MOSI

add wave -position insertpoint  \
sim:/tb/wrapper/slave/cs \
sim:/tb/wrapper/slave/ns \
sim:/tb/wrapper/slave/read_addr_received \
sim:/tb/wrapper/slave/rd_counter \
sim:/tb/wrapper/slave/wr_counter \
sim:/tb/wrapper/slave/invalid_rd_addr \
sim:/tb/wrapper/slave/invalid_rd_data \
sim:/tb/wrapper/slave/invalid_wr

add wave -position insertpoint  \
sim:/tb/wrapper/ram/addr \
sim:/tb/wrapper/ram/mem

run -all
#quit -sim
```

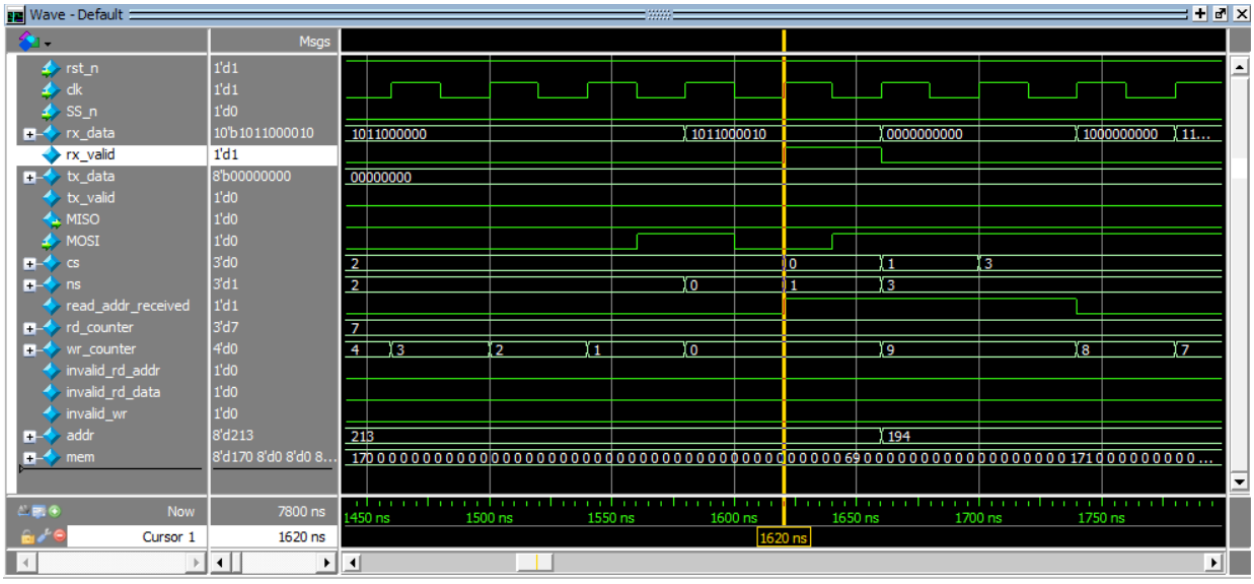
- *Waveform:*

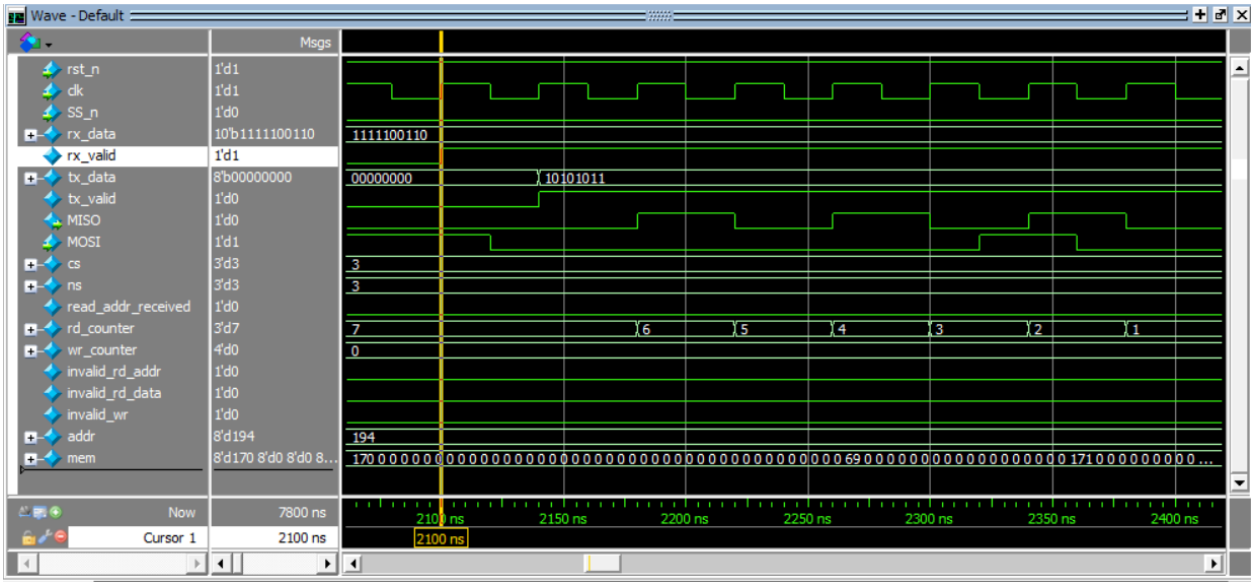

Wave - Default
Msgs
rst_n
clk
SS_n
rx_data
rx_valid
tx_data
tx_valid
MISO
MOSI
cs
ns
read_addr_received
rd_counter
wr_counter
invalid_rd_addr
invalid_rd_data
invalid_wr
addr
mem
Now
7800 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns

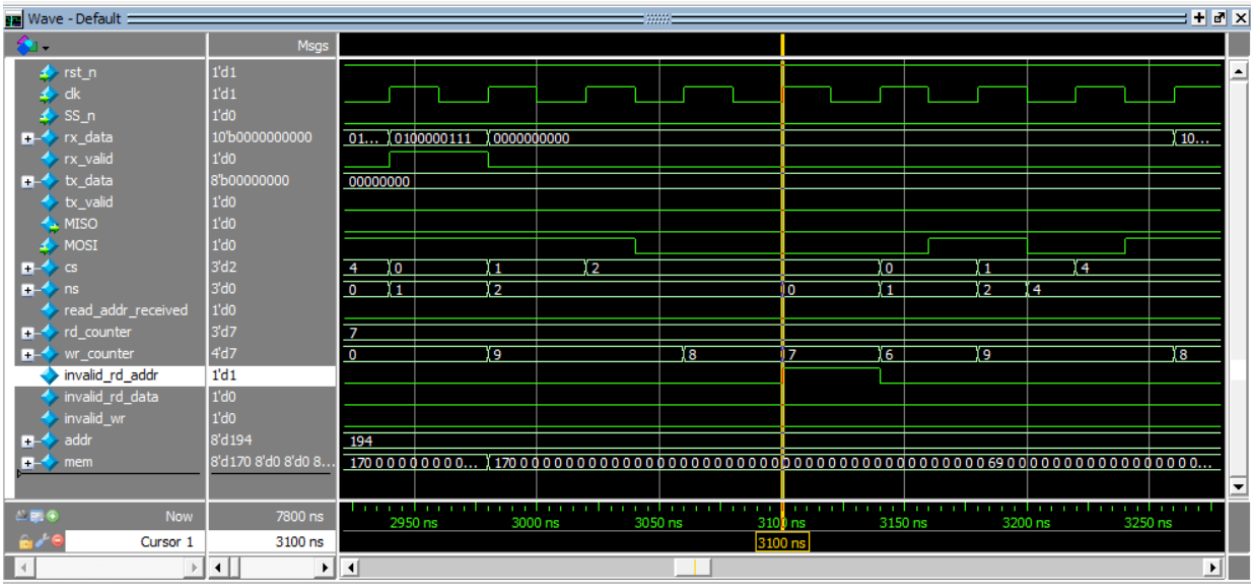

Wave - Default
Msgs
rst_n
clk
SS_n
rx_data
rx_valid
tx_data
tx_valid
MISO
MOSI
cs
ns
read_addr_received
rd_counter
wr_counter
invalid_rd_addr
invalid_rd_data
invalid_wr
addr
mem
Now
7800 ns
Cursor 1
660 ns
500 ns
550 ns
600 ns
650 ns
700 ns
750 ns
800 ns

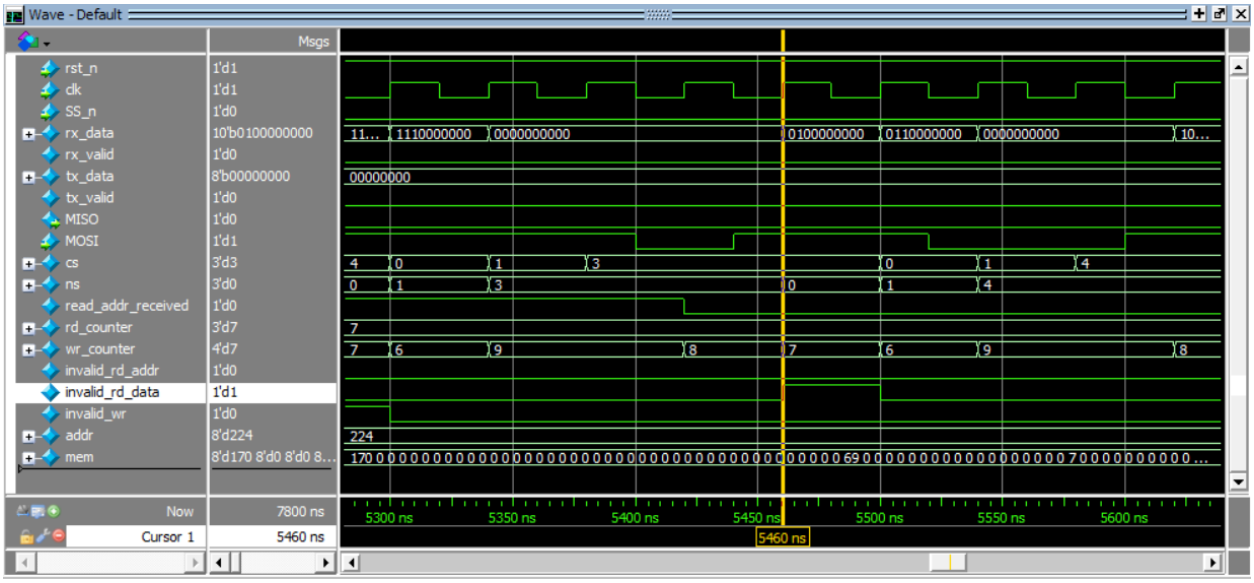

Wave - Default
Msgs
rst_n
clk
SS_n
rx_data
rx_valid
tx_data
tx_valid
MISO
MOSI
cs
ns
read_addr_received
rd_counter
wr_counter
invalid_rd_addr
invalid_rd_data
invalid_wr
addr
mem
1'd1
1'd1
1'd0
10'b0101000101
1'd1
8'b00000000
1'd0
1'd0
1'd1
3'd0
3'd1
1'd0
3'd7
4'd0
1'd0
1'd0
1'd0
8'd213
8'd170 8'd0 8'd0 8...
0101000000
0101000100
0101000101
0000000000
1000000000
00000000
Now
7800 ns
Cursor 1
1140 ns
1000 ns
1050 ns
1100 ns
1150 ns
1200 ns
1250 ns
1300 ns
Wave
spi_tb.v

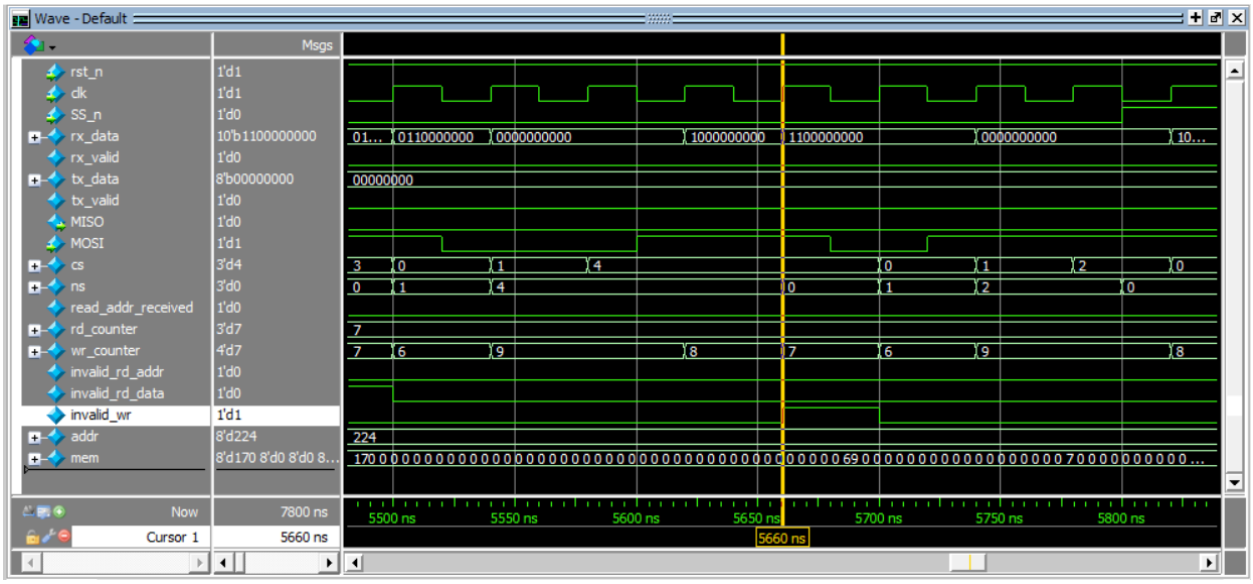

Wave - Default
Msgs
[227]
[226]
[225]
[224]
[223]
[222]
[221]
[220]
[219]
[218]
[217]
[216]
[215]
[214]
[213]
[212]
[211]
[210]
[209]
[208]
8'd0
69
Now
7800 ns
Cursor 1
1140 ns
1000 ns
1050 ns
1100 ns
1150 ns
1200 ns
1250 ns
1300 ns


Wave - Default
Msgs
rst_n
clk
SS_n
rx_data
rx_valid
tx_data
tx_valid
MISO
MOSI
cs
ns
read_addr_received
rd_counter
wr_counter
invalid_rd_addr
invalid_rd_data
invalid_wr
addr
mem
1'd1
1'd1
1'd0
10'b1011000010
1'd1
8'b00000000
1'd0
1'd0
1'd0
3'd0
3'd1
1'd1
3'd7
4'd0
1'd0
1'd0
1'd0
8'd213
8'd170 8'd0 8'd0 8...
1011000000
1011000010
0000000000
1000000000
11...
00000000
213
194
Now
7800 ns
Cursor 1
1620 ns
1450 ns
1500 ns
1550 ns
1600 ns
1650 ns
1700 ns
1750 ns
1620 ns

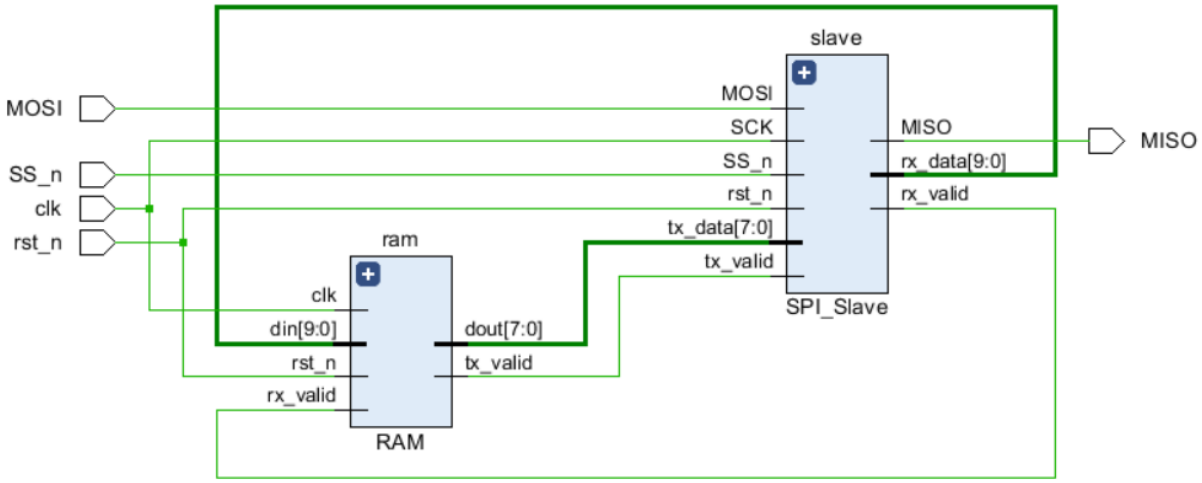

Wave - Default
Msgs
rst_n
clk
SS_n
rx_data
rx_valid
tx_data
tx_valid
MISO
MOSI
cs
ns
read_addr_received
rd_counter
wr_counter
invalid_rd_addr
invalid_rd_data
invalid_wr
addr
mem
1'd1
1'd1
1'd0
10'b1111100110
1'd1
8'b00000000
1'd0
1'd0
1'd1
3'd3
3'd3
1'd0
3'd7
4'd0
1'd0
1'd0
1'd0
8'd194
8'd170 8'd0 8'd0 8...
1111100110
00000000
10101011
194
Now
7800 ns
Cursor 1
2100 ns
2100 ns
2150 ns
2200 ns
2250 ns
2300 ns
2350 ns
2400 ns
2100 ns


Wave - Default
Msgs
rst_n
clk
SS_n
rx_data
rx_valid
tx_data
tx_valid
MISO
MOSI
cs
ns
read_addr_received
rd_counter
wr_counter
invalid_rd_addr
invalid_rd_data
invalid_wr
addr
mem
1'd1
1'd1
1'd0
10'b0000000000
1'd0
8'b00000000
1'd0
1'd0
1'd0
3'd2
3'd0
1'd0
3'd7
4'd7
1'd1
1'd0
1'd0
8'd194
8'd170 8'd0 8'd0 8...
01...
0100000111
0000000000
10...
00000000
194
Now
7800 ns
Cursor 1
3100 ns
2950 ns
3000 ns
3050 ns
3150 ns
3200 ns
3250 ns

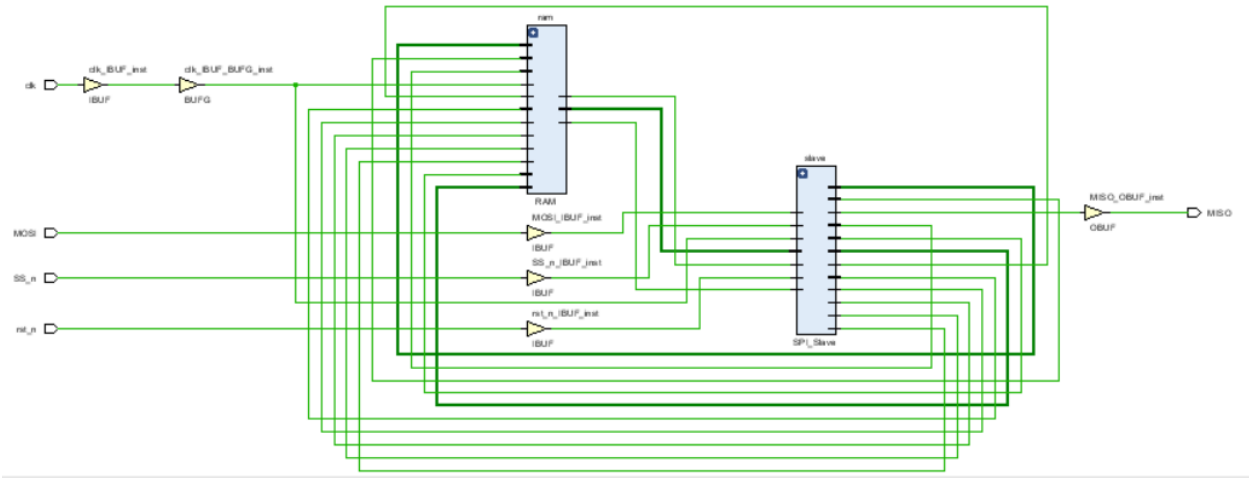

Wave - Default
Msgs
rst_n
clk
SS_n
rx_data
rx_valid
tx_data
tx_valid
MISO
MOSI
cs
ns
read_addr_received
rd_counter
wr_counter
invalid_rd_addr
invalid_rd_data
invalid_wr
addr
mem
1'd1
1'd1
1'd0
10'b0100000000
1'd0
8'b00000000
1'd0
1'd0
1'd1
3'd3
3'd0
1'd0
3'd7
4'd7
1'd0
1'd1
1'd0
8'd224
8'd170 8'd0 8'd0 8...
11...
1110000000
0000000000
0100000000
0110000000
10...
00000000
224
Now
7800 ns
Cursor 1
5460 ns
5300 ns
5350 ns
5400 ns
5450 ns
5500 ns
5550 ns
5600 ns



- *Elaboration*



- *Synthesis:*



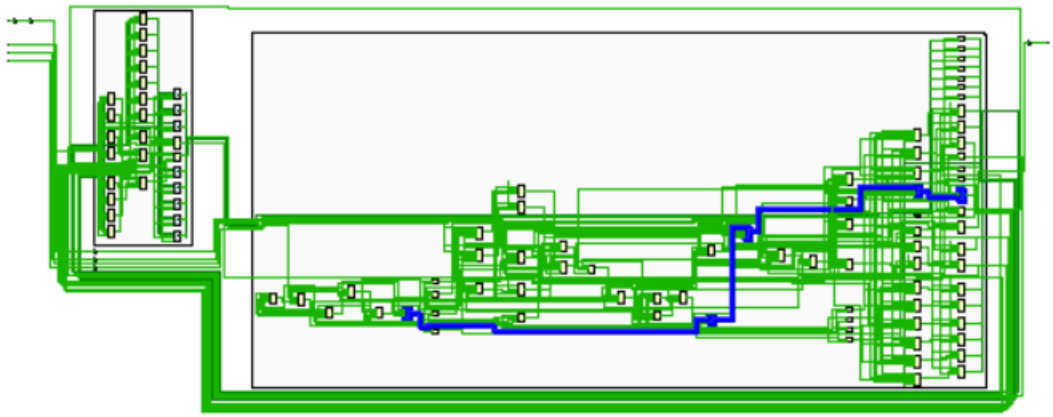
1. *Gray:*

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
READ_DATA	011	011
READ_ADD	010	010
WRITE	111	100

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'gray' in module 'SPI_Slave'
```

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.443 ns	Worst Hold Slack (WHS):	0.077 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	382	Total Number of Endpoints:	382	Total Number of Endpoints:	73

All user specified timing constraints are met.



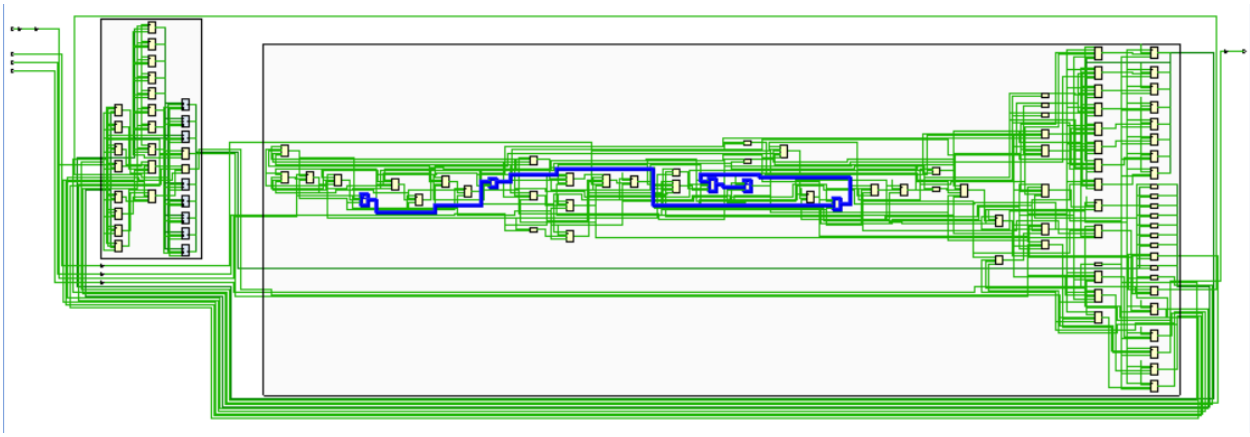
2. *One-hot:*

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
READ_DATA	00100	011
READ_ADD	01000	010
WRITE	10000	100

```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'one-hot' in module 'SPI_Slave'
```

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.654 ns	Worst Hold Slack (WHS):	0.077 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	384	Total Number of Endpoints:	384	Total Number of Endpoints:	75

All user specified timing constraints are met.



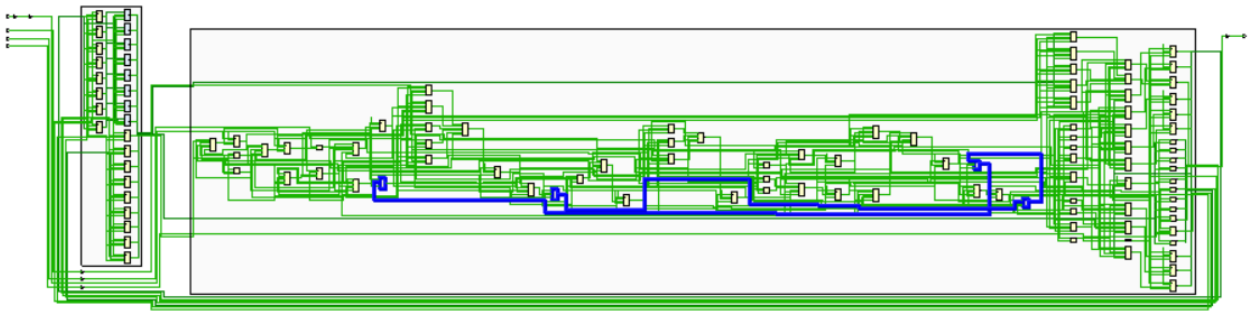
3. *Binary (chosen):*

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
READ_DATA	010	011
READ_ADD	011	010
WRITE	100	100

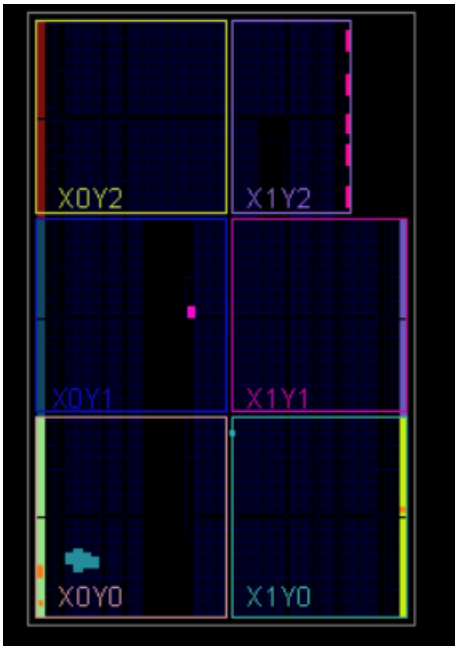
```
INFO: [Synth 8-3354] encoded FSM with state register 'cs_reg' using encoding 'sequential' in module 'SPI_Slave'
```

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.936 ns	Worst Hold Slack (WHS):	0.077 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	382	Total Number of Endpoints:	382	Total Number of Endpoints:	73

All user specified timing constraints are met.



- *Implementation:*
  - *Without debug core:*

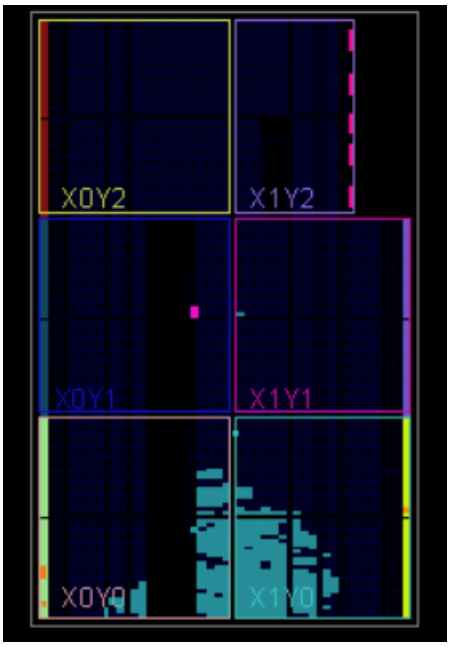


Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	5.928 ns	Worst Hold Slack (WHS):	0.052 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	382	Total Number of Endpoints:	382	Total Number of Endpoints:	73

All user specified timing constraints are met.

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
N SPI_wrapper	89	40	16	8	26	57	32	27	5	1
ram (RAM)	32	17	16	8	13	0	32	0	0	0
slave (SPI_Slave)	57	23	0	0	16	57	0	23	0	0

- *With debug core:*



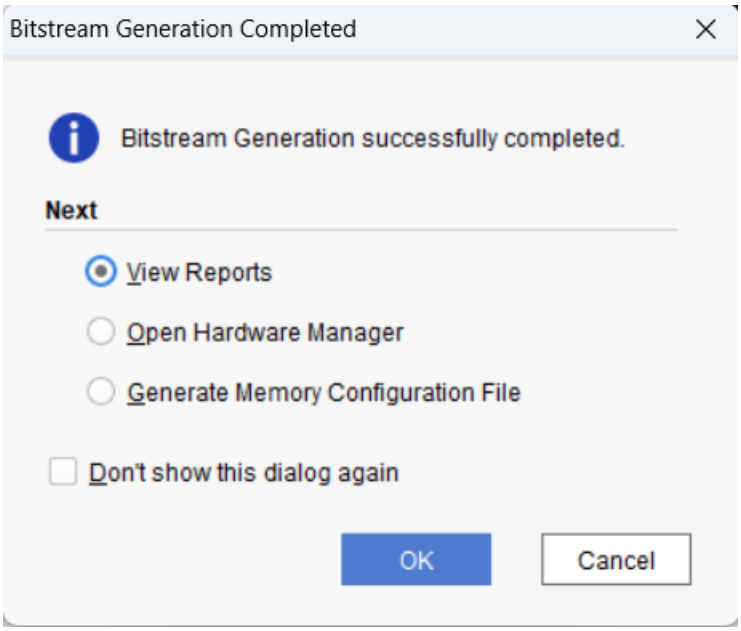
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.216 ns	Worst Hold Slack (WHS):	-0.353 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	-0.625 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	2	Number of Failing Endpoints:	0
Total Number of Endpoints:	4167	Total Number of Endpoints:	4151	Total Number of Endpoints:	2173

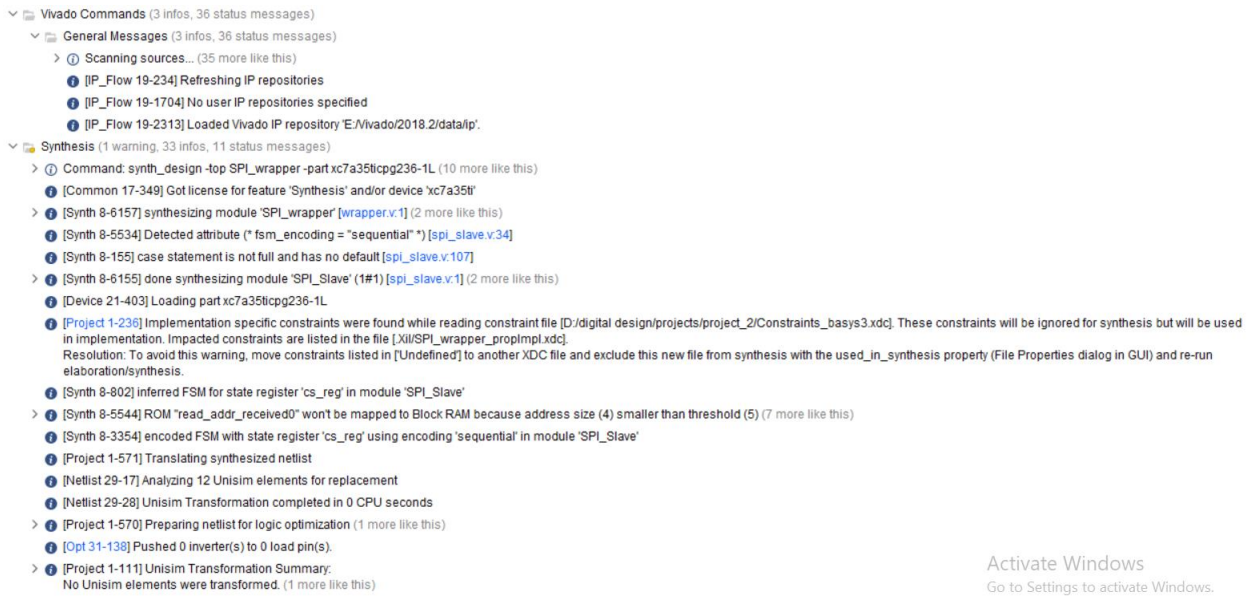
Timing constraints are not met.

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
SPI_wrapper	1328	1956	26	8	642	1188	140	762	0.5	5	2	1
dbg_hub (dbg_hub)	475	727	0	0	242	451	24	316	0	0	1	1
ram (RAM)	32	17	16	8	12	0	32	0	0	0	0	0
slave (SPI_Slave)	57	23	0	0	18	57	0	23	0	0	0	0
u_ila_0 (u_ila_0)	764	1189	10	0	375	680	84	418	0.5	0	0	0

- *Bitstream Generation:*



- *Messages:*
  - *Without debug core:*



- [Common 17-83] Releasing license: Synthesis
- [Constraints 18-5210] No constraint will be written out.
- [Common 17-1381] The checkpoint 'D:/digital design/projects/project_2/SPI Project/SPI Project.runs/synth_1/SPI_wrapper.dcp' has been generated.
- [runtcl-4] Executing : report_utilization -file SPI_wrapper_utilization_synth.rpt -pb SPI_wrapper_utilization_synth.pb
- [Common 17-206] Exiting Vivado at Thu Aug 22 03:53:23 2024...

Implementation (112 infos, 239 status messages)

Design Initialization (11 infos, 7 status messages)

- Command: open_checkpoint {D:/digital design/projects/project_2/SPI Project/SPI Project.runs/impl_1/SPI_wrapper.dcp} (6 more like this)
- [Netlist 29-17] Analyzing 12 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Device 21-403] Loading part xc7a35ticpg236-1L
- [Project 1-570] Preparing netlist for logic optimization
- [Timing 38-478] Restoring timing data from binary archive.
- [Timing 38-479] Binary timing data restore complete.
- [Project 1-856] Restoring constraints from binary archive.
- [Project 1-853] Binary constraint restore complete.
- [Project 1-111] Unisim Transformation Summary:
  A total of 8 instances were transformed.
  RAM256X1S => RAM256X1S (MUXF7, MUXF7, MUXF8, RAMS64E, RAMS64E, RAMS64E, RAMS64E): 8 instances
- [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646

Opt Design (24 infos, 45 status messages)

- Command: opt_design (44 more like this)
- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
- [Project 1-461] DRC finished with 0 Errors
- [Project 1-462] Please refer to the DRC report (report_drc) for more information.
- [Timing 38-35] Done setting XDC timing constraints.
- [Opt 31-49] Retargeted 0 cell(s).
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
- [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
- [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
- [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
- [Common 17-83] Releasing license: Implementation
- [Timing 38-480] Writing timing data to binary archive.
- [Common 17-1381] The checkpoint 'D:/digital design/projects/project_2/SPI Project/SPI Project.runs/impl_1/SPI_wrapper_opt.dcp' has been generated.
- [runtcl-4] Executing : report_drc -file SPI_wrapper_drc_opted.rpt -pb SPI_wrapper_drc_opted.pb -rpx SPI_wrapper_drc_opted.rpx
- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'E:/Vivado/2018.2/data/ip'.
- [DRC 23-27] Running DRC with 2 threads (1 more like this)
- [Coretcl 2-168] The results of DRC are in file SPI_wrapper_drc_opted.rpt.

Place Design (21 infos, 90 status messages)

- Command: place_design (89 more like this)
- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
- [DRC 23-27] Running DRC with 2 threads (1 more like this)
- [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
- [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
- [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
- [Physopt 32-65] No nets found for high-fanout optimization.
- [Physopt 32-232] Optimized 0 net. Created 0 new instance.
- [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
- [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
- [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
- [Place 30-746] Post Placement Timing Summary WNS=6.770. For the most accurate timing information please run report_timing.
- [Common 17-83] Releasing license: Implementation
- [Timing 38-480] Writing timing data to binary archive.
- [Common 17-1381] The checkpoint 'D:/digital design/projects/project_2/SPI Project/SPI Project.runs/impl_1/SPI_wrapper_placed.dcp' has been generated.
- [runtcl-4] Executing : report_io -file SPI_wrapper_io_placed.rpt (2 more like this)

Route Design (34 infos, 77 status messages)

- Command: route_design (76 more like this)
- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
- [Vivado_Tcl 4-198] DRC finished with 0 Errors
- [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
- [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
- [Route 35-416] Intermediate Timing Summary | WNS=6.754 | TNS=0.000 | WHS=-0.203 | THS=-25.280| (2 more like this)
- [Route 35-57] Estimated Timing Summary | WNS=5.892 | TNS=0.000 | WHS=0.049 | THS=0.000 |
- [Route 35-327] The final timing numbers are based on the router estimated timing analysis. For a complete and accurate timing signoff, please run report_timing_summary.
- [Route 35-16] Router Completed Successfully
- [Common 17-83] Releasing license: Implementation
- [Timing 38-480] Writing timing data to binary archive.
- [Common 17-1381] The checkpoint 'D:/digital design/projects/project_2/SPI Project/SPI Project.runs/impl_1/SPI_wrapper_routed.dcp' has been generated.
- [DRC 23-27] Running DRC with 2 threads (1 more like this)
- [Coretcl 2-168] The results of DRC are in file SPI_wrapper_drc_routed.rpt.
- [runtcl-4] Executing : report_drc -file SPI_wrapper_drc_routed.rpt -pb SPI_wrapper_drc_routed.pb -rpx SPI_wrapper_drc_routed.rpx (7 more like this)
- [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
- [DRC 23-133] Running Methodology with 2 threads
- [Coretcl 2-1520] The results of Report Methodology are in file SPI_wrapper_methodology_drc_routed.rpt.
- [Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.
- [Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)
- [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)

Write Bitstream (22 infos, 20 status messages)

- Command: open_checkpoint SPI_wrapper_routed.dcp (19 more like this)
- [Netlist 29-17] Analyzing 12 Unisim elements for replacement
- [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
- [Project 1-479] Netlist was created with Vivado 2018.2
- [Device 21-403] Loading part xc7a35ticpg236-1L
- [Project 1-570] Preparing netlist for logic optimization
- [Timing 38-478] Restoring timing data from binary archive.
- [Timing 38-479] Binary timing data restore complete.
- [Project 1-856] Restoring constraints from binary archive.
- [Project 1-853] Binary constraint restore complete.
- [Project 1-111] Unisim Transformation Summary:
  A total of 8 instances were transformed.
  RAM256X1S => RAM256X1S (MUXF7, MUXF7, MUXF8, RAMS64E, RAMS64E, RAMS64E, RAMS64E): 8 instances
- [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
- [IP_Flow 19-234] Refreshing IP repositories
- [IP_Flow 19-1704] No user IP repositories specified
- [IP_Flow 19-2313] Loaded Vivado IP repository 'E:/Vivado/2018.2/data/ip'.
- [DRC 23-27] Running DRC with 2 threads
- [Vivado 12-3199] DRC finished with 0 Errors
- [Vivado 12-3200] Please refer to the DRC report (report_drc) for more information.
- [Designutils 20-2272] Running write_bitstream with 2 threads.
- [Vivado 12-1842] Bitgen Completed Successfully.
- [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage_statistics_webtalk.html or usage_statistics_webtalk.xml file in the implementation directory.
- [Common 17-83] Releasing license: Implementation

- Implemented Design (9 infos, 6 status messages)
  - General Messages (9 infos, 6 status messages)
    - [Netlist 29-17] Analyzing 12 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Project 1-570] Preparing netlist for logic optimization
    - [Timing 38-478] Restoring timing data from binary archive.
    - [Timing 38-479] Binary timing data restore complete.
    - [Project 1-856] Restoring constraints from binary archive.
    - [Project 1-853] Binary constraint restore complete.
    - Reading XDEF placement. (5 more like this)
    - [Project 1-111] Unisim Transformation Summary:
      A total of 8 instances were transformed.
      RAM256X1S => RAM256X1S (MUXF7, MUXF7, MUXF8, RAMS64E, RAMS64E, RAMS64E, RAMS64E): 8 instances

- *With debug core:*

- Implementation (1 critical warning, 3 warnings, 108 infos, 249 status messages)
  - Design Initialization (11 infos, 7 status messages)
    - Command: open_checkpoint {D:/digital design/projects/project_2/SPI Project/SPI Project.runs/impl_1/SPI_wrapper.dcp} (6 more like this)
    - [Netlist 29-17] Analyzing 12 Unisim elements for replacement
    - [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds
    - [Project 1-479] Netlist was created with Vivado 2018.2
    - [Device 21-403] Loading part xc7a35ticpg236-1L
    - [Project 1-570] Preparing netlist for logic optimization
    - [Timing 38-478] Restoring timing data from binary archive.
    - [Timing 38-479] Binary timing data restore complete.
    - [Project 1-856] Restoring constraints from binary archive.
    - [Project 1-853] Binary constraint restore complete.
    - [Project 1-111] Unisim Transformation Summary:
      A total of 8 instances were transformed.
      RAM256X1S => RAM256X1S (MUXF7, MUXF7, MUXF8, RAMS64E, RAMS64E, RAMS64E, RAMS64E): 8 instances
    - [Project 1-604] Checkpoint was created with Vivado v2018.2 (64-bit) build 2258646
  - Opt Design (35 infos, 54 status messages)
    - Command: opt_design (53 more like this)
    - [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
    - [Project 1-461] DRC finished with 0 Errors
    - [Project 1-462] Please refer to the DRC report (report_drc) for more information.
    - [IP_Flow 19-234] Refreshing IP repositories
    - [IP_Flow 19-1704] No user IP repositories specified
    - [IP_Flow 19-2313] Loaded Vivado IP repository 'E:/Vivado/2018.2/data/ip'.
    - [Chipscope 16-329] Generating Script for core instance : dbg_hub (1 more like this)
    - [IP_Flow 19-3806] Processing IP xilinx.com:ip:xsdbm:3.0 for cell dbg_hub_CV. (1 more like this)
    - [Opt 31-49] Retargeted 0 cell(s).

- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s). (1 more like this)
- [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells (4 more like this)
- [Opt 31-662] Phase BUFG optimization created 0 cells of which 0 are BUFGs and removed 0 cells.
- [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.
- [Pwropt 34-9] Applying IDT optimizations ...
- [Timing 38-35] Done setting XDC timing constraints. (1 more like this)
- [Pwropt 34-10] Applying ODC optimizations ...
- [Physopt 32-619] Estimated Timing Summary | WNS=4.856 | TNS=0.000 |
- [Pwropt 34-162] WRITE_MODE attribute of 0 BRAM(s) out of a total of 1 has been updated to save power. Run report_power_opt to get a complete listing of the BRAMs updated.
- [Pwropt 34-201] Structural ODC has moved 0 WE to EN ports
- [Common 17-83] Releasing license: Implementation
- [Timing 38-480] Writing timing data to binary archive.
- [Common 17-1381] The checkpoint 'D:/digital design/projects/project_2/SPI Project/SPI Project.runs/impl_1/SPI_wrapper_opt.dcp' has been generated.
- [runtcl-4] Executing : report_drc -file SPI_wrapper_drc_opted.rpt -pb SPI_wrapper_drc_opted.pb -rpx SPI_wrapper_drc_opted.rpx
- [IP_Flow 19-1839] IP Catalog is up to date.
- [DRC 23-27] Running DRC with 2 threads (1 more like this)
- [Coretcl 2-168] The results of DRC are in file SPI_wrapper_drc_opted.rpt.

Place Design (24 infos, 90 status messages)

- [Chipscope 16-240] Debug cores have already been implemented
- Command: place_design (89 more like this)
- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
- [DRC 23-27] Running DRC with 2 threads (1 more like this)
- [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
- [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
- [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs

- [Vivado_Tcl 4-198] DRC finished with 0 Errors (1 more like this)
- [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information. (1 more like this)
- [Place 30-611] Multithreading enabled for place_design using a maximum of 2 CPUs
- [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).
- [Timing 38-35] Done setting XDC timing constraints. (2 more like this)
- [Physopt 32-65] No nets found for high-fanout optimization.
- [Physopt 32-232] Optimized 0 net. Created 0 new instance.
- [Physopt 32-775] End 1 Pass. Optimized 0 net or cell. Created 0 new cell, deleted 0 existing cell and moved 0 existing cell
- [Place 46-31] BUFG insertion identified 0 candidate nets, 0 success, 0 skipped for placement/routing, 0 skipped for timing, 0 skipped for netlist change reason.
- [Place 30-746] Post Placement Timing Summary WNS=4.358. For the most accurate timing information please run report_timing.
- [Common 17-83] Releasing license: Implementation
- [Timing 38-480] Writing timing data to binary archive.
- [Common 17-1381] The checkpoint 'D:/digital design/projects/project_2/SPI Project/SPI Project.runs/impl_1/SPI_wrapper_placed.dcp' has been generated.
- [runtcl-4] Executing : report_io -file SPI_wrapper_io_placed.rpt (2 more like this)

Route Design (1 critical warning, 3 warnings, 38 infos, 98 status messages)

- Command: route_design (97 more like this)
- [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a35ti'
- [Vivado_Tcl 4-198] DRC finished with 0 Errors
- [Vivado_Tcl 4-199] Please refer to the DRC report (report_drc) for more information.
- [Route 35-254] Multithreading enabled for route_design using a maximum of 2 CPUs
- [Route 35-416] Intermediate Timing Summary | WNS=4.398 | TNS=0.000 | WHS=-1.088 | THS=-103.818| (6 more like this)
- [Route 35-459] Router was unable to fix hold violation on 2 pins. This could be due to a combination of congestion, blockages and run-time limitations. Such pins are:
  u_ila_0/inst/ila_core_inst/probeDelay1[0]_i_1/I2
  u_ila_0/inst/ila_core_inst/shifted_data_in_reg[7][0]_srl8/D

  Resolution: You may try high effort hold fixing by turning on param route.enableGlobalHoldIter.
- [Route 35-57] Estimated Timing Summary | WNS=3.214 | TNS=0.000 | WHS=-0.354 | THS=-0.627 |

[Route 35-328] Router estimated timing not met.
Resolution: For a complete and accurate timing signoff, report_timing_summary must be run after route_design. Alternatively, route_design can be run with the -timing_summary option to enable a complete timing signoff at the end of route_design.

[Route 35-16] Router Completed Successfully

[Common 17-83] Releasing license: Implementation

[Timing 38-480] Writing timing data to binary archive.

[Common 17-1381] The checkpoint 'D:/digital design/projects/project_2/SPI Project/SPI Project.runs/impl_1/SPI_wrapper_routed.dcp' has been generated.

[IP_Flow 19-1839] IP Catalog is up to date.

[DRC 23-27] Running DRC with 2 threads (1 more like this)

[Coretcl 2-168] The results of DRC are in file SPI_wrapper_drc_routed.rpt.

[runtcl-4] Executing : report_drc -file SPI_wrapper_drc_routed.rpt -pb SPI_wrapper_drc_routed.pb -rpx SPI_wrapper_drc_routed.rpx (7 more like this)

[Timing 38-35] Done setting XDC timing constraints. (2 more like this)

[DRC 23-133] Running Methodology with 2 threads

[Coretcl 2-1520] The results of Report Methodology are in file SPI_wrapper_methodology_drc_routed.rpt.

[Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations.

[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.

[Vivado_Tcl 4-545] No incremental reuse to report, no incremental placement and routing data was found.

[Timing 38-91] UpdateTimingParams: Speed grade: -1L, Delay Type: min_max, Timing Stage: Requireds. (1 more like this)

[Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs (1 more like this)

Implemented Design (1 critical warning, 1 warning, 10 infos, 7 status messages)

General Messages (1 critical warning, 1 warning, 10 infos, 7 status messages)

[Netlist 29-17] Analyzing 110 Unisim elements for replacement

[Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

[Project 1-479] Netlist was created with Vivado 2018.2

[Project 1-570] Preparing netlist for logic optimization

[Chipscope 16-324] Core: u_ila_0 UUID: 23e7d65a-79bc-59f7-bc47-406c1714dfae

[Timing 38-478] Restoring timing data from binary archive.

[Timing 38-479] Binary timing data restore complete.

[Project 1-856] Restoring constraints from binary archive.

[Project 1-853] Binary constraint restore complete.

Reading XDEF placement. (6 more like this)

[Project 1-111] Unisim Transformation Summary:
A total of 62 instances were transformed.
CFGLUT5 => CFGLUT5 (SRLC32E, SRL16E): 48 instances
RAM256X1S => RAM256X1S (MUXF7, MUXF7, MUXF8, RAMS64E, RAMS64E, RAMS64E, RAMS64E): 8 instances
RAM32M => RAM32M (RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMD32, RAMS32, RAMS32): 6 instances

[Timing 38-282] The design failed to meet the timing requirements. Please see the timing summary report for details on the timing violations.

[Timing 38-436] There are set_bus_skew constraint(s) in this design. Please run report_bus_skew to ensure that bus skew requirements are met.