Electronic Devices

Lecture 17

Field Effect Transistor

"JFFT"

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Field Effect Transistor

- FET is a three terminal semiconductor device. It is unipolar transistor i.e. depends only on one type of charge carrier, either electron or hole.

- FET is simple to fabricate and occupies less space on a chip than a BJT. About 100000 FETs can be fabricated in a single chip. This makes them useful in VLSI (Very Large Scale Integrate) system.

- FET is a voltage-sensitive device which has extremely high input impedance ($10^{14}\Omega$ as well as high output impedance).

- There are two types of FET – the JFET (Junction Field Effect Transistor) and MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

Field Effect Transistor

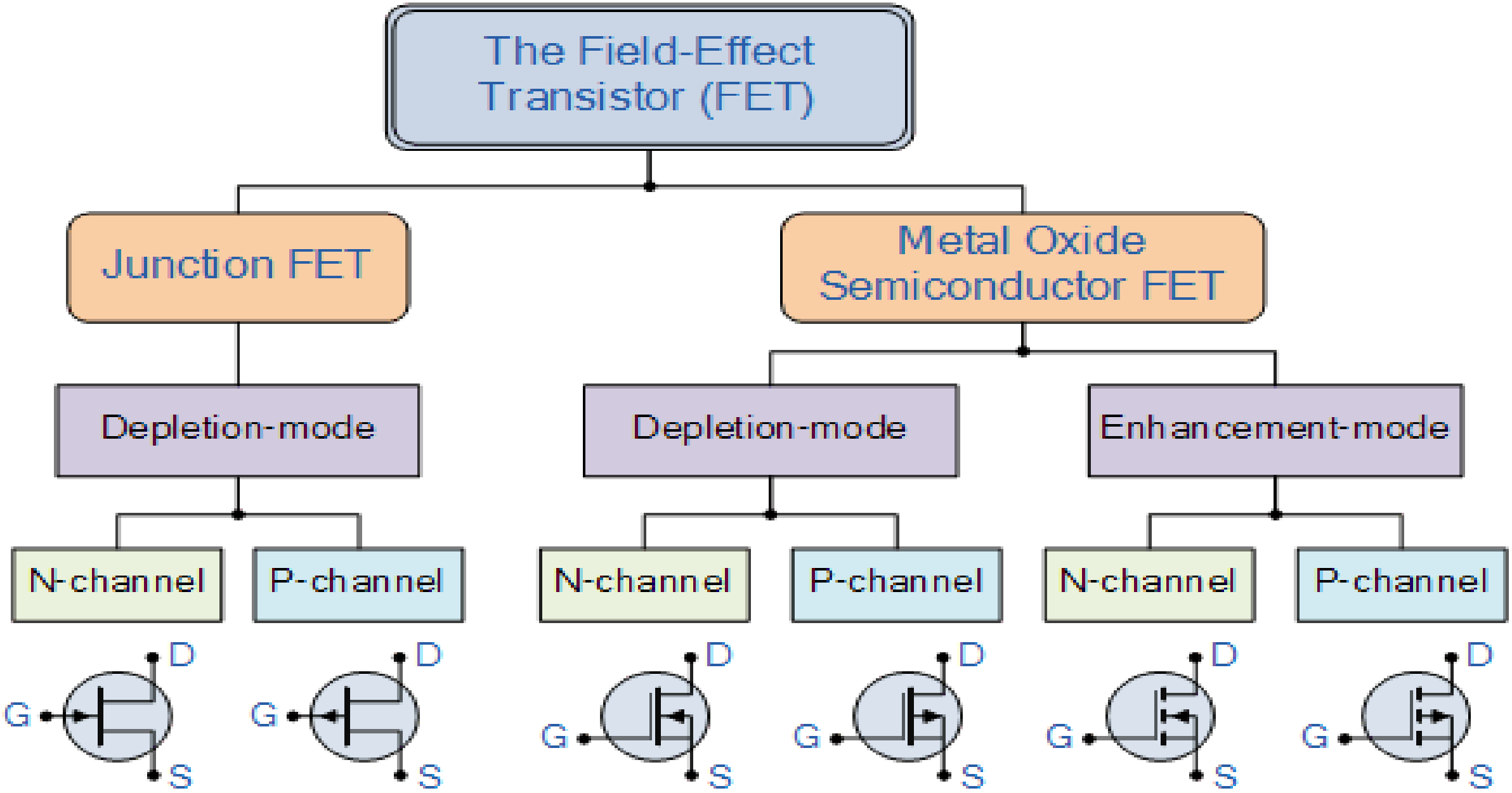
- FET is a three terminal unipolar semiconductors device has a very similar characteristics to BJT such as :

- High efficiency.
- Instant operation.
- Robust and cheap.
- Can be used in most electronic circuit applications.

- **FET advantages over BJT:**

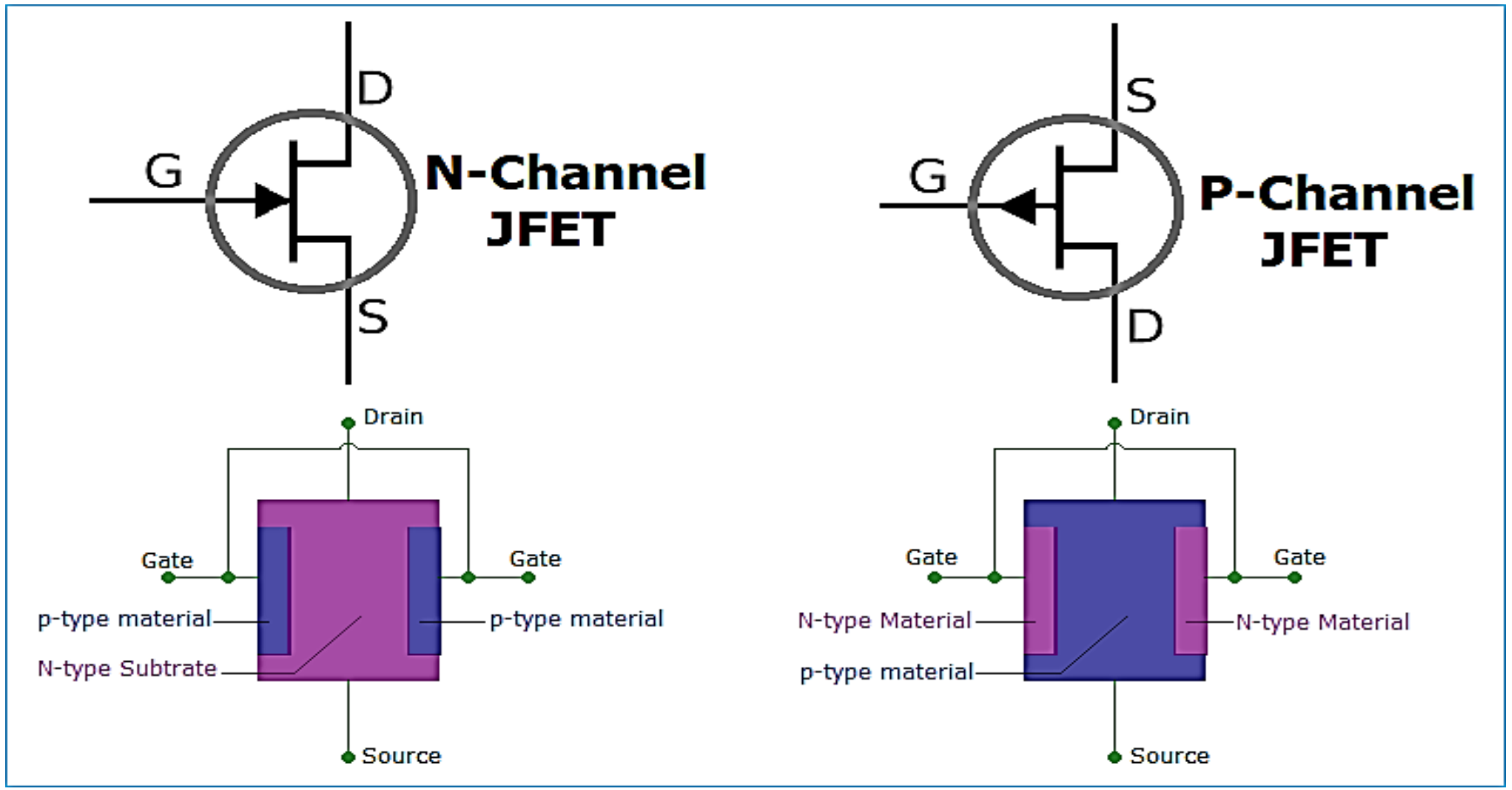
- FET can be made much smaller than BJT.
- Their low power consumption and power dissipation makes them ideal for use in integrated circuit.
- Rin is very high, makes them very sensitive to input voltage signal, but for this sensitivity it will be damage easily by static electricity.

Field Effect Transistor



Junction Field Effect Transistor “JFET”

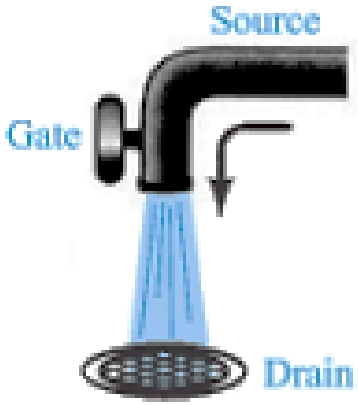
- It is of two types
- P-channel JFET
- n-channel JFET

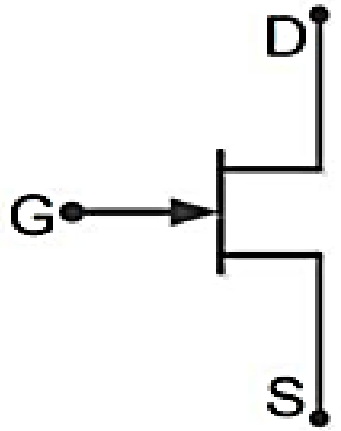


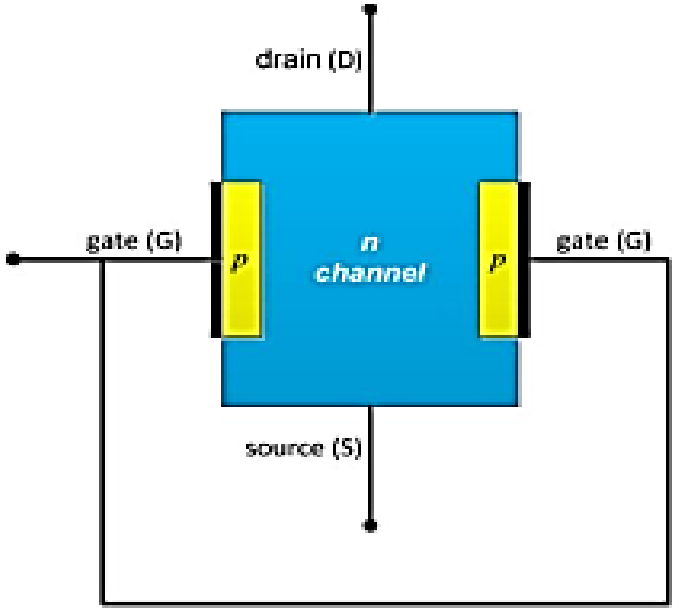
- The n- channel JFET consists of a bar of n-type semiconductor with two islands of p- type material embedded in the sides. The drain and source terminals are made by ohmic contacts at the end of semiconductor bar.

Junction Field Effect Transistor “JFET”

- Majority charge carrier i.e. electrons can be cause to flow along length of bar by means of a voltage applied between the source and drain. The third terminal, known as the gate is formed by electrically connecting the two p-type regions.







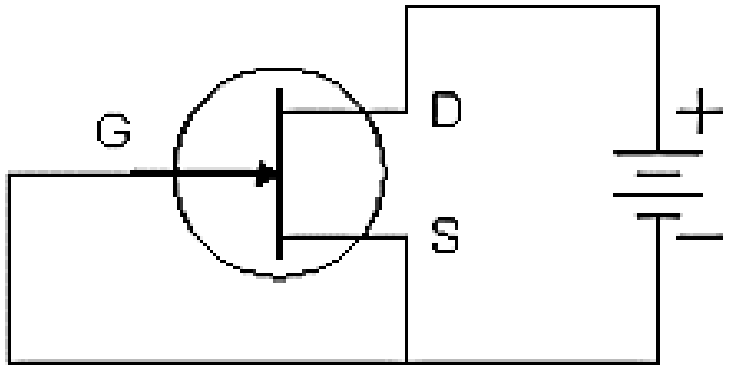
Symbol & Structure of n-channel JFET

Junction Field Effect Transistor “JFET”

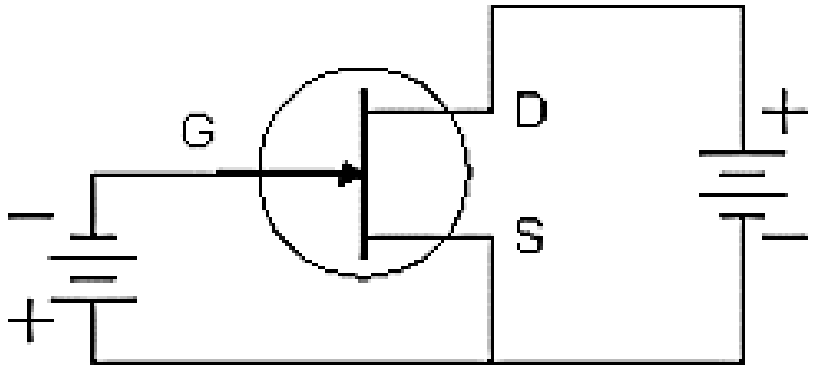
The circuit symbol of p- channel JFET is similar to that of an n-channel JFET except that the gate arrow points outward as shown in below.

Symbol & Structure of p-channel JFET

JFET Operation and Circuit analysis (N Channel)



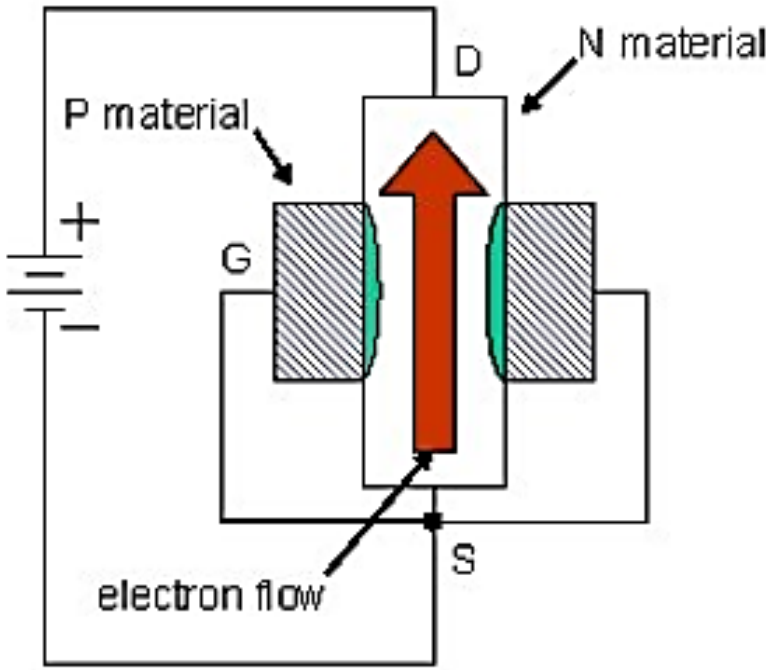
When the gate and the source are at the same voltage, the JFET freely conducts. The current flowing from drain to source is limited only by the resistance of the semiconductor materials making up the transistor.

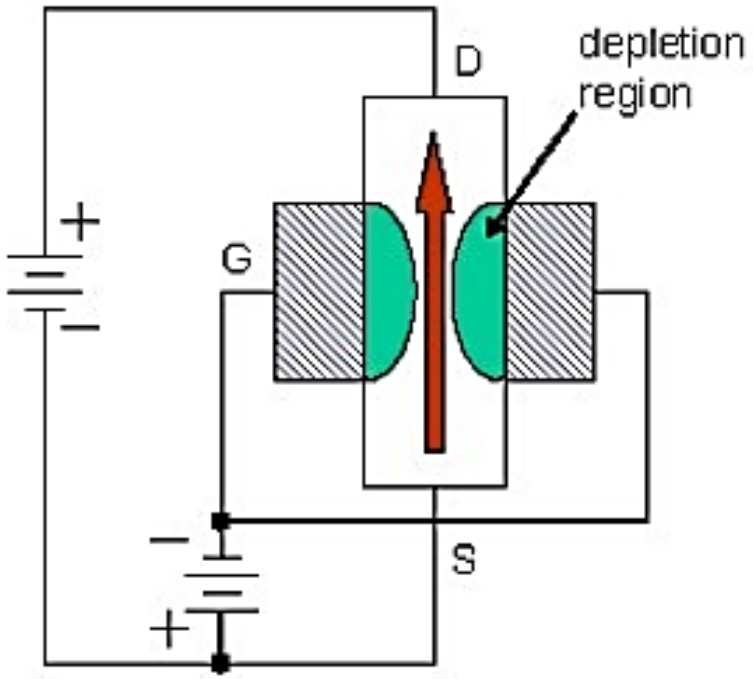


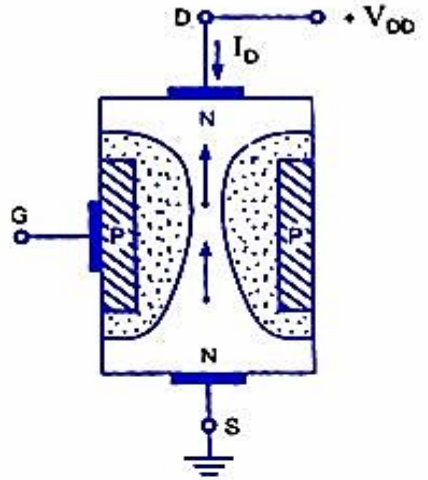
Current from drain to source is controlled by making the gate voltage more negative than the source voltage. If the voltage at the gate is made sufficiently more negative than the voltage at the source, the JFET is cut off--no current will flow from drain to source.

(Remember--for the p-channel JFET, reverse the polarity of each of the voltages.)

JFET Operation and Circuit analysis

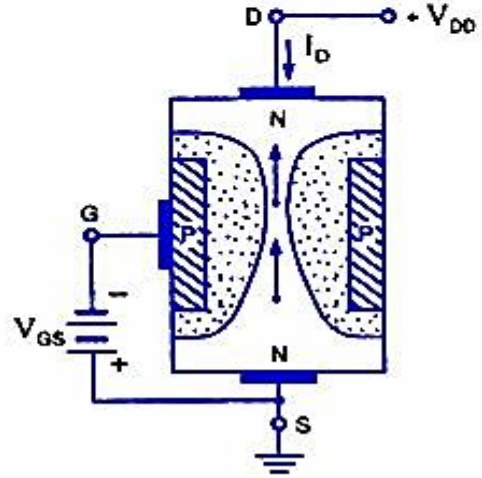






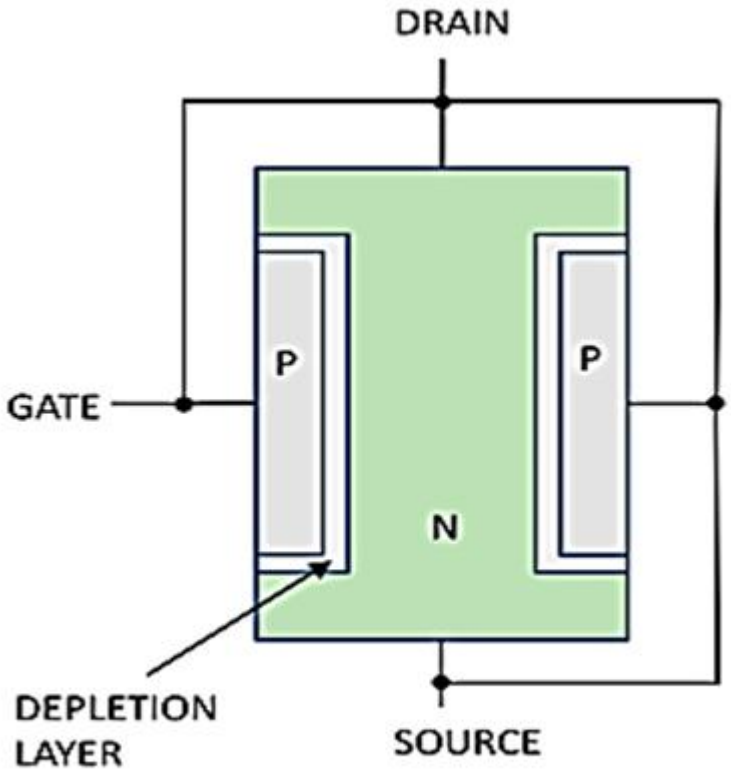
JFET With No Bias Voltage

The drain and source are at opposite ends of a continuous length of n-type semiconductor. The gate is constructed of two regions of p-type semiconductor. When the gate-source junctions are reverse biased, a depletion region (free of charge carriers--electrons and holes) is created. This forces the electron flow to channel into a smaller area, effectively increasing resistance and reducing current flow.

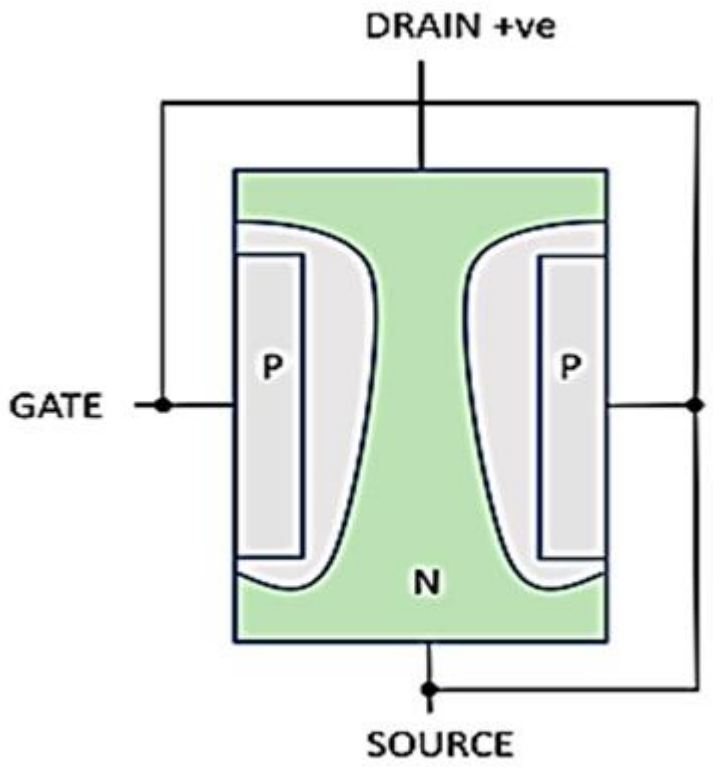


JFET With Small –Ve Gate Source Bias

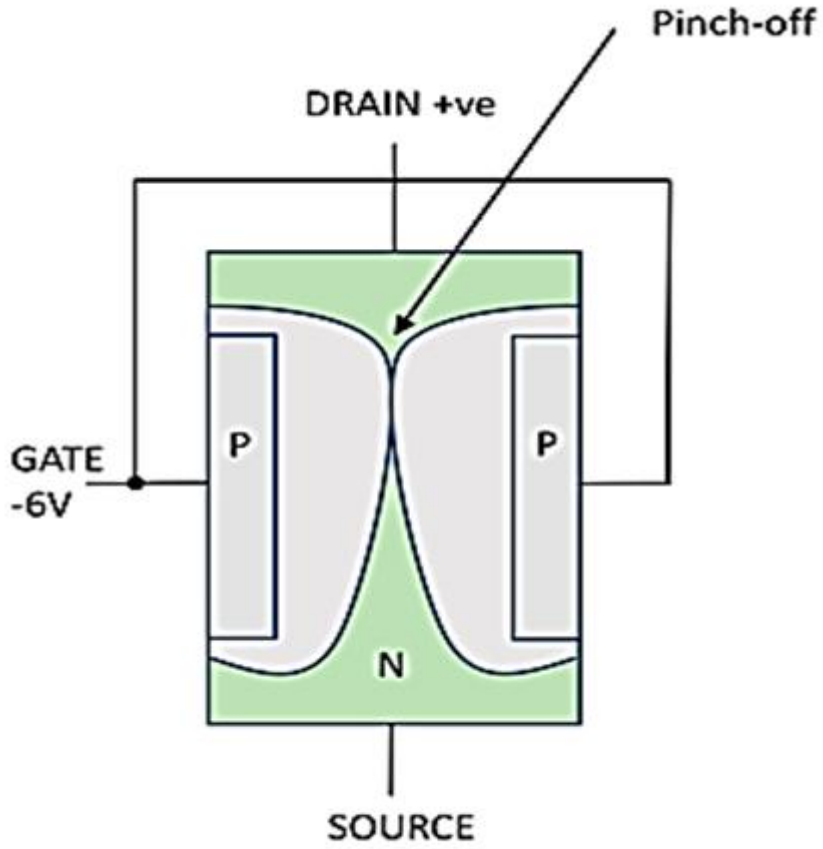
JFET Operation and Circuit analysis



VDS and VGS = 0V



VDS = +ve and VGS = 0V



VDS = +ve and VGS = -6V

JFET Operation and Circuit analysis

- The Gate and channel constitute a PN junction diode which is reverse biased by the gate to the source voltage.
- A depletion layer is developed in the channel as reverse bias increases the width of depletion layer increases.
- For a fixed drain to source voltage, the drain current will be a function of reverse bias voltage across the gate junction.
- At a gate-to-source voltage VGS known as the “Pinch- off” voltage which eliminates the channel, the channel width is reduces to zero.
- The term Field Effect is used to describe this device because of mechanism to control current using reverse bias voltage VGS.

Drain characteristics (N channel)

- **Ohmic Region**

When $V_{GS} = 0$ the depletion layer is very small and JFET as voltage controlled resistor.

- **Saturation or Active region**

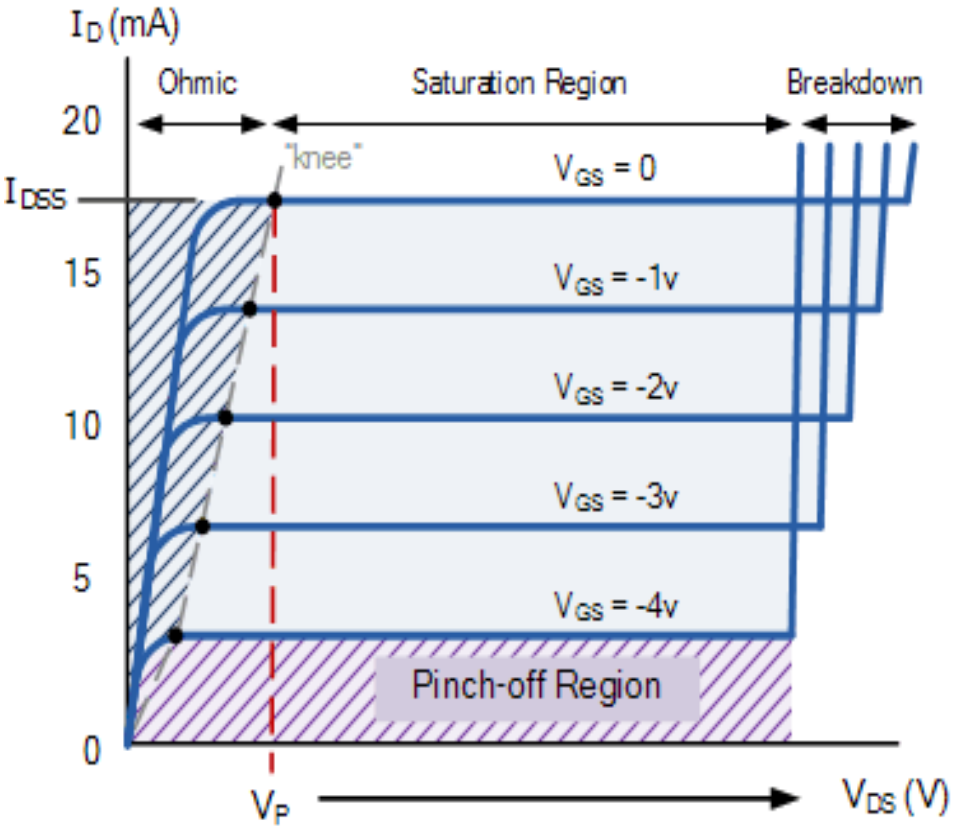
JFET become good conductor and controlled by V_{GS} which V_{DS} has little or no effect.

- **Cutoff region " pinch off region"**

V_{GS} is sufficient to cause the JFET to act as open circuit as channel resistance is maximum.

- **Breakdown region**

V_{DS} is high enough to cause JFET resistive channel to breakdown and pass uncontrolled maximum current



Drain characteristics

- V_p " pinch off voltage", the voltage that pinches off the channel connection between drain and source.

- **Ohmic region**

$V_{DS} < V_p$, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$ I_{DSS} is the maximum current

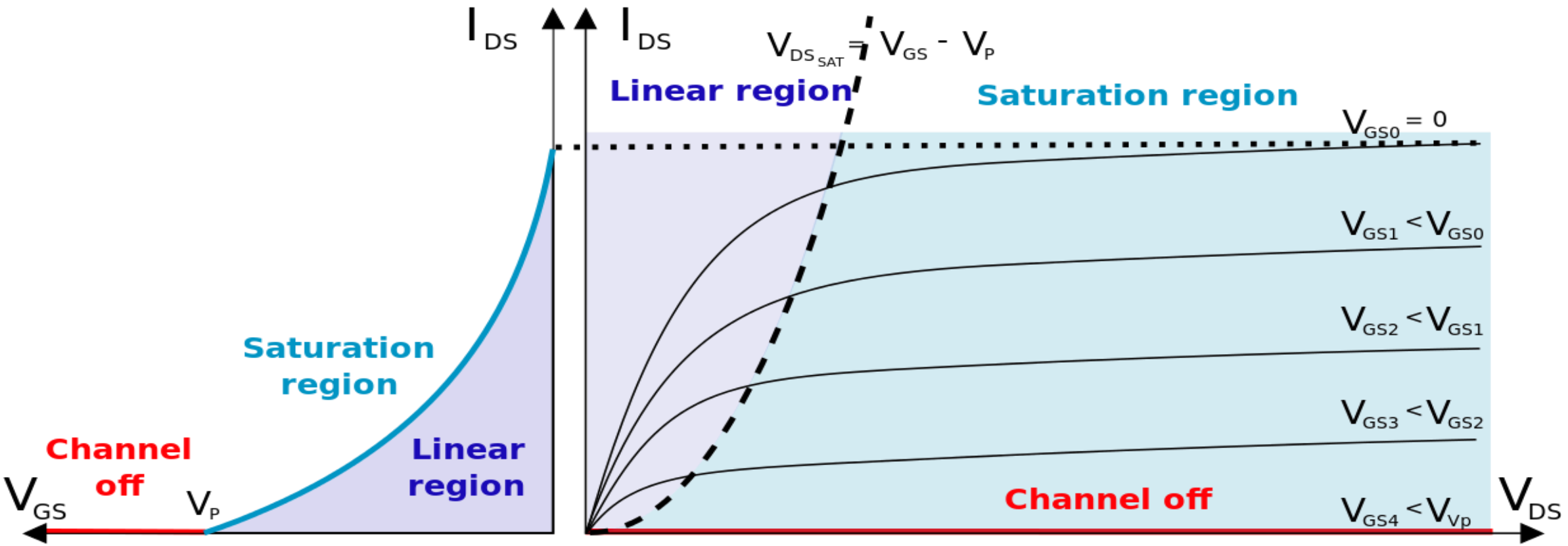
- **Saturation region**

$V_{DS} \geq V_p$, I_D remains constant

- **Breakdown**

$V_{DS} >>> V_p$

Transfer characteristics



Transfer characteristics

- **Drain – Source channel resistance**: The rate of change of V_{DS} with respect to change of I_D at a constant value of V_{GS} ($R_{DS} \approx 100k\Omega$ to $1M\Omega$)

$$R_{DS} = \frac{\triangle V_{DS}}{\triangle I_D}$$

Transconductance g_m : The rate of change of I_D with respect to change of V_{GS} at a constant value of V_{DS} ($g_m \approx 0.1$ to 20 mA/V)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$\frac{dI_D}{dV_{GS}} = -\frac{2I_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

Where g_{m0} is the transconductance when $V_{GS} = 0$

$$g_{m0} = -\frac{2I_{DSS}}{V_{GS(off)}}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

Current Equations of JFET

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

$$I_D = I_S$$

$$I_G = 0$$

JFET Biasing

- There are several different ways of biasing the JFET, for many configurations I_{DSS} and V_{GS}(off) "V_p" will be needed.

- Fixed-Bias.
- Self Bias.
- Combination Bias.
- Constant current Bias.
- Voltage Divider Bias.

Fixed-Bias JFET

- The simplest form of bias is the constant voltage bias.

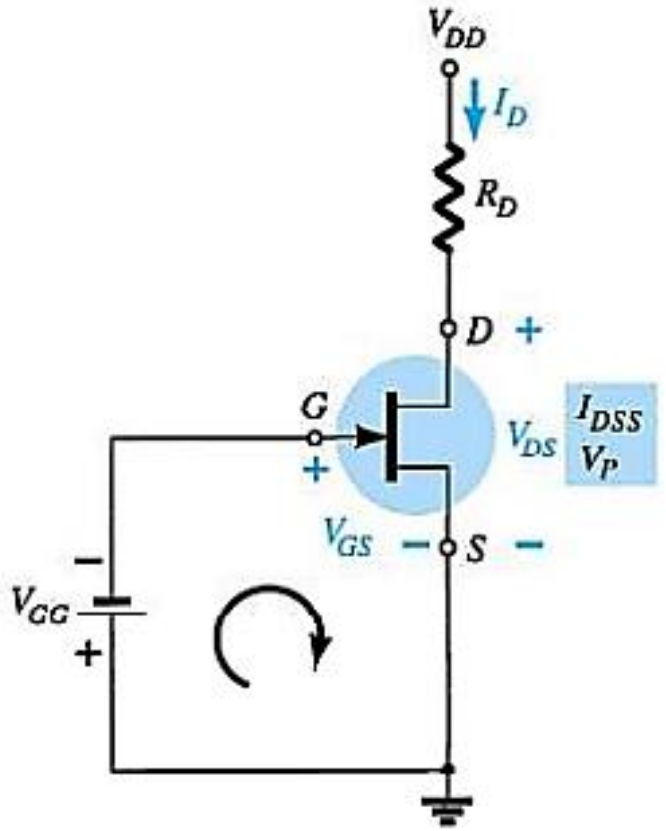
Using KVL in Gate –Source loop

IG is approximately zero

$$V_{GS} = -V_{GG}$$

Using KVL in Drain–Source loop

$$V_{DS} = V_{DD} - I_D R_D$$



Example

Determine I_D and V_{DS}. Assume I_{DSS}= 10 mA , V_{GS}(off) = -5V.

- **Solution**

First, because $I_G \approx 0$, the drop across R_G is ≈ 0 and $V_{GS} = V_{GG}$.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$I_D = 10mA\left(1 - \frac{-2V}{-5V}\right)^2$$

$$I_D = 3.6mA$$

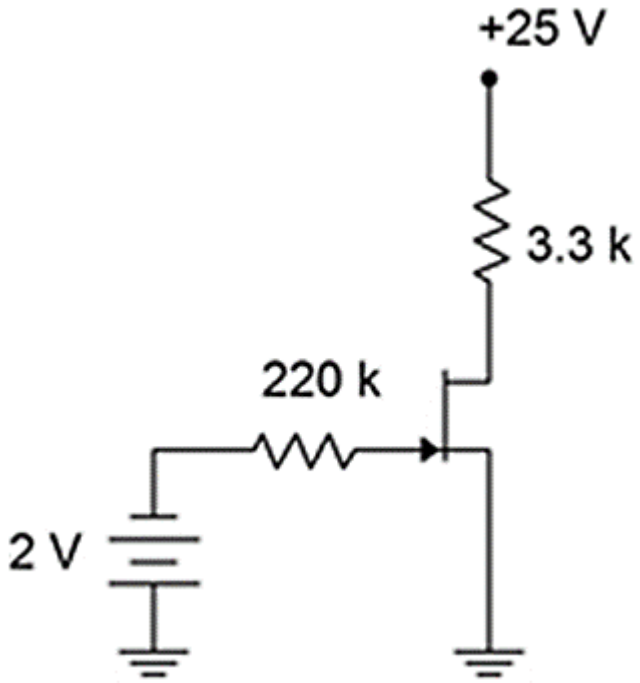
Looking at the drain-source loop, KVL shows

$$V_{DD} = I_D R_D + V_{DS}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DS} = 25V - 3.6mA \times 3.3k\Omega$$

$$V_{DS} = 13.1V$$



Self Bias

- Self bias using a small number of components and only a single power supply, it offers a better stability than fixed voltage bias.

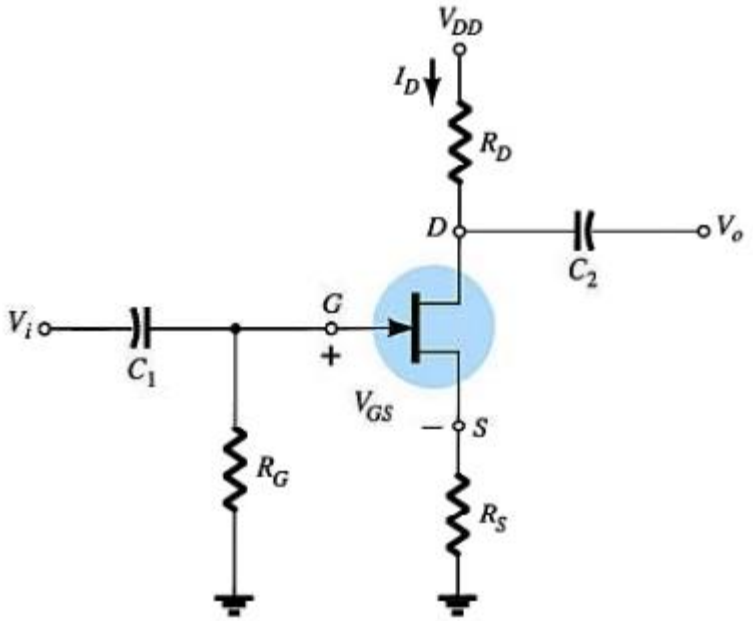
$I_G = 0$, and $I_D = I_S$

$$V_{GS} = -I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

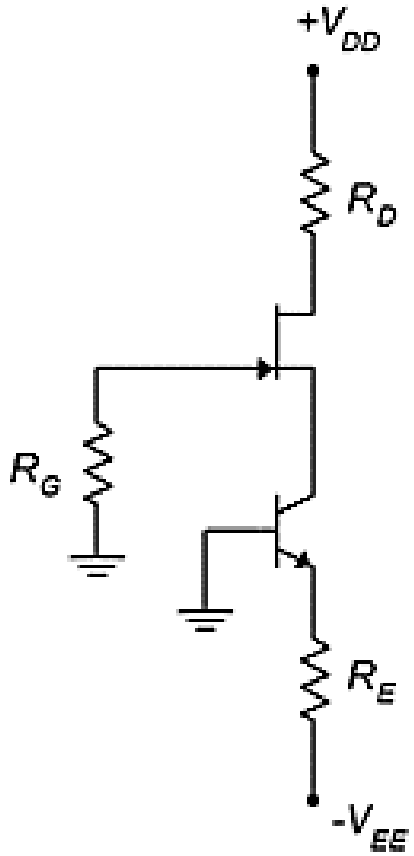
$$V_S = I_D R_S$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$



Constant current Bias

- The most stable bias of JFET relies on a current source made with BJT.
- An NPN BJT is used for an N-channel JFET and a PNP would be used with a P-channel JFET.



Voltage Divider Bias

V_G is equal to the voltage across divider resistor R_2:

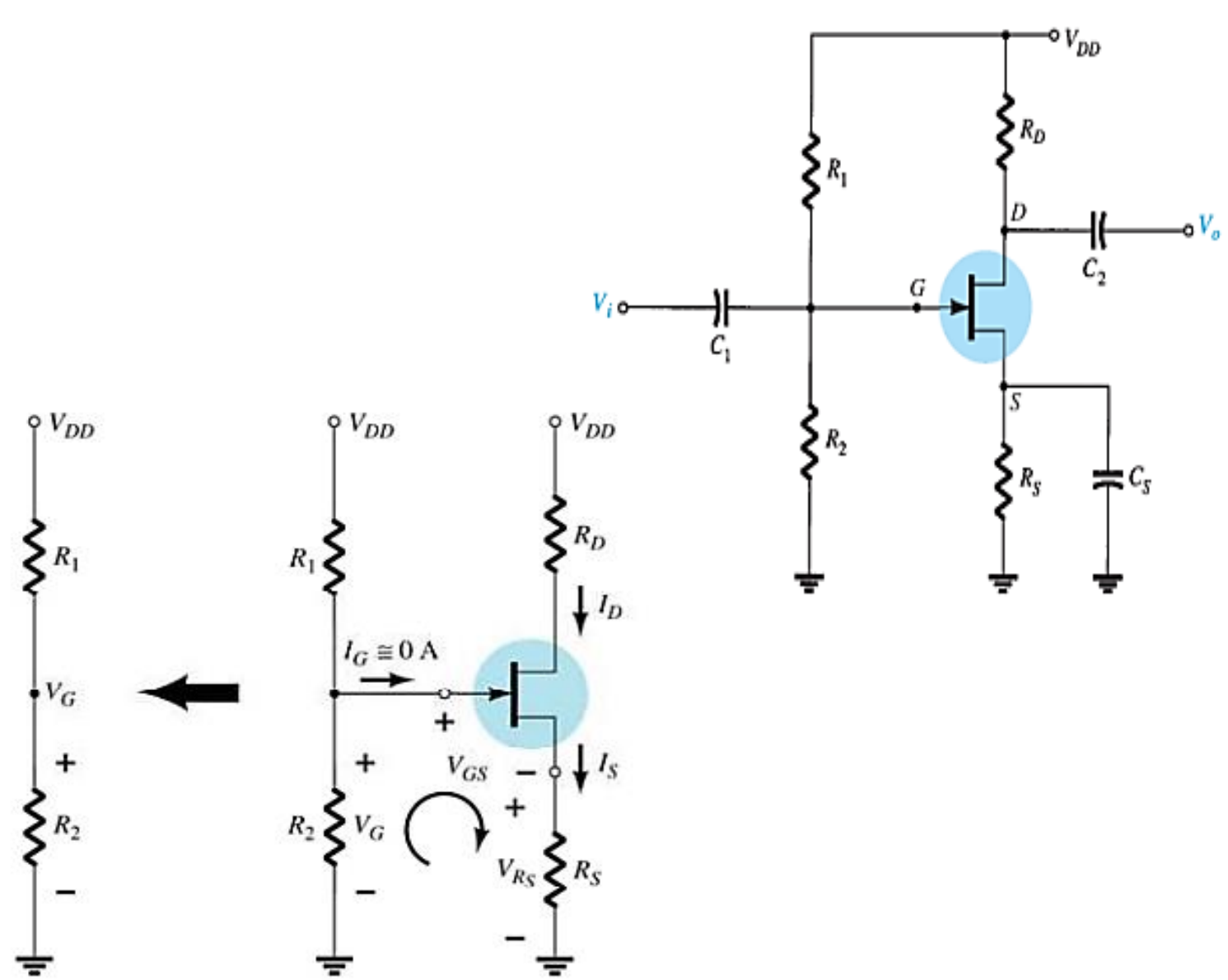
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchhoff's Law:

$$V_{GS} = V_G - I_D R_S$$

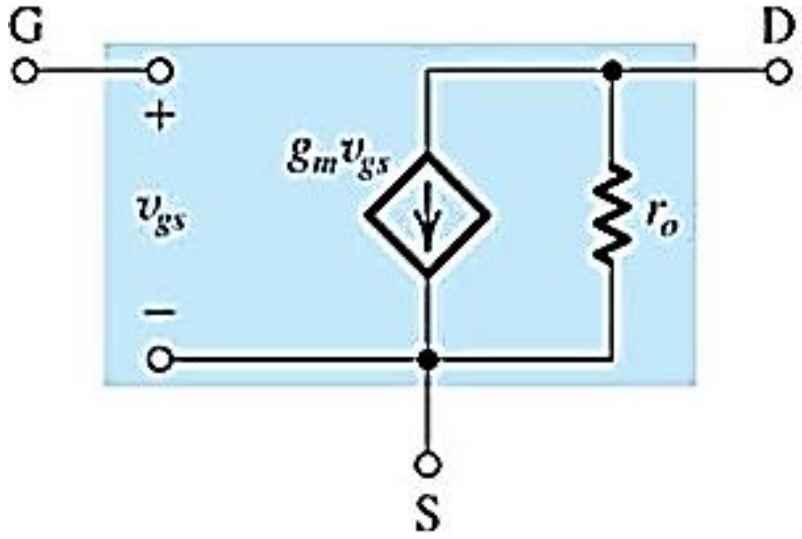
$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

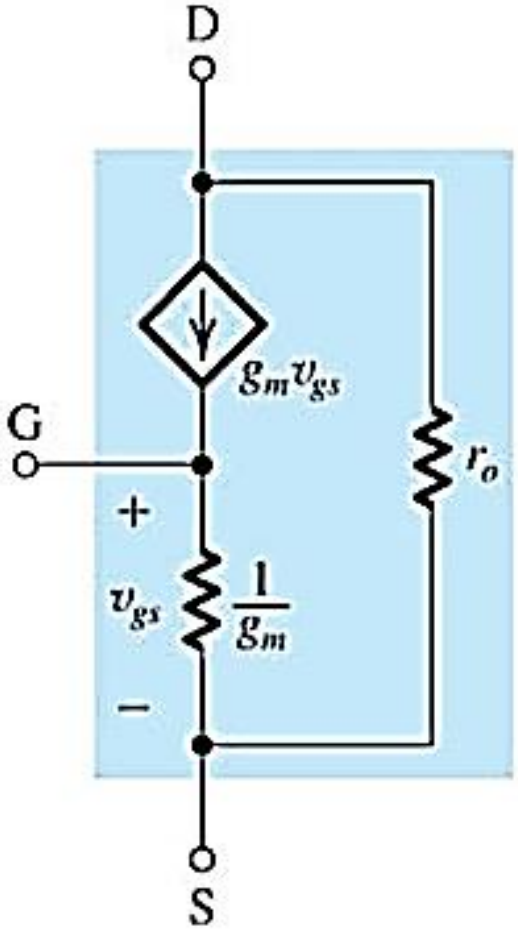


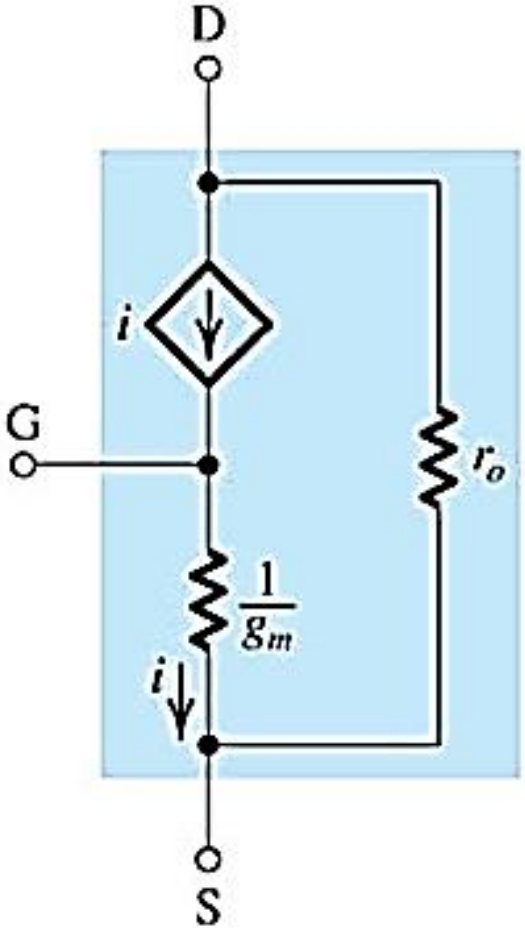
JFET small signal model (Hybrid Model)

π Model



T- Model





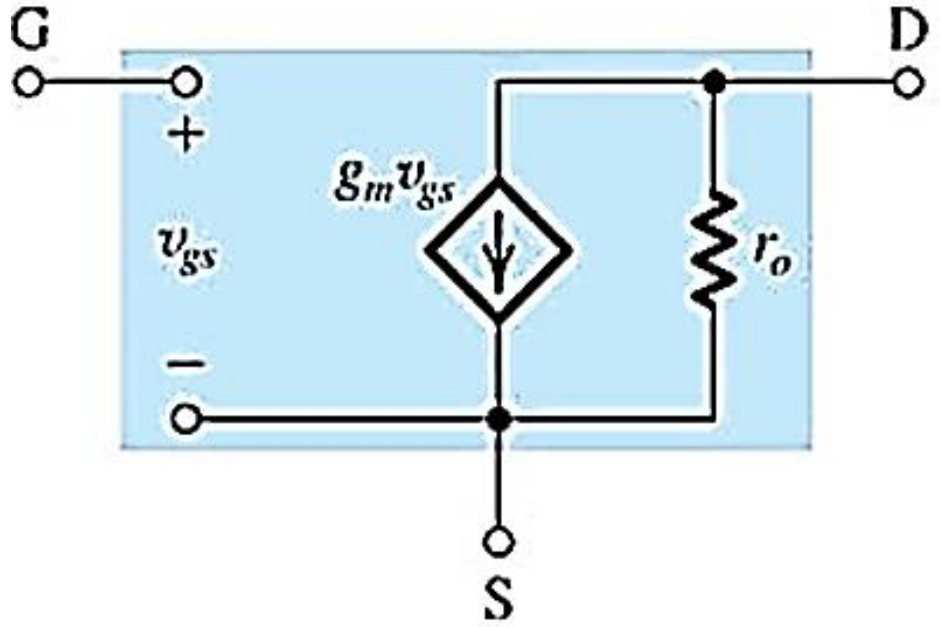
JFET Hybrid π Model

$$g_m = -\frac{2I_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

$$r_o = r_d = \frac{\triangle V_{DS}}{\triangle I_D} = \frac{1}{g_{os}}$$

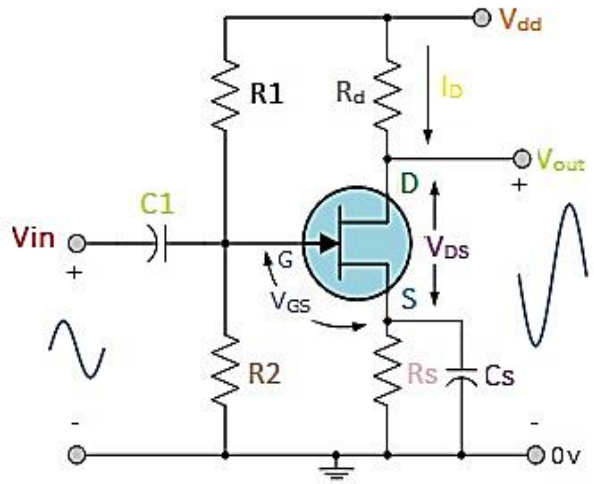
$$Z_i = \infty$$

$$Z_o = r_d$$

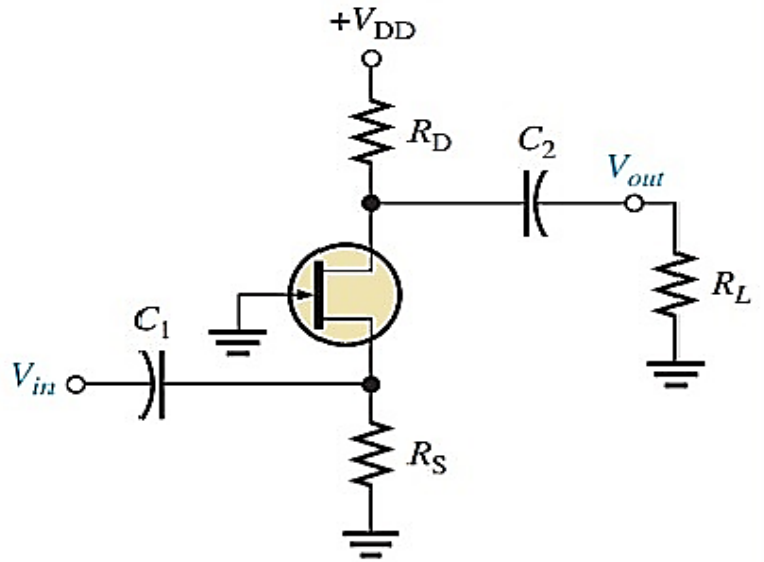


JFET different configuration

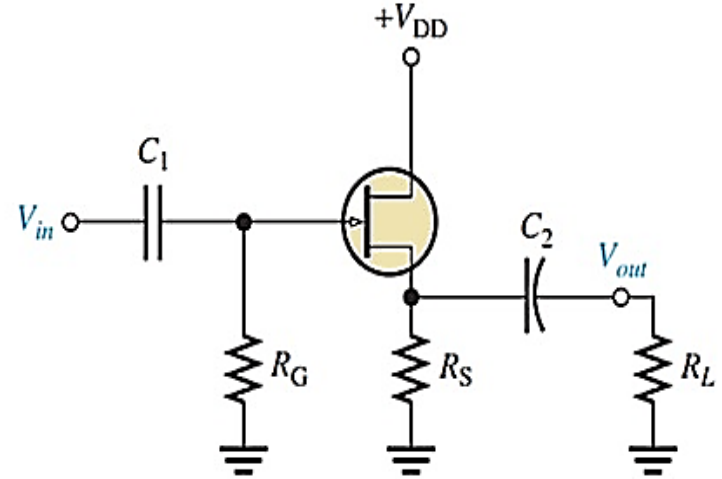
Common Source JFET Amplifier



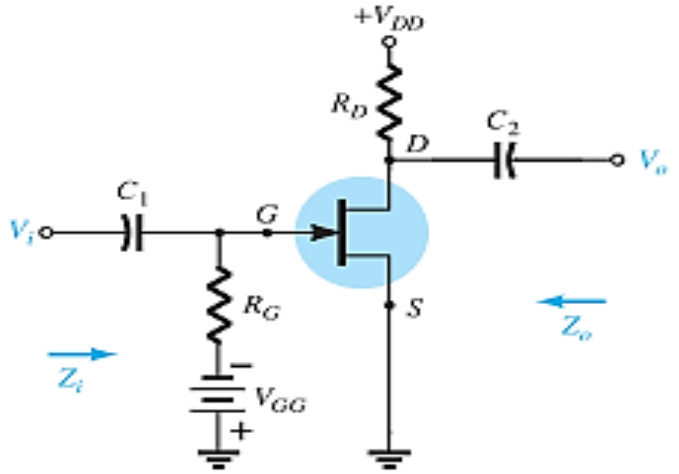
JFET Common-Gate Amplifier

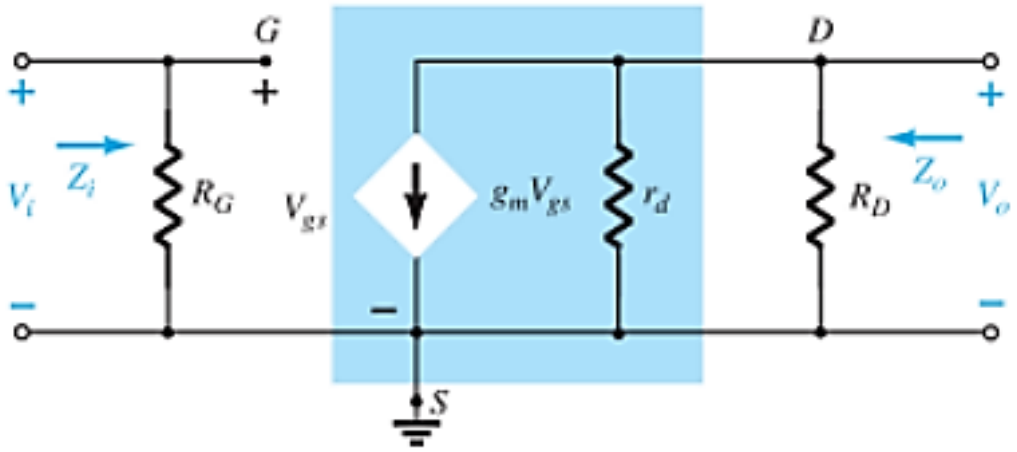


Common-Drain FET Amplifiers



Fixed biased CS Configuration



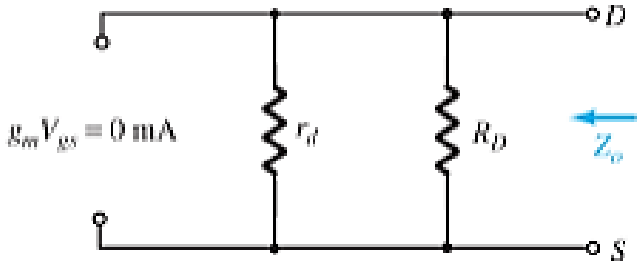


$$Z_i = R_G$$

$$Z_o = R_D \| r_d$$

$$Z_o \cong R_D$$

$r_d \geq 10R_D$



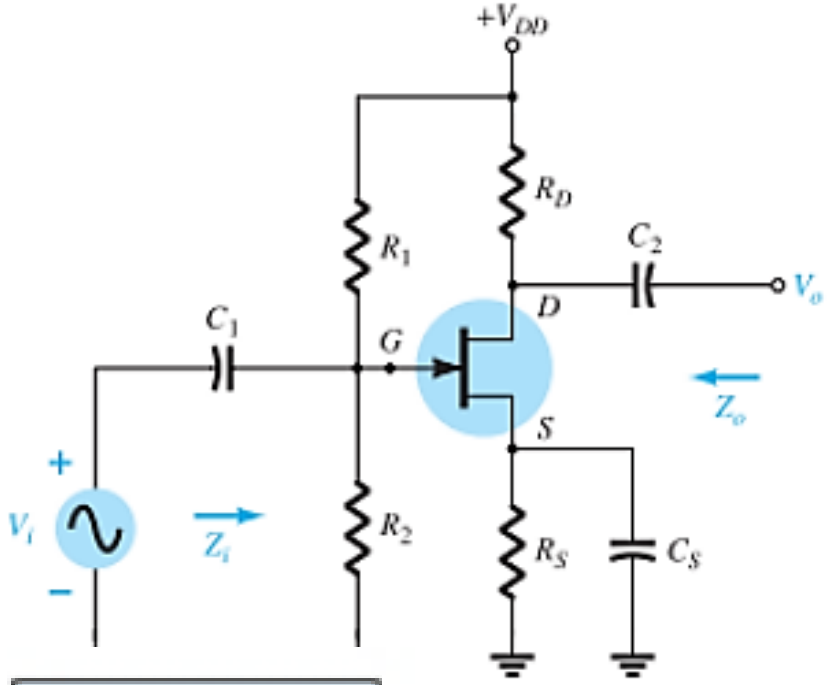
$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D$$

$r_d \geq 10R_D$

phase shift of 180° between input and output voltages.

Voltage Divider CS Configuration

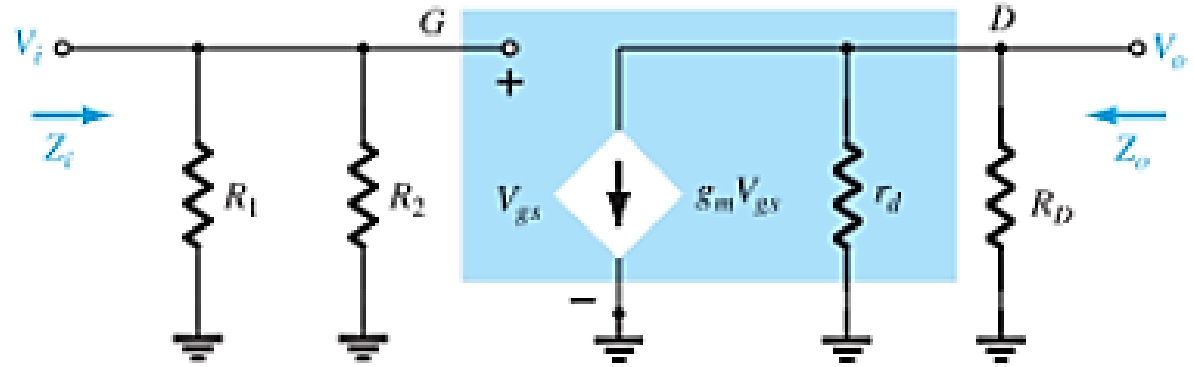


$$Z_i = R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

$$Z_o \cong R_D$$

$r_d \geq 10R_D$



$$V_{gs} = V_i$$

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D$$

$r_d \geq 10R_D$