Electronic Devices

Lecture 13
Bipolar Junction Transistor

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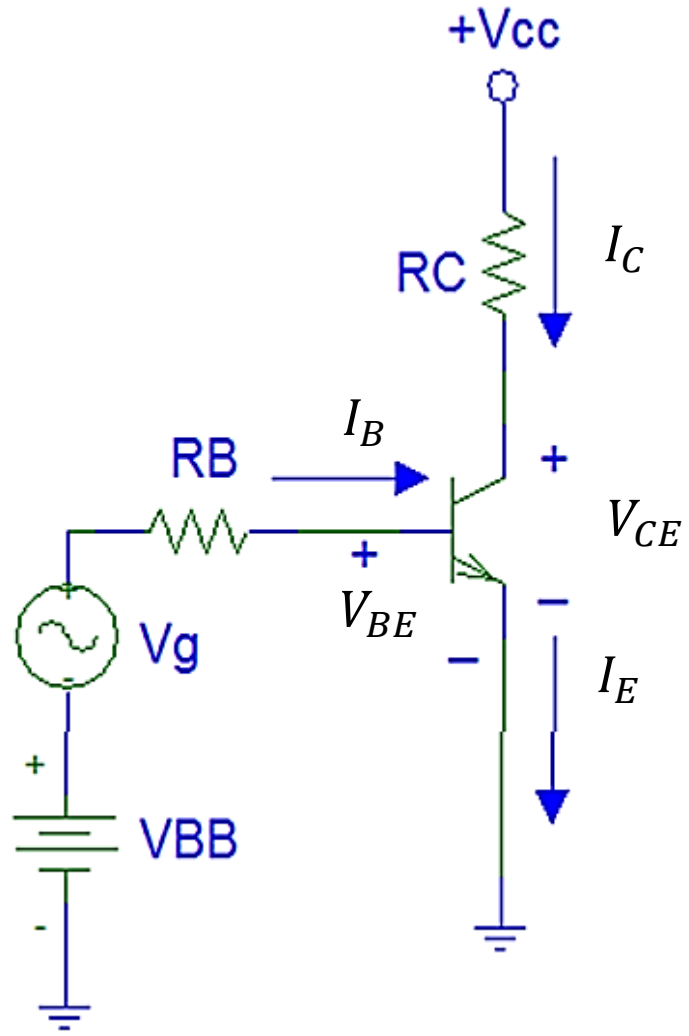
BJT Biasing

- Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.
- The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. In fact, the amplifier increases the strength of a weak signal by transferring the energy from the applied DC source to the weak input ac signal The analysis or design of any electronic amplifier therefore has two components:

❑The dc portion and

❑The ac portion



BJT Biasing

- During the design stage, the choice of parameters for the required dc levels will affect the ac response.
- Biasing: Application of dc voltages to establish a fixed level of current and voltage.

Purpose of the DC biasing circuit

- To turn the device “ON”
- To place it in operation in the region of its characteristic where the device operates most linearly .
- Proper biasing circuit which it operate in linear region and circuit have centered Q-point or midpoint biased
- Improper biasing cause:
  - Distortion in the output signal.
  - Produce limited or clipped at output signal.

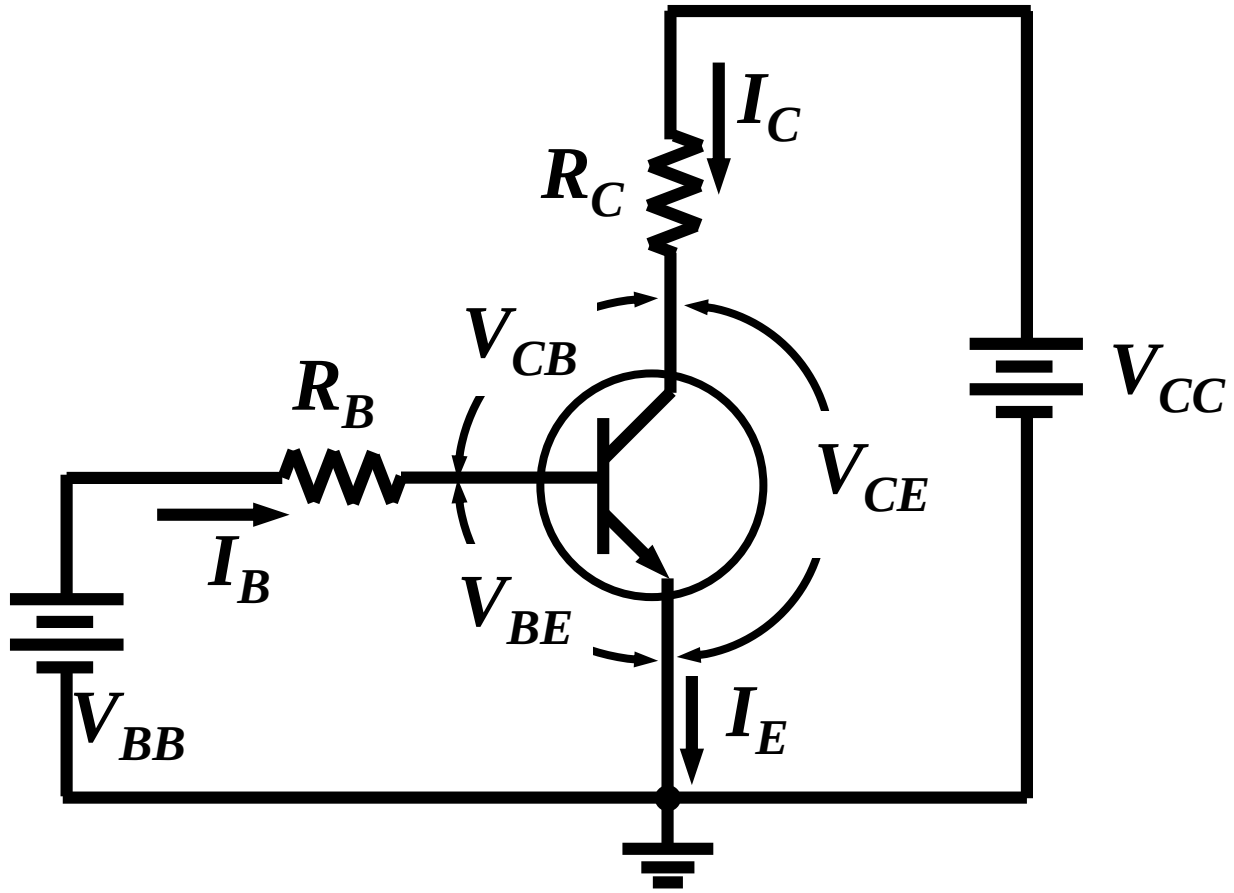
Important basic relationship

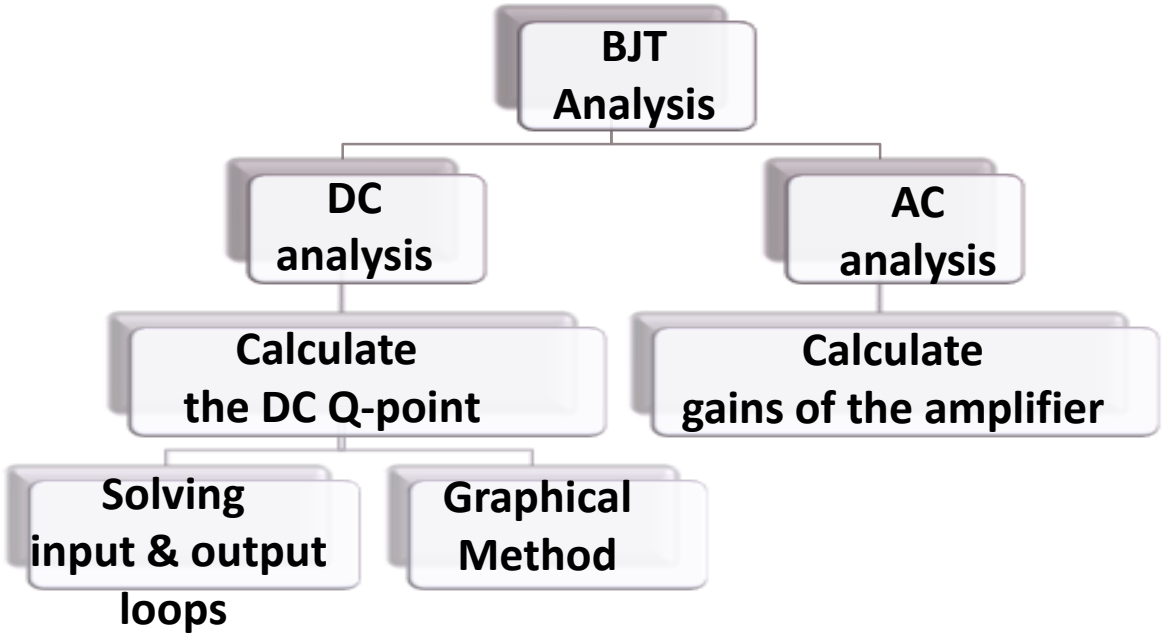
$$I_E = I_B + I_C$$

$$I_C = \beta I_B$$

$$I_E = (1 + \beta) I_B$$

$$V_{CB} = V_{CE} - V_{BE}$$



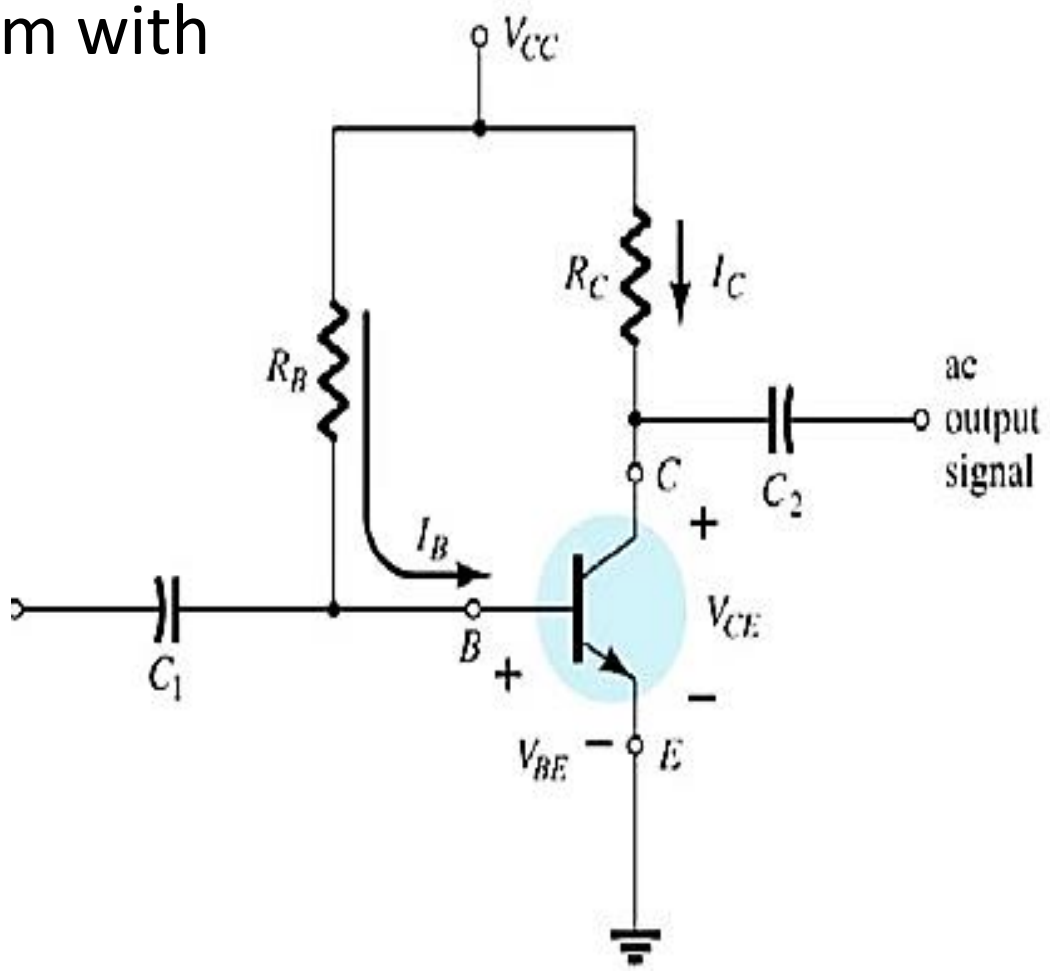


- **DC Biasing Circuits**

1. Fixed-bias circuit
2. Emitter-stabilized bias circuit
3. Voltage divider bias circuit
4. DC bias with voltage feedback

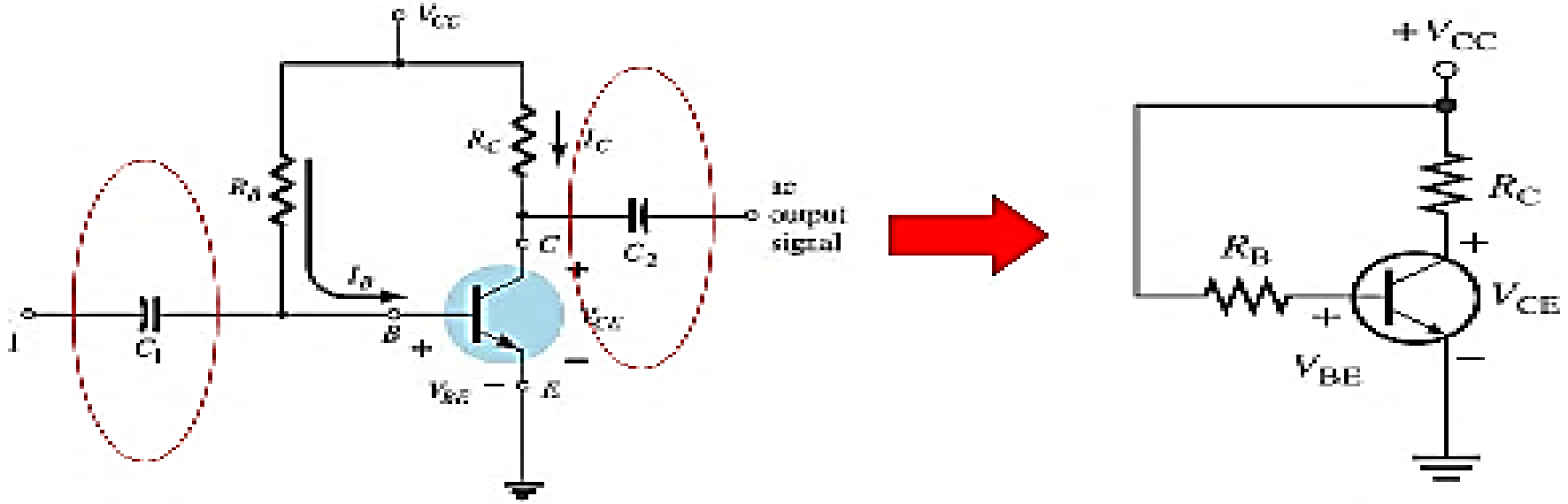
1. Fixed Bias circuit

- This is common emitter (CE) configuration
  - 1st step: Locate capacitors and replace them with an open circuit
  - 2nd step: Locate 2 main loops which;
    - **BE loop (input loop)**
    - **CE loop(output loop)**



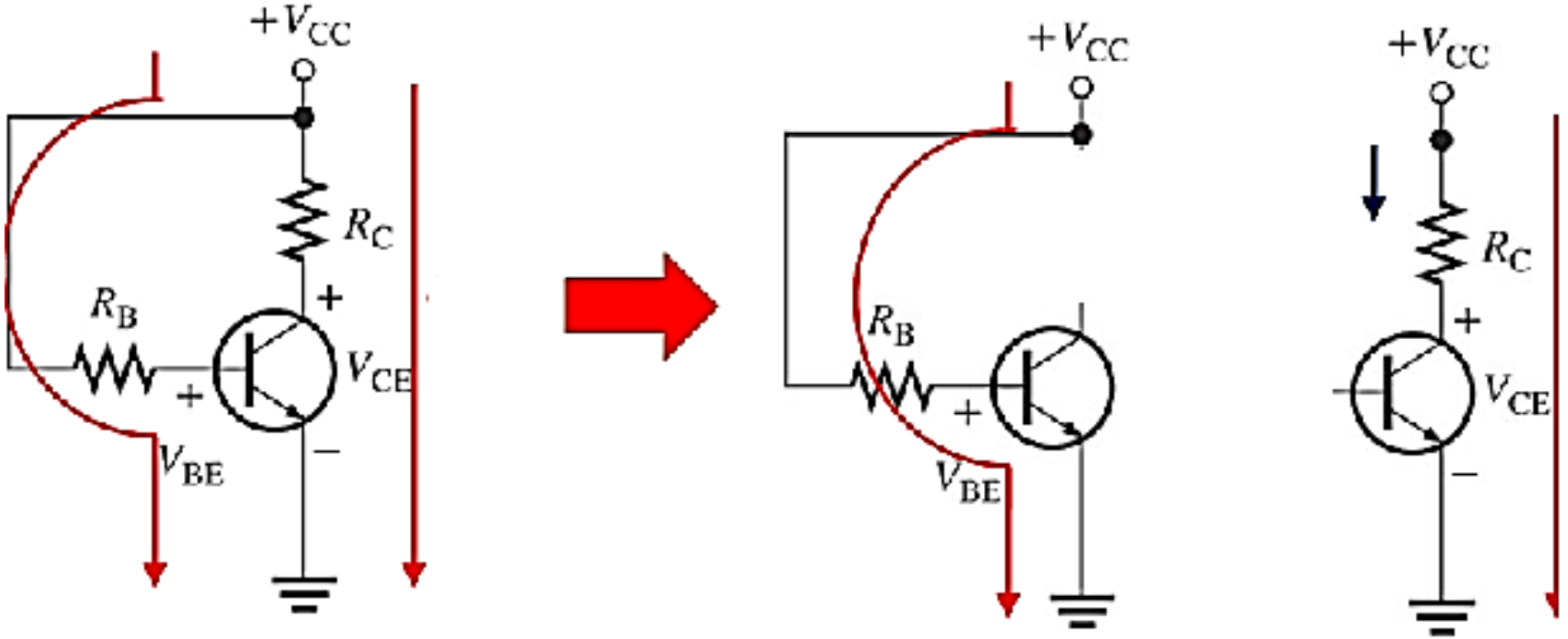
1. Fixed Bias circuit

- 1st step: Locate capacitors and replace them with an open circuit



1. Fixed Bias circuit

- 2nd step: Locate 2 main loops.



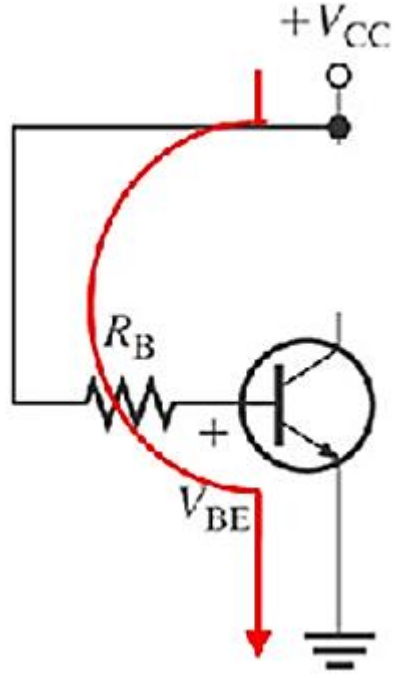
1. Fixed Bias circuit

- BE Loop Analysis

From KVL:

$$-V_{cc} + R_B I_B + V_{BE} = 0$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$



- CE Loop Analysis

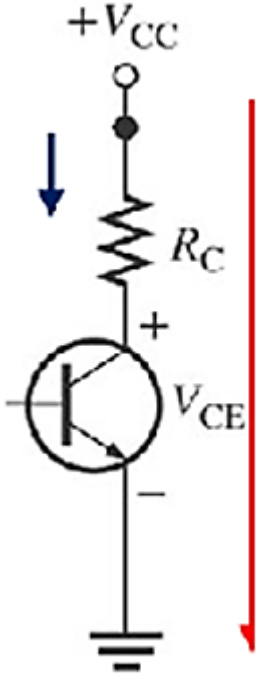
From KVL:

$$-V_{cc} + R_c I_C + V_{CE} = 0$$

$$V_{CE} = V_{cc} - R_c I_C$$

$$I_C = \boldsymbol{\beta} I_B$$

$$I_C = \boldsymbol{\beta}\left(\frac{V_{cc} - V_{BE}}{R_B}\right)$$



Note that R_c does not affect the value of Ic

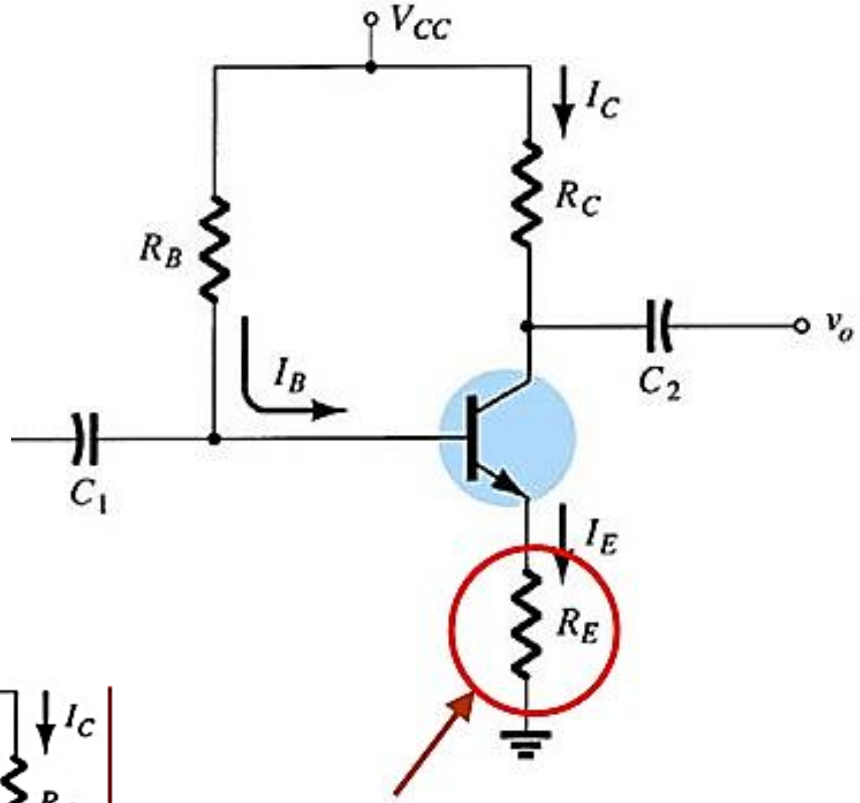
1. Fixed Bias circuit

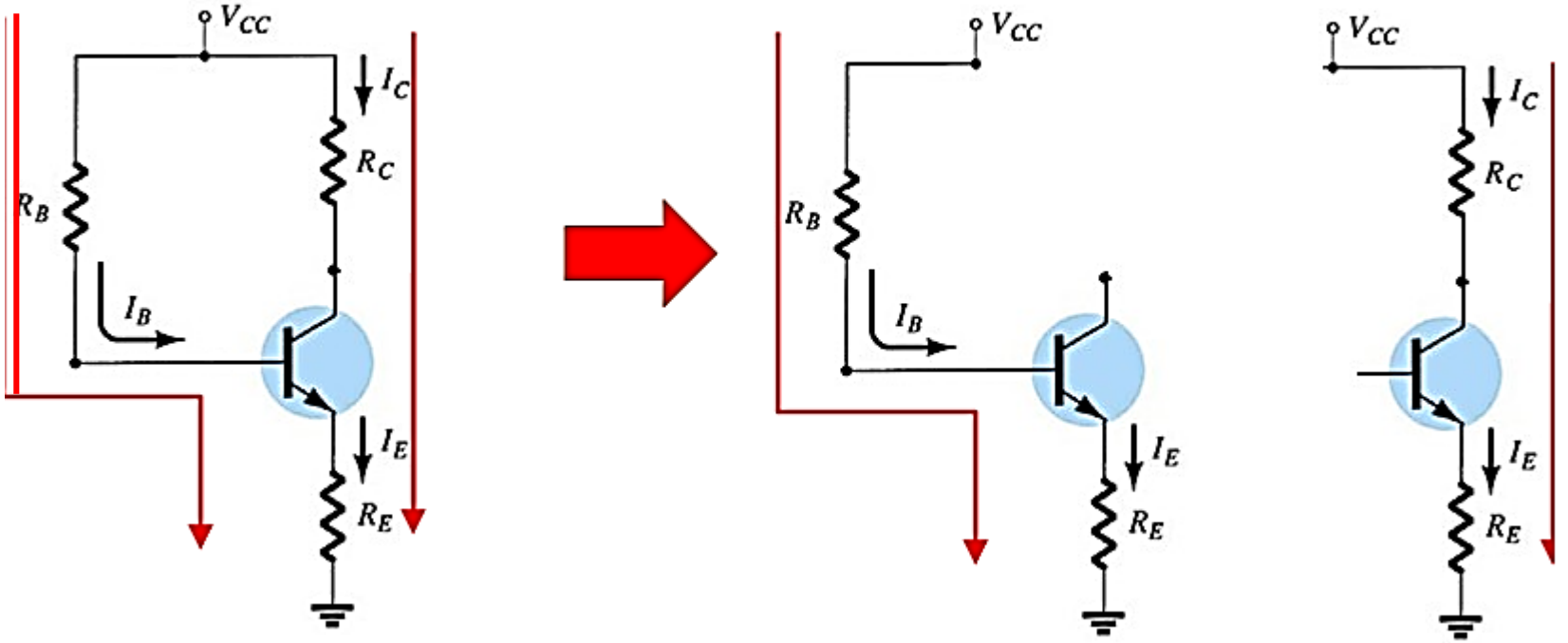
- The transistors base current, I_B remains constant for given values of Vcc, and therefore the transistors operating point must also remain fixed. Hence referred as fixed biasing.
- This two resistor biasing network is used to establish the initial operating region of the transistor using a fixed current bias.

- **DISADVANTAGE**
  - Unstable – because it is too dependent on β and produce width change of Q-point
  - For improved bias stability , add emitter resistor to dc bias.

2. Emitter-Stabilized bias circuit

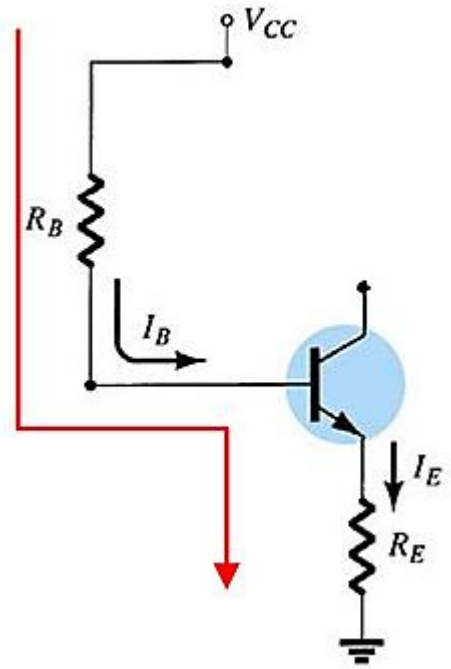
- **An emitter resistor, R_E is added to improve stability**
- **1st step**: Locate capacitors and replace them with an open circuit
- **2nd step: Locate 2 main loops which;**
  - **BE loop**
  - **CE loop**





2. Emitter-Stabilized bias circuit

- BE loop Analysis



- From kvl;

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

Recall; $I_E = (\beta + 1) I_B$

Substitute for I_E

$$-V_{CC} + I_B R_B + V_{BE} + (\beta + 1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

- CE loop Analysis

- From KVL;

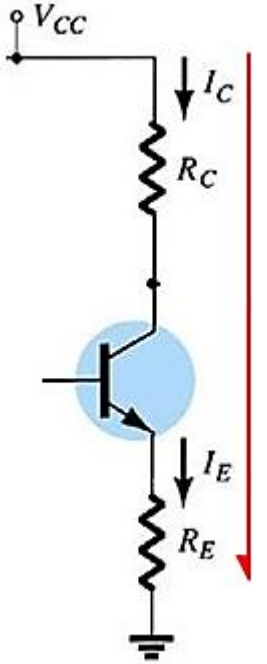
$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

- Assume;

$$I_E \approx I_C$$

- Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$



Improved Bias Stability

- The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.

Without Re

$$I_c = \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \beta$$

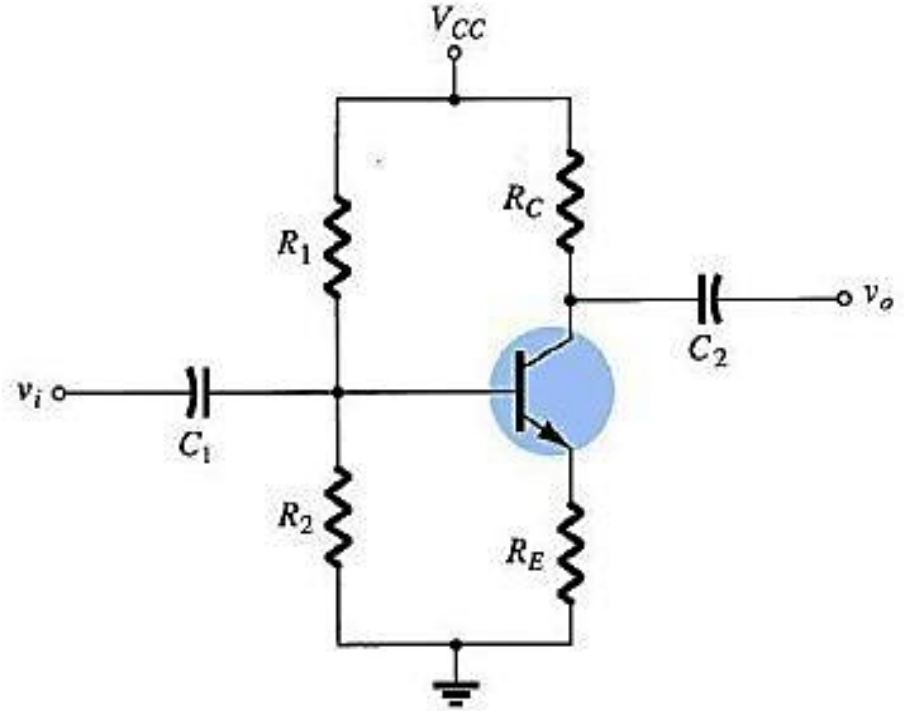
With Re

$$I_c = \left(\frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \right) \beta$$

Note :it seems that beta in numerator canceled with beta in denominator

3. Voltage Divider Bias Circuit

- Provides good Q-point stability with a single polarity supply voltage.
- This is the biasing circuit wherein, ICQ and VCEQ are almost independent of beta.
- The level of IBQ will change with beta so as to maintain the values of ICQ and VCEQ almost same, thus maintaining the stability of Q point.

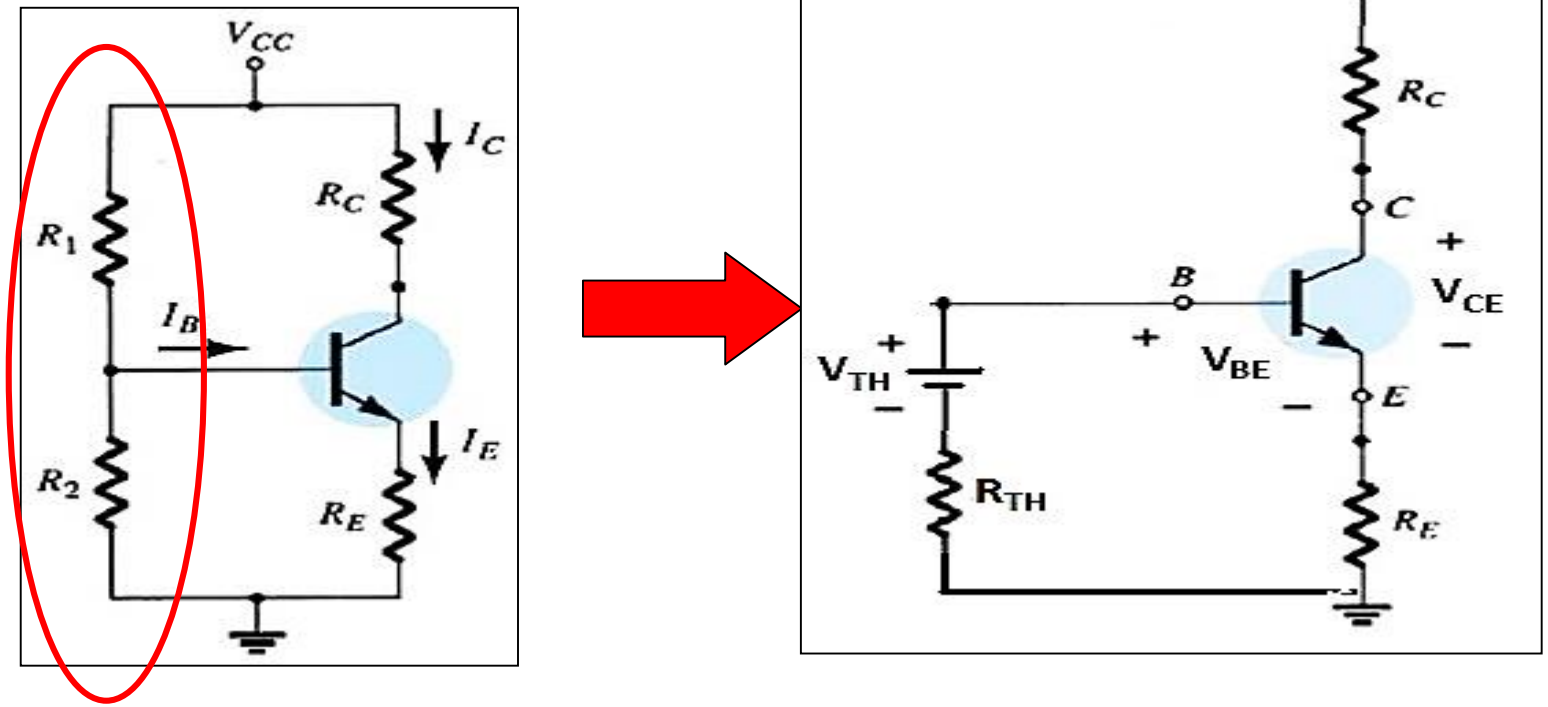


3. Voltage Divider Bias Circuit

- Two methods of analyzing a voltage divider bias circuit are:
- **Exact method : can be applied to any voltage divider circuit**
- **Approximate method : direct method, saves time and energy,**
  - 1st step: Locate capacitors and replace them with an open circuit.
  - 2nd step: Simplified circuit using Thevenin Theorem.
  - 3rd step: Locate 2 main loops which;
    - BE loop
    - CE loop

3. Voltage Divider Bias Circuit

- 2nd step: : Simplified circuit using **Thevenin Theorem**



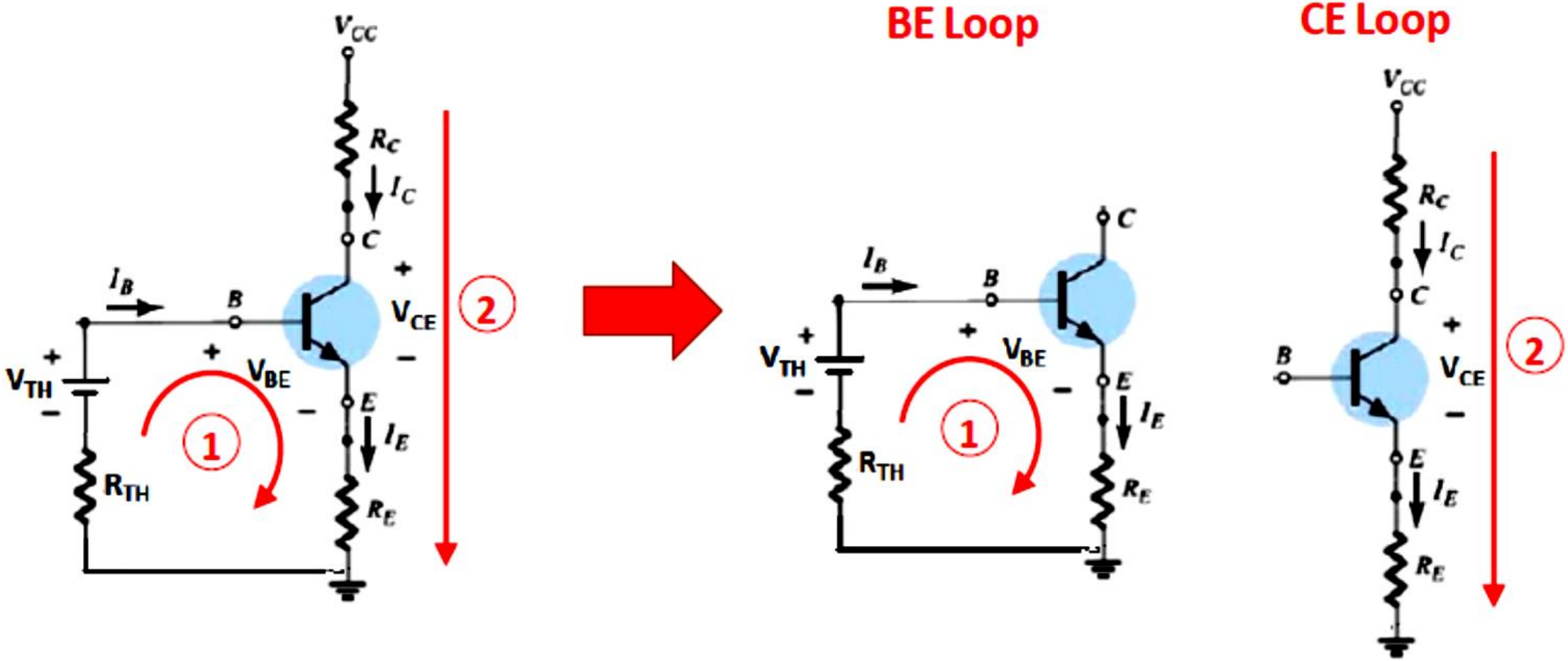
From Thevenin Theorem;

$$R_{TH} = R_1 // R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

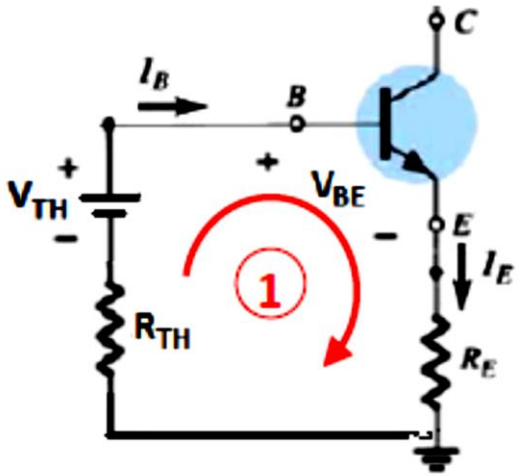
Voltage Divider Bias Circuit

- 3rd step: Locate 2 main loops.



Voltage Divider Bias Circuit

- BE loop Analysis



- From KVL;

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0$$

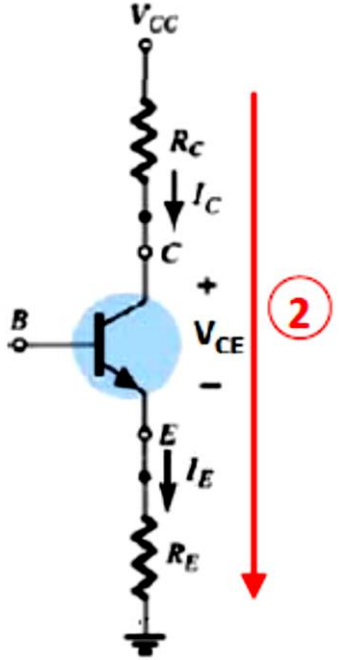
Recall; $I_E = (\beta + 1) I_B$

Substitute for I_E

$$-V_{TH} + I_B R_{TH} + V_{BE} + (\beta + 1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{TH} - V_{BE}}{R_{RTH} + (\beta + 1) R_E}$$

- CE loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

- Assume;

$$I_E \approx I_C$$

- Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

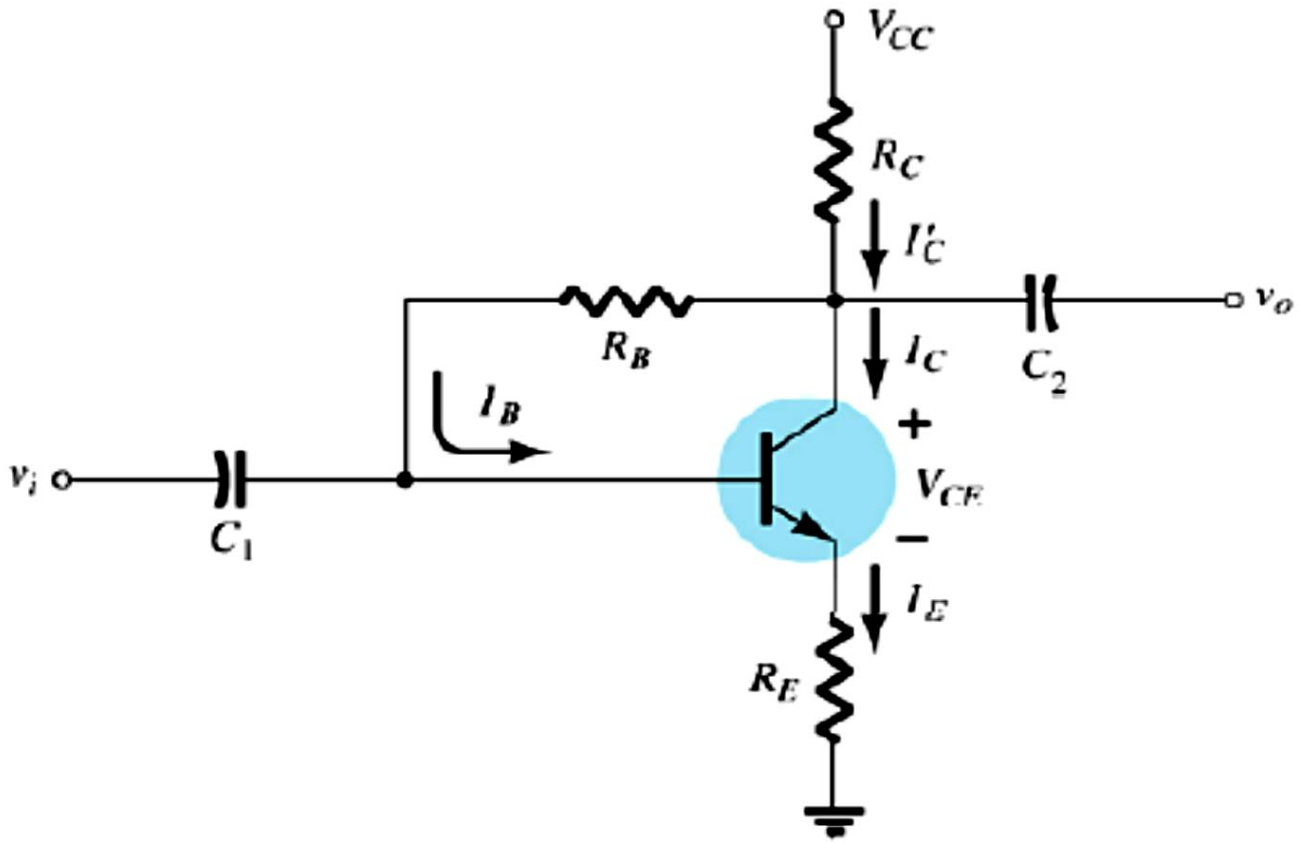
3. Voltage Divider Bias Circuit

- This voltage divider biasing configuration is the most widely used transistor biasing method.

- Also, voltage divider network biasing makes the transistor circuit independent of changes in beta as the voltages at the transistors base, emitter, and collector are dependent on external circuit values.

4. DC Bias with Voltage Feedback

- Another way to improve the stability of a bias circuit is to add a feedback path from collector to base.
- In this bias circuit the Q-point is only slightly dependent on the transistor beta, **β**



Calculate the DC Q-point

Calculating the DC Q point is done by two methods:

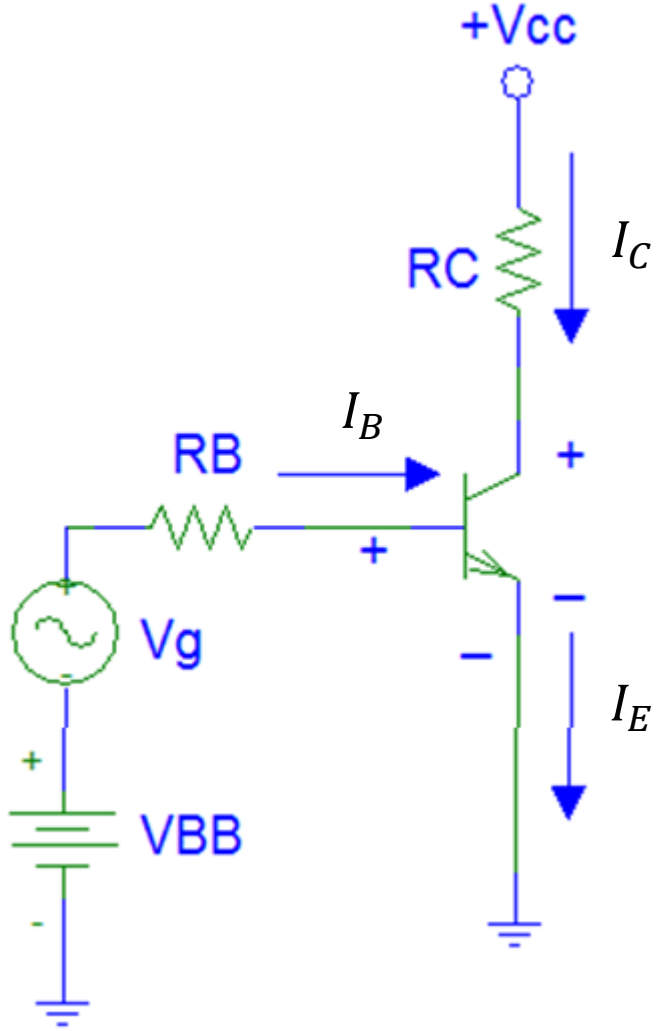
- Graphical Method " Load Line"
- Solving input & output loops

Load line analysis

- A fixed bias circuit with given values of VCC,RC and RB can be analyzed (means, determining the values of IBQ, ICQ and VCEQ) using the concept of load line also.
- Here the input loop KVL equation is not used for the purpose of analysis, instead, the output characteristics of the transistor used in the given circuit and output loop KVL equation are made use of

$$-V_{cc} + R_c I_C + V_{CE} = 0$$

$$V_{CE} = V_{cc} - R_c I_C$$



Load line analysis

$$V_{CE} = V_{cc} - R_c I_C$$

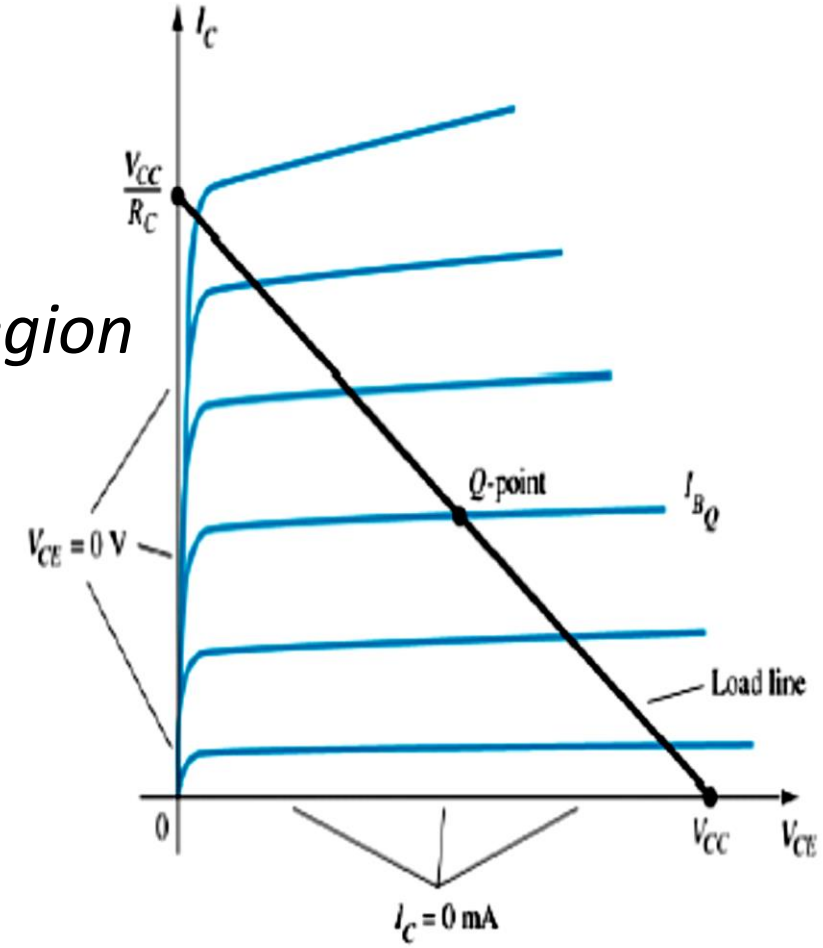
- $I_{C(sat)}$ occurs when transistor operating in *saturation region*

$$I_{C_{sat}} = \left.\frac{V_{CC}}{R_C}\right|_{V_{CE}=0}$$

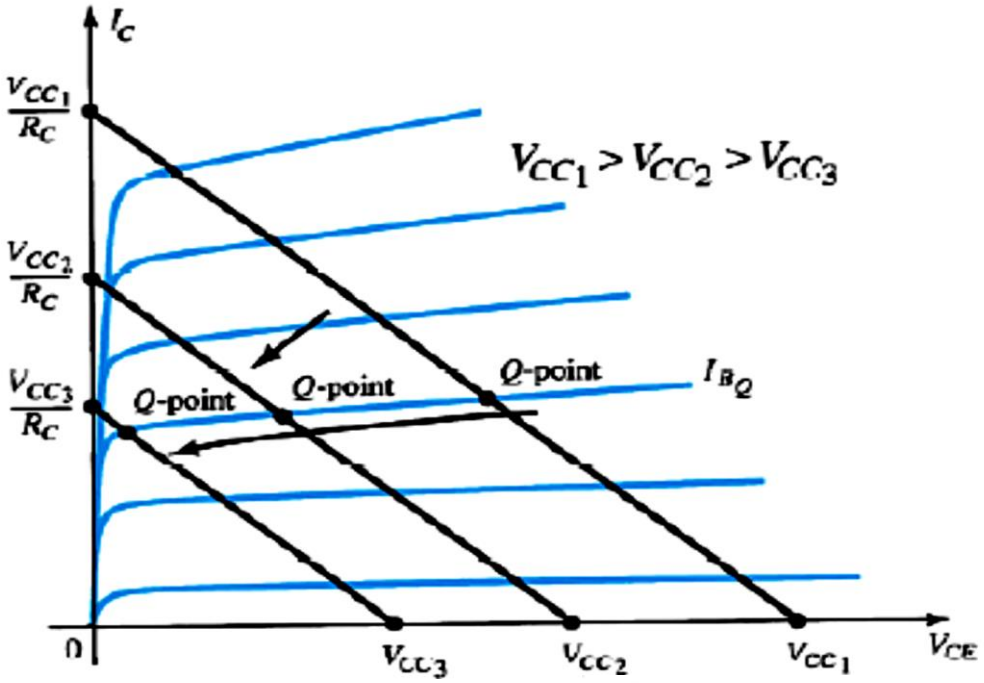
- VCE(off) occurs when transistor operating in *cut-off region*

$$V_{CE_{(off)}} = V_{CC} - I_C R_C\big|_{I_C=0}$$

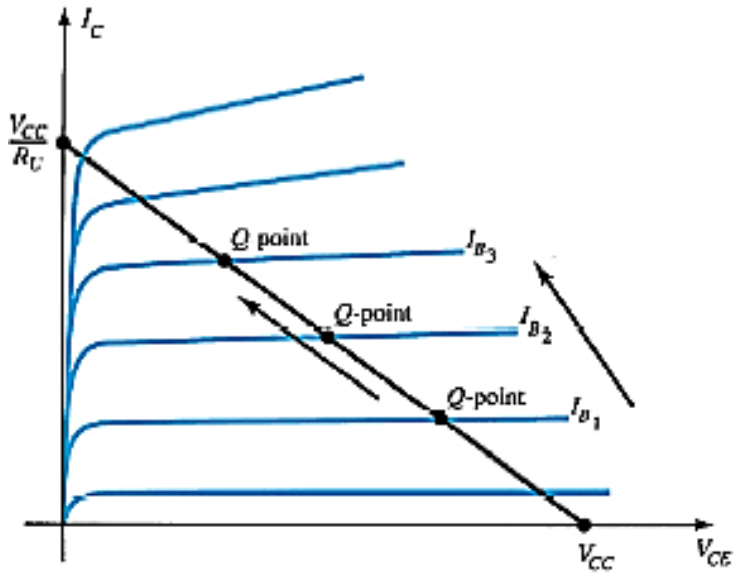
- Put these two point at given output characteristics

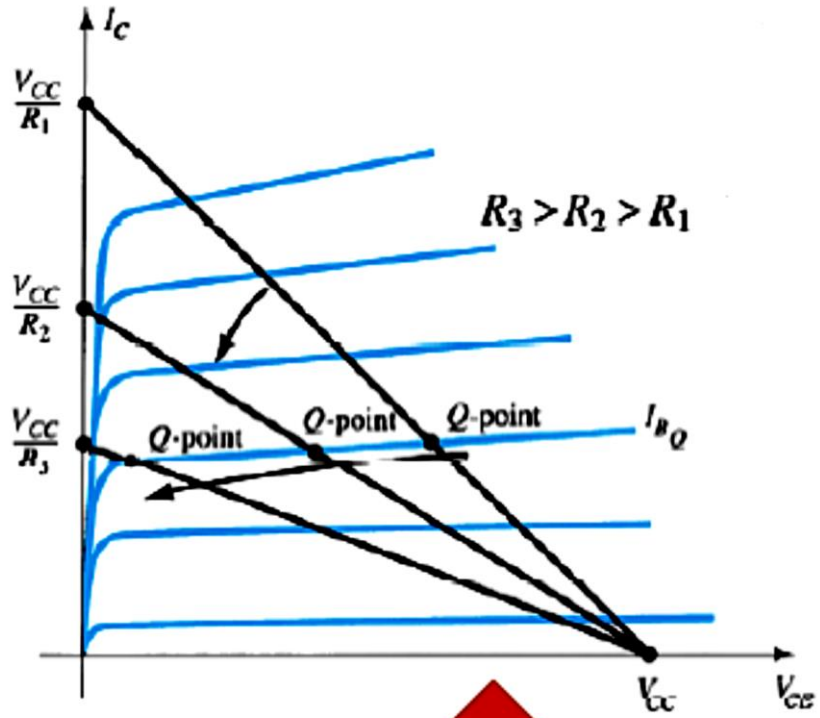


Circuit values affect the Q-point



Decreasing Vcc





Increasing Rc

Varying Ib

Solving input & output loops

Problem- solving Technique (Bipolar DC analysis) NPN:

- Before analyzing we need to know the mode of BJT operation

1- Assume that transistor is biased in the forward- Active mode in which case,

$V_{BE} = V_{BE}(ON) = 0.7\ V\ ,\quad I_B > 0,\quad I_C = \boldsymbol{\beta}\ I_B$

2- Analyze the circuit with this assumption.

3- Evaluate the resulting state of the transistor , If the initial assumed parameter values and $V_{CE} > V_{CE}$ (sat) =0.2V are true, then the initial assumption is correct. However if $I_B < 0$ then the transistor is probably cutoff and if $V_{CE} < V_{CE}$ (sat) then the transistor is likely in saturation.

4- If the initial assumption is proven incorrect, then a new assumption must be made and the new circuit must be analyzed, step 3 must then repeated.

Solving input & output loops

$$I_E = I_B + I_C$$

Active

$I_C = \boldsymbol{\beta} I_B, V_{BE} = V_{BE}(ON) = 0.7\ V$, All the current are positive.

Saturation

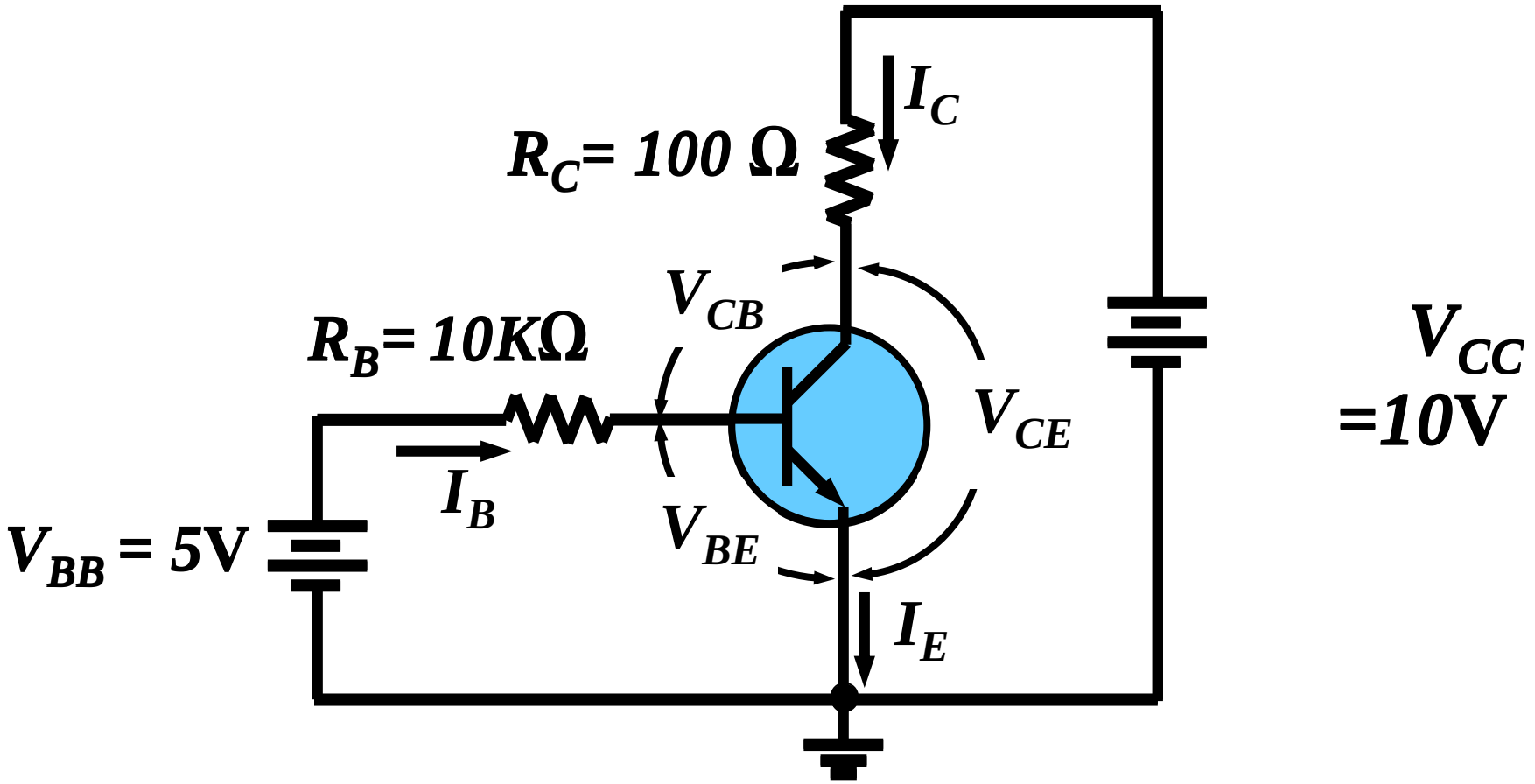
$I_C < \boldsymbol{\beta} I_B, \frac{I_C}{I_B} = \boldsymbol{\beta}_{forced} < \boldsymbol{\beta}, V_{BE} = V_{BE}(ON) = 0.7\ V, V_{CE} = V_{CE}$ (sat) $\leqslant$0.2V.

Cutoff

$I_B = I_C = I_E = 0$

Example 1

- *Determine I_B, I_C, I_E, V_{BE}, V_{CE} in the following circuit if β_{DC} is 150*



Solution

$$V_{BE} = 0.7V$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{10K\Omega} = 430\mu A$$

$$I_C = \beta_{dc} I_B = (150)(430\mu A) = 64.5mA$$

$$I_E = I_C + I_B = 64 = 64.5mA + 430\mu A = 64.9mA$$

$$V_{CE} = V_{CC} - I_C Rc$$

$$= 10V - (64.5mA)(100\Omega)$$

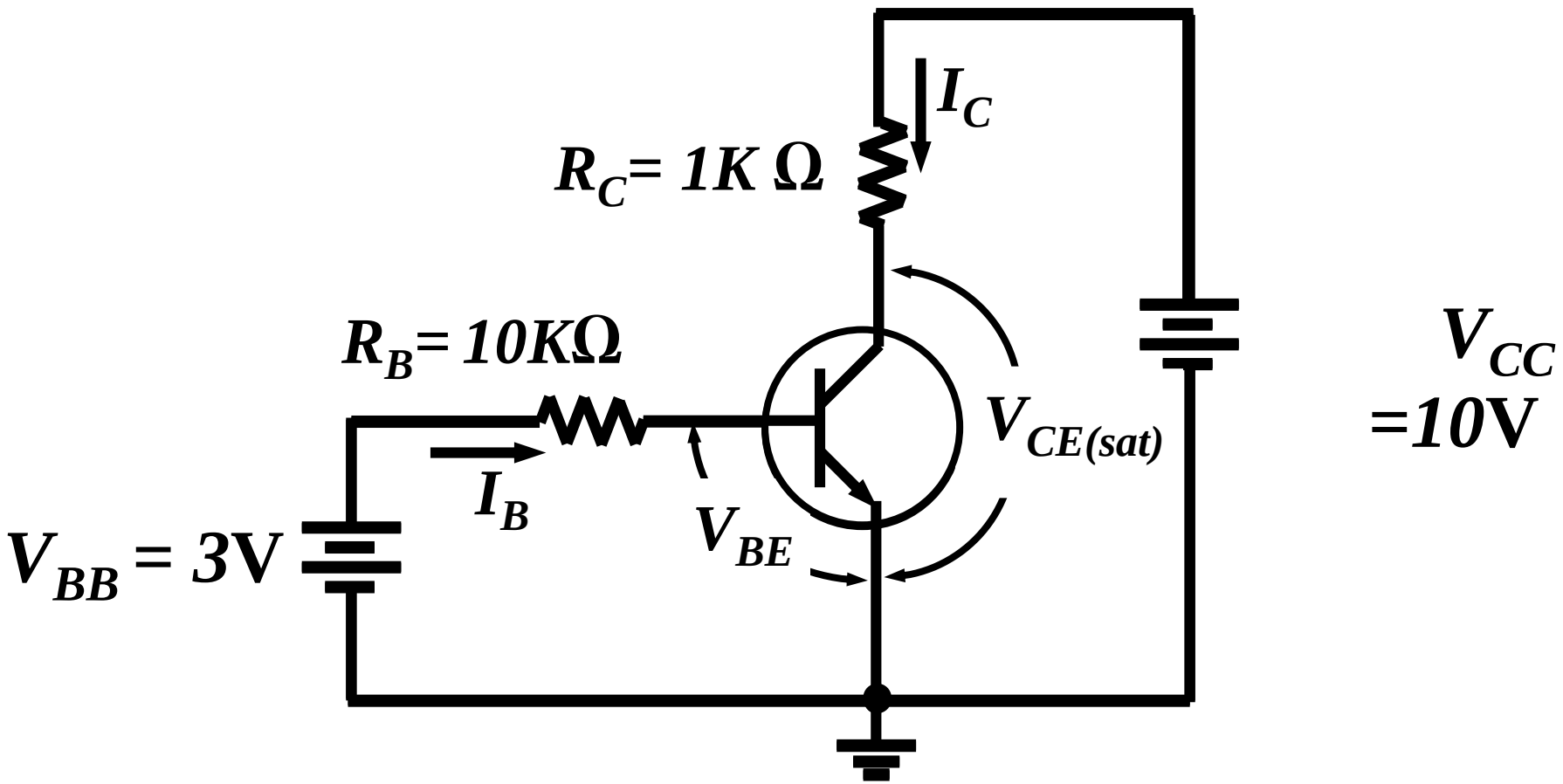
$$= 10V - 6.45V = 3.55V$$

$$V_{CB} = V_{CE} - V_{BE}$$

$$= 3.55V - 0.7V = 2.85V$$

Example 2

Determine whether or not the transistor shown in the following figure in saturation. Assume $V_{CE(sat.)}$ = 0.2 V and β_{dc} =100



Solution

Applying KVL to input circuit, we get

$$V_{BB} = I_B R_B + V_{BE}$$

$$3\text{V} = (10\ k\Omega)\ I_B + 0.7\text{V}$$

$$\therefore \boldsymbol{I_B = \frac{3\text{V} - 0.7\text{V}}{10k\Omega} = \frac{2.3\text{V}}{10k\Omega} = 0.230\text{mA}}$$

Applying KVL to output circuit, we get

$$V_{CC} = I_C R_C + V_{CE(sat)}$$

$$10V = (1k\Omega)\, I_C + 0.2V$$

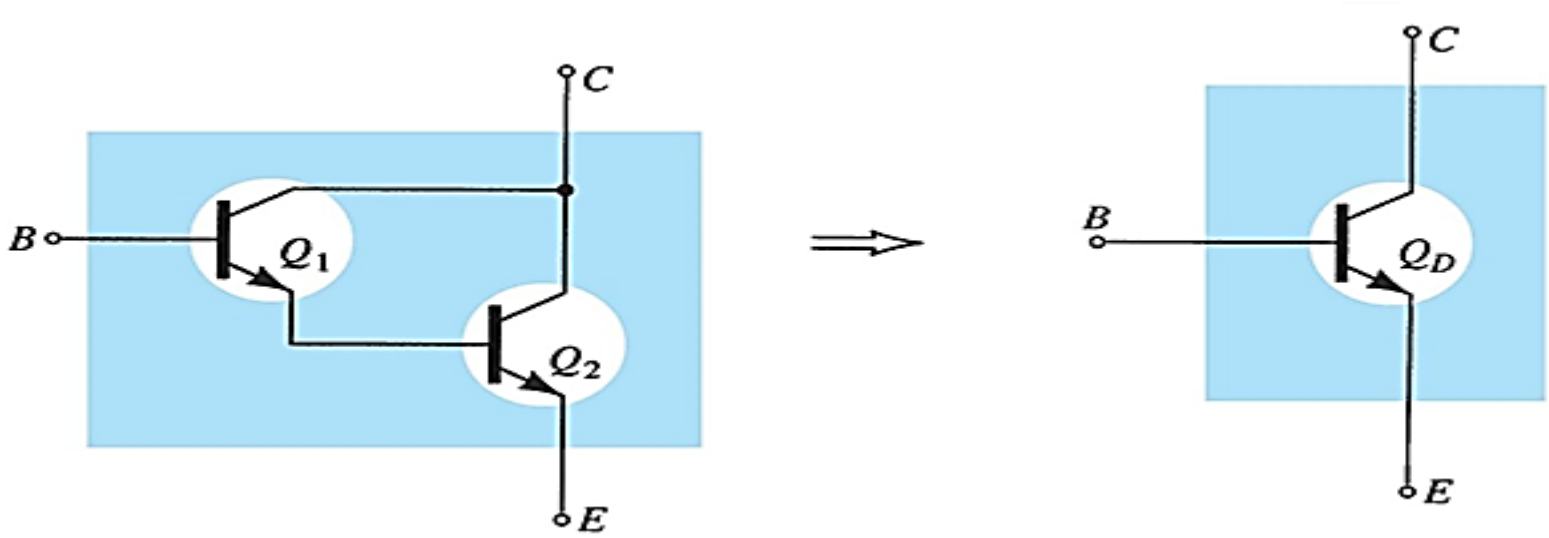
$$\therefore I_C = \frac{10\text{V} - 0.2\text{V}}{1k\Omega} = \frac{9.8\text{V}}{1k\Omega} = 9.8\text{mA}$$

$$I_{B(\min)} = I_C / \beta_{dc} = 9.8 \text{ mA} / 100 = 0.098 \text{ mA}$$

$$\because I_B = 0.220mA > I_{B(\min)} = 0.098mA$$

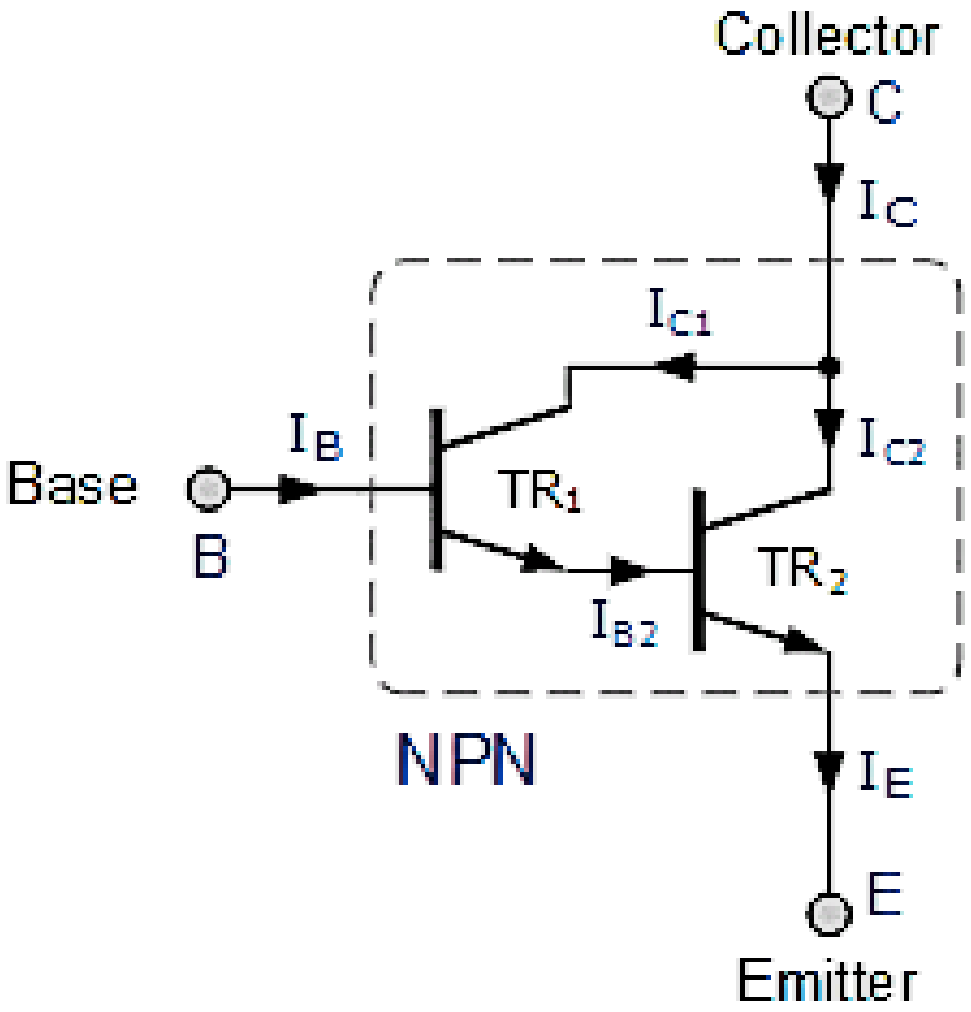
Therefore, the transistor is saturated

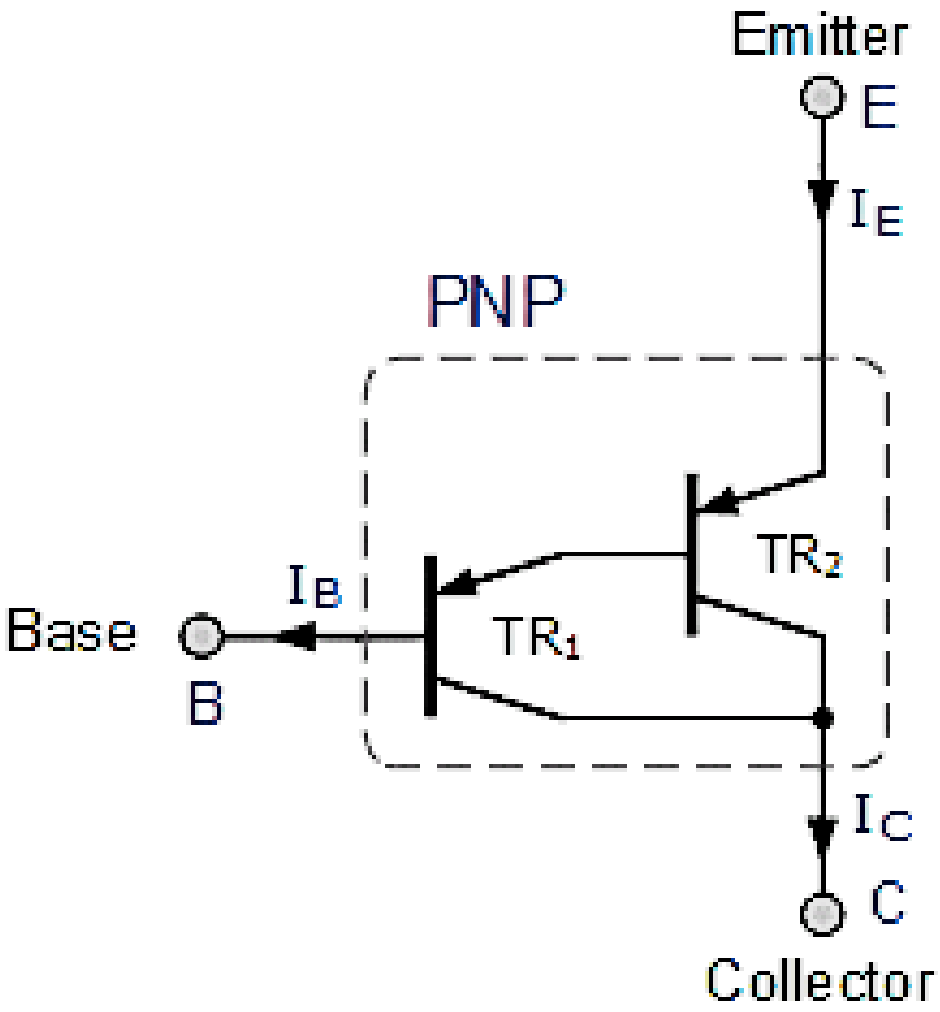
Darlington Connection



- The Darlington circuit provides a very high current gain—the product of the individual current gains: $\beta_D = \beta_1 \beta_2$
- A Darlington transistor connection provides a transistor having a very large current gain, typically a few thousand.
- Darlington pairs are available as complete packages.
- A Darlington pair is sufficiently sensitive to respond to the small current.

Darlington Connection





DC Bias of Darlington Circuits

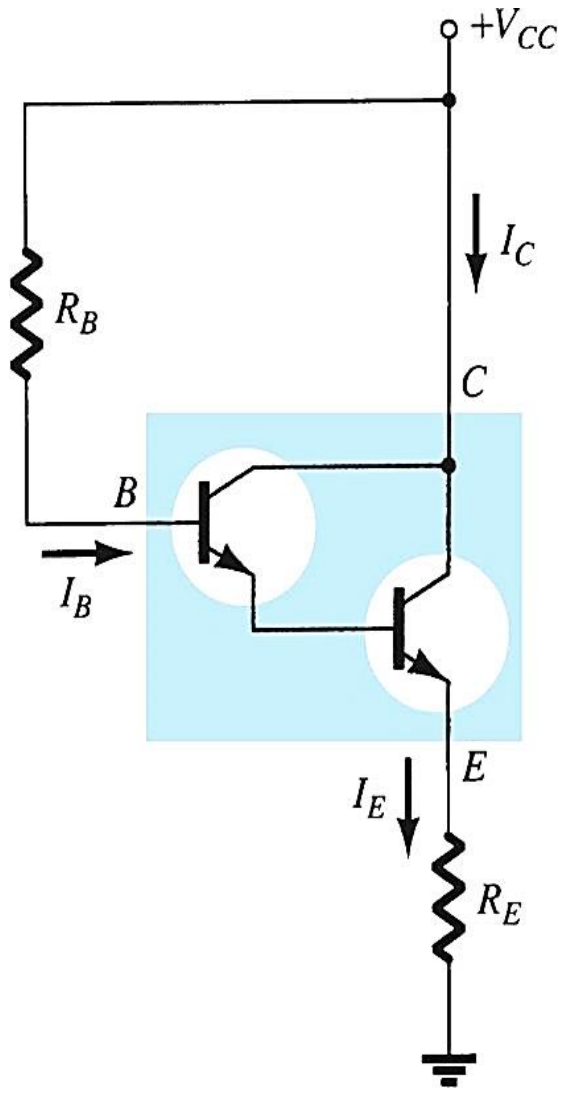
$$-V_{cc} + I_B R_B + V_B = 0$$

$$V_B = V_{BE} + V_E$$

$$V_E = I_E R_E$$

$$I_E = (\beta_D + 1) I_B \cong \beta_D I_B$$

$$-V_{cc} + I_B R_B + V_{BE} + \beta_D I_B R_E = 0$$



- Base current $$\mathbf{I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta_D R_E}}$$
- Emitter Current $$\mathbf{I_E = (\beta_D + 1) I_B \cong \beta_D I_B}$$