# Electronic Circuits

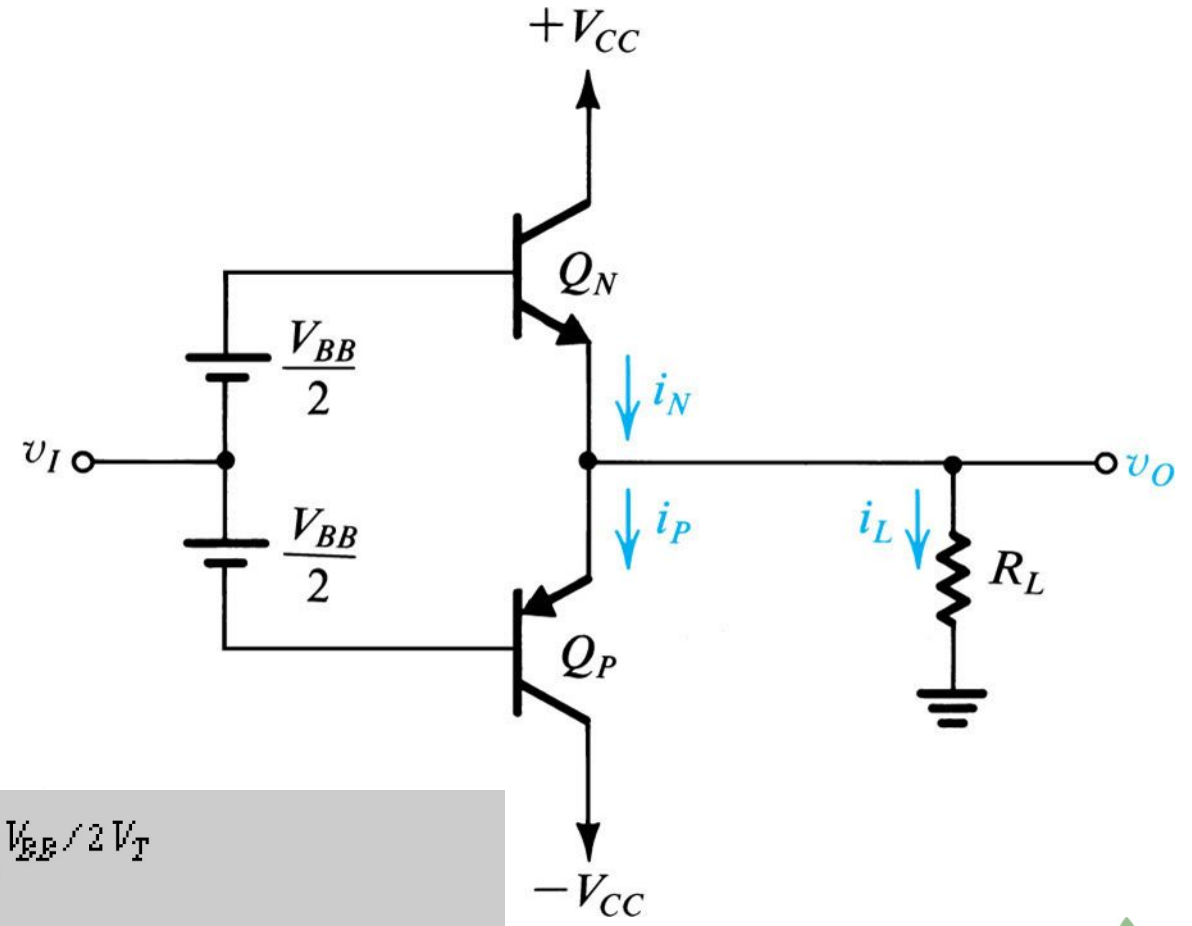
## Lecture (9)

## Power Amplifiers Class AB Amplifiers

## Power BJTs

# 3. Class AB Output Stage

- Crossover distortion can be virtually eliminated by biasing the complementary output transistors at a small nonzero current.
- The result is the class AB output stage shown in Figure.
- A bias voltage $V_{BB}$ is applied between the bases of $Q_N$ and $Q_P$.
- For Vi = 0, Vo= 0, and a voltage appears across the base–emitter junction of each of of $Q_N$ and $Q_P$. Assuming matched devices,




$$i_N = i_P = I_Q = I_S e^{V_{BB}/2V_T}$$

The value of $V_{BB}$ is selected to yield the required quiescent current $I_Q$

# Circuit Operation

When $v_I$ goes positive by a certain amount, the voltage at the base of $Q_N$ increases by the same amount and the output becomes positive at an almost equal value,

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN} \tag{11.24}$$

The positive $v_O$ causes a current $i_L$ to flow through $R_L$, and thus $i_N$ must increase; that is,

$$i_N = i_P + i_L \tag{11.25}$$

The increase in $i_N$ will be accompanied by a corresponding increase in $v_{BEN}$ (above the quiescent value of $V_{BB}/2$). However, since the voltage between the two bases remains constant at $V_{BB}$, the increase in $v_{BEN}$ will result in an equal decrease in $v_{EBP}$ and hence in $i_P$. The relationship between $i_N$ and $i_P$ can be derived as follows:

$$v_{BEN} + v_{EBP} = V_{BB}$$

$$V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S}$$

$$i_N i_P = I_Q^2 \tag{11.26}$$

Thus, as $i_N$ increases, $i_P$ decreases by the same ratio while the product remains constant. Equations (11.25) and (11.26) can be combined to yield $i_N$ for a given $i_L$ as the solution to the quadratic equation

$$i_N^2 - i_L i_N - I_Q^2 = 0 \tag{11.27}$$

We conclude that the class AB stage operates in much the same manner as the class B circuit, with one important exception: For small $v_I$, both transistors conduct, and as $v_I$ is increased or decreased, one of the two transistors takes over the operation.

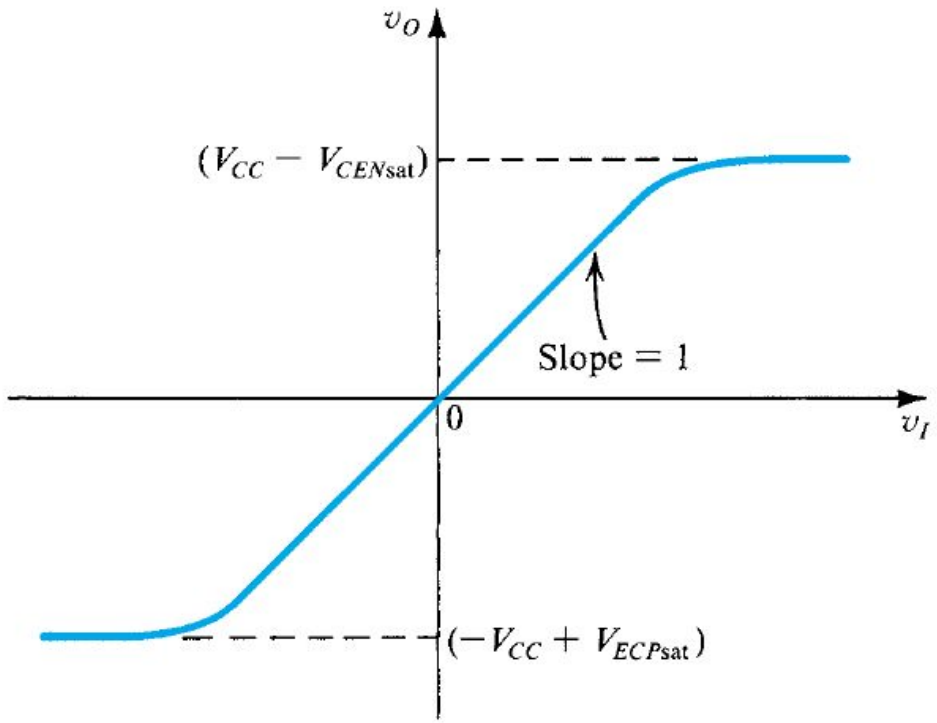


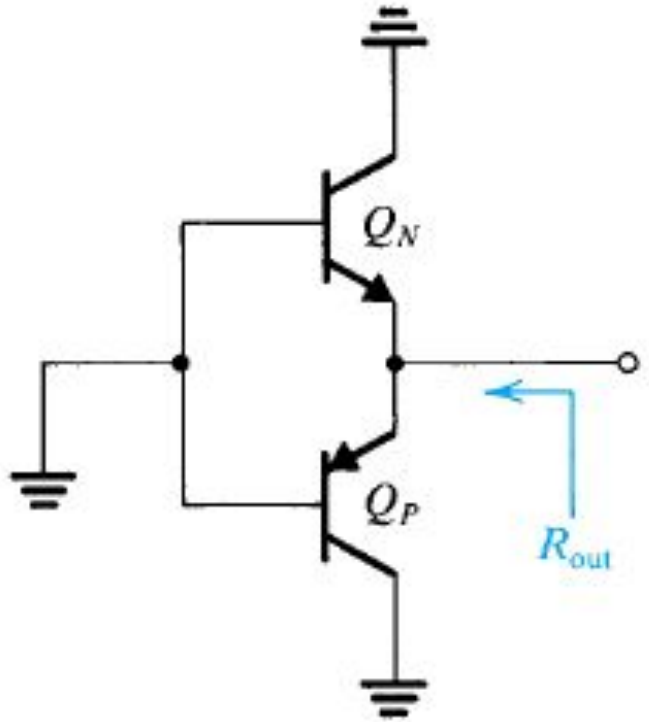

**Figure 11.12** Transfer characteristic of the class AB stage

# Output Resistance

$$R_{\text{out}} = r_{eN} \| r_{eP}$$

$$r_{eN} = \frac{V_T}{i_N}$$

$$r_{eP} = \frac{V_T}{i_P}$$




$$R_{\text{out}} = \frac{V_T}{i_N} \| \frac{V_T}{i_P} = \frac{V_T}{i_P + i_N}$$

# Example:

A class AB output stage with:

$V_{cc}$ = 15 V, $I_Q$ = 2 mA and $R_L$ = 100 Ω.

Assuming $Q_N$ and $Q_P$ are matched and have $I_S = 10^{-13}$ A ,

1. Calculate the bias voltage ($V_{BB}$).
2. Calculate $i_L$, $i_N$, $i_P$, $V_{BEN}$, $V_{EBP}$, $V_I$ , DC gain($V_o/V_I$)

and

$R_{out}$ for $Vo$ = +10V, 0V and -10V.

3. Calculate the quiescent power dissipation (PQ).

# Solution:

[1] $V_{BB} = 2V_T \ln \frac{I_Q}{I_S}$

$V_{BB} = 2 \times 0.025 \ln \frac{2 \times 10^{-3}}{1 \times 10^{-13}} = 1.186V$

[2] [a] $V_o = 10V$

* $i_L = \frac{V_o}{R_L} = \frac{10V}{0.1K\Omega} = 100\,mA$

* $i_N^2 - i_L i_N - I_Q^2 = 0$

$i_N^2 - 100\, i_N - 4 = 0$ solving

$i_N = 100.04\,mA$

* $i_P = i_N - i_L = 100.04\,mA - 100$

$i_P = 0.04\,mA$

* $V_{BEN} = V_T \ln \frac{i_N}{I_S}$

$= 0.025 \ln \frac{100.04 \times 10^{-3}}{10^{-13}} = .691\,V$

* $V_{EBP} = V_T \ln \frac{i_P}{I_S}$

$= 0.025 \ln \frac{0.04 \times 10^{-3}}{10^{-13}} = 0.495\,V$

* $V_O = V_I + \frac{V_{BB}}{2} - V_{BEN}$

$\therefore \boxed{V_I = V_o + V_{BEN} - \frac{V_{BB}}{2}} = 10 + 0.691 - \frac{1.186}{2} = 10.\%8$

$\boxed{V_I \cong 10.1V}$

* $\frac{V_o}{V_I} = \frac{10}{10.1} = 0.99$ ( D.C gain)

* $R_{out} = \frac{V_T}{i_p + i_N} = \frac{0.025}{0.04 + 100.04} = 0.0.0.25k\Omega = 0.25\Omega$

* $A_V = \frac{R_L}{R_{out} + R_L} = \frac{100}{100 + 0.25} = 0.9975$ (incremental gain)

[3] $P_Q = 2V_{CC} I_Q = 2 \times 15 \times 2 = 60mW$

[4] $V_o = 0 \rightarrow i_L = \frac{V_o}{R_L} = 0$

$\therefore i_N^2 = I_Q^2 \rightarrow i_N = I_Q = 2mA$

* $i_p = i_N - i_L = 2mA$

[5] $V_o = -10V \rightarrow i_L = \frac{-10V}{100\Omega} = -100mA$

# Biasing Class AB

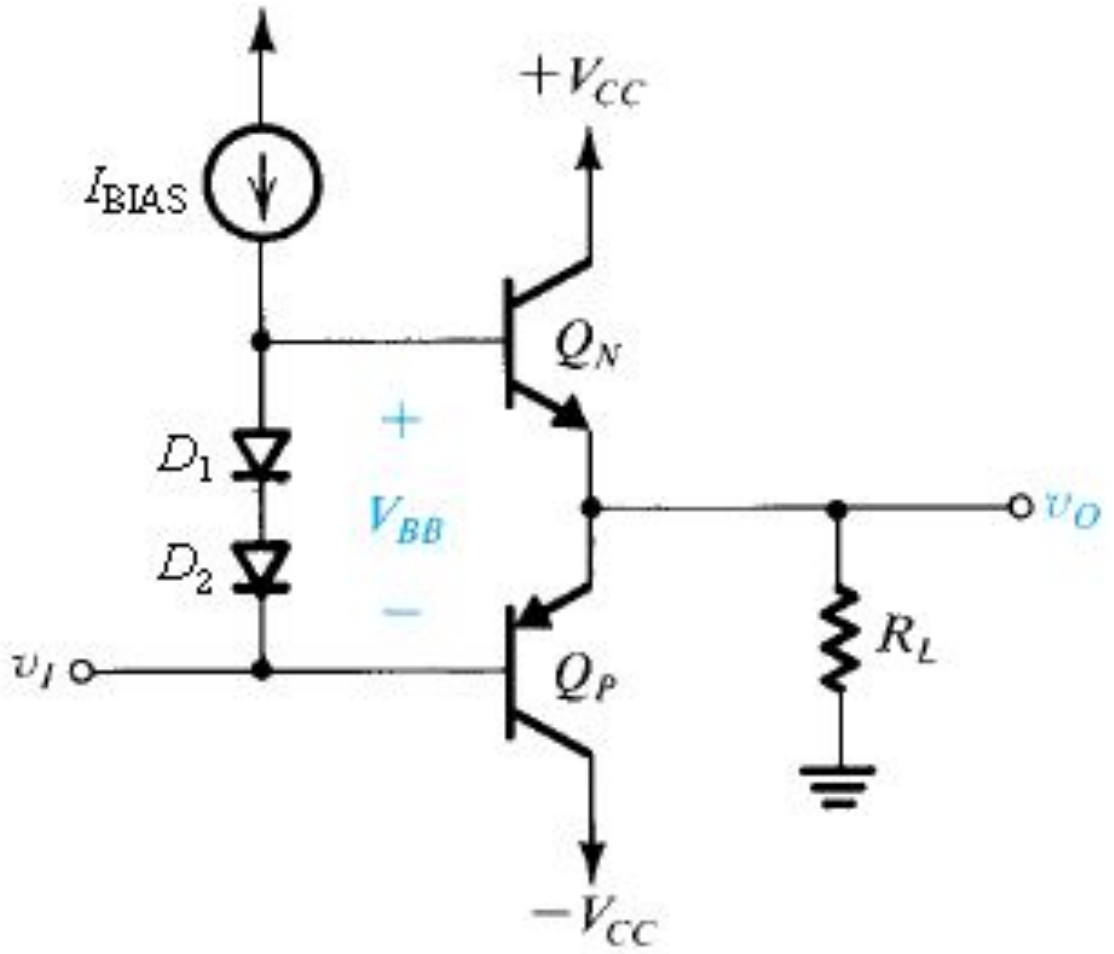
## Biasing Using Diodes

* $V_{BB}$ is generated by passing a constant current $I_{Bias}$ through a pair of diodes $D_1, D_2$ or diode-connected transistors.
* The output BJTs are Large geometry device.
* The diodes $D_1, D_2$ not required to be Large.
* The quiscent current in $Q_N$ and $Q_P$ ($I_Q$)

$$I_Q = n\, I_{Bias}$$

$$n = \frac{(E\text{-}B)\ \text{Junction area of } Q_N, Q_P}{\text{Area of } D_1, D_2}$$

↳ Relative size ratio



$$n = \frac{I_Q}{I_{Bias}} = \frac{I_S(Q_N, Q_P)}{I_S(D_1, D_2)}$$

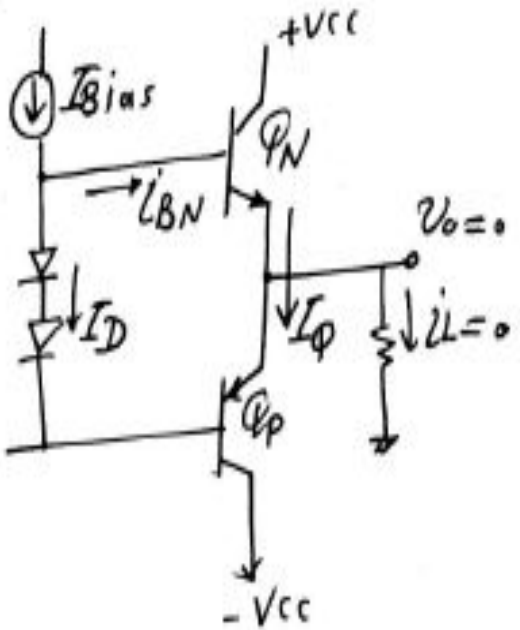
* $V_{BB} = 2 V_T \ln \frac{I_D}{I_S}$ → diodes $D_1, D_2$ ; → For $D_1, D_2$

[1] For $V_O = 0$

$$i_{EN} = i_{EP} = I_Q$$

* $i_{BN} = \frac{I_Q}{1+\beta} \cong \frac{I_Q}{\beta}$

* $I_{Bias} = i_{BN} + I_D$

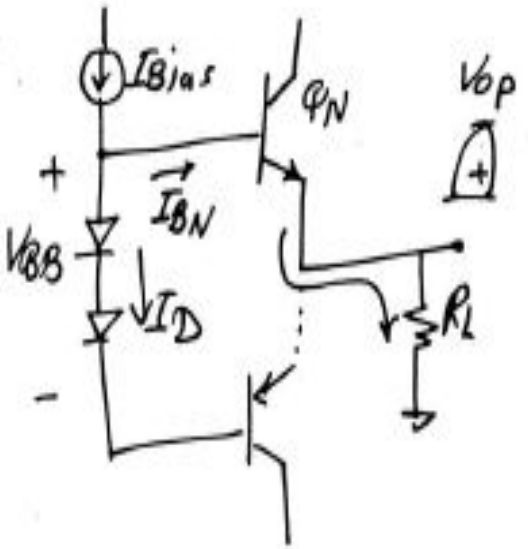



[2] For $V_O = V_{op}$ (peak +ve o/p)

* $i_L = i_{EN} = \frac{V_o}{R_L}$

* $i_{BN} = \frac{i_{EN}}{1+\beta} \cong \frac{i_{EN}}{\beta}$

* $I_{Bias} = i_{BN} + I_D$




[3] For $V_O = -V_{op}$ (peak -ve)

$Q_N$ draw very small base current $i_{BN} \cong 0$

$\therefore I_D = I_{Bias}$

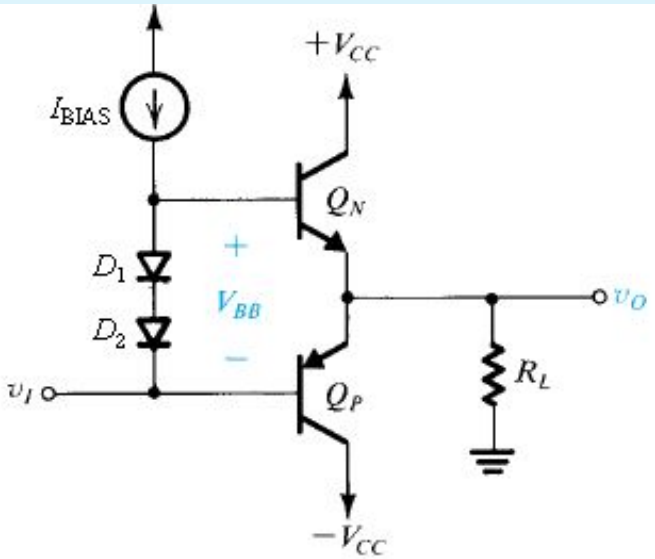
$R_{out} = r_{eN} \| r_{eP}$ , $r_{eN} = r_{eP}$

$R_{out} = \frac{r_e}{2}$ , $r_e = \frac{V_T}{I_Q}$

$A_V = \frac{R_L}{R_{out} + R_L}$

# Example:

Consider the class AB output stage under the conditions that $V_{CC} = 15$ V, $R_L = 100\ \Omega$, and the output is sinusoidal with a maximum amplitude of 10 V. Let $Q_N$ and $Q_P$ be matched with $I_S = 10^{-13}$ A and $\beta = 50$. Assume that the biasing diodes have one-third the junction area of the output devices. Find the value of $I_{BIAS}$ that guarantees a minimum of 1 mA through the diodes at all times. Determine the quiescent current and the quiescent power dissipation in the output transistors (i.e., at $v_O = 0$). Also find $V_{BB}$ for $v_O = 0$, +10 V, and −10 V.



# Solution:

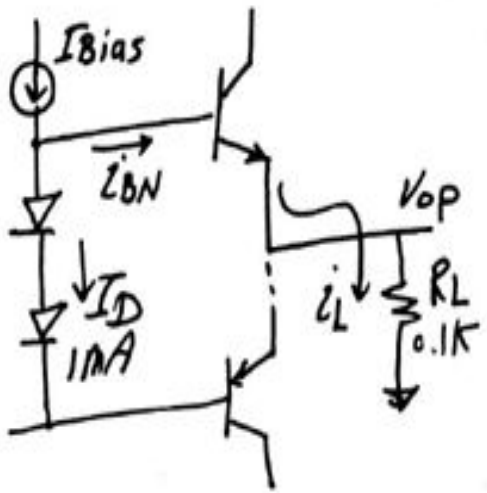
* $V_{CC} = 15V$ $\quad R_L = 100\Omega$ $\quad V_{op} = 10V$

* $I_S(Q_N, Q_P) = 10^{-13} A$ $\quad \beta = 50$.

$$\frac{Area(D_1, D_2)}{Area(Q_N, Q_P)} = \frac{1}{3} \rightarrow I_S(D_1, D_2) = \frac{1}{3} \times 10^{-13} A$$

[a] * Find $I_{Bias}$ such that $I_{D(min)} = 1mA$

* For $V_o = +10V$




* $i_L = i_{EN} = \frac{V_{op}}{R_L} = \frac{10}{0.1K}$

$\boxed{i_{EN} = 100mA}$

* $i_{BN} = \frac{i_{EN}}{1+\beta} \cong \frac{i_{EN}}{\beta} = \frac{100}{50}$

$\boxed{i_{BN} = 2mA}$

* $I_D = 1mA$ (given)

$\therefore \boxed{I_{Bias} = 3mA}$

[b] Quiescent Current ($I_Q$)

$$n = \frac{area(Q_N, Q_P)}{area(D_1, D_2)} = 3 = \frac{I_Q}{I_{Bias}}$$

$\therefore \boxed{I_Q = 3 \times 3 = 9mA}$

Quiescent power dissipation

$P_Q = 2 V_{CC} . I_Q = 2 \times 15 \times 9 = 270mW$

[c] Find VBB for :-

[1] $V_o = 0$

* $i_{EN} = i_{Ep} = I_\Phi = 9mA$
* $i_{BN} = \frac{i_{EN}}{1+\beta} = \frac{9}{51} \simeq \frac{9}{50} = 0.18mA$
* $I_D = I_{Bias} - i_{BN} = 3 - 0.18 = 2.82mA$
* $V_{BB} = 2V_T \ln \frac{I_D}{I_S}$

$\therefore V_{BB} = 2 \times 0.025 \ln \frac{2.82 \times 10^{-3}}{\frac{1}{3} \times 10^{-13}} = 1.26V$

$\boxed{V_{BB} = 1.26V}$

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[2] $V_o = 10V$

* $i_{EN} = i_L = 100mA$
* $i_{BN} = 2mA$
* $I_D = 3 - 2 = 1mA$
* $V_{BB} = 2V_T \ln \frac{I_D}{I_S} = 2 \times 0.025 \ln \frac{1 \times 10^{-3}}{\frac{1}{3} \times 10^{-13}}$

$\boxed{V_{BB} = 1.21V}$

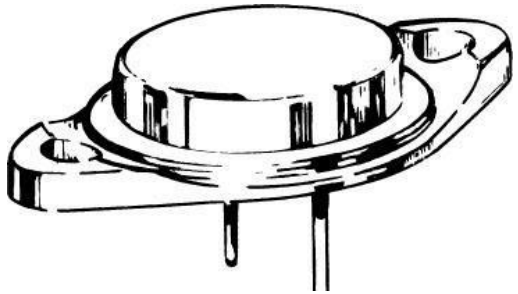
[3] $V_o = -10V$

* $i_{EN} \simeq 0$
* $i_{BN} \simeq 0$
* $I_D = I_{Bias} = 3mA$
* $V_{BB} = 2 \times 0.025 \ln \frac{3 \times 10^{-3}}{\frac{1}{3} \times 10^{-13}}$

$V_{BB} \simeq 1.26V$

# The Power BJTs

**Transistors that are required to conduct currents in the ampere range and to withstand power dissipation in the watts and tens-of-watts ranges differ in their physical structure, packaging, and specification from the small-signal transistors.**



## Junction Temperature

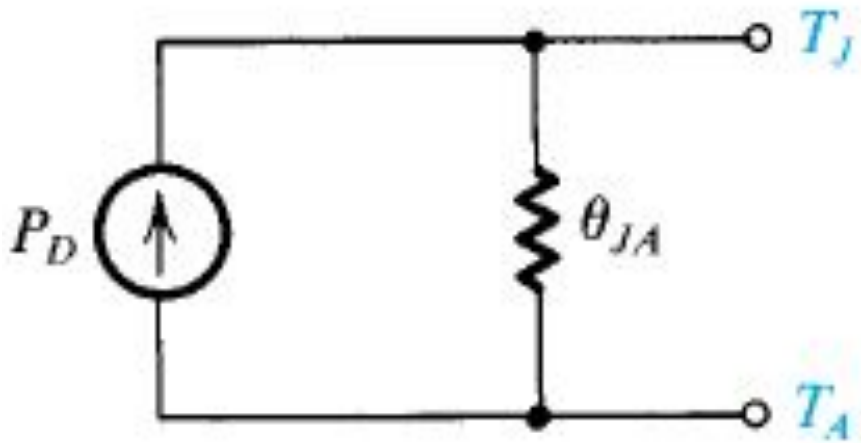
Power transistors dissipate large amounts of power in their collector–base junctions. The dissipated power is converted into heat, which raises the junction temperature. However, the junction temperature $T_j$ must not be allowed to exceed a specified maximum, $T_{jmax}$; otherwise the transistor could suffer permanent damage. For silicon devices, $T_{jmax}$ is in the range of 150°C to 200°C.

# Thermal Resistance

Consider first the situation of a transistor operating in free air—that is, with no special arrangements for cooling. The heat dissipated in the transistor junction will be conducted away from the junction to the transistor case, and from the case to the surrounding environment. In a steady state in which the transistor is dissipating $P_D$ watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as

$$T_J - T_A = \theta_{JA} P_D$$

where $\theta_{JA}$ is the **thermal resistance** between junction and ambience, having the units of degrees Celsius per watt.



# Power Dissipation Versus Temperature

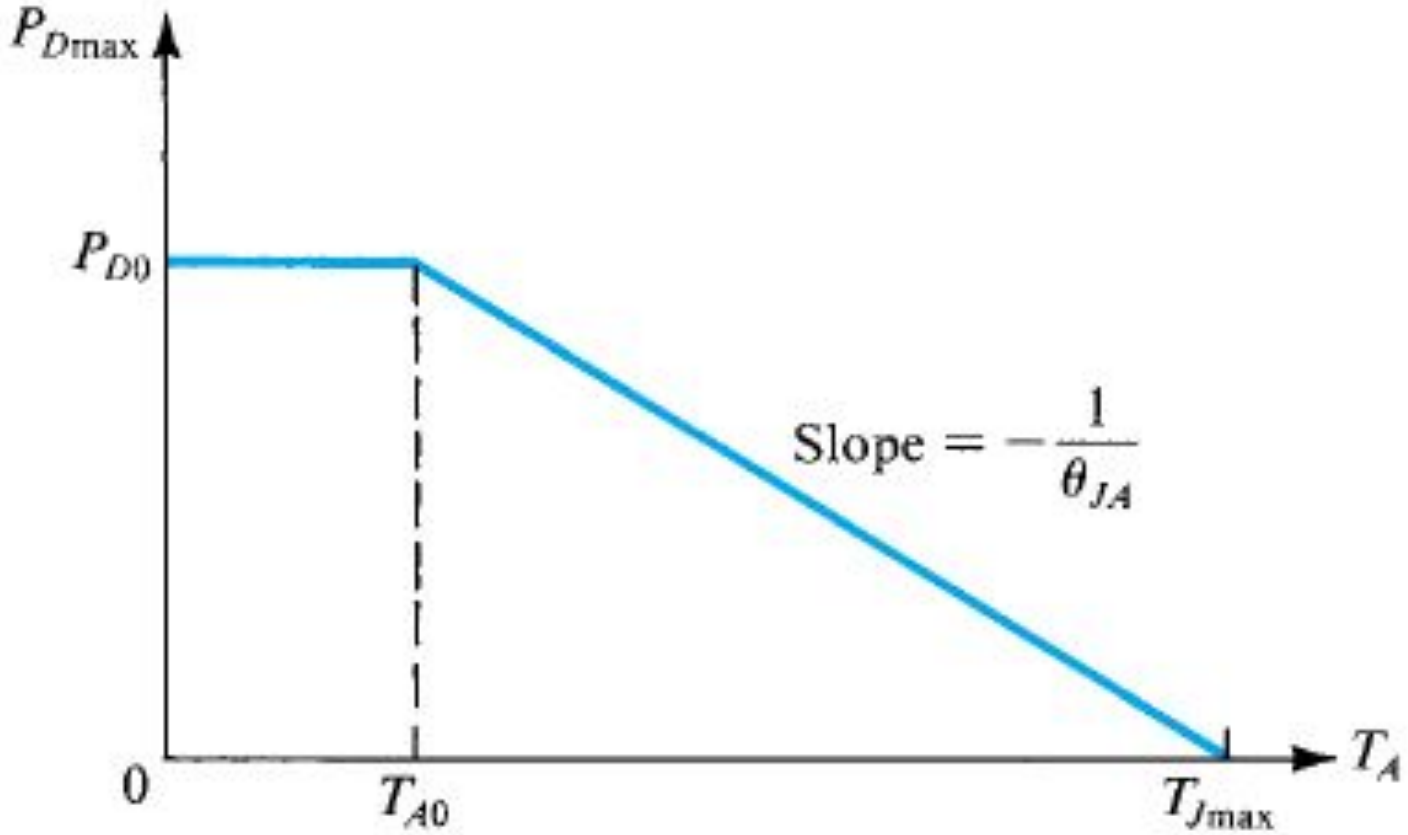



**Figure 11.24** Maximum allowable power dissipation versus ambient temperature for a BJT operated in free air. This is known as a "power-derating" curve.

thermal resistance $\theta_{JA}$. In addition, a graph such as that shown in Fig. 11.24 is usually provided. The graph simply states that for operation at ambient temperatures below $T_{A0}$, the device can safely dissipate the rated value of $P_{D0}$ watts. However, if the device is to be operated at higher ambient temperatures, the maximum allowable power dissipation must be **derated** according to the straight line shown in Fig. 11.24. The **power-derating curve** is a graphical representation of Eq. (11.69). Specifically, note that if the ambient temperature is $T_{A0}$ and the power dissipation is at the maximum allowed ($P_{D0}$), then the junction temperature will be $T_{J\max}$. Substituting these quantities in Eq. (11.69) results in

$$\theta_{JA} = \frac{T_{J\max} - T_{A0}}{P_{D0}} \tag{11.70}$$

which is the inverse of the slope of the power-derating straight line. At an ambient temperature $T_A$, higher than $T_{A0}$, the maximum allowable power dissipation $P_{D\max}$ can be obtained from Eq. (11.69) by substituting $T_J = T_{J\max}$; thus,

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} \tag{11.71}$$

Observe that as $T_A$ approaches $T_{J\max}$, the allowable power dissipation decreases; the lower thermal gradient limits the amount of heat that can be removed from the junction. In the extreme situation of $T_A = T_{J\max}$, no power can be dissipated because no heat can be removed from the junction.

## Example 11.7

A BJT is specified to have a maximum power dissipation $P_{D0}$ of 2 W at an ambient temperature $T_{A0}$ of 25°C, and a maximum junction temperature $T_{Jmax}$ of 150°C. Find the following:

(a) The thermal resistance $\theta_{JA}$.
(b) The maximum power that can be safely dissipated at an ambient temperature of 50°C.
(c) The junction temperature if the device is operating at $T_A = 25°C$ and is dissipating 1 W.

### Solution

(a) $$\theta_{JA} = \frac{T_{Jmax} - T_{A0}}{P_{D0}} = \frac{150 - 25}{2} = 62.5\,°C/W$$

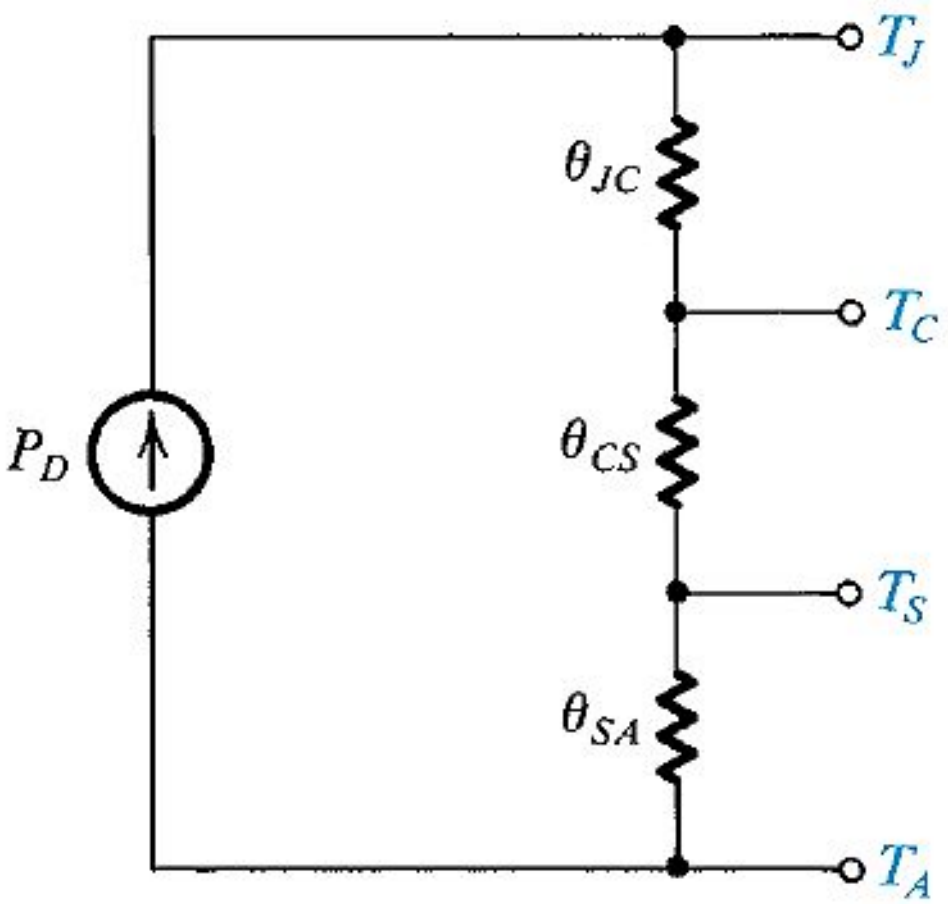
(b) $$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6\ W$$

(c) $$T_J = T_A + \theta_{JA} P_D = 25 + 62.5 \times 1 = 87.5°C$$

# Transistor Case and Heat Sink

$$T_J - T_A = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

$$P_{D\max} = \frac{T_{J\max} - T_C}{\theta_{JC}}$$



# Example 11.8

A BJT is specified to have $T_{J\max} = 150°C$ and to be capable of dissipating maximum power as follows:

$$40 \text{ W at } T_C = 25°C$$
$$2 \text{ W at } T_A = 25°C$$

Above 25°C, the maximum power dissipation is to be derated linearly with $\theta_{JC} = 3.12°C/W$ and $\theta_{JA} = 62.5°C/W$. Find the following:

(a) The maximum power that can be dissipated safely by this transistor when operated in free air at $T_A = 50°C$.
(b) The maximum power that can be dissipated safely by this transistor when operated at an ambient temperature of 50°C, but with a heat sink for which $\theta_{CS} = 0.5°C/W$ and $\theta_{SA} = 4°C/W$. Find the temperature of the case and of the heat sink.
(c) The maximum power that can be dissipated safely if an *infinite heat sink* is used and $T_A = 50°C$.

## Solution

(a)

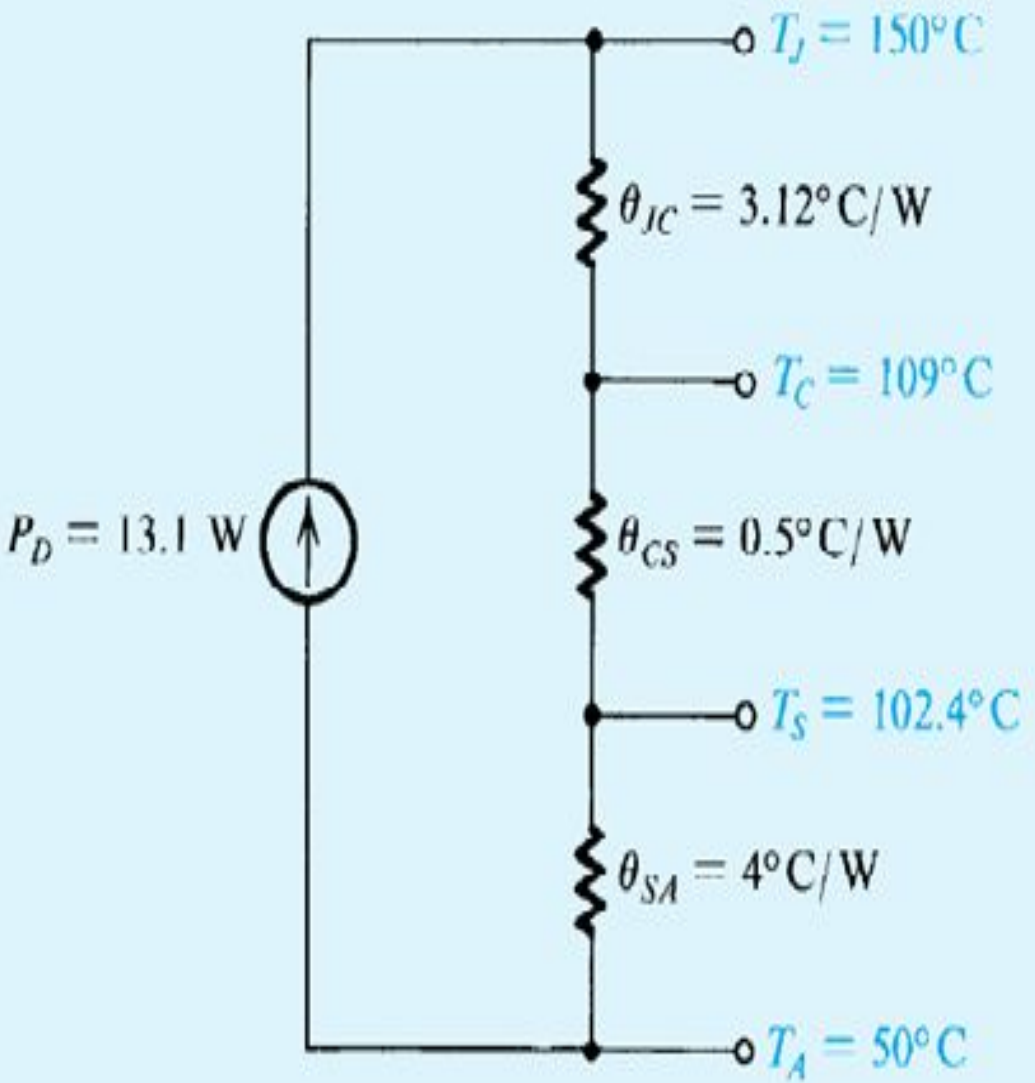
$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JA}} = \frac{150 - 50}{62.5} = 1.6 \text{ W}$$

(b) With a heat sink, $\theta_{JA}$ becomes

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$
$$= 3.12 + 0.5 + 4 = 7.62°\text{C/W}$$

Thus,

$$P_{D\max} = \frac{150 - 50}{7.62} = 13.1 \text{ W}$$



(c) An infinite heat sink, if it existed, would cause the case temperature $T_C$ to equal the ambient temperature $T_A$. The infinite heat sink has $\theta_{CA} = 0$. Obviously, one cannot buy an infinite heat sink; nevertheless, this terminology is used by some manufacturers to describe the power-derating curve of Fig. 11.27. The abscissa is then labeled $T_A$ and the curve is called "power dissipation versus ambient temperature with an infinite heat sink." For our example, with infinite heat sink,

$$P_{D\max} = \frac{T_{J\max} - T_A}{\theta_{JC}} = \frac{150 - 50}{3.12} = 32 \text{ W}$$

# Electronics and Comm. Department