
Q.1] For an NMOS differential pair with a common-mode voltage v_{CM} applied, as shown in Fig.1, let $V_{DD} = V_{ss}$ =2.5 V, k_n' W/L = 3 mA/V^2, V_{tn} = 0.7 V, I = 0.2 mA, and R_D =5kΩ.
(a) Find V_{OV} and V_{GS} for each transistor.
(b) For v_{CM} = 0, find v_S, i_{Dl}, i_{D2}, v_{Dl}, and v_{D2}.
(c) Repeat (b) for v_{CM} = +l V.
(d) Repeat (b)for v_{CM} = -l V.

$V_S = V_{CM} + V_{GS}$

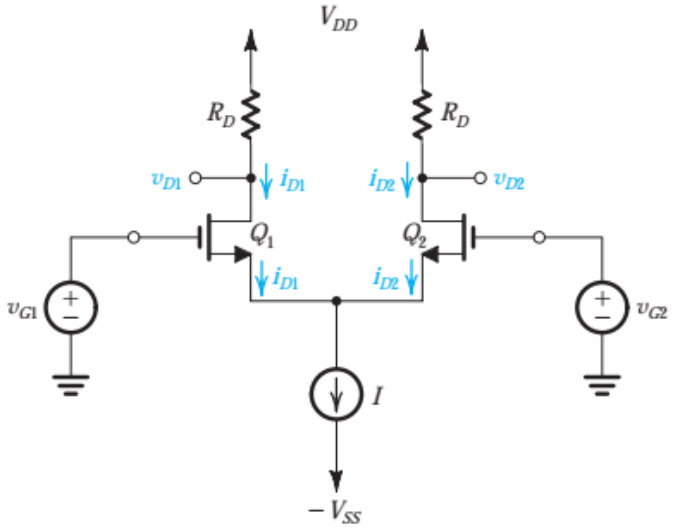

Fig. 1

Q.2] For the PMOS differential amplifier shown in Fig. 2 let V_{tp} = -0.8 V and k_p' W/L = 3.5 mA/V^2. For v_{G1} = v_{G2} = 0 V, find V_{OV} and V_{GS} for each of Q_1 and Q_2. Also find v_S, v_{D1}, and v_{D2}.

$V_{ov} = -\sqrt{\frac{2ID}{kp}}$ (change sign)

$V_{GS} = V_{ov} + V_{tp}$ (same sign)

$V_S = V_{CM} + |V_{GS}|$ (+ve)

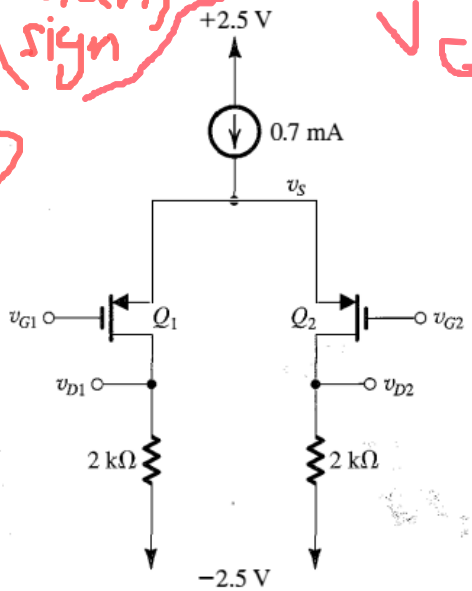

Fig.2

Q.3] An NMOS differential amplifier is operated at a bias current I of 0.5 mA and has a W/L ratio of 50, $\mu_n C_{ox}$= 250 μA/V2, V_A = 10 V, and R_D = 4 kΩ. Find V_{OV}, g_m, r_o, and A_d.

Q.4] An NMOS differential pair is biased by a current source I =0.2 mA having an output resistance R_{SS} = 100 kΩ. The amplifier has drain resistances R_D = 10 kΩ, using transistors with k_n' W/L = 3 mA/V^2, and r_o that is large. If the output is taken differentially and there is a 1% mismatch between the drain resistances, find $|A_d|$, $|A_{cm}|$, and CMRR.

Q.5] For the differential amplifier shown in Fig. 2, let Q_1 and Q_2 have k_p' (W/L) = 3.5 mA/V^2, and assume that the bias current source has an output resistance of 30 KΩ. Find V_{OV}, g_m, $|A_d|$, $|A_{cm}|$, and CMRR (in dB) obtained with the output taken differentially. The drain resistances are known to have a mismatch of 2%.

Q.6] The differential amplifier in Fig.3 utilizes a resistor R_{SS} to establish a l-mA dc bias current. Note that this amplifier uses a single 5-V supply and thus needs a dc common-mode voltage V_{CM}. Transistors Q_1 and Q_2 have $k_n' W/L$ = 2.5 mA/V^2, and V_t = 0.7 V.
(a) Find the required value of V_{CM}.
(b) Find the value of R_D that results in a differential gain A_d of 8 V/V.
(c) Determine the dc voltage at the drains.

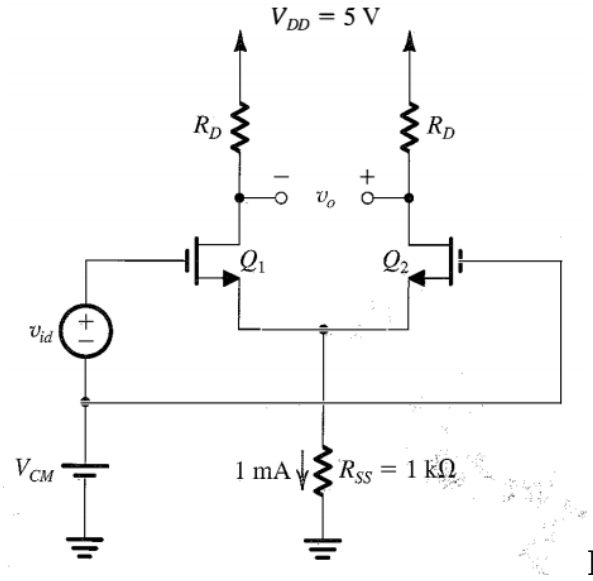

Fig. 3

Q.7] For the differential amplifier of Fig. 4 let I =1 mA, V_{CC} = 5 V, v_{CM} = -2 V, R_C = 3 kΩ, and β= 100. Assume that the BJTs have v_{BE} = 0.7 V at i_C = 1 mA. Find the voltage at the emitters and at the outputs.

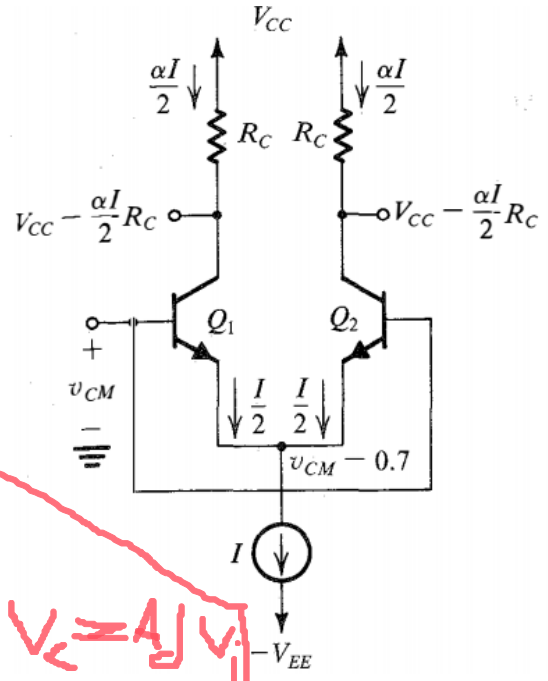

Fig. 4

Q.8] For a differential amplifier to which a total difference signal of 10 m V is applied, what is the equivalent signal to its corresponding CE half-circuit? If the emitter current source is 100 μA, what is r_e of the half-circuit? For a load resistance of 10 KΩ in each collector, what is the half-circuit gain? What magnitude of signal output voltage would you expect at each collector?

Q.9] Find the voltage gain and the input resistance of the amplifier shown in Fig. 5 assuming β = 100.

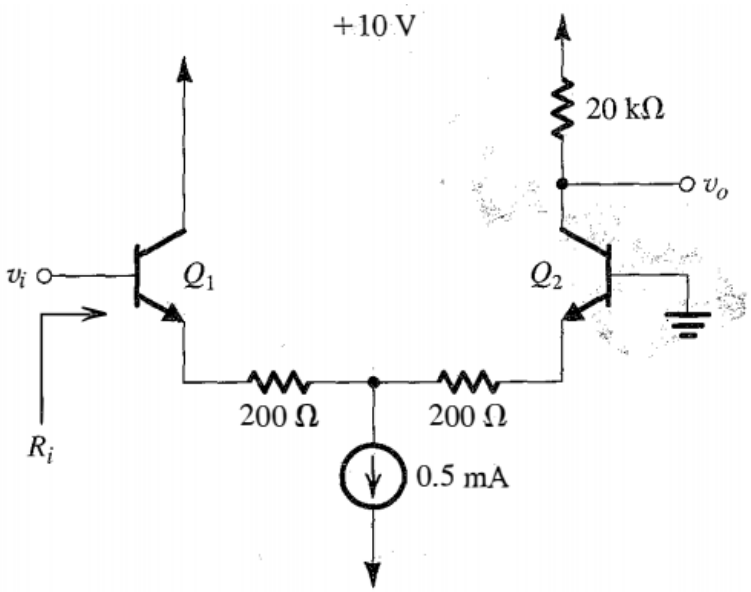

Fig. 5

Q.10] The differential amplifier circuit of Fig. 6 utilizes a resistor connected to the negative power supply to establish the bias current *I*.
(a) For $v_{Bl} = v_{id}/2$ and $v_{B2} = -v_{id}/2$, where *vid* is a small signal with zero average, find the magnitude of the differential gain, $|v_O/v_{id}|$.
(b) For $v_{Bl} = v_{Bl} = v_{icm}$, find the magnitude of the common-mode gain, $|v_O/v_{icm}|$.
(c) Calculate the CMRR.

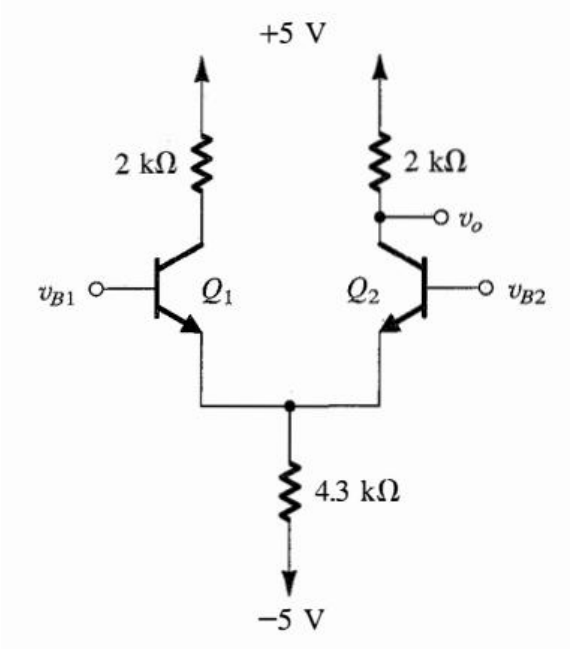

Fig. 6

Best wishes