Electronic Devices

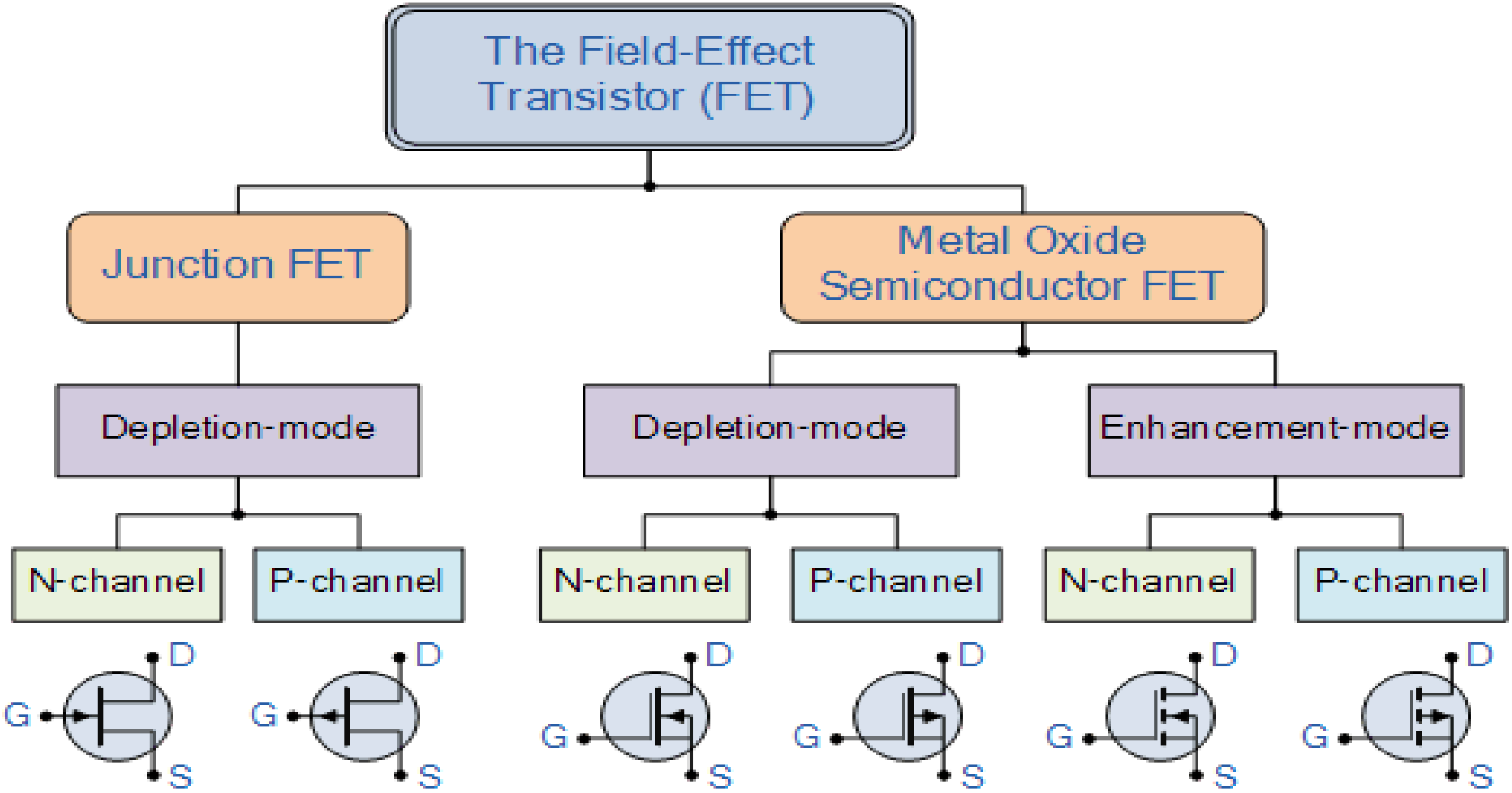
Lecture 18

Field Effect Transistor

“MOSFFT”

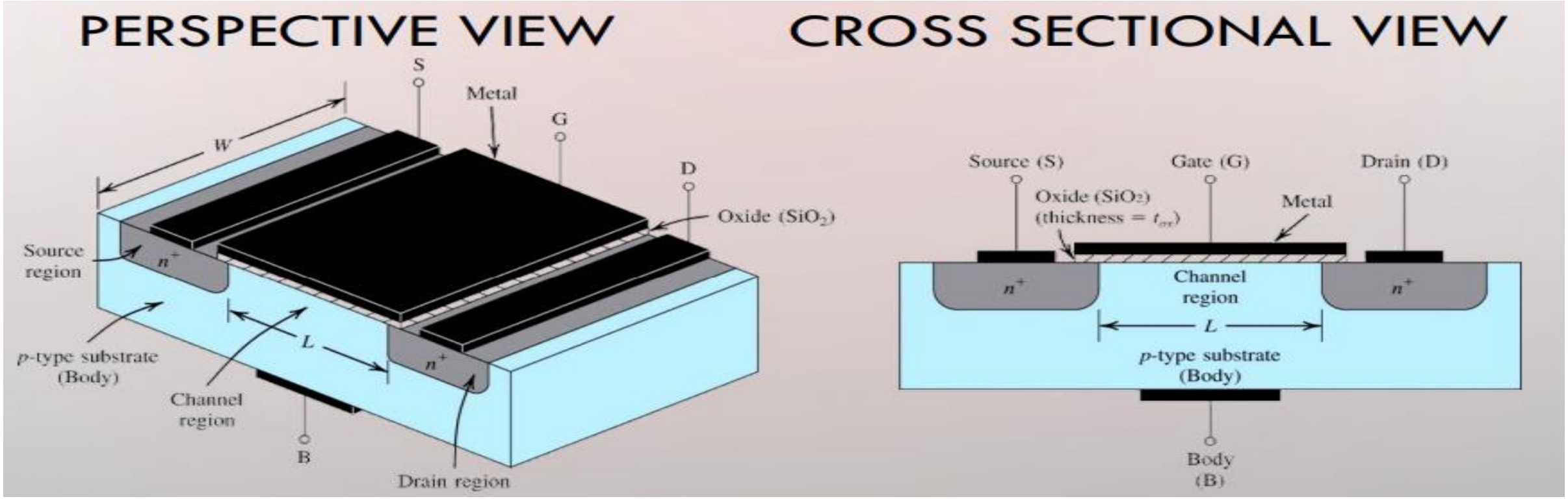
Dr. Roaa Mubarak

Field Effect Transistor



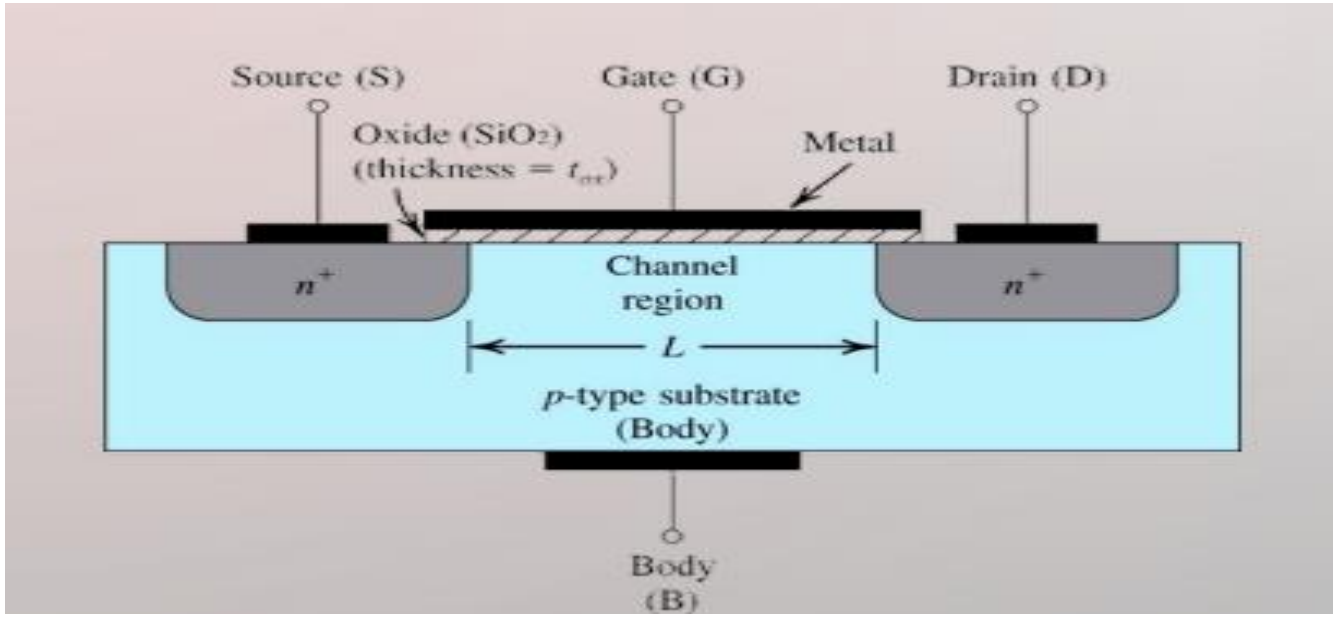
Metal Oxide Semiconductors Field Effect Transistor

- The MOSFET transistor is a semiconductor device that is widely used for switching purposes and for the amplification of electronic signals in electronic devices.
- A MOSFET is either a core or integrated circuit where it is designed and fabricated in a single chip because the device is available in very small sizes. The introduction of the MOSFET device has brought a change in the domain of **switching in electronics**.



Metal Oxide Semiconductors Field Effect Transistor

- A MOSFET is a four-terminal device having source(S), gate (G), drain (D) and body (B) or substrate terminals. In general, The body of the MOSFET is in connection with the source terminal thus forming a three-terminal device such as a field-effect transistor.
- MOSFET is a FET is made by growing a very thin layer of Sio_2 (0.1μm) over a semiconductor material. Metal such as aluminum is deposited over dielectric layer of Sio_2 is known as MOSFET.

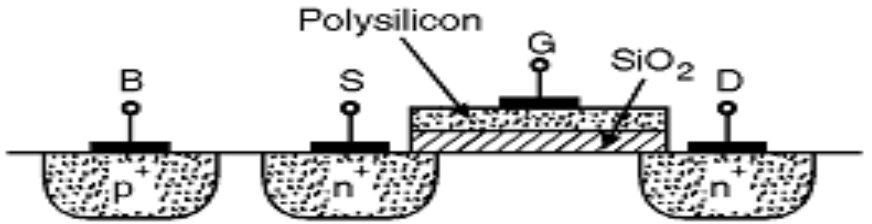


- There are two types of MOSFET:
- Enhancement MOSFET
- Depletion MOSFET

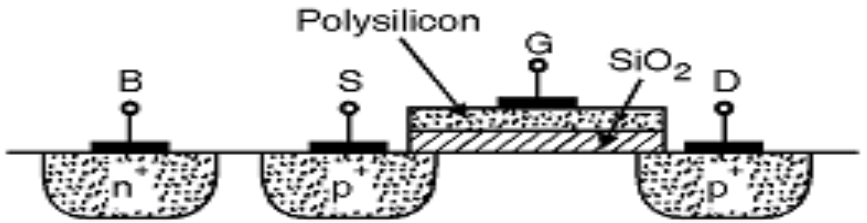
Metal Oxide Semiconductors Field Effect Transistor

- Similar to JFET , It has n-channel as well as p-channel. Construction wise we can categorize the device into four types:

- P-channel Enhancement MOSFET
- n-channel Enhancement MOSFET
- n-channel Depletion MOSFET
- p-channel Depletion MOSFET



NMOS structure



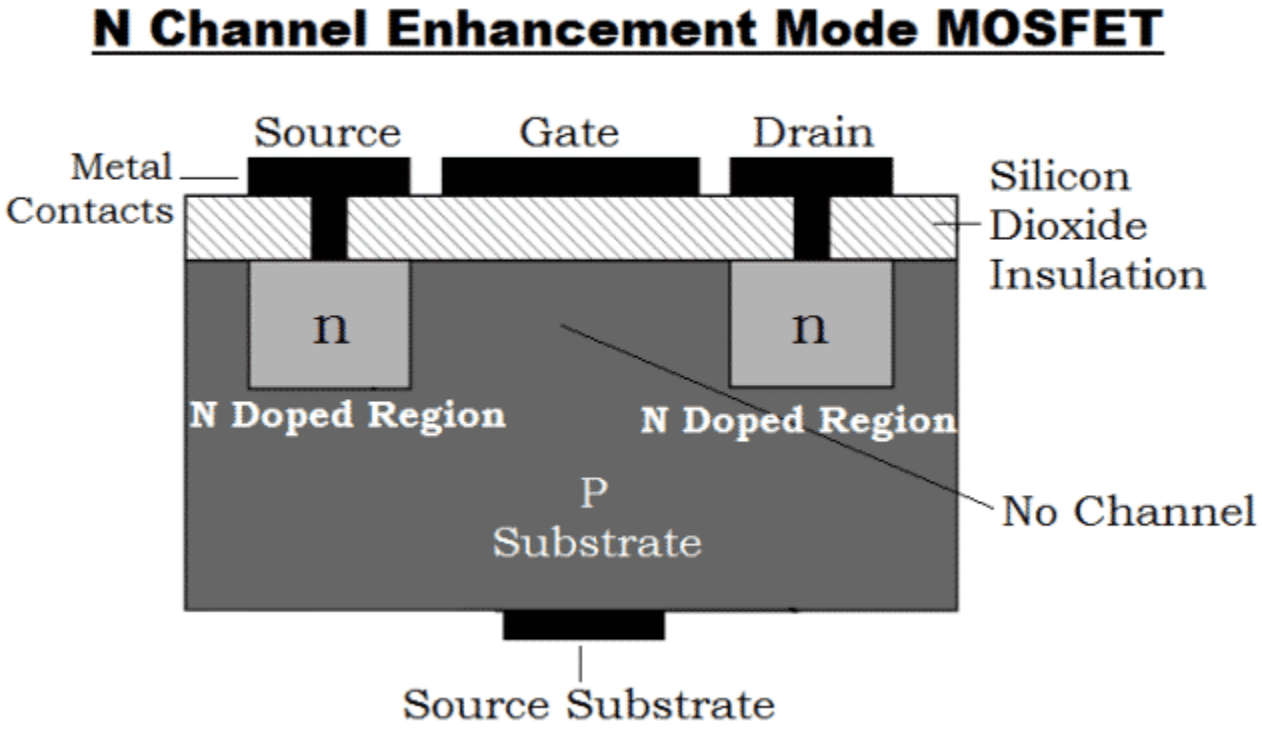
PMOS structure

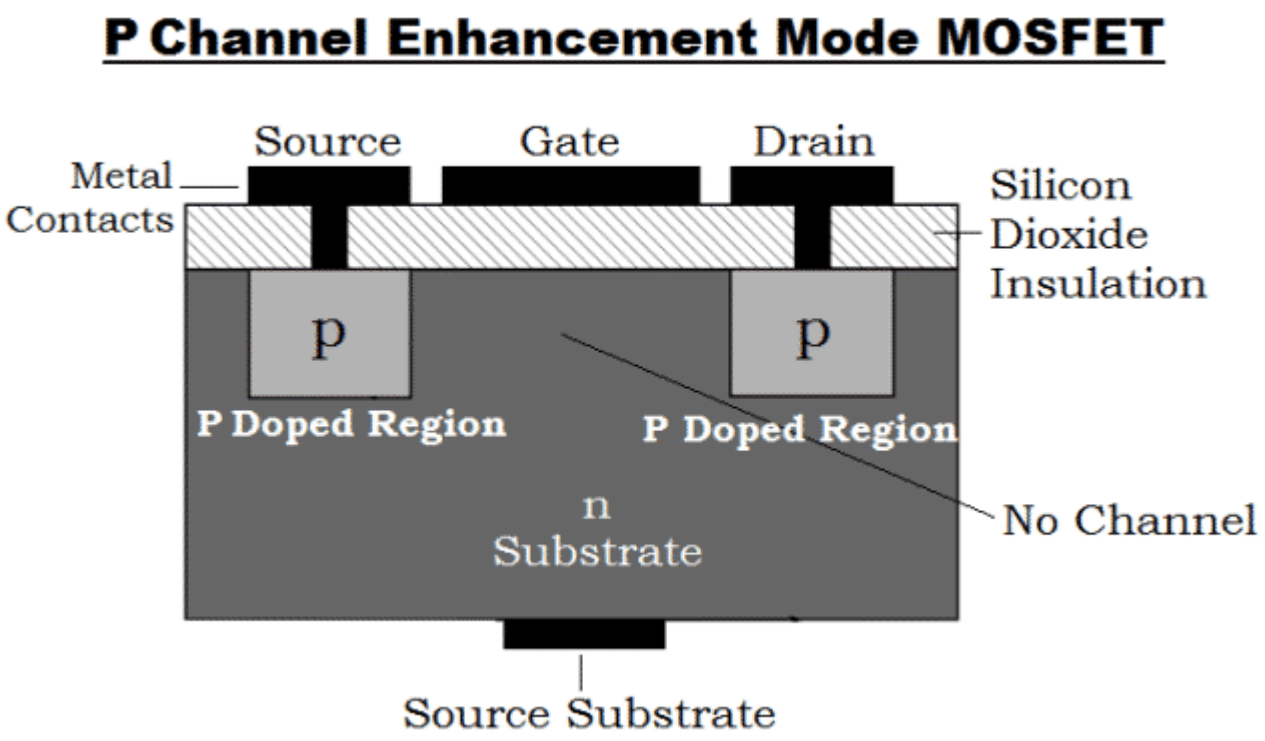
The Ideal MOS Structure

- The metallic gate is sufficiently thick so that it can be considered to be an equipotential region under both AC and DC biasing.
- The oxide is perfect insulator with zero current flowing through the oxide layer under all static biasing condition.
- There are no charge centers located in the oxide or in oxide semiconductor interface .
- The semiconductor is sufficiently thick to ensure that regardless of the applied gate potential, a field-free region is encountered before reaching the black contact.
- The semiconductor is uniformly doped.
- An ohmic contact has been established between the semiconductor and the metal on the black side of the device.

Enhancement MOSFET

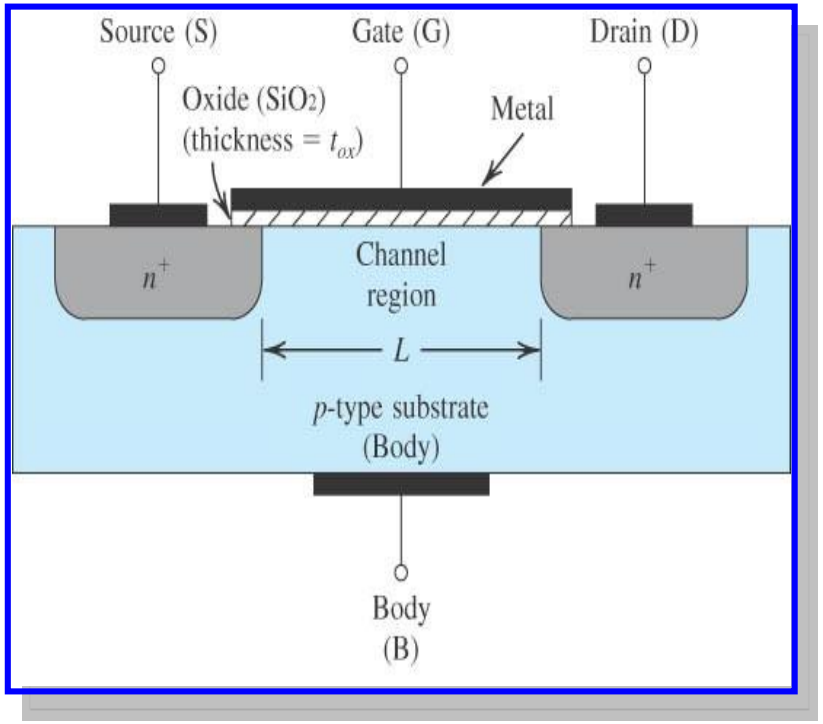
- The structure of Enhancement MOSFET has no built-in channel between drain and source.





Enhancement NMOS

- Moreover, each terminal has a specific **name**:
  - Source (**S**), Drain (**D**), Gate (**G**), Body (**B**)
- Each terminal is associated with a **metal electrode** that is attached to the semiconductor device.
- The **Body (Substrate)** electrode is connected directly to the *p*-type substrate.
- Two **heavily** doped *n*-type "wells" are implanted into the *p*- type substrate. The **Source** and **Drain** electrodes are each connected to one of these n^+ wells.
- The region between these n^+ wells is called the channel. The channel has two important geometries—channel width W, and channel length L.
- Typical values for channel length L are 0.1 to 3 mm, while channel width W is typically 0.2 to 100 mm.

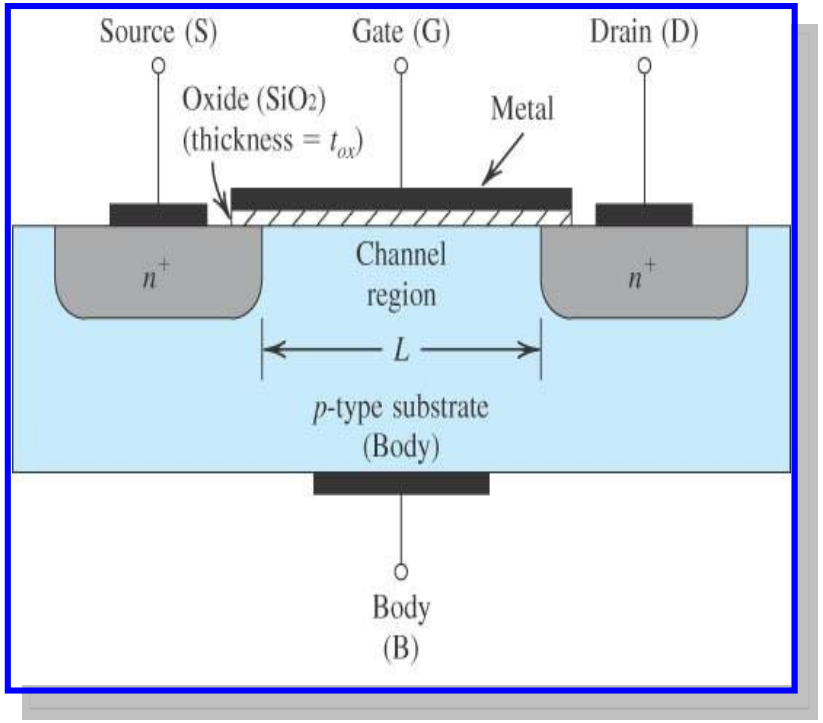


Enhancement NMOS

- The Gate electrode rests on top of the channel, but is not connected directly to it. Instead, the channel and gate electrode are separated by a thin (e.g., 2-5 nm) layer of Silicon Dioxide (SiO_2).

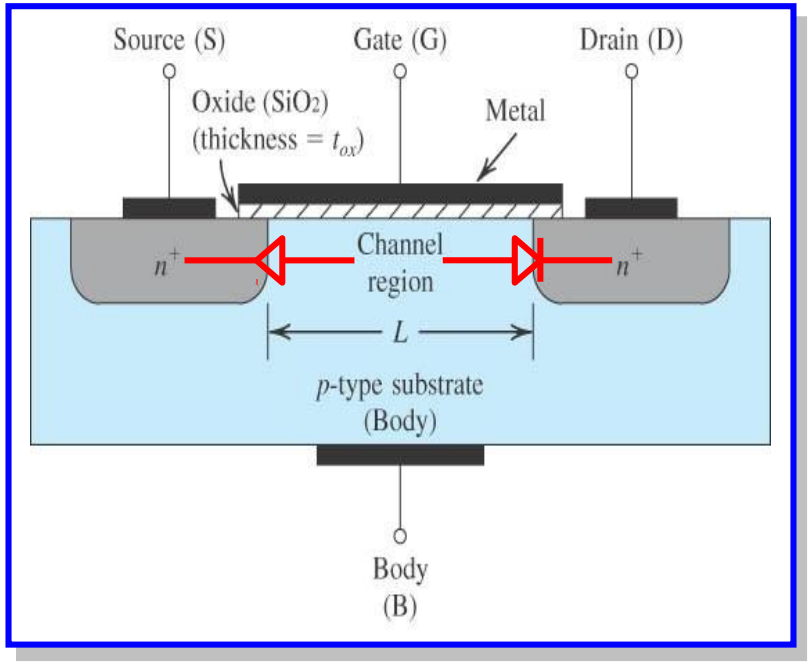
- Silicon Dioxide is essentially glass! Glass is a very good insulator—thus, no current can flow from the gate into the MOSFET device!

- Thus, the Silicon Dioxide layer is **sandwiched** between the metal Gate electrode and the channel. It is these **three** materials that give the **MOS**FET its name—**M**etal (Gate electrode) **O**xide (SiO_2) **S**emiconductor (channel) FET.



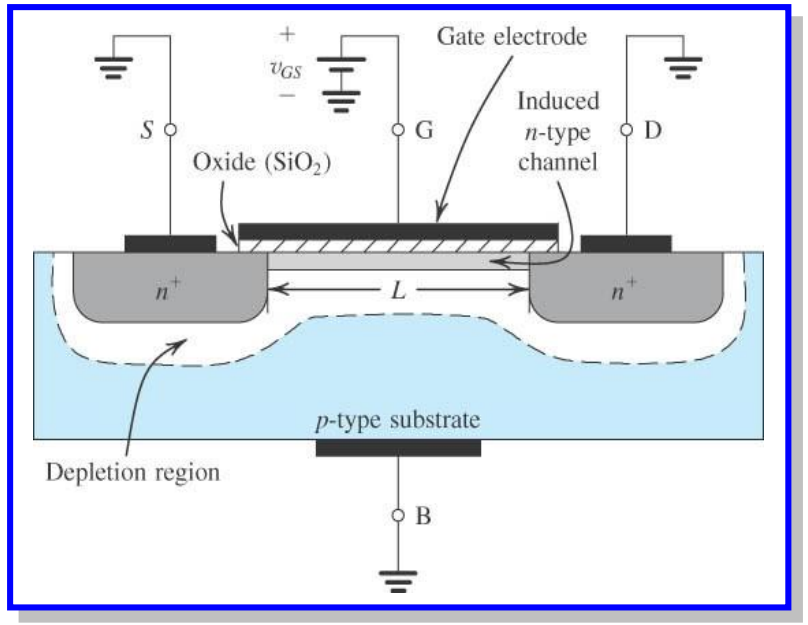
Enhancement NMOS

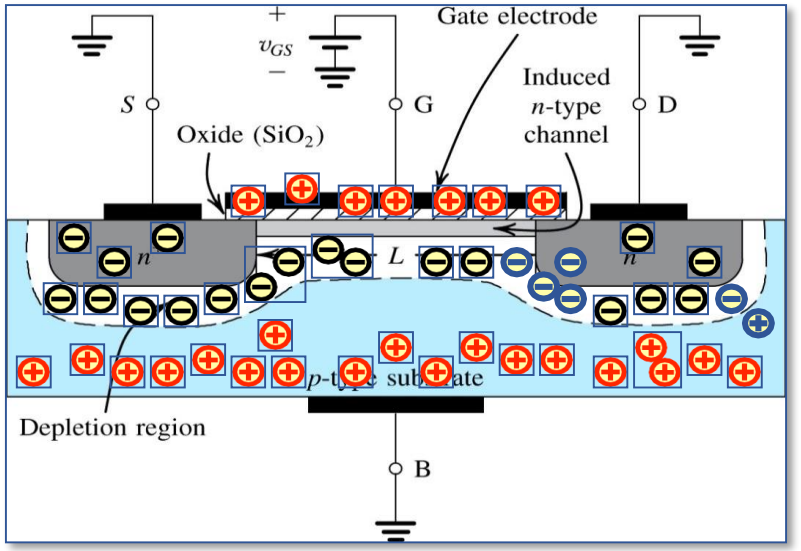
- When we first look at an NMOS device, it appears that no current can flow from the Drain electrode to the Source electrode (or vice versa) as we must contend with two *p*-*n* junctions.
- Current seemingly cannot flow **into** channel from the Drain, as this would require current flowing from an *n*-type (cathode) region into a *p*-type (anode) region.
- Likewise, current cannot flow **into** channel from the Source, as this would require current flowing from an *n*-type (cathode) region into a *p*-type (anode) region.
- Recall that we have previously determined that current **cannot** flow into (or out of) the channel from (into) the **gate**, as the SiO2 layer is a very good **insulator**!



Enhancement NMOS

- We must induce a channel—that is, create a thin layer of *n*- type Si connecting the source and drain!
- To do this, we place a positive voltage at the gate electrode. This creates an electric field within the *p*-type substrate, which pushes the positively charged holes in the *p*-type substrate away from the gate electrode.
- The electric field under the gate electrode will repel positively charged holes, but will attract negatively charged free electrons!
- So, By applying a positive voltage to the gate, we have induced a conducting channel, In other words, current flowing from drain to source no longer encounters any *p*-*n* junctions!





Enhancement NMOS

- The gate voltage must be sufficiently large to **induce** a conducting channel, the voltage value must exceed some **threshold.**

$$V_{GS} > V_{th}$$

to induce NMOS channel;

$$V_{GS} - V_{th} > 0$$

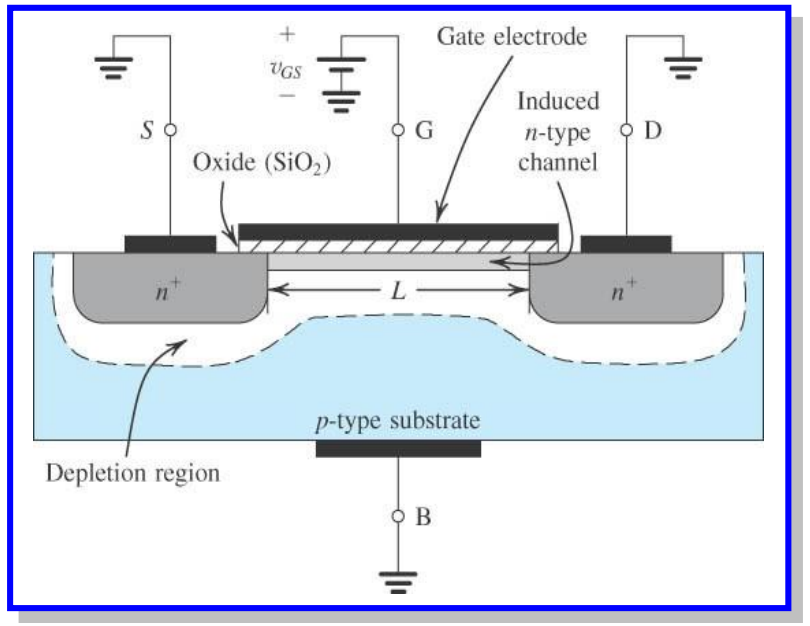
- Now, say that we additionally place a voltage at the NMOS **drain** electrode, such that:

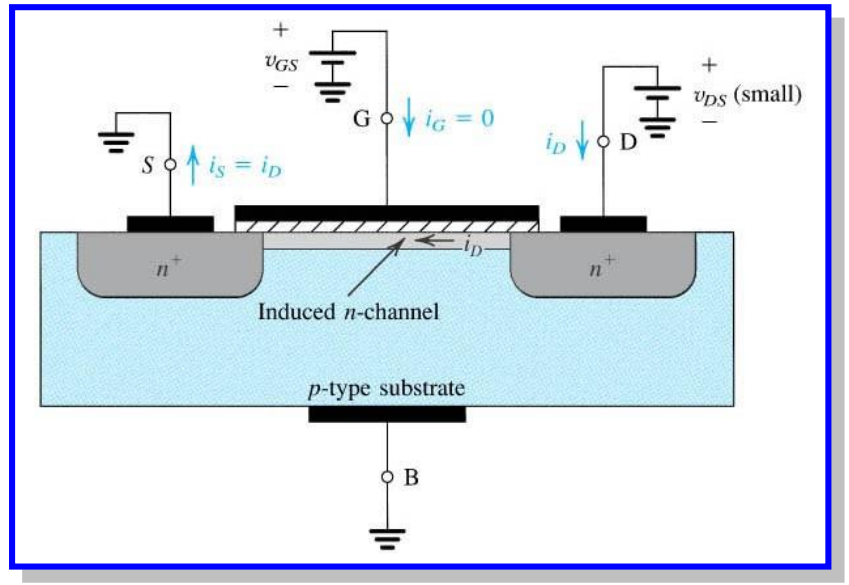
$$V_{DS} > 0, \quad V_{DS} < V_{GS} - V_{th}$$

- So, the current begins to flow through the channel, all current **entering the drain** will **exit the source**. We therefore conclude that:

$$I_S = I_D$$

- As a result, we refer to the channel current for NMOS devices as simply the **drain current I_D.**



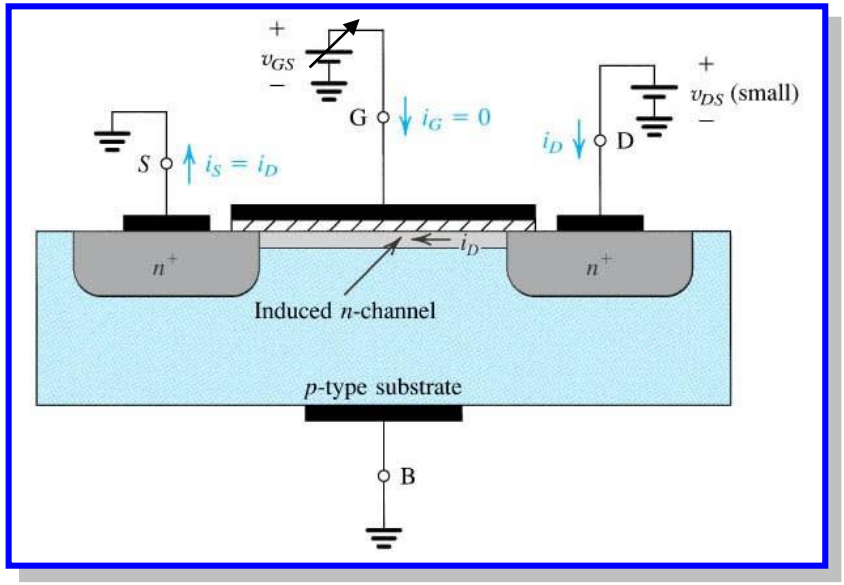


Enhancement NMOS

- We find that an increasing V_{GS} or, more specifically, an increasing excess gate voltage V_{GS}-V_{th} will result in a higher channel conductivity (in other words, a lower channel resistivity).

- Thus, we find that the drain current I_D will increase as a positive excess gate voltage V_{GS}-V_{th} increases (assuming that V_{DS} >0).

- This process, of increasing the induced channel conductivity by increasing the excess gate voltage, is otherwise known as channel enhancement. This is where the enhancement MOSFET gets its name!



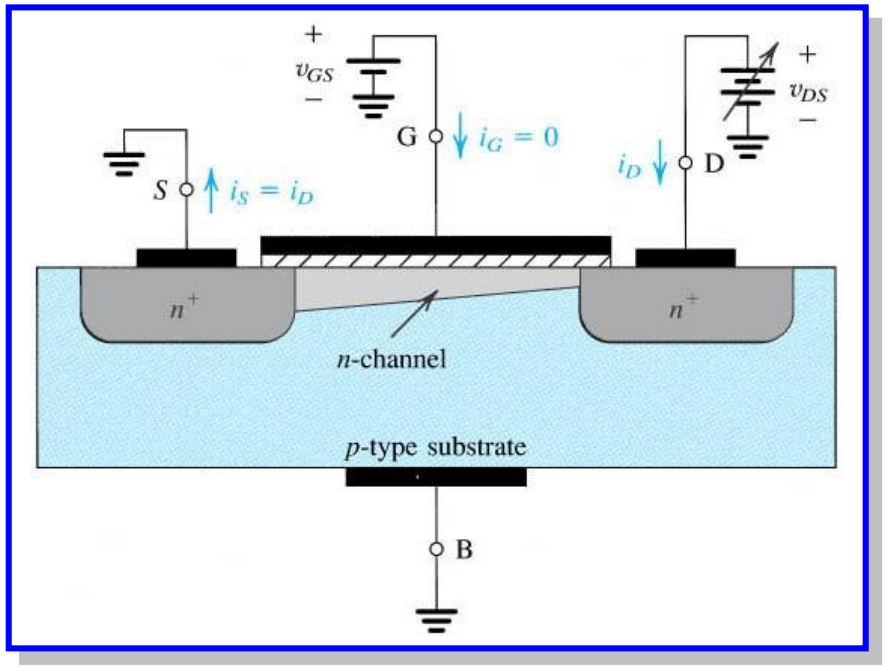
$$V_{DS} < V_{GS} - V_{th}$$

Enhancement NMOS

- In other words, if V_{DS} is zero, the drain current I_D is zero. Or, if the voltage V_{DS} increases by 10%, the drain current will likewise increase by 10%. Note this is just like a resistor!

$$I_D \boldsymbol{\alpha} V_{DS} \quad \text{if } V_{Ds} \text{ small}$$

- As V_{DS} increases much more, the free-electrons in the induced channel were attracted to the gate from the heavily doped n+ Silicon regions under the drain and source.
- The gate has competition in attracting these free electrons, But as the drain voltage increases, it begins to attract free electrons of its own!

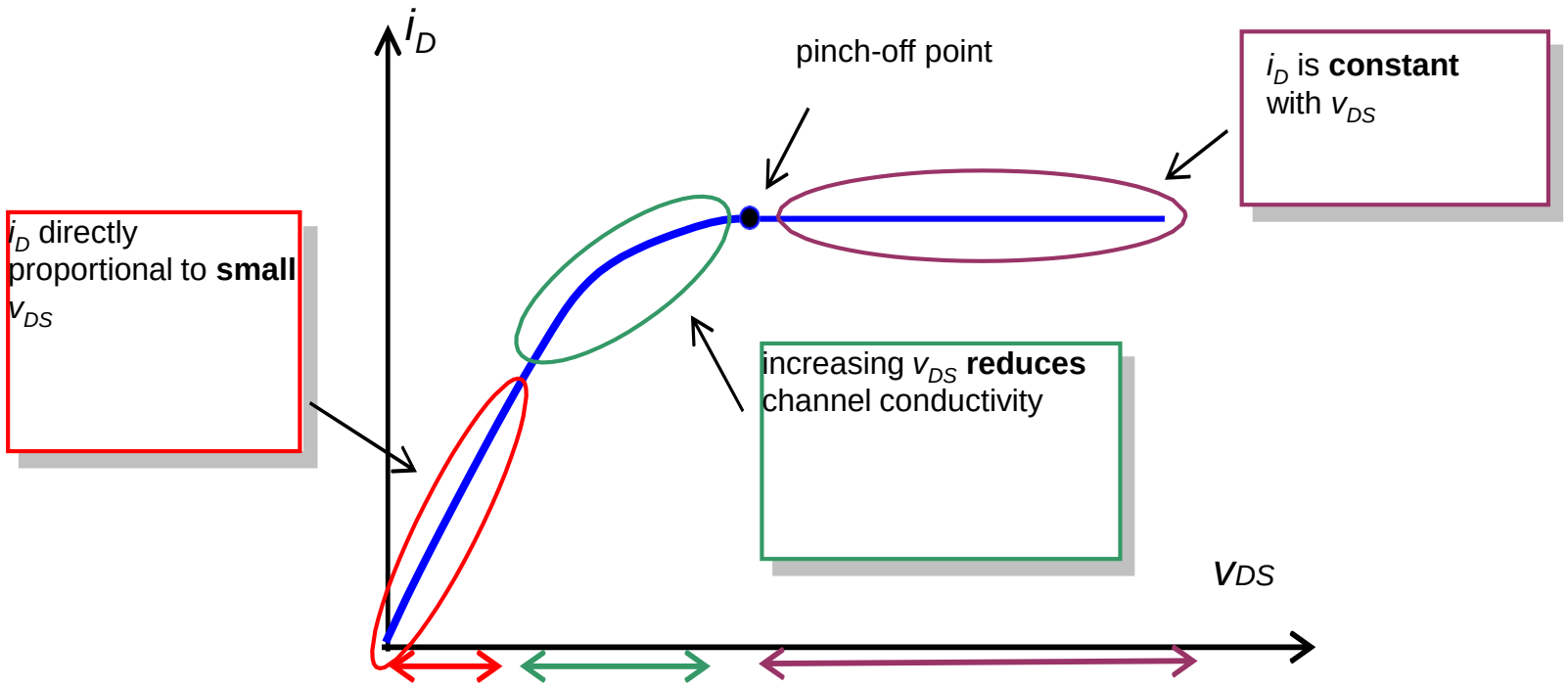


$$V_{DS} > V_{GS} - V_{th}$$

- Recall that positive current entering the drain will actually consist mainly of free electrons exiting the drain! As a result, the concentration of free-electrons in our inversion layer will begin to decrease in the vicinity of the drain, In other words, increasing v_{DS} will result in decreasing channel conductivity and makes channel pinched-off.

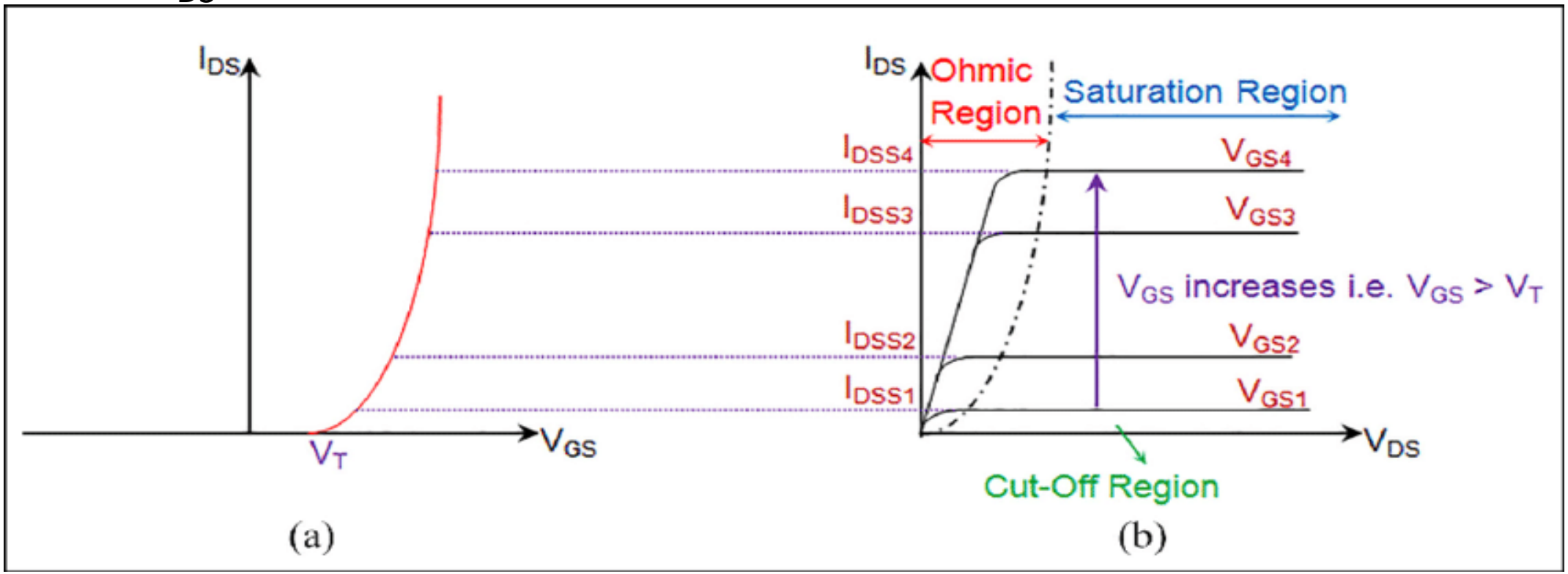
Enhancement NMOS

- When the channel is in pinch off, As we further increase V_{DS}, the drain current I_D will remain **unchanged** (approximately)! That is, the drain current will be a **constant** (saturated) with respect to V_{DS}.



Enhancement NMOS

- **Cutoff Region**- When V_{GS}-V_{th}< 0 , **no** channel is induced, and so I_D=0.
- **Ohmic Region -**When an induced channel **is** present (V_{GS}-V_{th}> 0), but the value of V_{DS} is **not** large enough to pinch-off this channel.
- **Saturation Region** - When an induced channel **is** present (V_{GS}-V_{th}> 0), and the value of V_{DS} **is** large enough to pinch-off this channel.



Transfer Characteristics

Drain Characteristics

Enhancement NMOS

- **Cutoff Region**:

  $V_{GS} < V_{th}$

  $I_D = 0$

- **Ohmic Region**

$V_{GS} > V_{th}$

$V_{DS} < V_{GS} - V_{th}$

$$I_D = K_n \left[(V_{GS} - V_{th}) V_{DS} - \frac{{V_{DS}}^2}{2} \right], R_{DS} = \frac{\triangle V_{DS}}{\triangle I_D}$$

K_n: transconductance of MOSFET

- **Saturation Region**

$V_{GS} > V_{th}$

$V_{DS} > V_{GS} - V_{th}$

$$I_D = \frac{1}{2} K_n (V_{GS} - V_{th})^2 \qquad K = \frac{1}{2} K_n$$

Enhancement NMOS

$$K_n = K_n' \left(\frac{W}{L}\right)$$

K_n: Transconductance Parameter of MOSFET

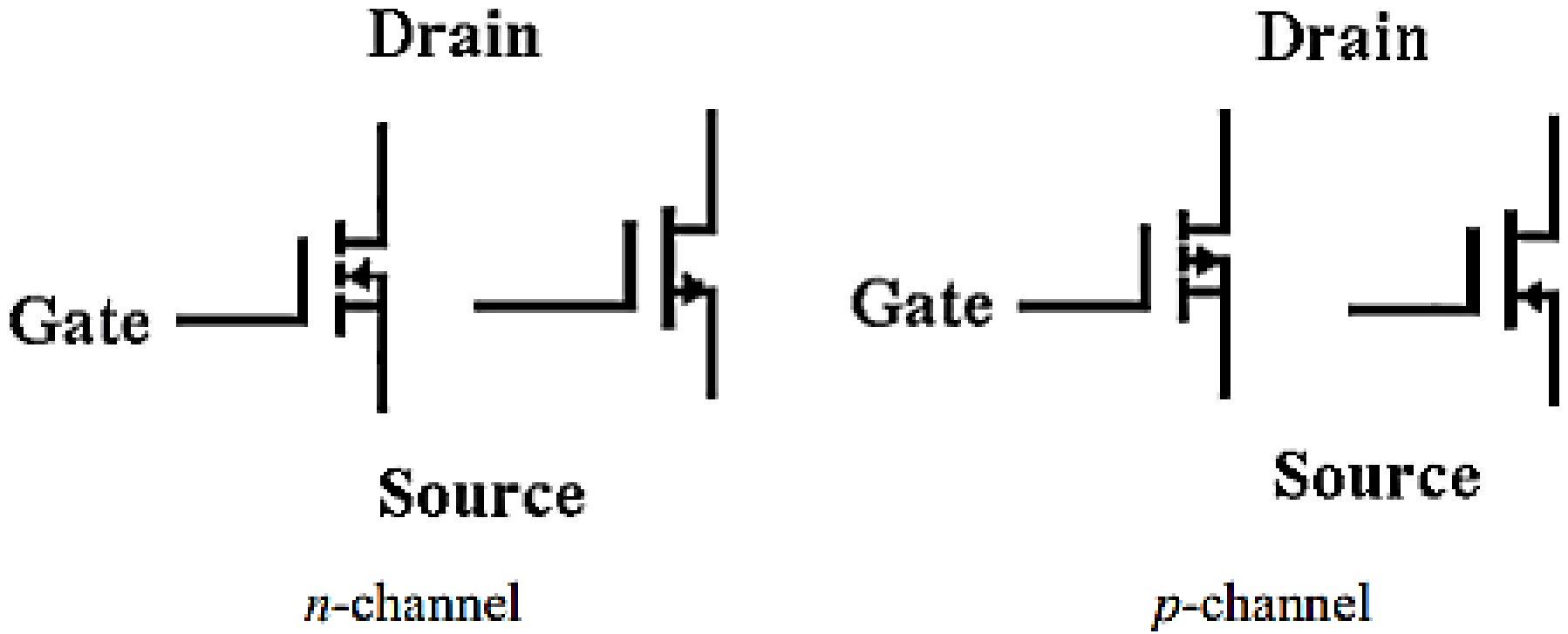
$K_n' = \mu_n C_{ox}$

μ_n: Electron mobility

C_{ox}: capacitance of gate per unit area.

W & L : the width and Length of channel

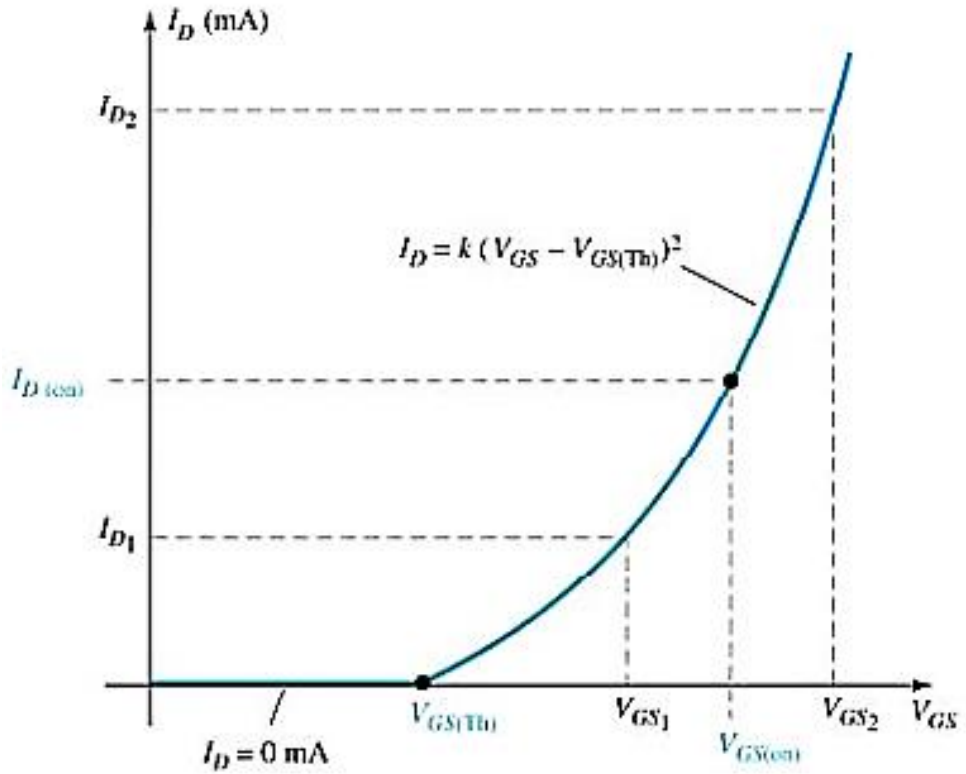
Enhancement MOSFET



EMOSFET Biasing

E-Type MOSFET Biasing Circuits

- Feedback Configuration
- Voltage-Divider Bias



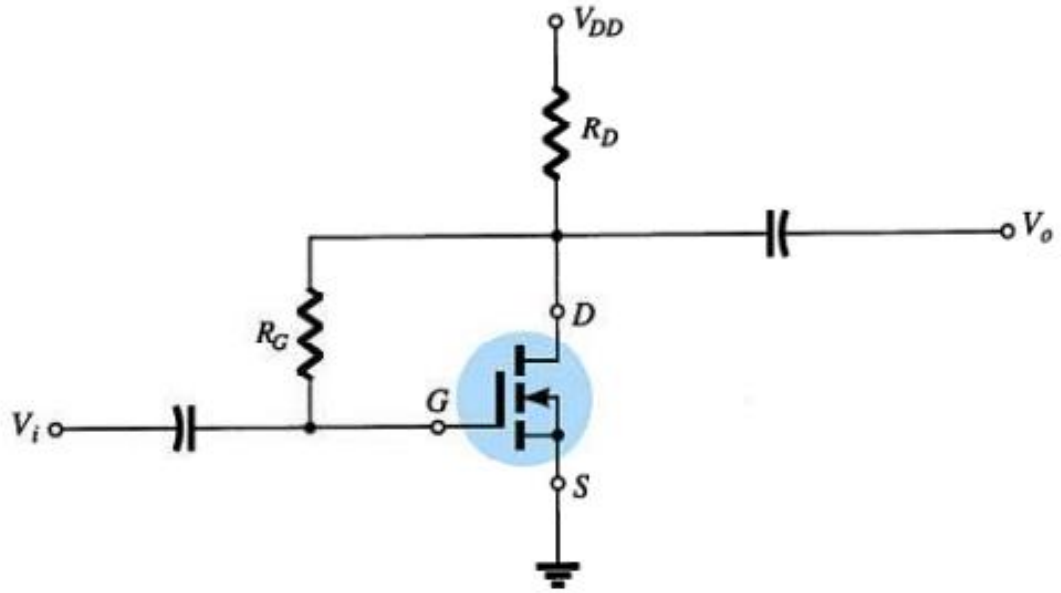
EMOSFET Feedback Bias

$I_G = 0\ A$

$V_{RG} = 0\ V$

$V_{DS} = V_{GS}$

$V_{GS} = V_{DD} - I_D R_D$



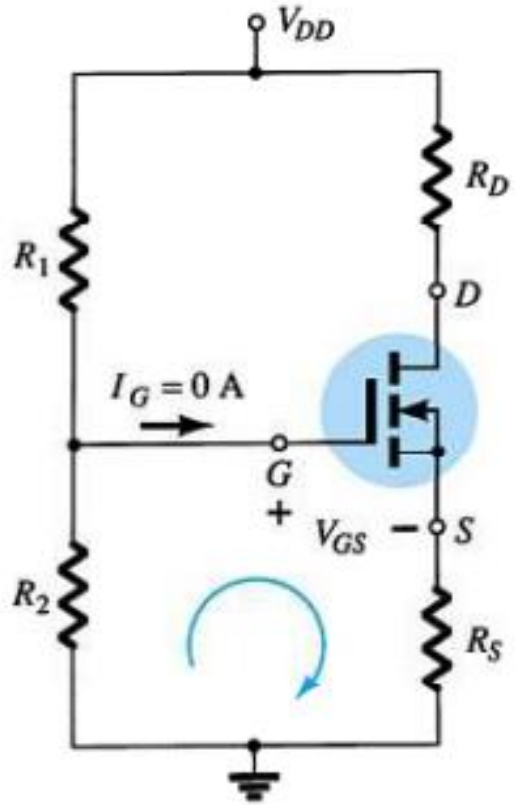
EMOSFET Voltage divider Bias

Plot the line and the transfer curve to find the Q-point. Use these equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

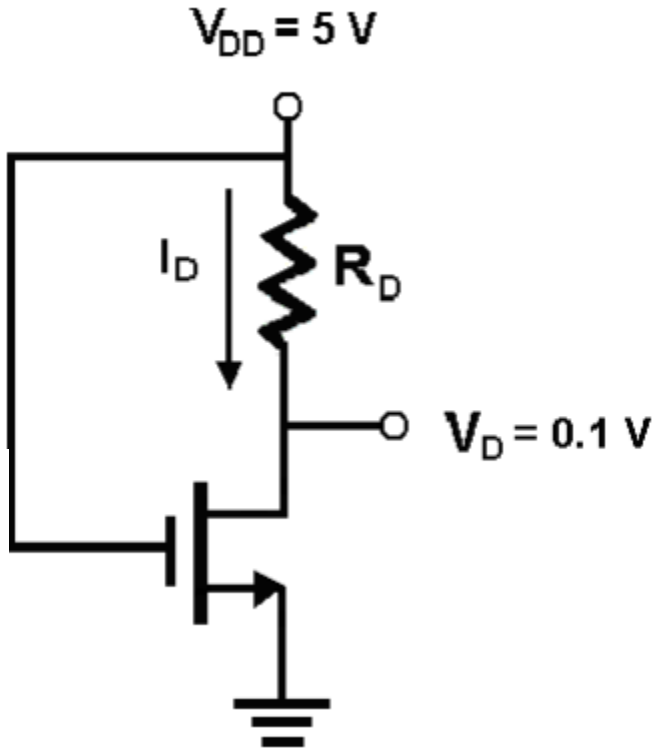
$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$



Example

If a V_D voltage of 0.1V needs to be established for the design, what will be the value of R_D and effective resistance r_{DS} between drain and source of this NMOS? Given that $V_{GS(th)} = 1V$ and $K = 1.0mA/V^2$.



- ***Solution***
- Since $V_D = 0.1V$, this shall mean that $V_{DS} = 0.1V$. This is also mean that the NMOS is operating at linear region because $V_{DS} \leqslant (V_{GS} - V_{GS(th)})$

$$I_D = 2K\left[(V_{GS} - V_{GS(th)})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

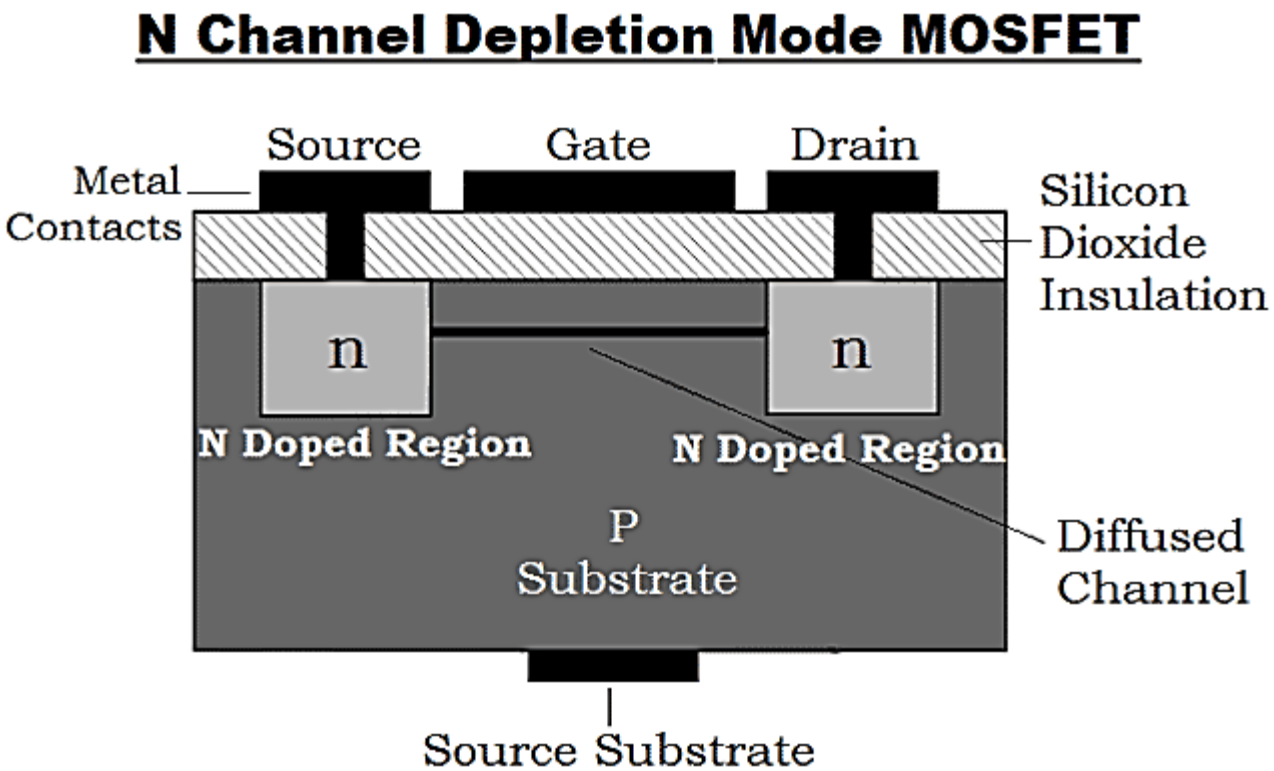
$$= 2\times 1x10^{-3} A/V^2\left[(5-1)\cdot 0.1 - \frac{1}{2}x0.01\right] = 0.79mA$$

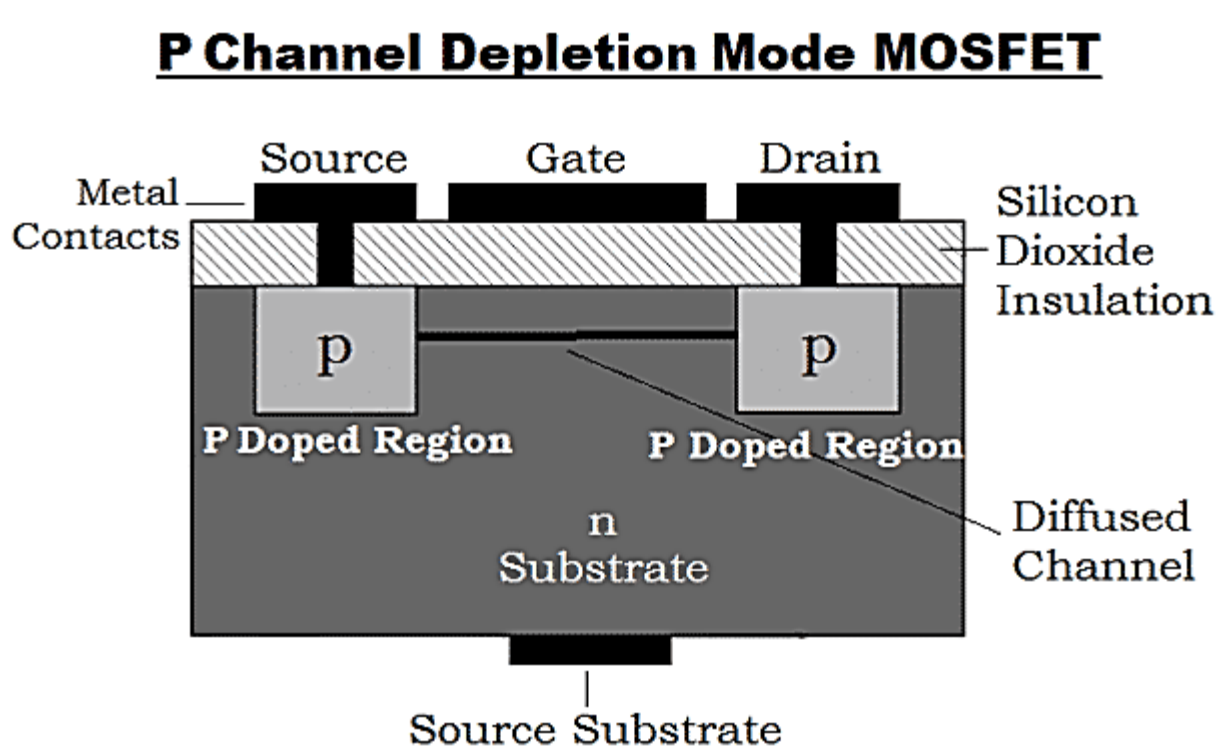
The required drain resistance R_D value is $R_D = \frac{V_{DD} - V_{DS}}{I_D} = \frac{5V - 0.1V}{0.79mA} = 6.2k\Omega$

The effective resistance across the drain and source r_{DS} is

$$r_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1V}{0.79mA} = 174.5\Omega$$

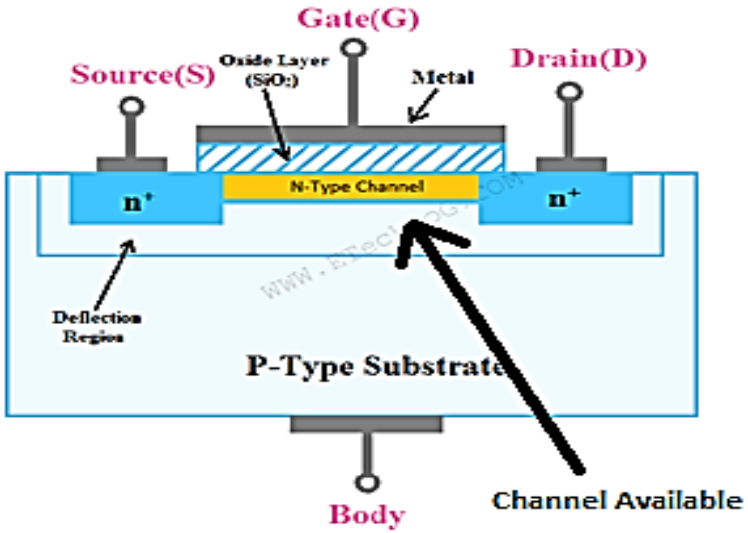
Depletion MOSFET



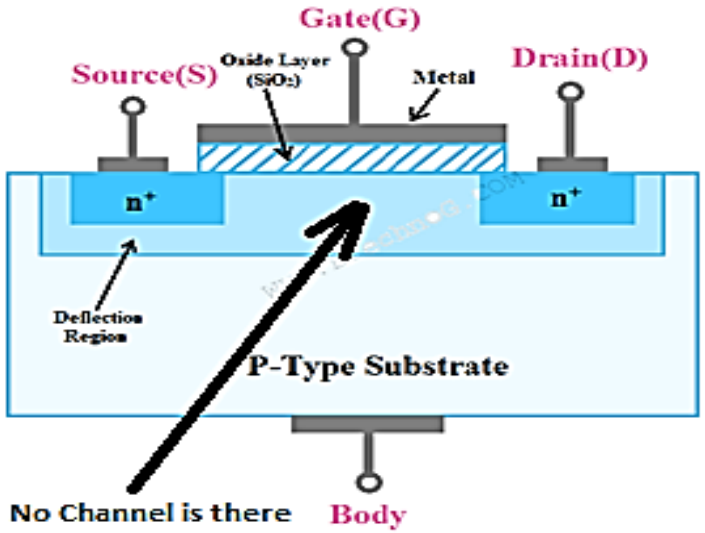


Depletion NMOS

- In this device a thin layer of N type silicon is deposited just below the gate–insulating layer, and forms a conducting channel between source and drain.
- Therefore when the gate source voltage V_{GS} is zero, current (in the form of free electrons) can flow between source and drain. Note that the gate is totally insulated from the channel by the layer of silicon dioxide. Now that a conducting channel is present the gate does not need to cover the full width between source and drain.



Depletion Type MOSFET



Enhancement Type MOSFET

Depletion NMOS

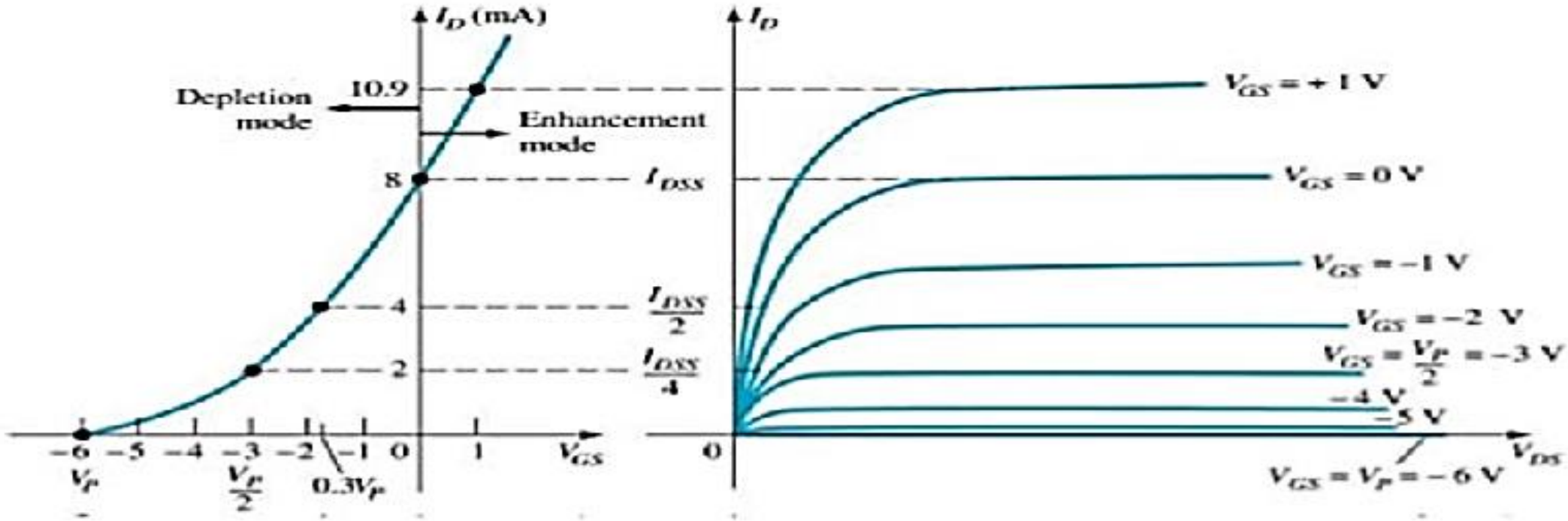
- The channel conductivity and depth can be controlled by voltage on gate VGS. By applying a positive voltage on gate enhance the channel by attracting more electrons into it.

- When we apply negative voltage on gate VGS causes electrons to repelled from the channel, and thus the channel becomes shallower and its conductivity decreases.

- The negative voltage on gate VGS is said to deplete the channel of its charge carrier, and this mode of operation is called depletion mode. As the voltage of the gate VGS increasing negatively, the channel is completely depleted of charge carriers and ID is reduced to zero even with VDS is applied.

Depletion NMOS

D-MOSFET Depletion Mode Operation



The transfer characteristics are similar to the JFET

In Depletion Mode operation:

When $V_{GS} = 0V$, $I_D = I_{DSS}$

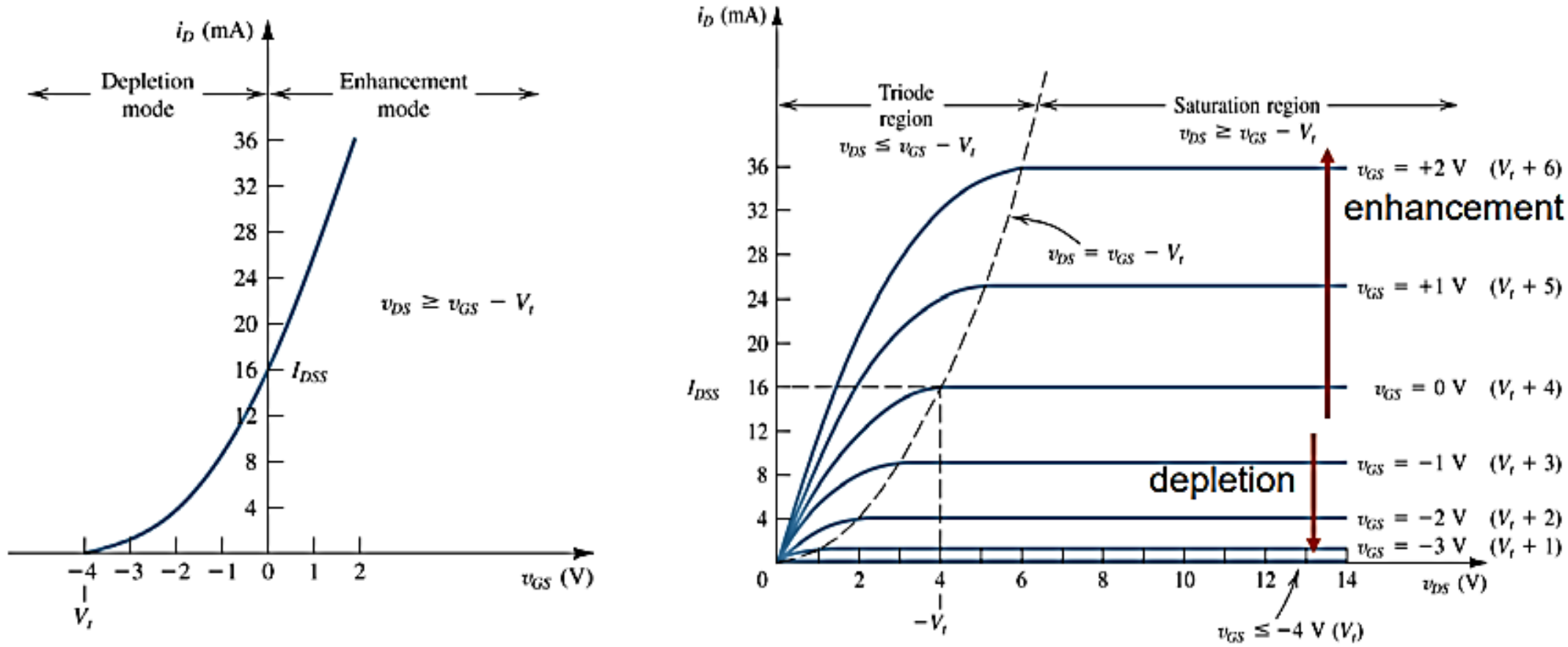
When $V_{GS} < 0V$, $I_D < I_{DSS}$

When $V_{GS} > 0V$, $I_D > I_{DSS}$

The formula used to plot the Transfer Curve, is:

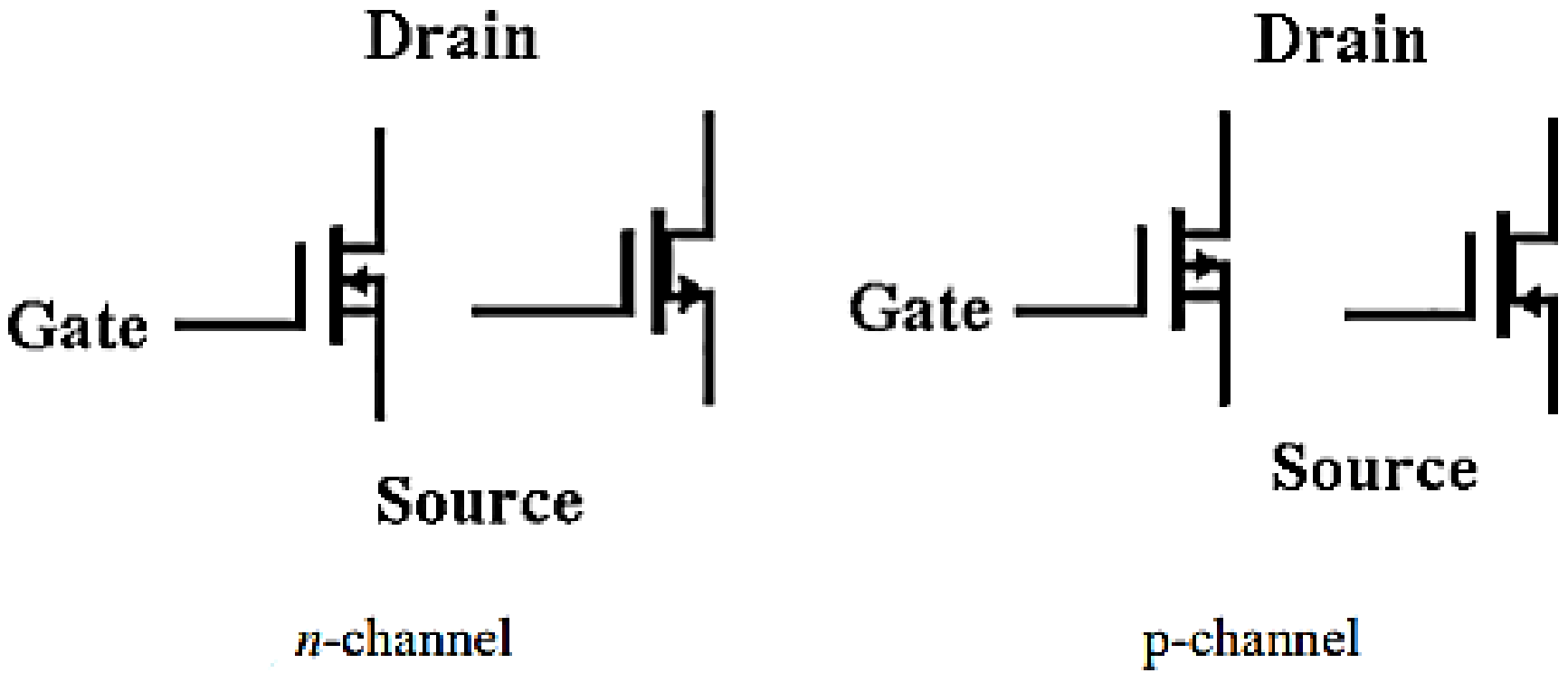
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Depletion-Enhancement MOSFET



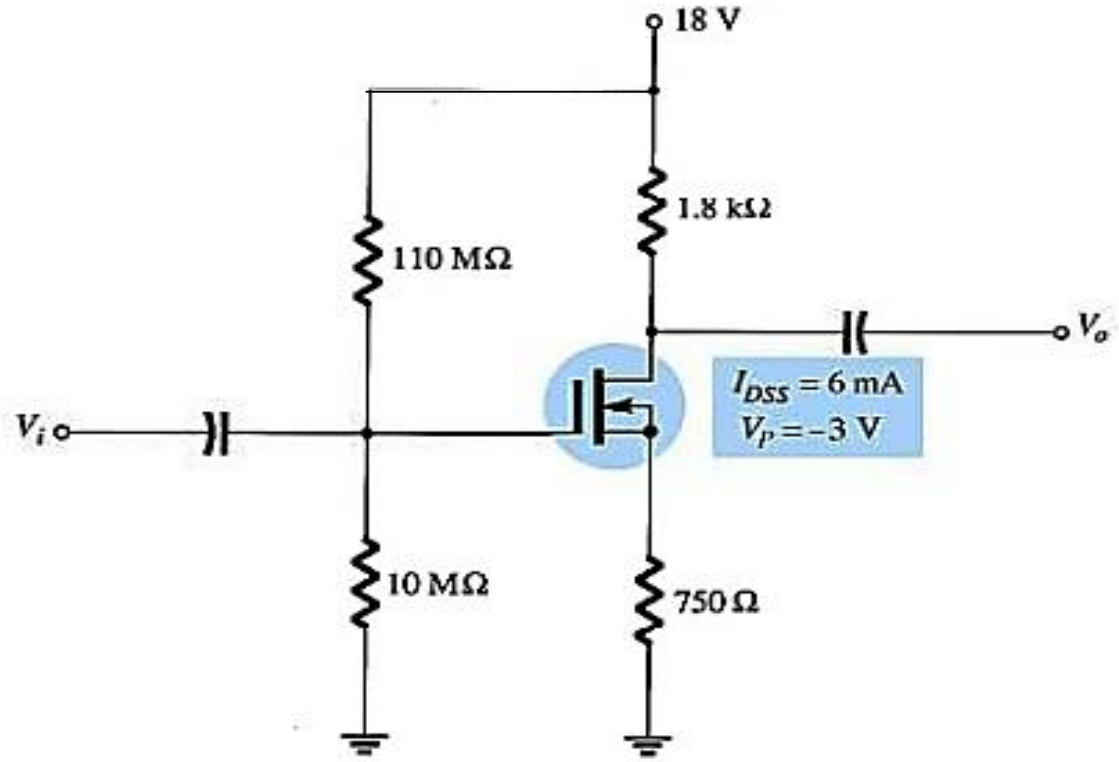
- DE-MOSFET can be operated with either a positive or a negative gate. When gate is positive with respect to the source it operates in the enhancement—or E-mode and when the gate is negative with respect to the source, it operates in depletion-mode.

DE MOSFET



DE-MOSFET Biasing

- **Self Bias**
- **Voltage Divider Bias**



Depletion-type MOSFET bias circuits are similar to those used to bias JFETs. The only difference is that depletion-type MOSFETs can operate with positive values of V_{GS} and with I_D values that exceed I_{DSS}.

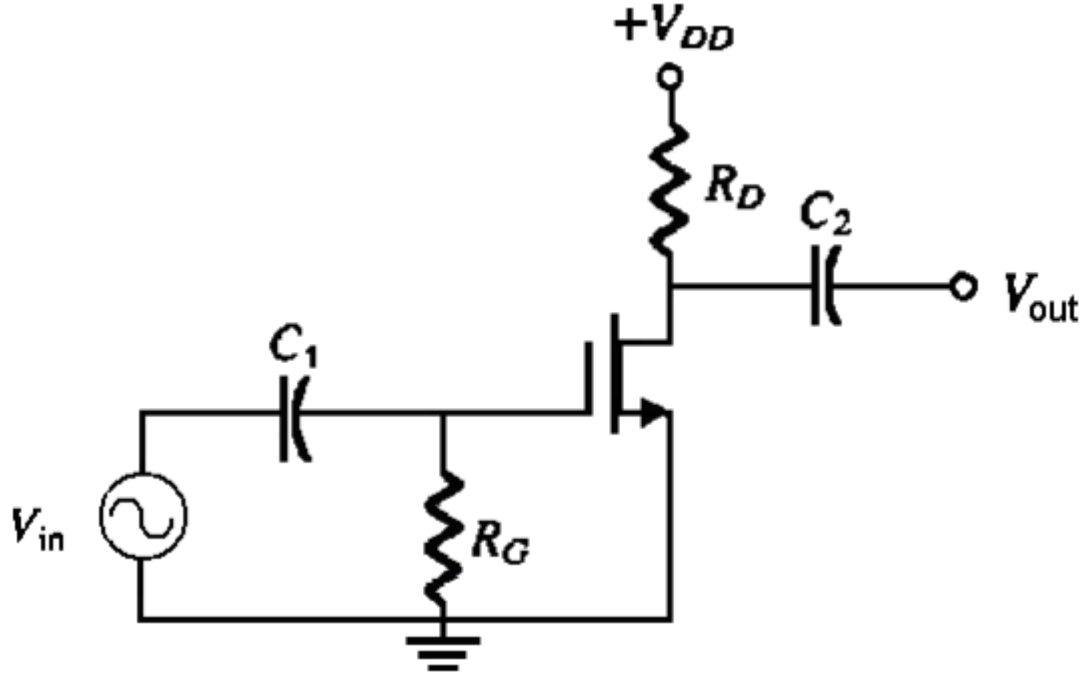
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS}(off)}\right]^2$$

$$I_D = I_S$$

$$I_G = 0$$

Example

Using the circuit shown, determine the drain current I_D and drain-to- source voltage V_{DS} given that $V_{GS}(off) = -8V$, $I_{DSS} = 12mA$, $V_{DD} = 15V$, $R_G = 10M\Omega$ and $R_D = 600\Omega$.



Solution

the drain current is $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$

Since $V_{GS} = 0V$ then

$$I_D = I_{DSS} = 12.0mA$$

$$V_{DS} = V_{DD} - I_D R_D = 15.0V - 12mA(600\Omega) = 7.8V$$