

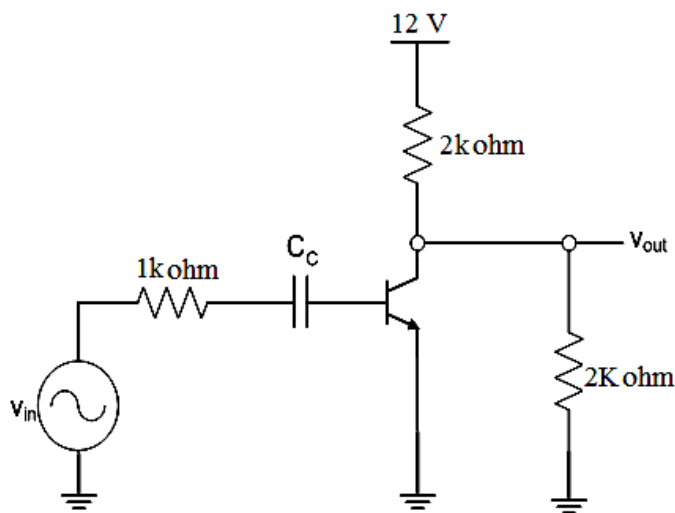
**Q.1] (a)** Calculate gain and bandwidth of a 2-stage amplifier with

$$A_{V1} = \frac{500}{\left(1 + \frac{s}{2000}\right)} \quad A_{V2} = \frac{250}{\left(1 + \frac{s}{4000}\right)}$$

**(b)** Draw the frequency response for the overall gain.

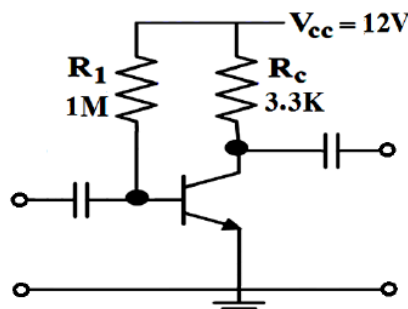
**Q.2]** Three identical stages have an overall upper 3dB frequency of 20 KHZ and a lower 3dB frequency of 20 HZ. What are  $f_L$  and  $f_H$  of each stage? Assume non-interacting stages.

**Q. 3]** For the amplifier shown in Fig. 1, the transistor has the parameters:  $g_m = 5 \text{ mS}$ ,  $r_\pi = 200\Omega$ ,  $r_o = \infty$ ,  $C_\pi = 100\text{pF}$ ,  $C_\mu = 10\text{pF}$ , and  $C_C = 0.1\mu\text{F}$ . If three non-interacting stages from this amplifier are connected in cascade, determine the mid-band gain and lower & higher 3dB frequencies.



**Fig. 1**

**Q. 4]** For the single stage CE amplifier shown in the Fig. 2, let  $I_{CQ} = 1\text{mA}$ . If three capacitively coupled stages of this amplifier are cascaded and the first stage is driven by a  $10\text{-}\mu\text{V-rms}$  signal source having resistance  $1\text{K}\Omega$ , what is the voltage across a  $50\text{K}\Omega$  load connected at the output of the third stage? ( $\beta = 100$ ,  $V_A = 100\text{V}$ )



**Fig. 2**

✓ Q. 5] Draw the AC equivalent circuit and calculate  $V_o/V_i$ ,  $R_i$  and  $R_o$ .

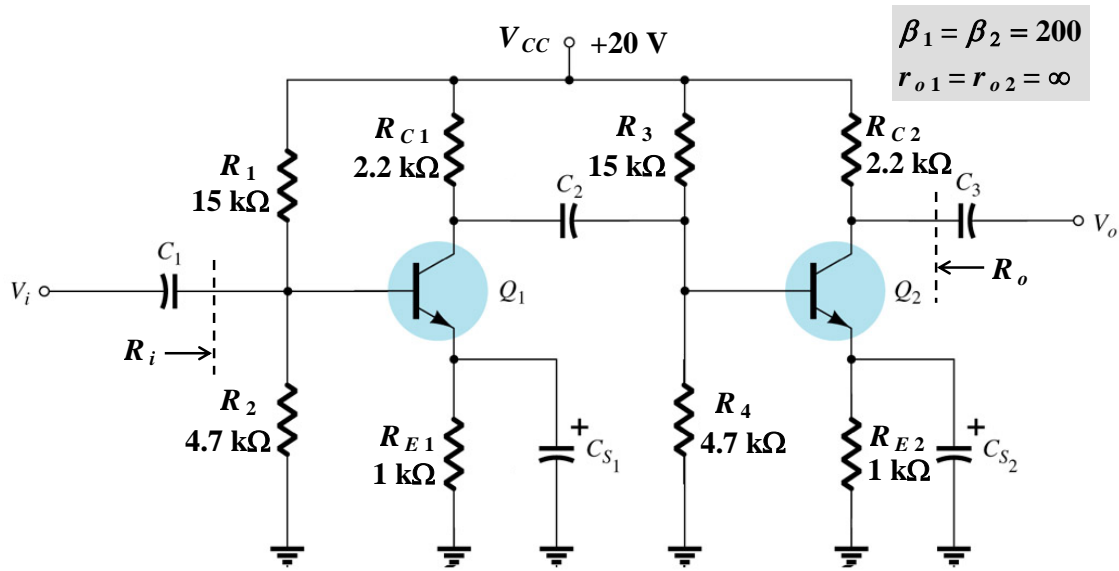


Fig. 3

Q. 6] A two-stage amplifier shown in Fig.4 is in CE-CC configuration. The transistor parameters are given as  $\beta=100$  and  $r_\pi = 0.5 \text{ K}\Omega$ . Determine the overall voltage gain and current gain. Assume  $r_o = \infty$ .

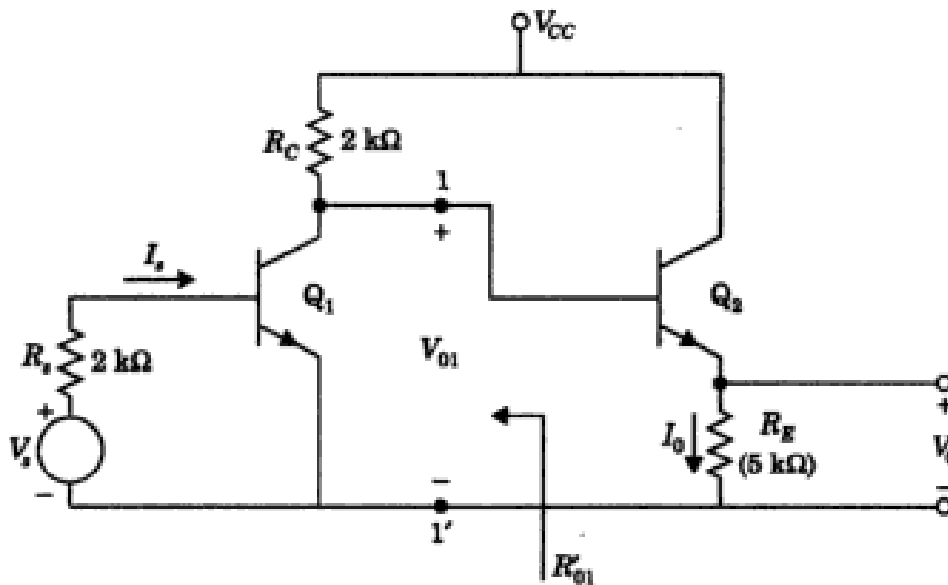
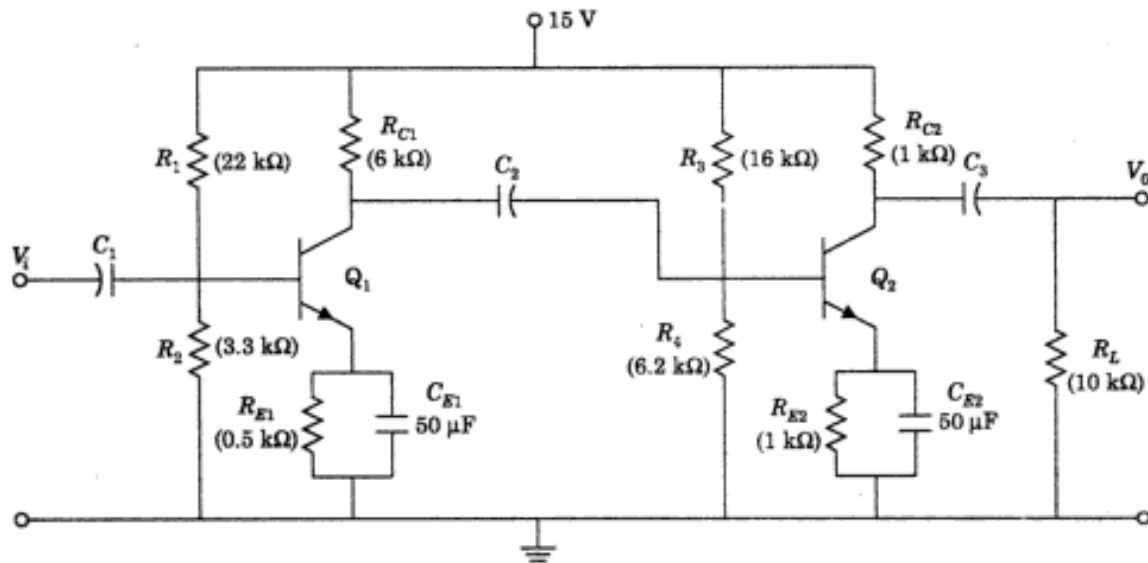


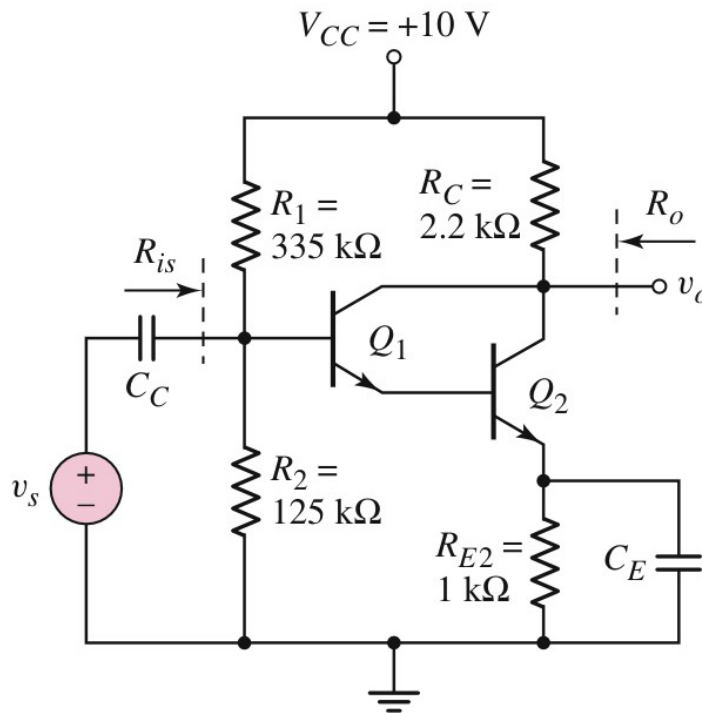
Fig. 4

**Q. 7]** Calculate the voltage gain ( $V_o/V_i$ ), input impedance and output impedance for the two-stage amplifier shown in Fig.5. Assume  $\beta = 100$ .



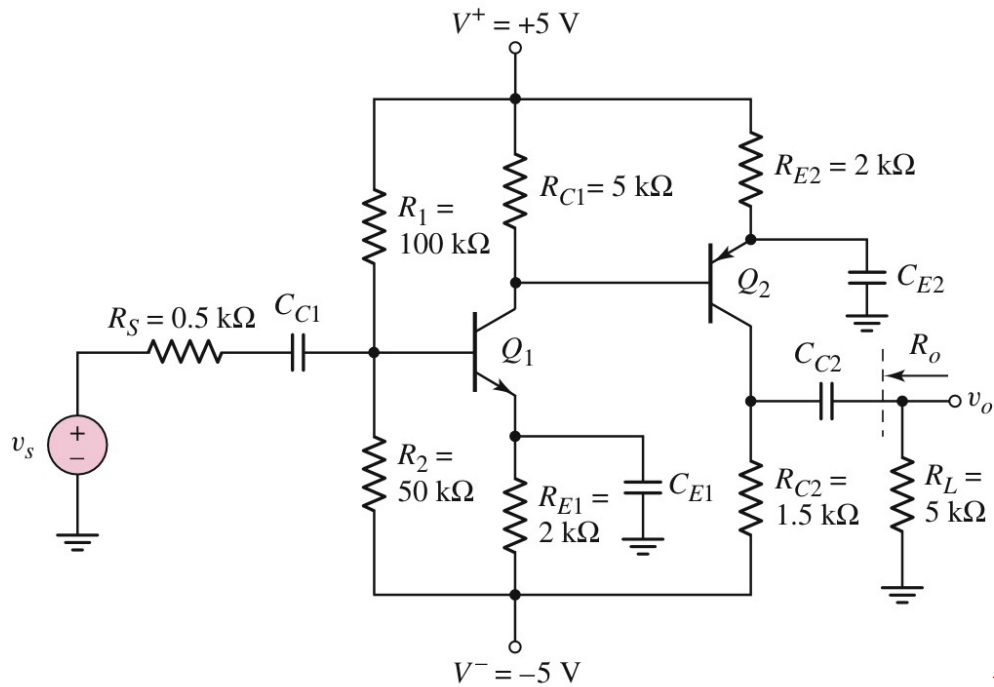
**Fig. 5**

✓ **Q. 8]** Determine the Q-point for  $Q_1$  and  $Q_2$ , voltage gain  $v_o/v_s$ , current gain, input resistance  $R_i$ , and output resistance  $R_o$  for the darlington configuration shown in Fig.6. Assuming  $\beta_1 = \beta_2 = 100$ ,  $V_{A1} = V_{A2} = \infty$ , and  $V_{BE1(ON)} = V_{BE2(ON)} = 0.7$  V.



**Fig. 6**

- ✓ **Q. 9]** Calculate the overall voltage gain ( $v_o/v_s$ ) for the circuit shown in Fig. 7. Assuming  $\beta_1 = 170$ ,  $\beta_2 = 150$  and  $V_{BE(ON)} = 0.7$  V.



**Fig. 7**

- Q. 10]** A two-stage FET capacitively coupled amplifier has the following parameters:  $g_m = 10$  mA/V,  $r_o = 6$  K $\Omega$ ,  $R_D = 10$  K $\Omega$ ,  $R_G = 1$  M $\Omega$  for each stage. Find the overall mid-band gain.

*Best wishes*