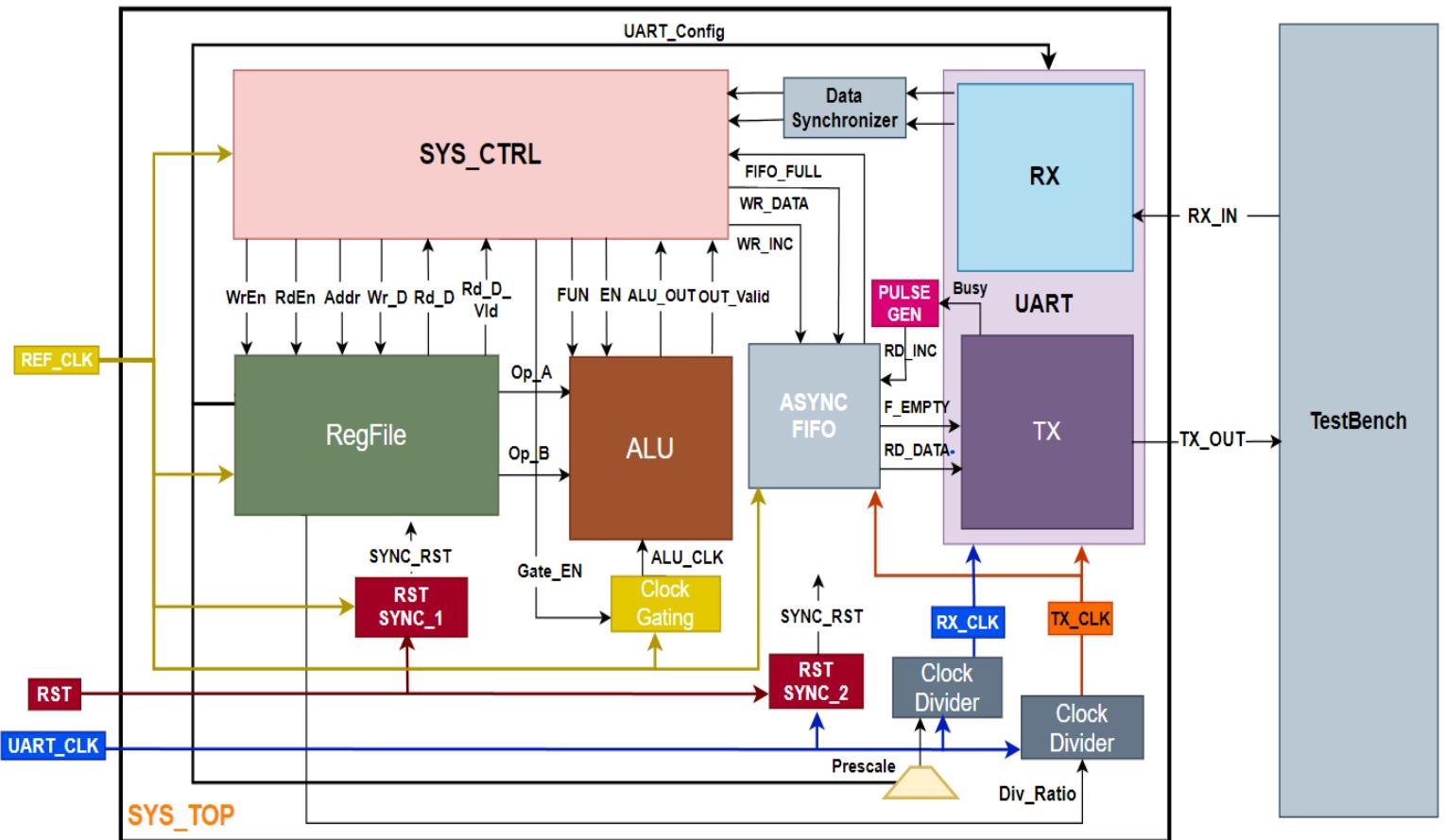


# Final System



- **Description: -**

- 1 . This system contains 10 blocks: -

- 1) **Clock Domain 1 (REF\_CLK)**

- **RegFile**
- **ALU**
- **Clock Gating**
- **SYS\_CTRL**

- **Clock Domain 2 (UART\_CLK)**

- **UART\_TX**
- **UART\_RX**
- **PULSE\_GEN**
- **Clock Dividers**

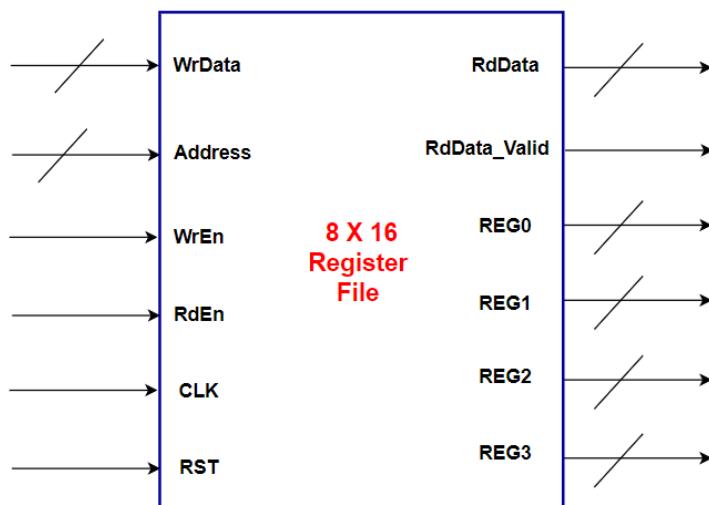
- **Data Synchronizers**

- **RST Synchronizer**
- **Data Synchronizer**
- **ASYNC FIFO**

## CLOCK Domain 1

### 1) RegFile: -

- **Block Interface:** -



- **Signal Description:** -

Port	Direction	Width	Description	Connected to
<b>CLK</b>	IN	1	Clock Signal	TOP Input Port <b>(REF_CLK)</b>
<b>RST</b>	IN	1	Active Low Reset	RST_SYNC
<b>Address</b>	IN	Parameterized (default : 4 bits)	Address bus	SYS_CTRL
<b>WrEn</b>	IN	1	Write Enable	SYS_CTRL
<b>RdEn</b>	IN	1	Read Enable	SYS_CTRL
<b>WrData</b>	IN	Parameterized (default : 8 bits)	Write Data Bus	SYS_CTRL
<b>RdData</b>	OUT	Parameterized (default : 8 bits)	Read Data Bus	SYS_CTRL
<b>RdData_Valid</b>	OUT	1	Read Data Valid	SYS_CTRL
<b>REG0</b>	OUT	Parameterized (default : 8 bits)	Register at Address 0x0	ALU
<b>REG1</b>	OUT	Parameterized (default : 8 bits)	Register at Address 0x1	ALU
<b>REG2</b>	OUT	Parameterized (default : 8 bits)	Register at Address 0x2	UART
<b>REG3</b>	OUT	Parameterized (default : 8 bits)	Register at Address 0x3	Clock Divider

- **Reserved Registers Description:** -

**1) REG0 (Address: 0x0)** ALU Operand A

**2) REG1 (Address: 0x1)** ALU Operand B

**3) REG2 (Address: 0x2)** UART Config

**REG2[0]: Parity Enable**

**(Default = 1)**

**REG2[1]: Parity Type**

**(Default = 0)**

**REG2[7:2]: Prescale**

**(Default = 32)**

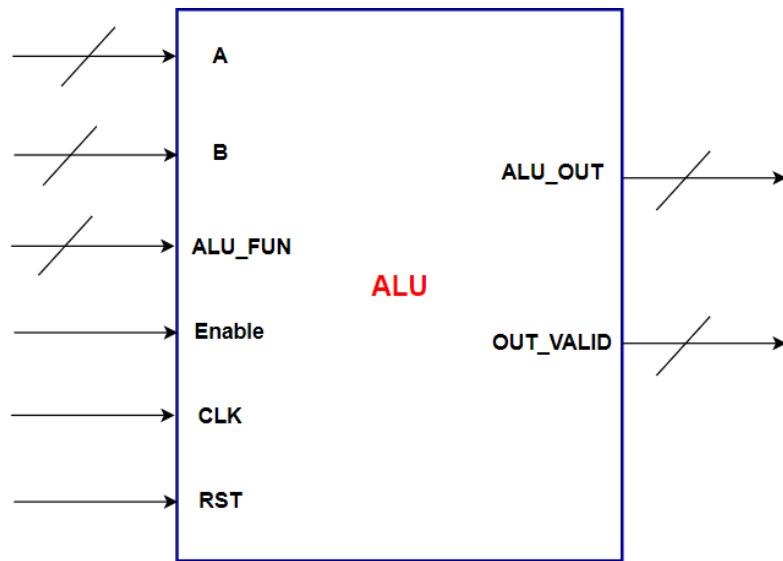
**4) REG3 (Address: 0x3)** Div Ratio

**REG3[7:0]: Division ratio**

**(Default = 32)**

## 2) ALU:

- **Block Interface:** -

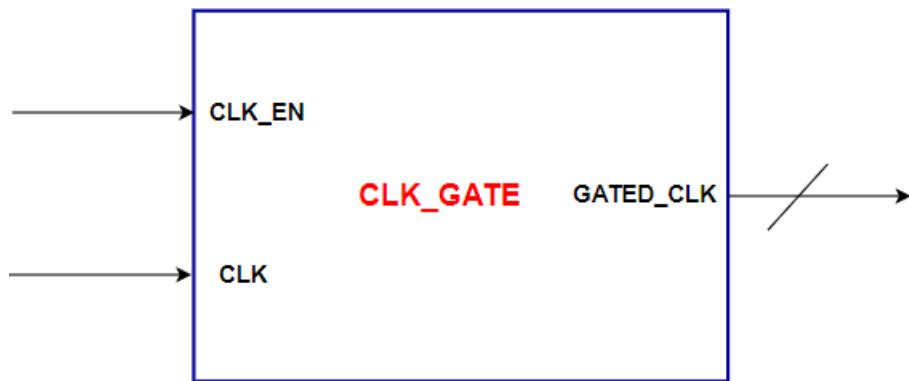


- **Signal Description:** -

Port	Direction	Width	Description	Connected to
<b>CLK</b>	IN	1	Clock Signal	CLK_GATE
<b>RST</b>	IN	1	Active Low Reset	RST_SYNC
<b>A</b>	IN	Parameterized (default : 8 bits)	Operand A	RegFile (REG0)
<b>B</b>	IN	Parameterized (default : 8 bits)	Operand B	RegFile (REG1)
<b>ALU_FUN</b>	IN	Parameterized (default : 4 bits)	ALU Function	SYS_CTRL
<b>Enable</b>	IN	1	ALU Enable	SYS_CTRL
<b>ALU_OUT</b>	OUT	Parameterized (default : 8 bits)	ALU Result	SYS_CTRL
<b>OUT_VALID</b>	OUT	1	Result Valid	SYS_CTRL

### 3) Clock Gating: -

- **Block Interface:** -

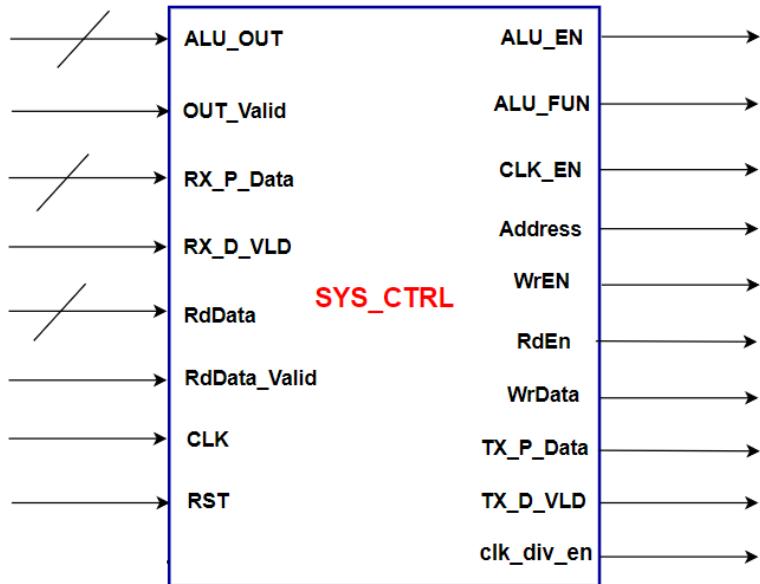


- **Signal Description:** -

Port	Direction	Width	Description	Connected to
<b>CLK</b>	IN	1	Clock Signal	TOP Input Port (REF_CLK)
<b>CLK_EN</b>	IN	1	Clock Enable	SYS_CTRL
<b>GATED_CLK</b>	out	1	Gated Clock signal	ALU

## 4) SYS\_CTRL:

- Block Interface: -



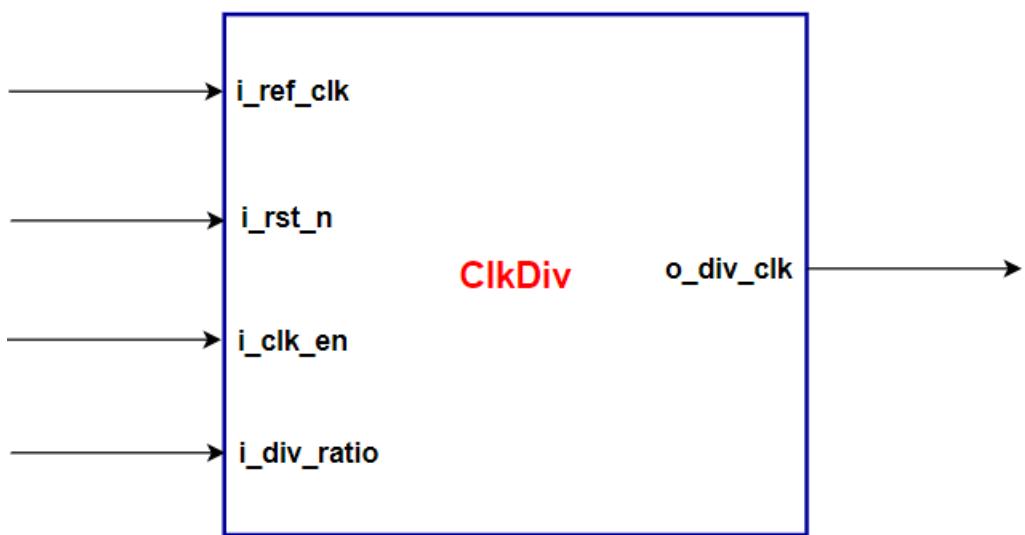
- Signal Description: -

Port	Direction	Width	Description	Connected to
<b>CLK</b>	IN	1	Clock Signal	TOP Input Port <b>(REF_CLK)</b>
<b>RST</b>	IN	1	Active Low Reset	<b>RST_SYNC</b>
<b>ALU_OUT</b>	IN	16	ALU Result	<b>ALU</b>
<b>OUT_Valid</b>	IN	1	ALU Result Valid	<b>ALU</b>
<b>ALU_FUN</b>	OUT	4	ALU Function signal	<b>ALU</b>
<b>EN</b>	OUT	1	ALU Enable signal	<b>ALU</b>
<b>CLK_EN</b>	OUT	1	Clock gate enable	<b>CLK_GATE</b>
<b>Address</b>	OUT	4	Address bus	<b>RegFile</b>
<b>WrEn</b>	OUT	1	Write Enable	<b>RegFile</b>
<b>RdEn</b>	OUT	1	Read Enable	<b>RegFile</b>
<b>WrData</b>	OUT	8	Write Data Bus	<b>RegFile</b>
<b>RdData</b>	IN	8	Read Data Bus	<b>RegFile</b>
<b>RdData_Valid</b>	IN	1	Read Data Valid	<b>RegFile</b>
<b>RX_P_DATA</b>	IN	8	UART_RX Data	<b>UART_RX</b>
<b>RX_D_VLD</b>	IN	1	RX Data Valid	<b>UART_RX</b>
<b>TX_P_DATA</b>	OUT	8	UART_TX Data	<b>UART_TX</b>
<b>TX_D_VLD</b>	OUT	1	TX Data Valid	<b>UART_TX</b>
<b>clk_div_en</b>	OUT	1	Clock divider enable	<b>CLKDiv</b>

## CLOCK Domain 2

### 1) Clock Divider: -

- **Block Interface: -**

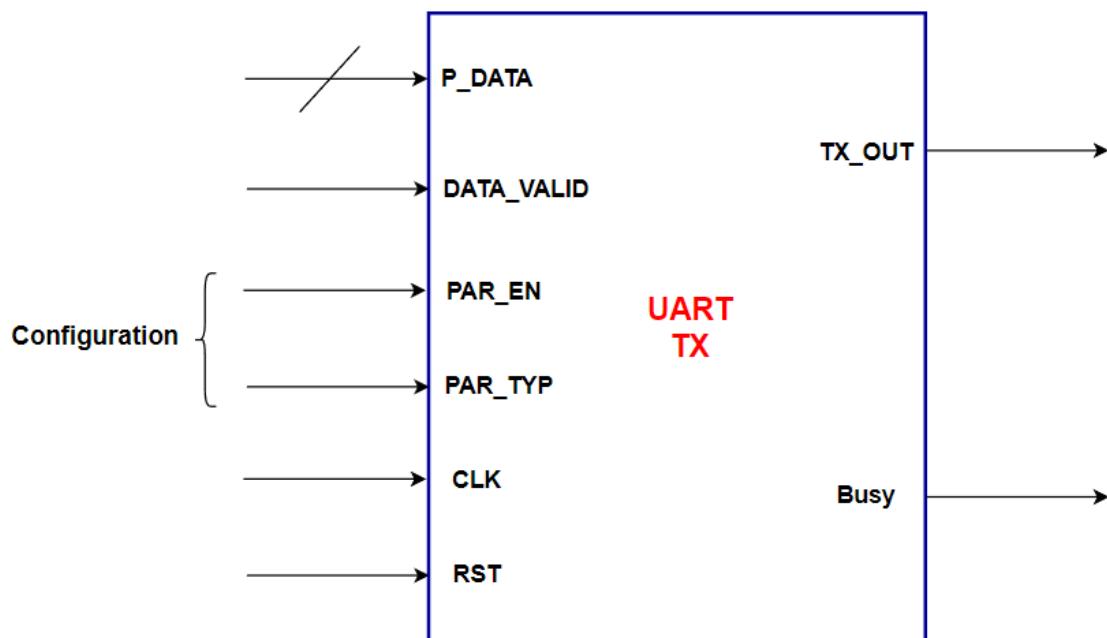


- **Signal Description: -**

Port	Direction	Width	Description	Connected to
I_ref_clk	IN	1	Clock Signal	TOP Input Port (UART_CLK)
I_rst_n	IN	1	Active Low Async Reset	RST_SYNC_2
I_clk_en	IN	1	Clock divider enable	1'b1 (Supply)
I_div_ratio	IN	Parameterized (default : 8 bits)	Division ratio	RegFile
O_div_clk	out	1	Divided clock	UART_TX UART_RX

## 2) UART\_TX: -

- **Block Interface: -**

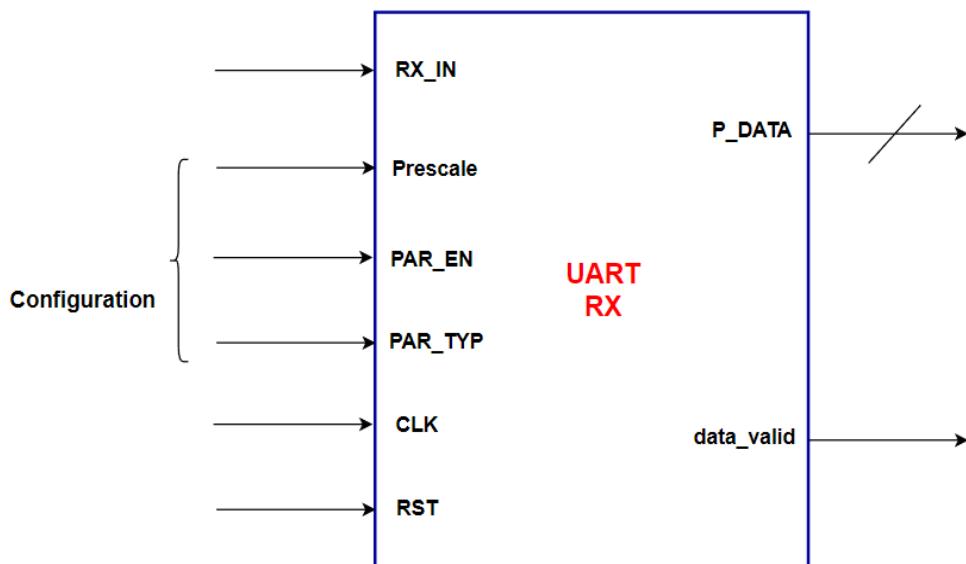


- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	CLKDiv
RST	IN	1	Active Low Reset	RST_SYNC_2
PAR_EN	IN	1	Parity Enable	RegFile
PAR_TYP	IN	1	Parity Type	RegFile
P_DATA	IN	Parameterized (default : 8 bits)	Parallel IN Data	ASYNC_FIFO
DATA_VALID	IN	1	IN Data Valid	ASYNC_FIFO
S_DATA	OUT	1	frame serial bits	TOP Output Port (TX_OUT)
Busy	OUT	1	Uart status signal	PULSE_GEN

### 3) UART\_RX: -

- **Block Interface: -**

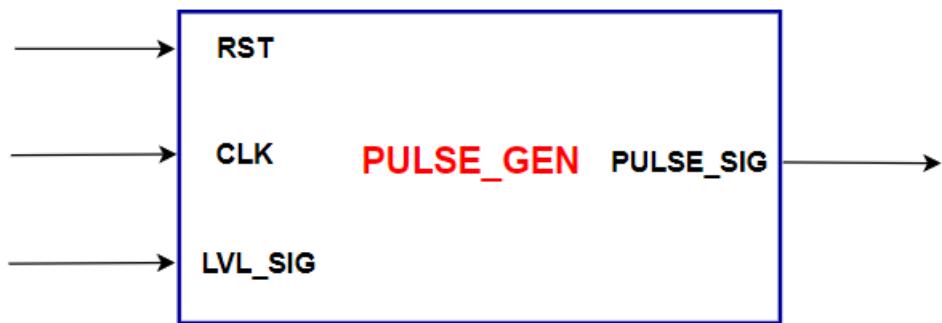


- **Signal Description: -**

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	TOP Input Port (UART_CLK)
RST	IN	1	Active Low Reset	RST_SYNC_2
Prescale	IN	6	Prescale	RegFile
PAR_EN	IN	1	Parity Enable	RegFile
PAR_TYP	IN	1	Parity Type	RegFile
RX_IN	IN	1	frame serial bits	TOP Input Port (RX_IN)
P_DATA	OUT	Parameterized (default : 8 bits)	Parallel Out Data	DATA_SYNC
DATA_VLD	OUT	1	Out Data Valid	DATA_SYNC
PAR_ERR	OUT	1	Frame parity error	TOP Output Port
STP_ERR	OUT	1	Frame stop error	TOP Output Port

#### 4) PULSE\_GEN: -

- Block Interface: -



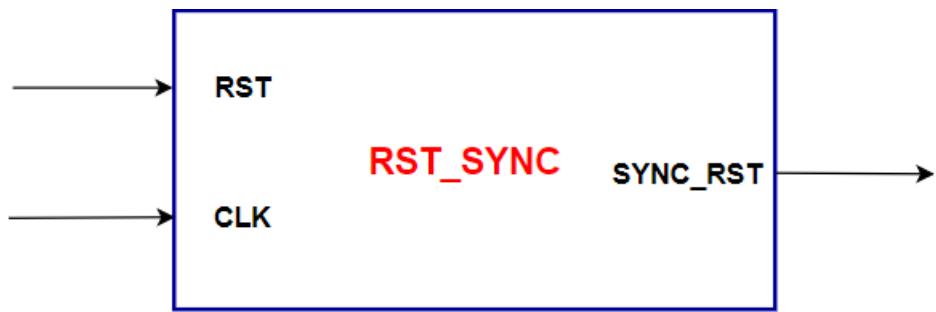
- Signal Description: -

Port	Direction	Width	Description	Connected to
CLK	IN	1	Clock Signal	TOP Input Port (UART_TX)
RST	IN	1	Active Low Reset	RST_SYNC_2
LVL_SIG	IN	1	Level signal	UART_TX
PULSE_SIG	OUT	1	Pulse signal	ASYNC_FIFO

## Synchronizers

### 1) RST\_Sync: -

- **Block Interface: -**

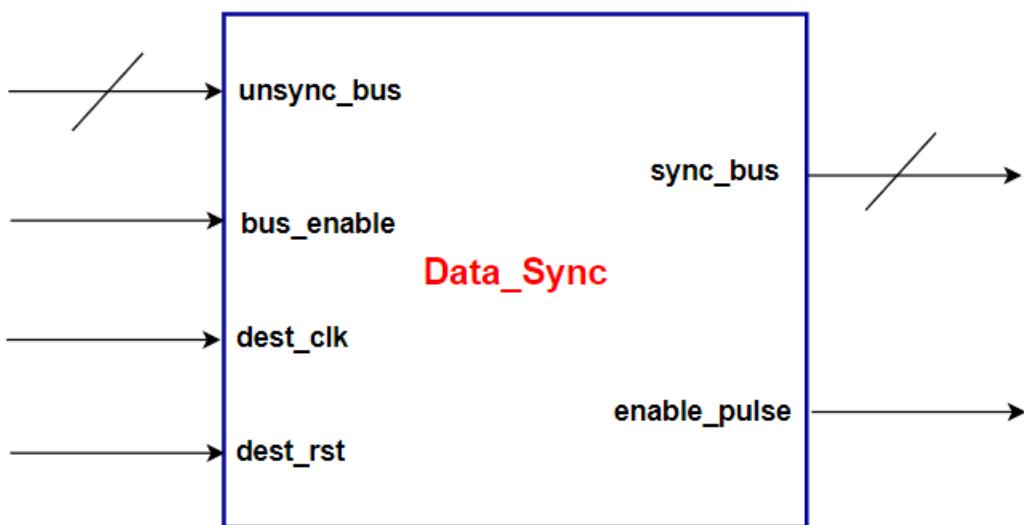


- **Signal Description: -**

Port	Direction	Width	Description
RST	IN	1	Clock Signal
CLK	IN	1	Active Low Async Reset
SYNC_RST	OUT	1	Active Low synchronized Reset

## 2) Data\_Sync: -

- **Block Interface: -**

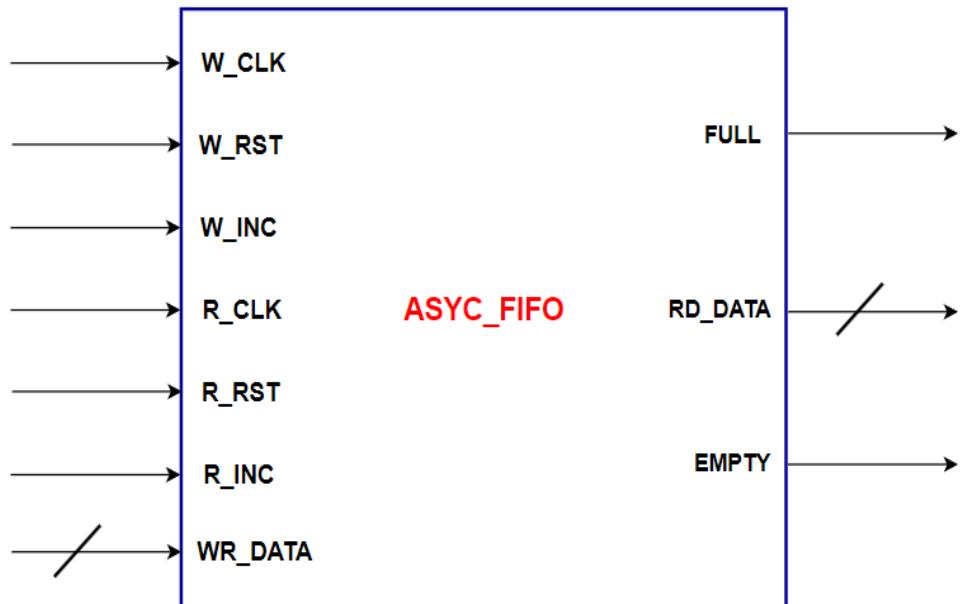


- **Signal Description: -**

Port	Direction	Width	Description
unsync_bus	IN	8	Unsynchronized bus
bus_enable	IN	1	Bus enable signal
dest_clk	IN	1	Destination Clock Signal
dest_rst	IN	1	Destination Active Low Reset
sync_bus	OUT	8	synchronized bus
enable_pulse_d	OUT	1	enable pulse signal

## 3) ASYNC\_FIFO: -

- **Block Interface: -**



- **Signal Description: -**

Port	Width	Description	Connected to
W_CLK	1	Source domain clock	TOP Input Port <a href="#">(REF_CLK)</a>
W_RST	1	Source domain Async reset	RST_SYNC_1
W_INC	1	Write operation enable	SYS_CTRL
R_CLK	1	Destination domain clock	RST_SYNC_2
R_RST	1	Destination domain Async reset	RST_SYNC_2
R_INC	1	Read operation enable	PULSE_GEN
WR_DATA	Parameterized default ( 8-bits )	Write Data Bus	SYS_CTRL
RD_DATA	Parameterized default ( 8-bits )	Read Data Bus	UART_TX
FULL	1	FIFO Buffer full flag	SYS_CTRL
EMPTY	1	FIFO Buffer empty flag	UART_TX

## Introduction

- The system is responsible to do some operation based on the received **commands** from the master through **UART\_RX** interface, once the operation is done, the system is responsible to send the result to the master through **UART\_TX** interface.

- Supported Operations: -

### 1. ALU Operations: -

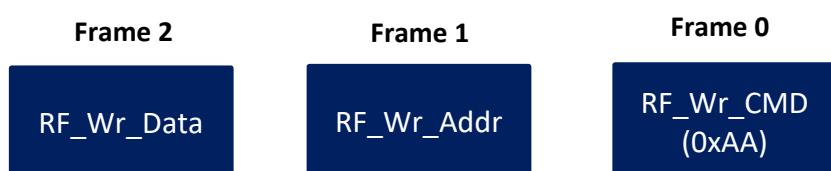
- Addition
- Subtraction
- Multiplication
- Division
- AND
- OR
- NAND
- NOR
- XOR
- XNOR
- CMP: A = B
- CMP: A > B
- SHIFT: A >> 1
- SHIFT: A << 1

### 2. Register File Operations

- Register File Write
- Register File read

- Supported Commands: -

#### 1. Register File Write command (3 frames)



## 2. Register File Read command (2 frames)



## 3. ALU Operation command with operand (4 frames)



## 4. ALU Operation command with No operand (2 frames)



### System Specifications: -

- Reference clock (REF\_CLK) is ~~50~~ MHz
- UART clock (UART\_CLK) is 3.6864 MHz
- Clock Divider is always on (clock divider enable = 1)

### Sequence of Operation (Must include in the testbench): -

- Initially configuration operations are performed through Register file write operations in addresses (0x2, 0x3).
- The Master (Testbench) start to send different commands (RegFile Operations, ALU operations)
- Our system will receive the command frames through UART\_RX, it sent to the SYS\_CTRL block to be processed
- Once the operation of the command is performed using ALU/RegFile, SYS\_CTRL sends the result to the master through UART\_TX
- Register File Address Range for normal write/read operations (From 0x4 to 0x15)
- Register File Addresses reserved for configurations and ALU operands (From 0x0 to 0x3)