Lab_DFT_1

You have to synthesize and insert DFT logic using DFT Compiler shell and generate Technology Dependent gate level netlists in Verilog format using standard cell libraries (typical, worst, best) inside std_cells folder:-

- scmetro_tsmc_cl013g_rvt_tt_1p2v_25c.db
- scmetro_tsmc_cl013g_rvt_ff_1p32v_m40c
- scmetro_tsmc_cl013g_rvt_ss_1p08v_125c

Steps: -

1. Copy Lab_DFT_1 folder from your computer into the virtual machine inside Labs directory
2. Perform RTL preparation
    - Add scan ports (SI, SE, SO, test_mode, scan_clk, scan_rst)
    - Instantiate mux2X1 module for clocks
    - Instantiate mux2X1 module for resets
    - Connect muxed clk and muxed rst to the Instantiated modules
3. Open dft_script.tcl and Read the verilog module “mux2X1”.
4. Run dft_script.tcl using (dc_shell -f dft_script.tcl | tee dft.log) to check that the instantiated file is consistent with the RTL files (No Errors, No Warnings)
5. Open dft_script.tcl and Add the following commands: -
    - Configuring scan chain style using set_scan_configuration command
    - Test-Ready Compile using compile -scan command
    - Defining the DFT Signals (SI, SE, SO, test_mode, scan_clk, scan_rst) using set_dft_signal command
    - Create Test Protocol using create_test_protocol command
    - Preform Pre-DFT Design Rule Checking using dft_drc -verbose command
    - Preview DFT using preview_dft -show scan_summary command
    - Insert DFT logic using insert_dft command
    - Optimize Post DFT Insertion using compile -scan -incremental command
    - Preform Post-DFT Design Rule Checking using dft_drc -verbose -coverage_estimate command

6. Run dft_script.tcl inside Lab_DFT_1 & check the log (dft.log) to be sure that: -
    - No Errors
    - No Warnings
    - No Latches
    - No Comb Loops
7. Check DFT Test Coverage.
8. Open Design Compiler GUI, View the DFT Scan chain.