Embedded Systems

5- Timers and Counters

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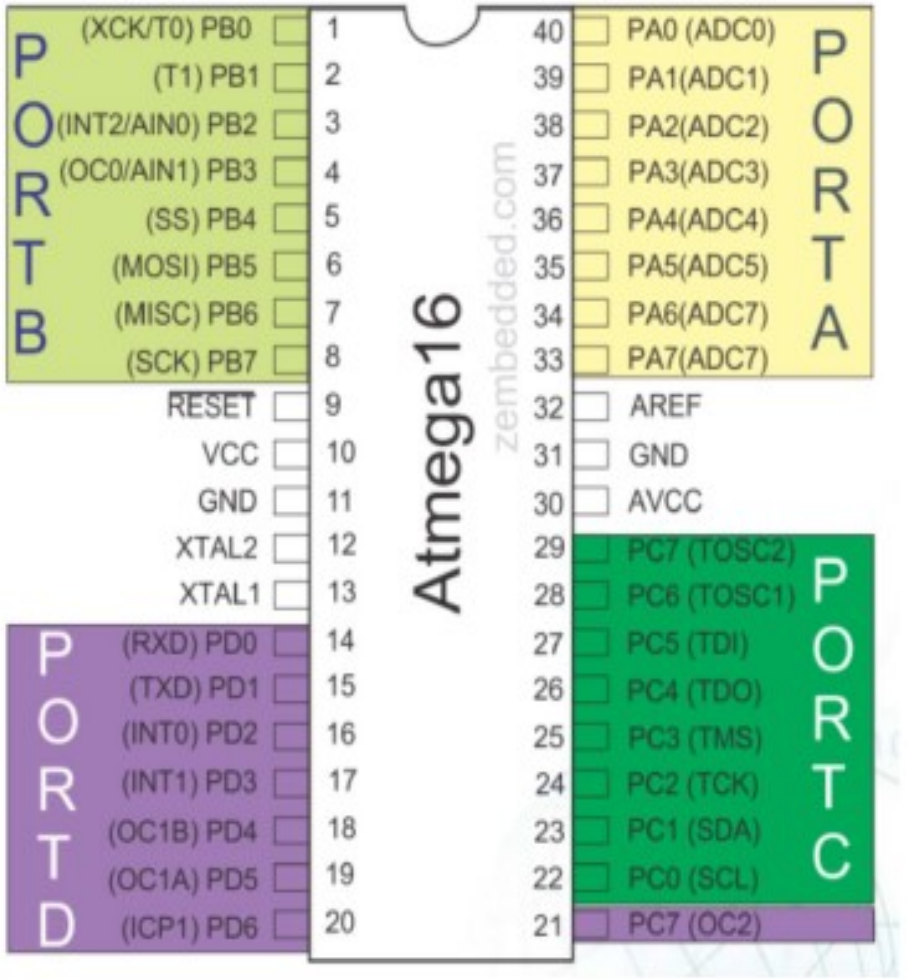
ATMEGA16 TIMERS/COUNTERS

ATmega16 has 3 timers: timer0 (8 bit), timer1 (16 bit) and timer2 (8bit).

Clock sources for these timers/counters are either internal (prescaled clock) or external.

Timers 0,1: external clock sources are synchronous produced by edge detection of input signals on pins T0 (PB0), and T1 (PB1) sampled once every system clock cycle.

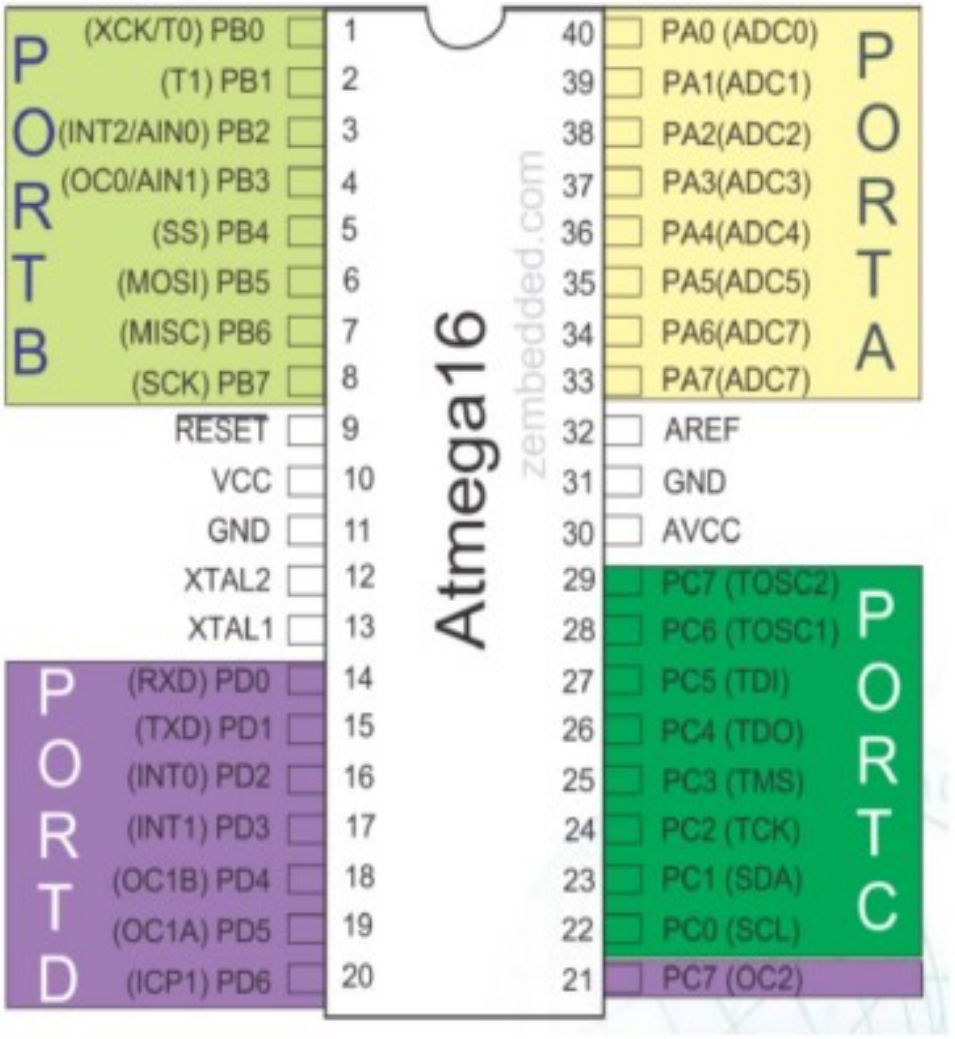
Timer2:external clock is asynchronous where a crystal can be connected between the TOSC1 and TOSC2 pins (PC6, PC7) to serve as an independent clock source that can be prescaled.



ATMEGA16 TIMERS/COUNTERS

When the internal system clock is used, a prescaler can be applied to make the timer count at a slower rate.

Example: Consider a system clock of 1Mhz (i.e. 1μs per cycle). Suppose that a timer prescaler of 64 is used. Then, timer will increment every 64μs.



Timer/Counter Events

Timer Overflow
Overflow interrupt is triggered when timer reaches its top limit;

Input Capture:
Input signal is connected to a pin, called input capture, of the timer.
When a preset event (rising edge, falling edge, change) occurs on this pin (ICP1), the current timer value is automatically stored in a register (ICR1).

Output Compare:
When the timer reaches a preset value (stored at the output compare register), the output compare pin can be automatically changed (set, reset, toggled) .

Bottom Count = 00
Max Count = FF (or FFFF for timer1)
Top Count = Count at which timer is cleared to zero and is either FF (FFFF) or the value stored in the Output Compare Register (OCR).

Timers/Counters modes of operation First look !!

- Normal Mode: Count from BOTTOM (0x00)to MAX (0xFF)

Take an action when overflow

- CTC (Clear Timer at Compare Match): Count from bottm to a specific value stored in OCR register

Mode	WGM01	WGM00	Timer/Counter Mode of Operation	TOP	Update of OCR0	TOV0 Flag Set-on
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR0	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

Counter Status

Status via Polling

- Timer status can be determined through polling
  - Read the Timer Interrupt Flag Register and check for set bits
  - The overflow and compare match events set the corresponding bits in TIFR
    - TOVn and OCFn (n=0, 1, or 2)
      - Timer 1 has two output compare registers: 1A and 1B
    - Clear the bits by writing a 1

Status via Interrupt

- Enable the appropriate interrupts in the Timer Interrupt Mask Register
- Each event has a corresponding interrupt enable bit in TIMSK
  - TOIEn (Timer overflow) and OCIEn(Output Compare) (n = 0, 1, 2)
    - Again, timer 1 has OCIE1A and OCIE1B
  - The interrupt vectors are located at OVFnaddr and OCnaddr

Clock sources

- Clock sources for these timers/counters are either internal (prescaled clock) or external.

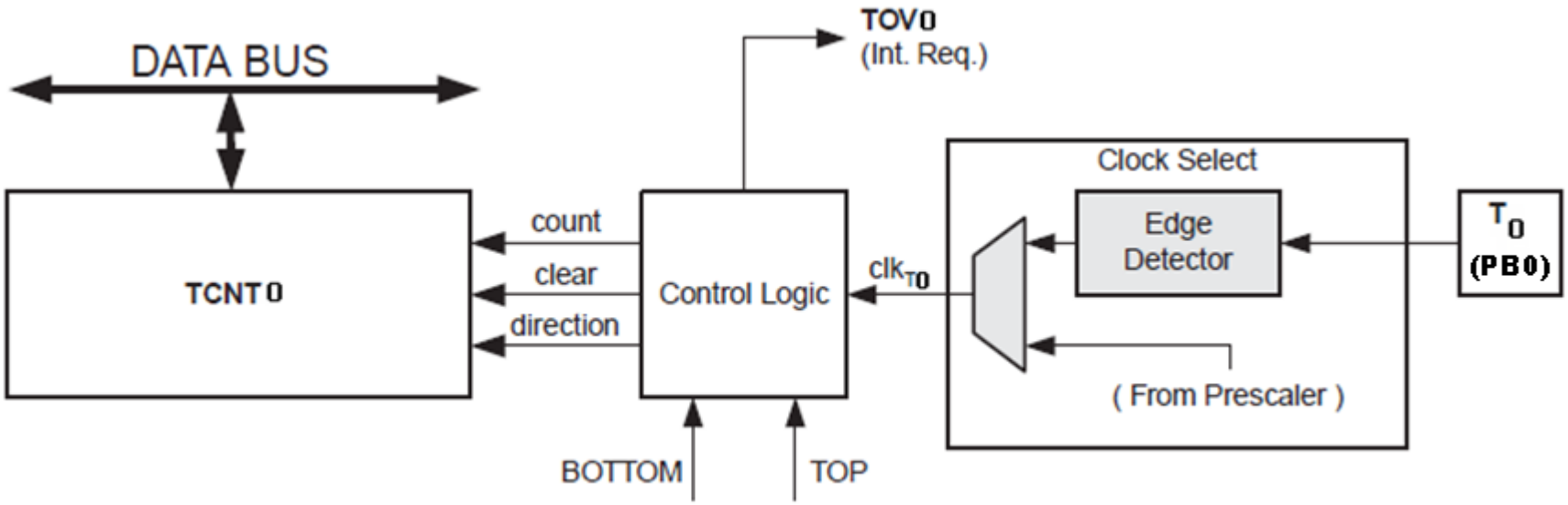
- By Timers 0,1 external clock sources are synchronous produced by edge detection of input signals on pins T0 (PB0), and T1 (PB1) sampled once every system clock cycle. On the other hand external clock for timer2 is **a**synchronous where a crystal can be connected between the TOSC1 and TOSC2 pins (PC6, PC7) to serve as an independent clock source that can be prescaled.

- Definitions:

Bottom Count = 00
Max Count = FF (or FFFF for timer1)
Top Count = Count at which timer is cleared to zero and is either FF (FFFF) or = Output Compare Register (OCR).

Simple Block Diagrams (Counter Unit)

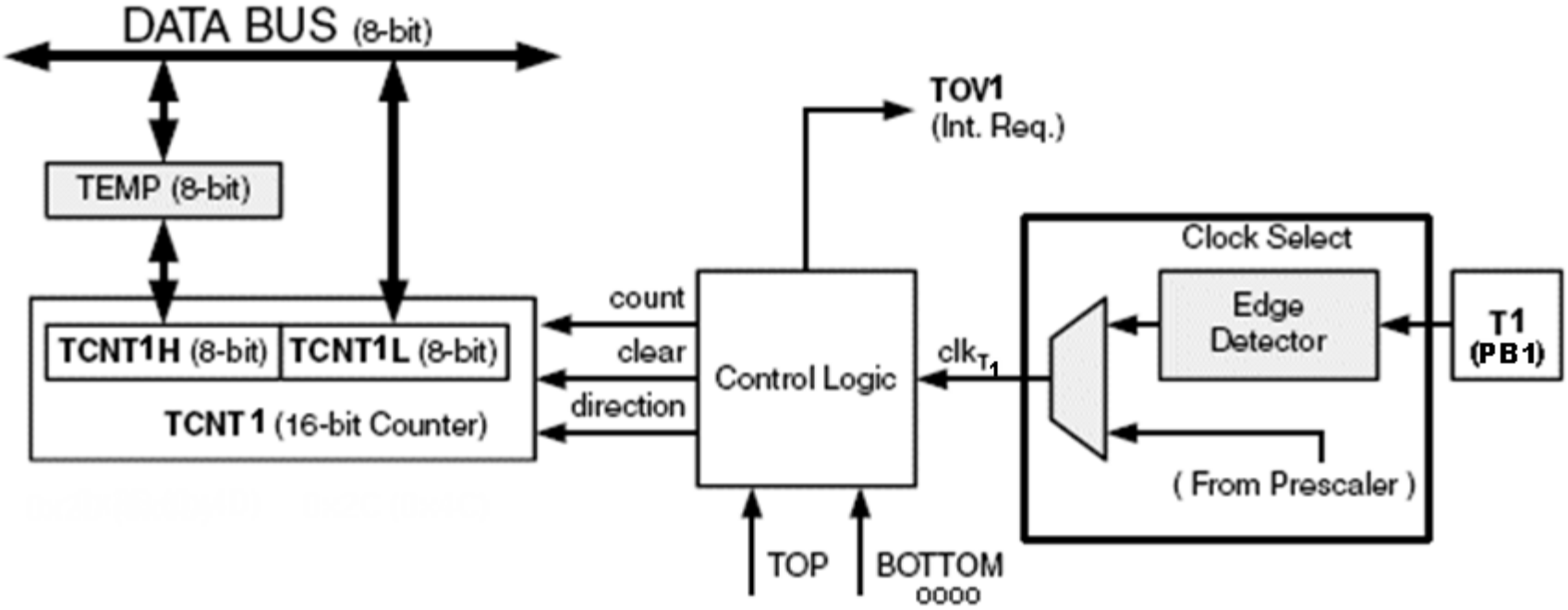
Timer/Counter 0



►By Timers 0,1 external clock sources are synchronous produced by edge detection of input signals on pins T0 (PB0), and T1 (PB1) sampled once every system clock cycle.

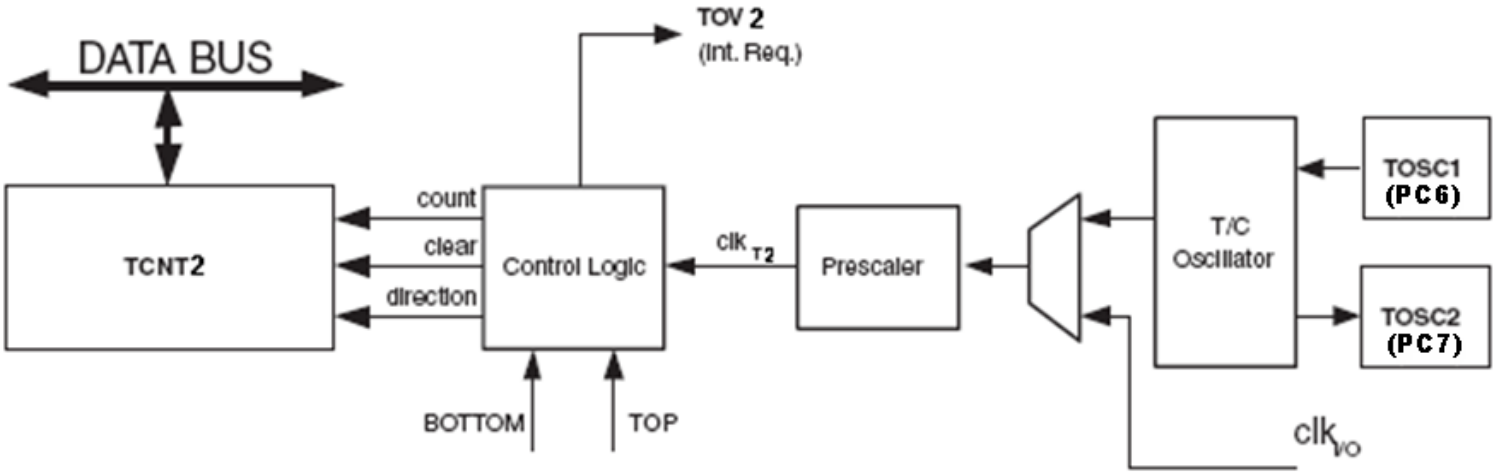
Simple Block Diagrams (Counter Unit)

Timer/Counter 1



Simple Block Diagrams (Counter Unit)

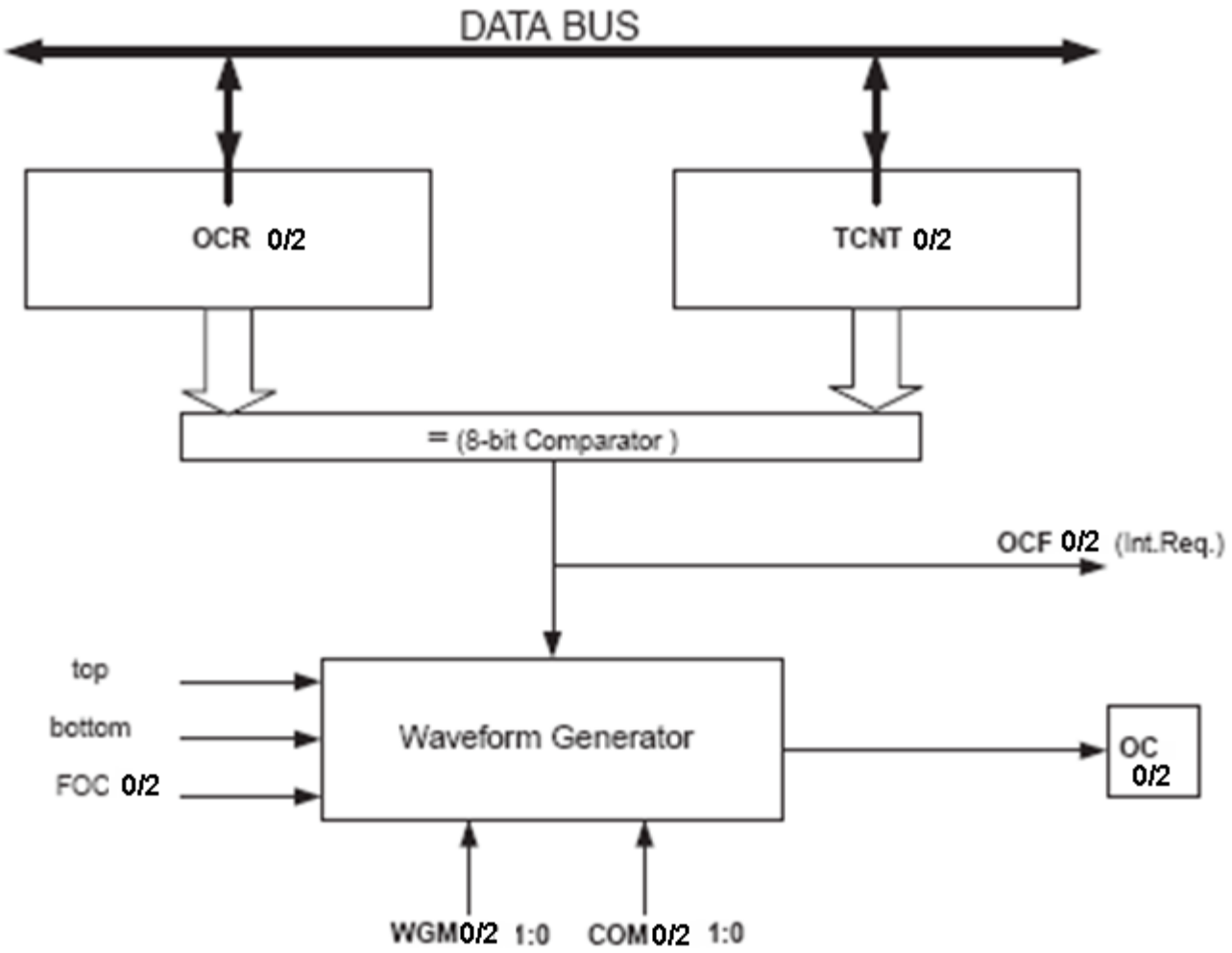
Timer/Counter 2



►On the other hand external clock for timer2 is **a**synchronous where a crystal can be connected between the TOSC1 and TOSC2 pins (PC6, PC7) to serve as an independent clock source that can be prescaled.

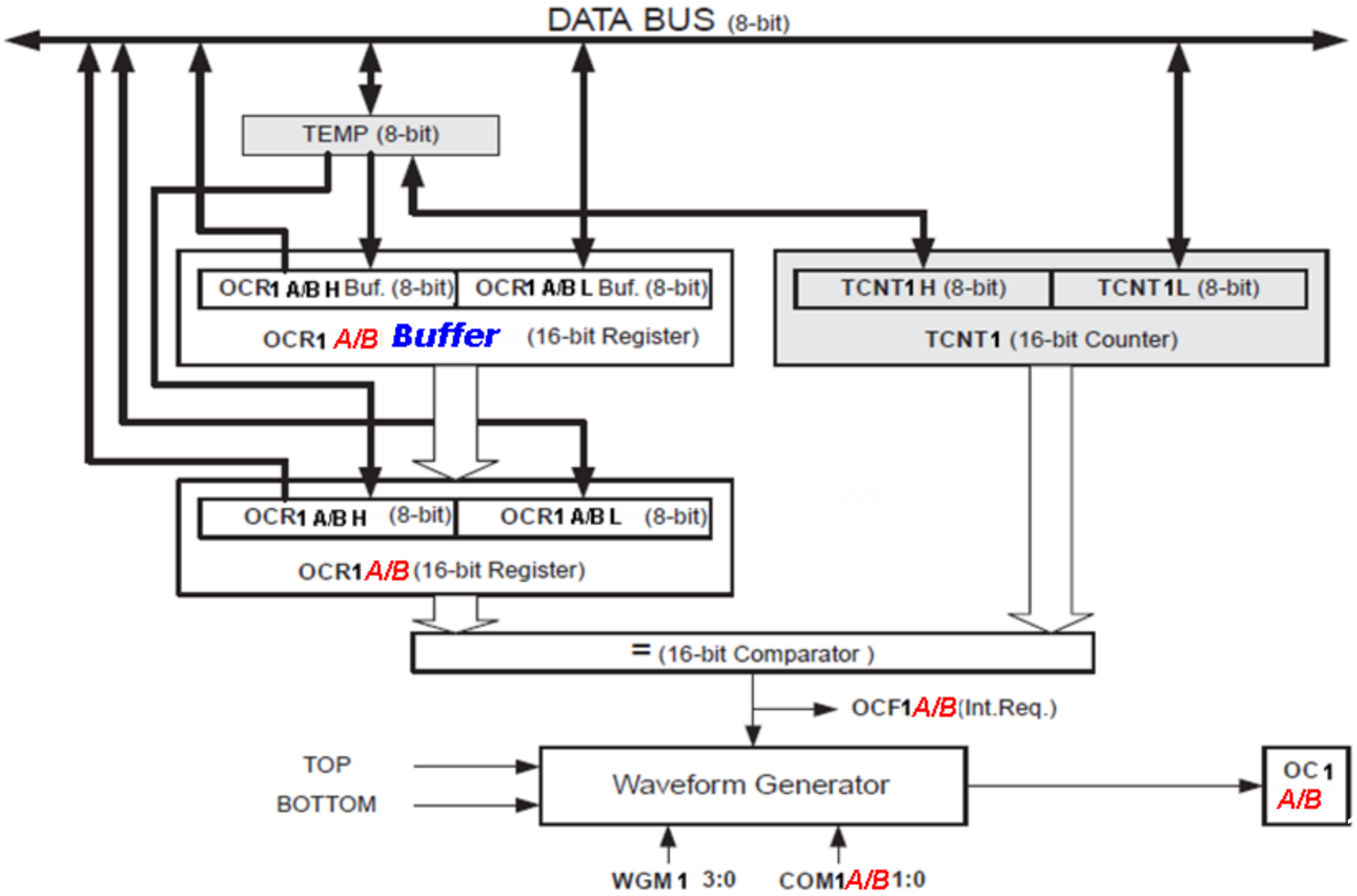
Output Compare Unit

Timer 0 & 2



Output Compare Unit

Timer1



Registers and Flags Associated with Timers

Each timer has following registers associated with it:

TCNTn: Timer/Counter Reg: Upon reset, it has zero value and counts up/down with each timer clock

TCCRn: Timer/Counter Control Reg: For setting modes of operation of Timer n

OCRn: Output Compare Reg: When contents of TCNT are equal to OCR, OCF flag is raised and value of TCNTn is reset to zero

TOVn: Timer Overflow Flag: When overflow occurs, this flag is raised

OCFn: Output Compare Flag.

Figure 34. Timer/Counter Timing Diagram, no Prescaling

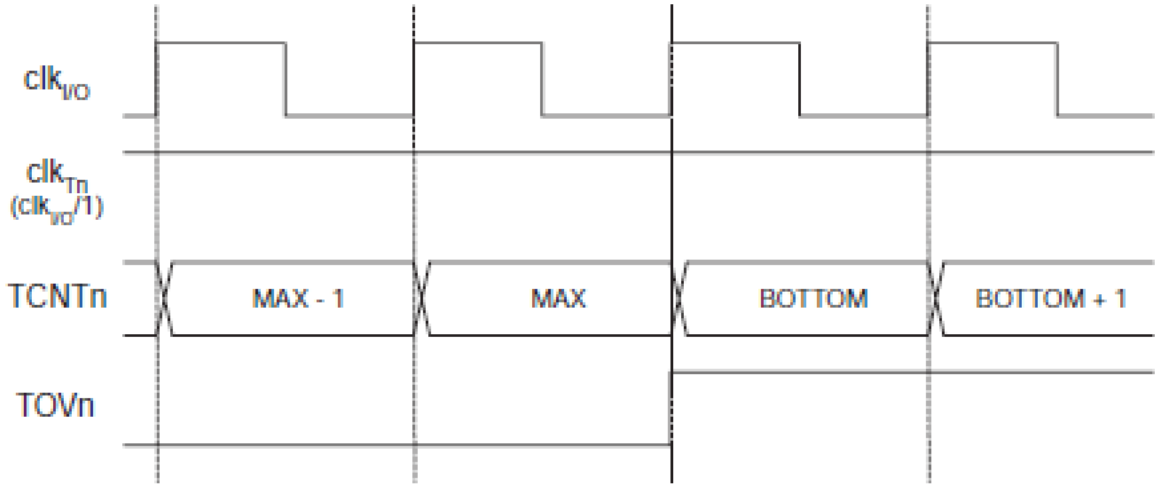


Figure 35 shows the same timing data, but with the prescaler enabled.

Figure 35. Timer/Counter Timing Diagram, with Prescaler ($f_{clk\_I/O}/8$)

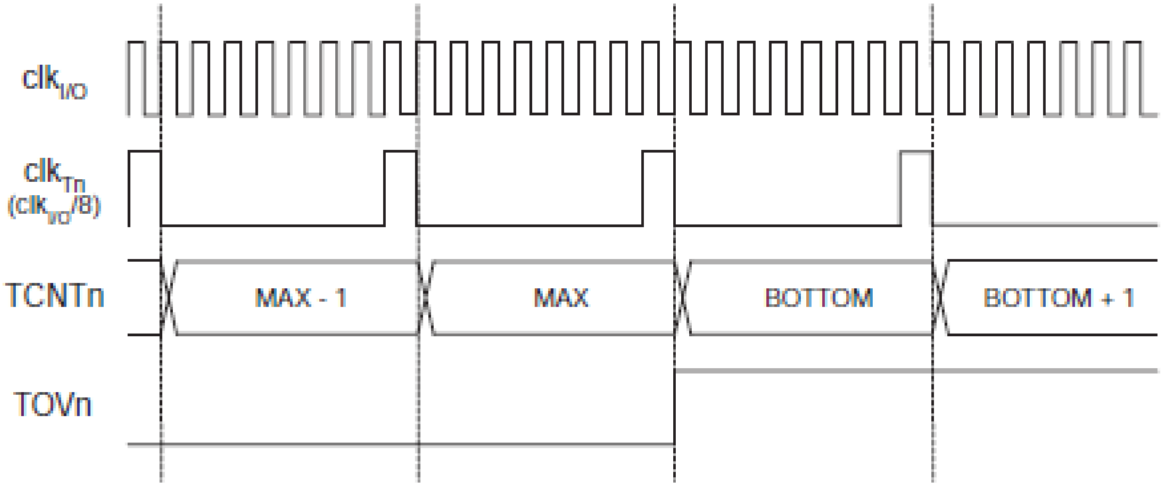


Figure 36 shows the setting of OCF0 in all modes except CTC mode.

Timer Control (Timer0)

TCCRO Timer/Counter 0 Control Register

7	6	5	4	3	2	1	0
FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00

- WGM01:0 Waveform Generation Mode
  - 00 Normal
  - 01 PWM
  - 10 CTC
  - 11 Fast PWM
- Clock Select
  - covered previously
- Compare Match Output Mode
  - 00 Nothing
  - 01 Toggle
  - 10 Clear
  - 11 Set
- Behavior is slightly different in each WG mode

8-bit Timer/Counter Register Description

Timer/Counter Control Register – TCCR0

7	6	5	4	3	2	1	0	
FOC0	WGM00	COM01	COM00	WGM01	CS02	CS01	CS00	TCCR0
W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Force Output Compare

When writing a logical one to the FOC0 bit, an immediate compare match is forced

Compare Output Mode

0	0	Normal port operation, OC0 disconnected.
0	1	Toggle OC0 on compare match
1	0	Clear OC0 on compare match
1	1	Set OC0 on compare match

non-PWM Mode

0	0	0	No clock source (Timer/Counter stopped).
0	0	1	$clk_{I/O}$/(No prescaling)
0	1	0	$clk_{I/O}$/8 (From prescaler)
0	1	1	$clk_{I/O}$/64 (From prescaler)
1	0	0	$clk_{I/O}$/256 (From prescaler)
1	0	1	$clk_{I/O}$/1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge
1	1	1	External clock source on T0 pin. Clock on rising edge.

Normal port operation, OC0 disconnected.
Reserved
Clear OC0 on compare match, set OC0 at TOP
Set OC0 on compare match, clear OC0 at TOP

Fast PWM Mode

Normal port operation, OC0 disconnected.
Reserved
Clear OC0 on compare match when up-counting. Set OC0 on compare match when downcounting.
Set OC0 on compare match when up-counting. Clear OC0 on compare match when downcounting.

Phase Correct PWM Mode

Waveform Generation Mode Bit Description

Mode	WGM01	WGM00	Timer/Counter Mode of Operation	TOP	Update of OCR0	TOV0 Flag Set-on
0	0	0	Normal	0xFF	Immediate	MAX
1	0	1	PWM, Phase Correct	0xFF	TOP	BOTTOM
2	1	0	CTC	OCR0	Immediate	MAX
3	1	1	Fast PWM	0xFF	TOP	MAX

Registers and Flags Associated with Timers

Timer/Counter Register – TCNT0

7	6	5	4	3	2	1	0	
TCNT0[7:0]								TCNT0

Output Compare Register – OCR0

7	6	5	4	3	2	1	0	
OCR0[7:0]								OCR0

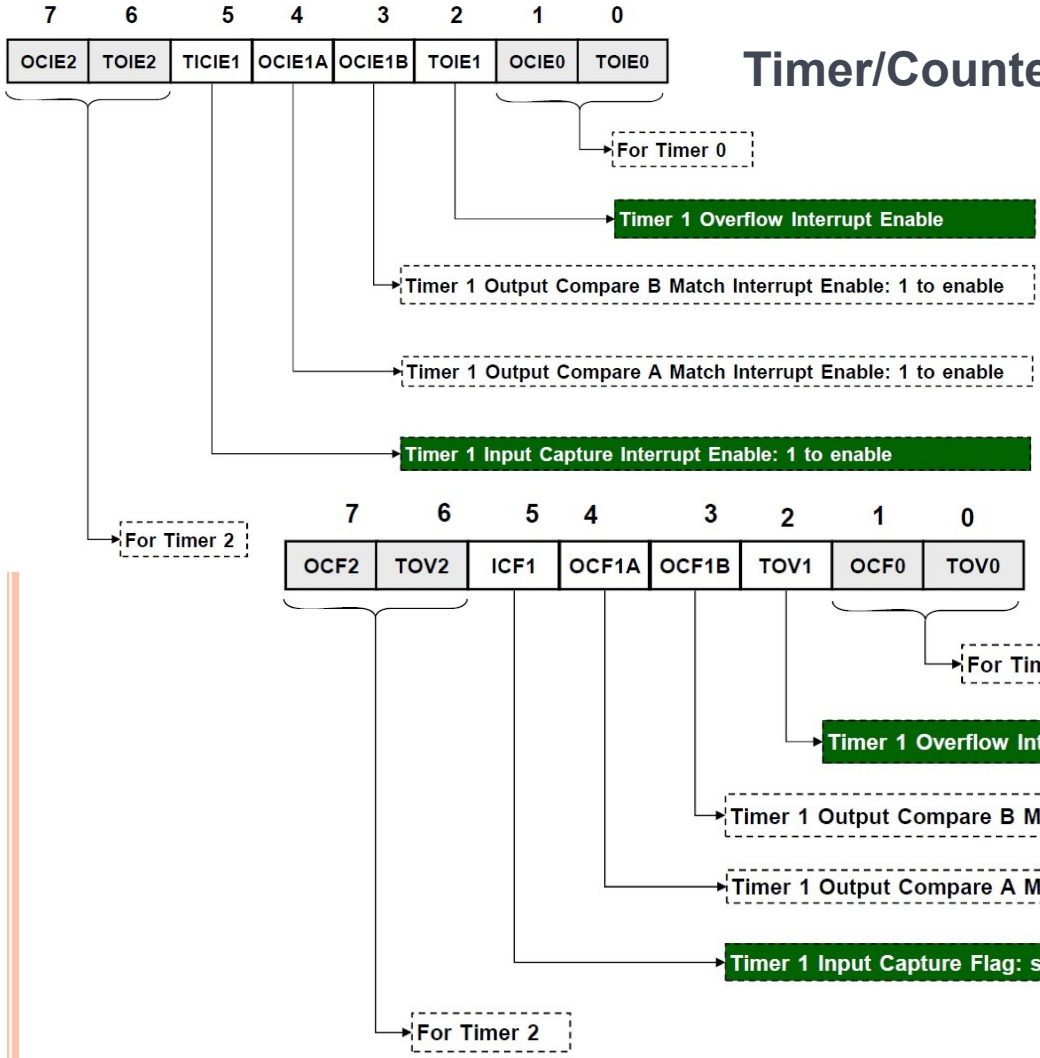
Timer/Counter Interrupt Mask Register – TIMSK

7	6	5	4	3	2	1	0	
OCIE2	TOIE2	TICIE1	OCIE1A	OCIE1B	TOIE1	OCIE0	TOIE0	TIMSK

Timer/Counter Interrupt Flag Register – TIFR

7	6	5	4	3	2	1	0	
OCF2	TOV2	ICF1	OCF1A	OCF1B	TOV1	OCF0	TOV0	TIFR

Registers and Flags Associated with Timers



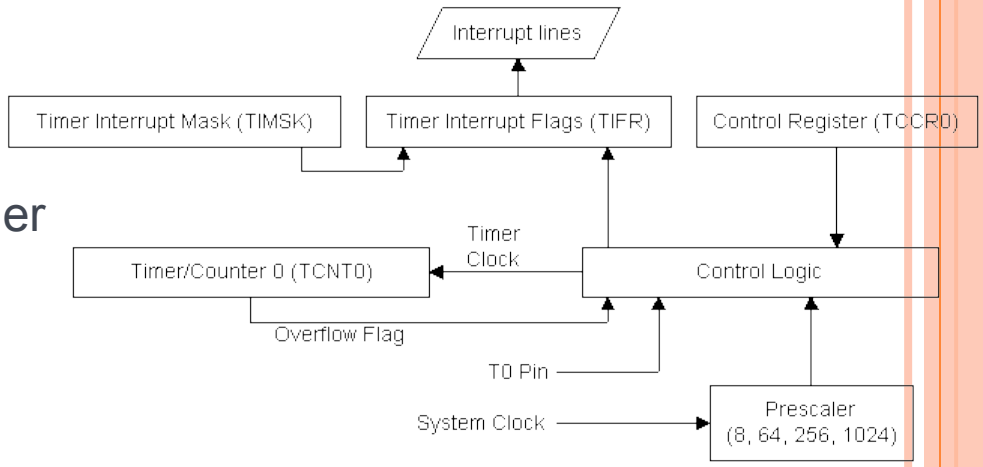
Timer/Counter Interrupt Mask Register (TIMSK)

Timer/Counter Interrupt Flag Register (TIFR)

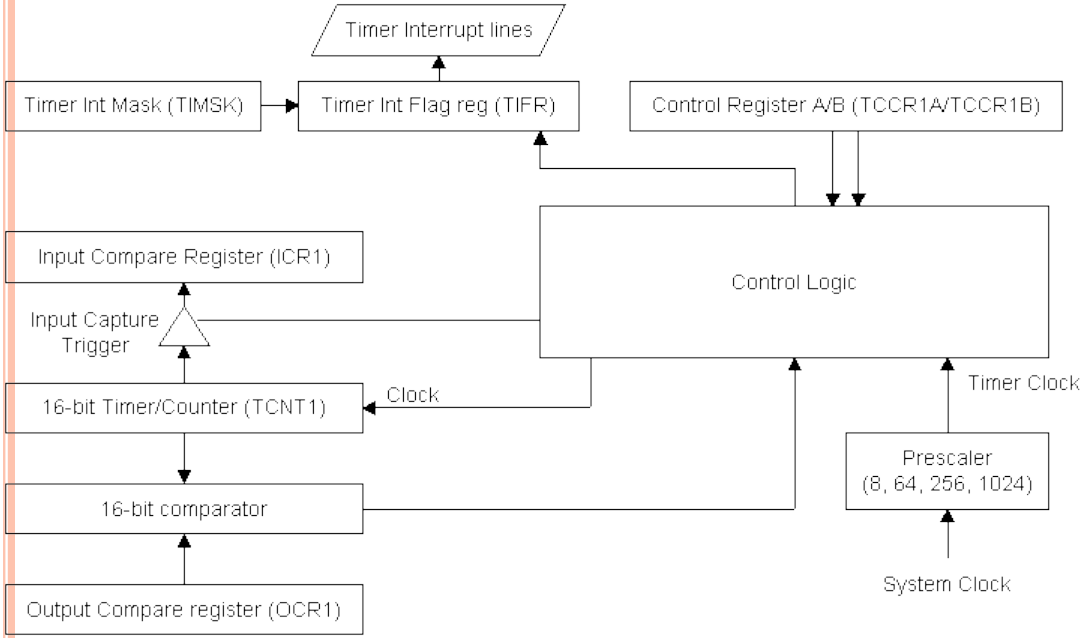
This register has flags that indicate when a timer interrupt occurs.

Timers/Counters

The 8-bit Timer



The 16-bit Timer



Timer 1 Overview

16-bit counter with 10-bit prescaler: 8, 64, 256, and 1024.

Can trigger:
Timer overflow interrupt when counter reaches MAX.

Input capture interrupt when an event occurs on the input capture pin.
- timer value is stored automatically in a register.
- input capture pin for Timer 1 is ICP1 (D.6).

Output compare match interrupt when timer reaches a preset value.
-There are two independent output compare channels A and B.

Timer 1 registers

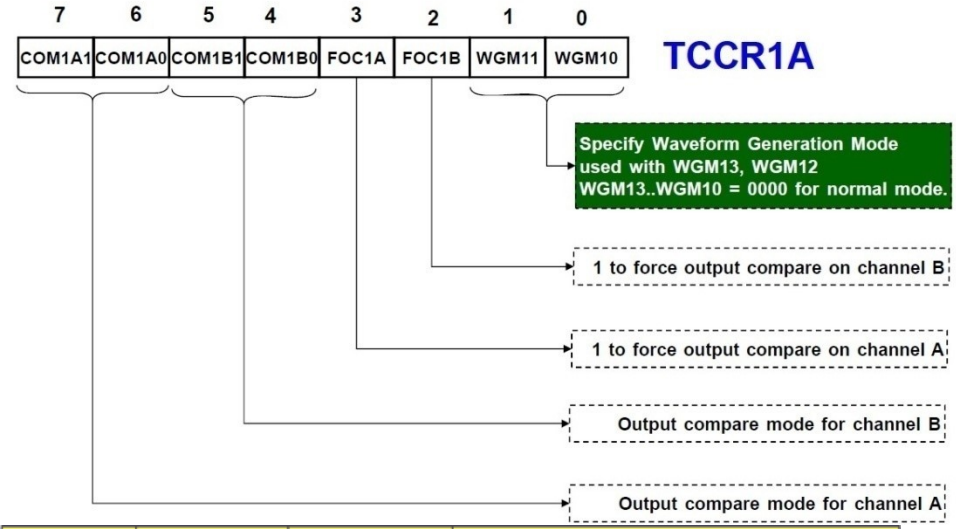
1) Timer/Counter 1 TCNT1: 16-bit register that stores the current value of the timer.
2) Timer/Counter 1 Control Registers TCCR1A and TCCR1B: To configure the operations of Timer 1.
3) Input Capture Register ICR1: To store timer value when an event occurs on input capture pin.
4) Interrupt registers

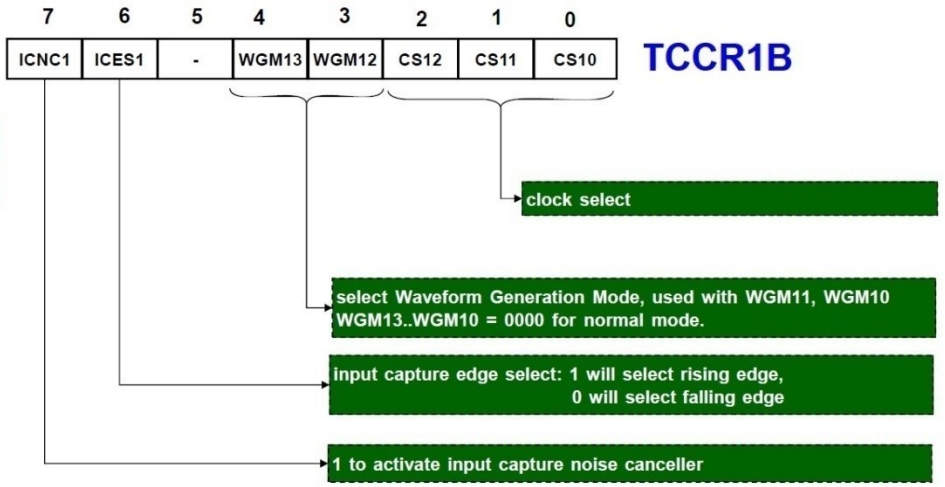
TIMSK: to enable timer interrupts

TIFR to monitor status of timer interrupts.

5) Output Compare Registers OCR1A, OCR1B: To store the preset values for output compare

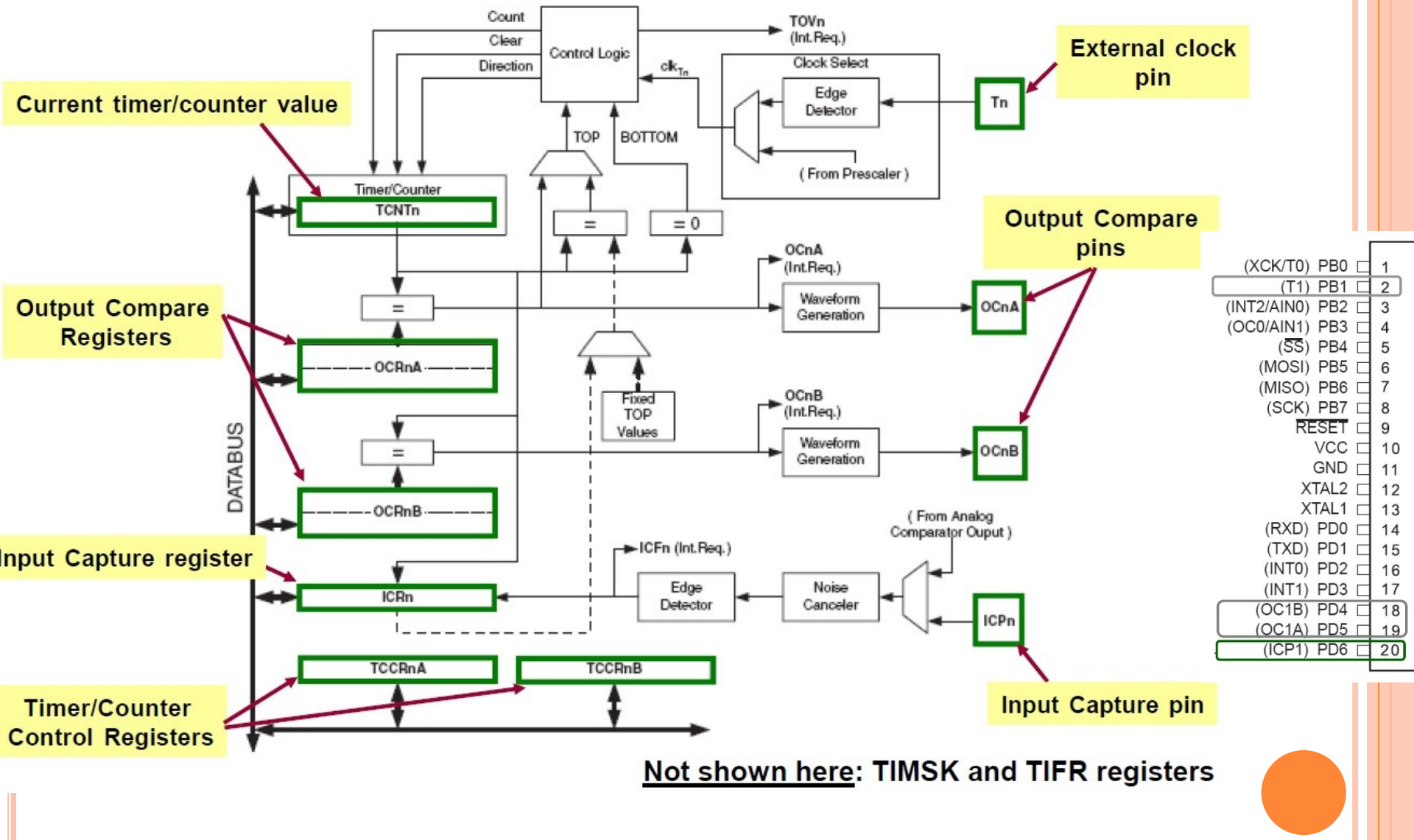
Timer 1 Control Registers





CS12	CS11	CS10	Description
0	0	0	No clock source (Timer/Counter stopped).
0	0	1	clkI/O/1 (No prescaling)
0	1	0	clkI/O/8 (From prescaler)
0	1	1	clkI/O/64 (From prescaler)
1	0	0	clkI/O/256 (From prescaler)
1	0	1	clkI/O/1024 (From prescaler)
1	1	0	External clock source on T1 pin. Clock on falling edge.
1	1	1	External clock source on T1 pin. Clock on rising edge.

TCNT1	16-bit counter register
TCCR1A	Mode of operation and other settings
TCCR1B	Mode of operation, prescaler and other settings
OCR1A	16-bit Compare Register A
OCR1B	16 bit Compare Register B
TIMSK	Interrupt Mask Register
TIFR0	Timer/Counter Interrupt Flag Register



Not shown here: TIMSK and TIFR registers

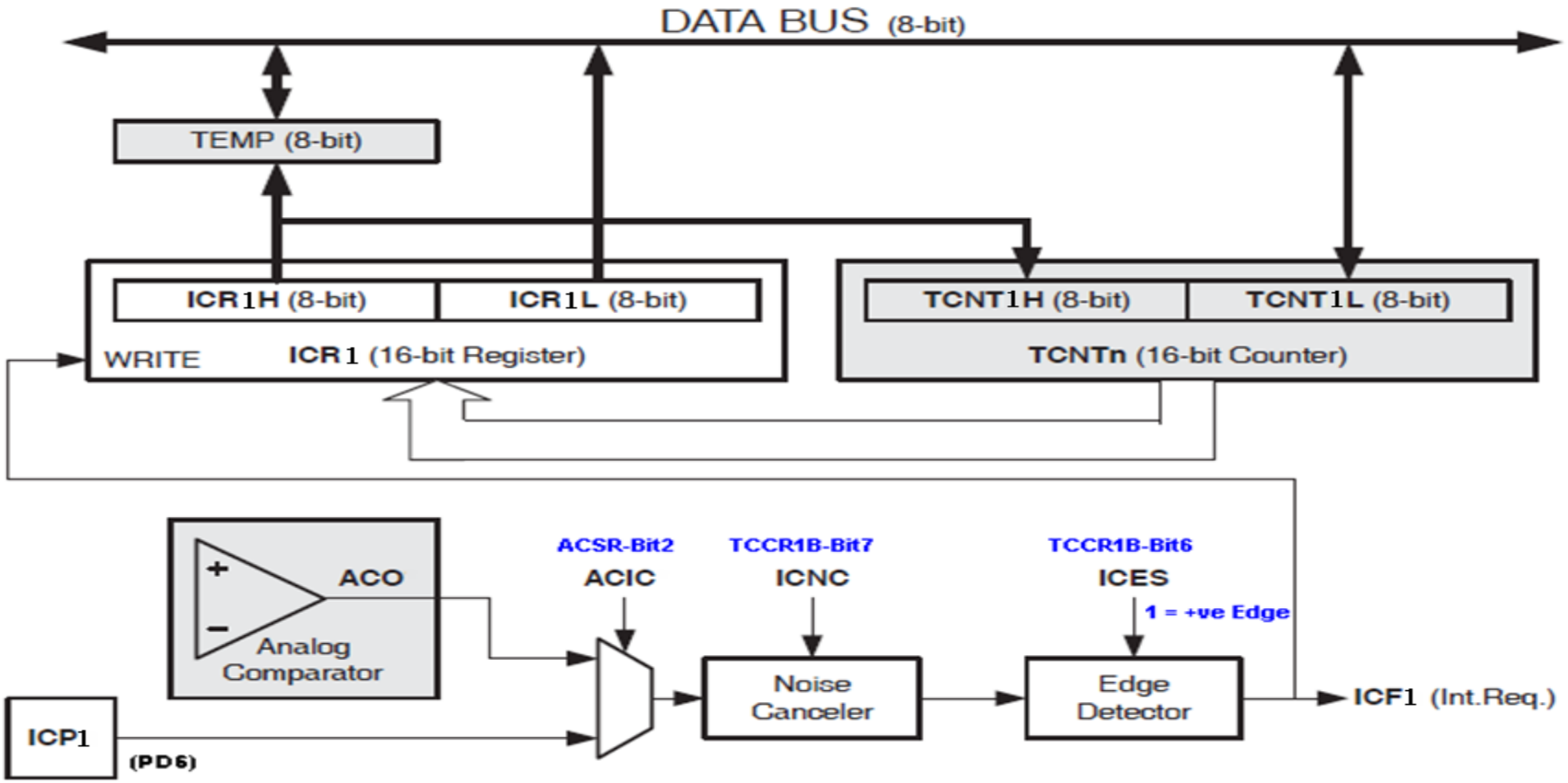
Timer 1 Input Capture

- The input Capture unit captures external events and It writes the 16-bit value of the counter (TCNT1) to the *Input Capture Register* (ICR1), and the *Input Capture Flag* (ICF1) is set.

- The Noise Canceller function requires four successive equal valued samples of the input for changing its output. Its Output is therefore delayed by four Oscillator cycles.

- If enabled, the Input Capture Flag ICF1 generates an Input Capture interrupt.

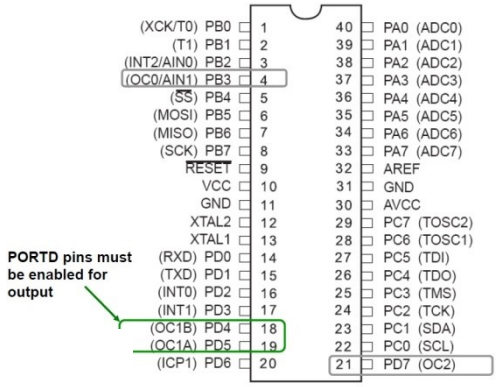
Timer 1 Input Capture

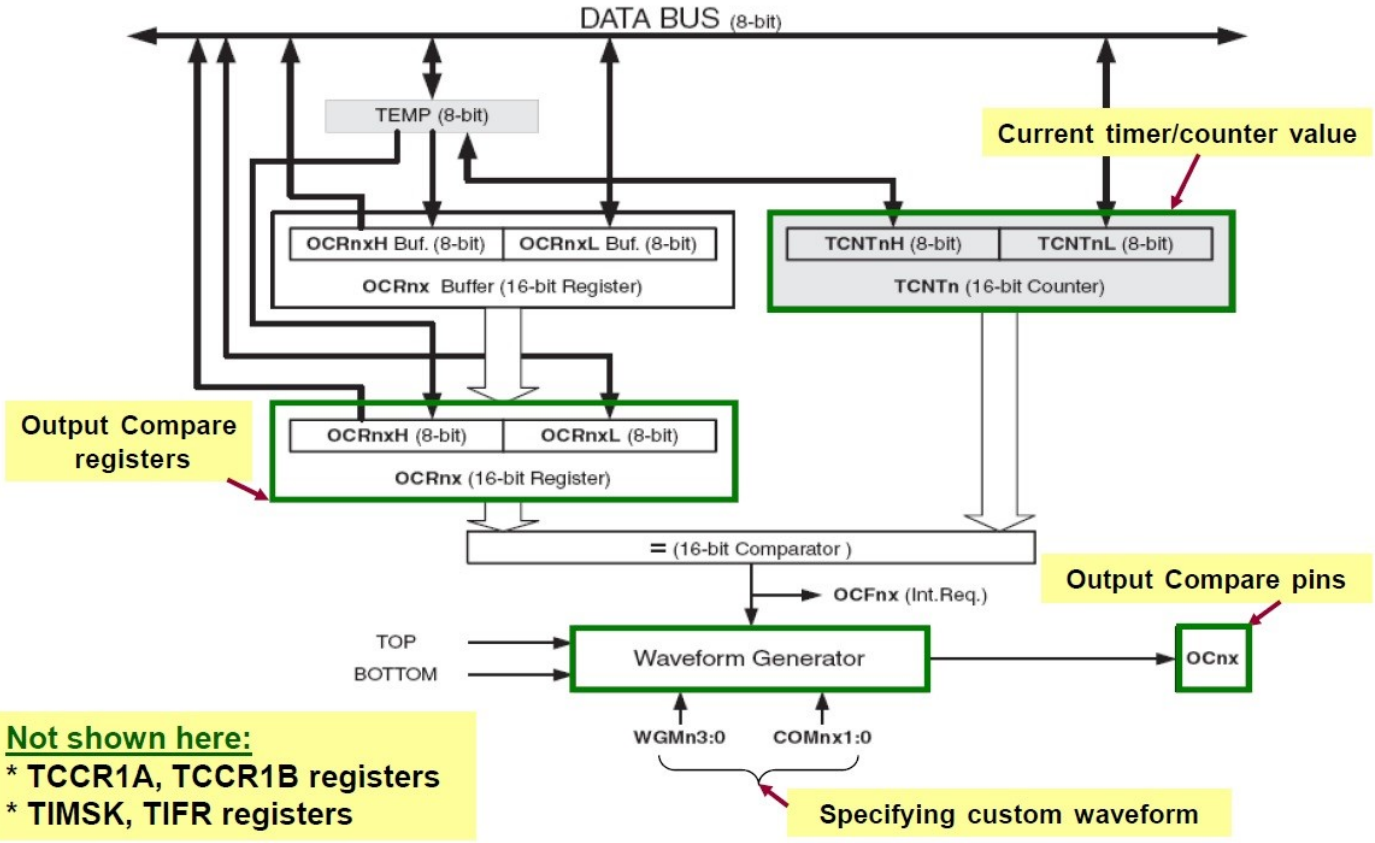


Timer 1 Output Compare

- Timer 1 has two output compare channels: A and B.
- Timer 1 is continuously compared to OCR1A, OCR1B, or a fixed limit.
- When a match occurs, flag OCF1x is set, where x = 'A' or 'B'.
- When a match occurs, Timer 1 can:
- - trigger an output compare interrupt.
- - change output compare pins OC1x.

Timer 1 Output Compare



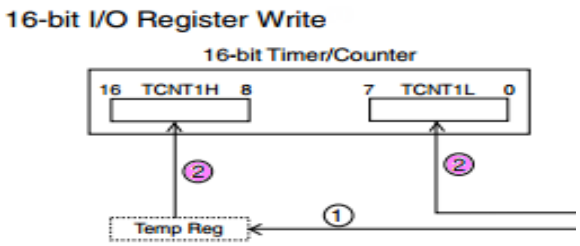


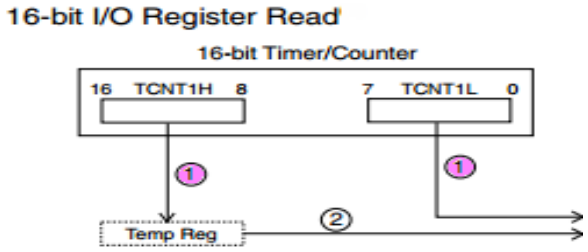
Not shown here:

* TCCR1A, TCCR1B registers
* TIMSK, TIFR registers

Accessing 16-bit Registers (Timer/Counter 1)

- The TCNT1, OCR1A/B, and ICR1 are 16-bit registers.
- The 16-bit register must be byte accessed using two read or write operations.
- A temporary storage register is shared between all 16-bit registers.
- Accessing the Low byte triggers the 16-bit read or write operation. When the Low byte of a 16-bit register is written by the CPU, the High byte stored in the temporary register, and the Low byte written are both copied into the 16-bit register in the same clock cycle.
- Also when the Low byte of a 16-bit register is read by the CPU, the High byte of the 16-bit register is copied into the temporary register in the same clock cycle as the Low byte is read.





Timers Usage through CodeVision Wizard