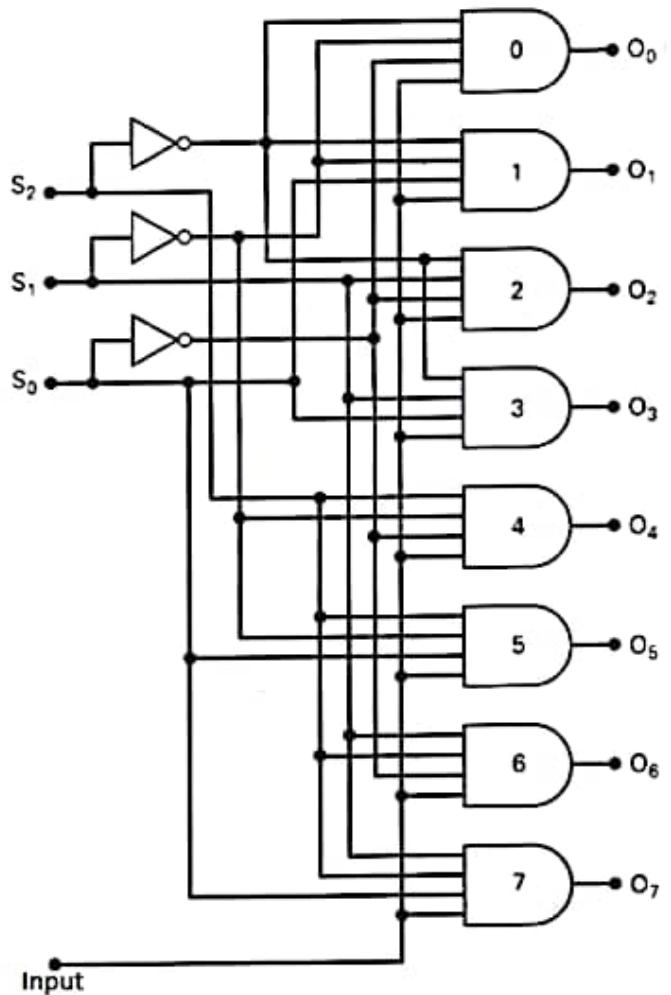


10. The output Q4 of this 1-to-8 demultiplexer is _____



- a) $Q_2.(Q_1)' . Q_0 . I$
- b) $Q_2.Q_1.(Q_0)' . I$
- c) $Q_2.(Q_1)' . (Q_0)' . I$
- d) $Q_2.(Q_1).Q_0 . I$

11. Which IC is used for the implementation of 1-to-16 DEMUX?

- a) IC 74154
- b) IC 74155
- c) IC 74139

CamScanner

30. The flash memory modules designed to replace the functioning of a hard disk is _____

- a) RIMM
- b) FIMM
- c) Flash drives
- d) DIMM

 [View Answer](#)

31. The drawback of building a large memory with DRAM is _____

- a) The Slow speed of operation
- b) The large cost factor
- c) The inefficient memory organisation
- d) All of the mentioned

 [View Answer](#)

32. In a 4M-bit chip organisation has a total of 19 external connections, then it has _____ address if 8 data lines are there.

- a) 2
- b) 5
- c) 9
- d) 8

 [View Answer](#)

33. What does ISO stands for?

- a) International Software Organisation
- b) Industrial Software Organisation
- c) International Standards Organisation
- d) Industrial Standards Organisation

34. The bit used to signify that the cache location is updated is _____

- a) Flag bit
- b) Reference bit
- c) Update bit
- d) Dirty bit

 View Answer

35. During a write operation if the required block is not present in the cache then _____ occurs.

- a) Write miss
- b) Write latency
- c) Write hit
- d) Write delay

 View Answer

36. While using the direct mapping technique, in a 16 bit system the higher order 5 bits are used for _____

- a) Id
- b) Word
- c) Tag
- d) Block

 View Answer

37. The bit used to indicate whether the block was recently used or not is _____

- a) Reference bit
- b) Dirty bit
- c) Control bit
- d) Idol bit

1. Half subtractor is used to perform subtraction of _____

- a) 2 bits
- b) 3 bits
- c) 4 bits
- d) 5 bits

 View Answer

2. For subtracting 1 from 0, we use to take a _____ from neighbouring bits.

- a) Carry
- b) Borrow
- c) Input
- d) Output

 View Answer

3. How many outputs are required for the implementation of a subtractor?

- a) 1
- b) 2
- c) 3
- d) 4

10. The IA-32 system follows which of the following design?

- a) CISC
- b) SIMD
- c) RISC
- d) None of the mentioned

 View Answer

11. Which of the following architecture is suitable for a wide range of data types?

- a) IA-32
- b) ARM
- c) ASUS firebird
- d) 68000

 View Answer

12. In IA-32 architecture along with the general flags, which of the following conditional flags are provided?

- a) TF
- b) IOPL
- c) IF
- d) All of the mentioned

 View Answer

13. The VLIW architecture follows ____ approach to achieve parallelism.

- a) SISD
- b) MIMD
- c) MISD
- d) SIMD

4. If A and B are the inputs of a half adder, the sum is given by _____

- a) A AND B
- b) A OR B
- c) A XOR B
- d) A EX-NOR B

 View Answer

5. If A and B are the inputs of a half adder, the carry is given by _____

- a) A AND B
- b) A OR B
- c) A XOR B
- d) A EX-NOR B

 View Answer

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6. Half-adders have a major limitation in that they cannot _____

- a) Accept a carry bit from a present stage
- b) Accept a carry bit from a next stage
- c) Accept a carry bit from a previous stage
- d) Accept a carry bit from the following stages

 View Answer

7. The difference between half adder and full adder is _____

- a) Half adder has two inputs while full adder has four inputs
- b) Half adder has one output while full adder has two outputs
- c) Half adder has two inputs while full adder has three inputs
- d) All of the Mentioned

13. The memory module obtained by placing a number of flash chips for higher memory storage called as _____

- a) FIMM
- b) SIMM
- c) Flash card
- d) RIMM

 View Answer

14. The flash memory modules designed to replace the functioning of a hard disk is _____

- a) RIMM
- b) Flash drives
- c) FIMM
- d) DIMM

 View Answer

15. The reason for the fast operating speeds of the flash drives is _____

- a) The absence of any movable parts
- b) The integrated electronic hardware
- c) The improved bandwidth connection

8. How many basic binary subtraction operations are possible?

- a) 1
- b) 4
- c) 3
- d) 2

 [View Answer](#)

9. When performing subtraction by addition in the 2's-complement system is?

- a) The minuend and the subtrahend are both changed to the 2's-complement
- b) The minuend is changed to 2's-complement and the subtrahend is left in its original form
- c) The minuend is left in its original form and the subtrahend is changed to its 2's-complement
- d) The minuend and subtrahend are both left in their original form

 [View Answer](#)

10. What are the two types of basic adder circuits?

- a) Sum and carry
- b) Half-adder and full-adder
- c) Asynchronous and synchronous
- d) One and two's-complement

 [View Answer](#)

11. Which of the following is correct for full adders?

- a) Full adders have the capability of directly adding decimal numbers
- b) Full adders are used to make half adders
- c) Full adders are limited to two inputs since there are only two binary digits
- d) In a parallel full adder, the first stage may be a half adder

 [View Answer](#)

12. The selector inputs to an arithmetic/logic unit (ALU) determine the _____

- a) Selection of the IC
- b) Arithmetic or logic function
- c) Data word selection

7. The design of an ALU is based on _____

- a) Sequential logic
- b) Combinational logic
- c) Multiplexing
- d) De-Multiplexing

 View Answer

8. If the two numbers are unsigned, the bit conditions of interest are the ____ carry and a possible ____ result.

- a) Input, zero
- b) Output, one
- c) Input, one
- d) Output, zero

 View Answer

9. If the two numbers include a sign bit in the highest order position, the bit conditions of interest are the sign of the result, a zero indication and _____

- a) An underflow condition
- b) A neutral condition
- c) An overflow condition
- d) One indication

 View Answer

10. The flag bits in an ALU is defined as _____

- a) The total number of registers
- b) The status bit conditions
- c) The total number of control lines
- d) All of the Mentioned

6. Which of the architecture is power efficient?

- RISC
- b) ISA
- c) IANA
- d) CISC

 View Answer

7. What does CSA stands for?

- Computer Service Architecture
- Computer Speed Addition
- c) Carry Save Addition
- d) None of the mentioned

 View Answer

8. If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have _____

- a) Generation word
- b) Exception handling
- Imprecise exceptions
- d) None of the mentioned

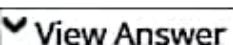
 View Answer

9. To reduce the memory access time we generally make use of _____

- a) SDRAM's
- b) Heaps
- Cache's
- d) Higher capacity RAM's

1. The basic building blocks of the arithmetic unit in a digital computers are _____

- a) Subtractors
- b) Adders
- c) Multiplexer
- d) Comparator

 View Answer

2. A digital system consists of ___ types of circuits.

- a) 2
- b) 3
- c) 4
- d) 5

 View Answer

3. In a combinational circuit, the output at any time depends only on the ___ at that time.

- a) Voltage
- b) Intermediate values
- c) Input values
- d) Clock pulses

4. The difference between the EPROM and ROM circuitry is _____

- a) The usage of MOSFET's over transistors
- b) The usage of JFET's over transistors
- c) The usage of an extra transistor
- d) None of the mentioned

 [View Answer](#)

5. The ROM chips are mainly used to store _____

- a) System files
- b) Root directories
- c) Boot files
- d) Driver files

 [View Answer](#)

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6. The contents of the EPROM are erased by _____

- a) Overcharging the chip
- b) Exposing the chip to UV rays
- c) Exposing the chip to IR rays
- d) Discharging the Chip

 [View Answer](#)

7. The disadvantage of the EPROM chip is _____

- a) The high cost factor
- b) The low efficiency
- c) The low speed of operation
- d) The need to remove the chip physically to reprogram it

8. How many basic binary subtraction operations are possible?

- a) 1
- b) 4
- c) 3
- d) 2

 View Answer

9. When performing subtraction by addition in the 2's-complement system _____

- a) The minuend and the subtrahend are both changed to the 2's-complement
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- d) The minuend and subtrahend are both left in their original form

 View Answer

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 View Answer

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 View Answer

12. The selector inputs to an arithmetic/logic unit (ALU) determine the _____

- a) Selection of the IC
- b) Arithmetic or logic function
- c) Data word selection

8. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?
- a) Actual circuit trial and error evaluation and waveform analysis
 - b) Karnaugh mapping and circuit waveform analysis
 - c) Boolean algebra and Karnaugh mapping
 - d) Boolean algebra and actual circuit trial and error evaluation

 [View Answer](#)

9. Looping on a K-map always results in the elimination of _____
- a) Variables within the loop that appear only in their complemented form
 - b) Variables that remain unchanged within the loop
 - c) Variables within the loop that appear in both complemented and uncomplemented form
 - d) Variables within the loop that appear only in their uncomplemented form

 [View Answer](#)

10. Which of the following expressions is in the sum-of-products form?
- a) $(A + B)(C + D)$
 - b) $(A * B)(C * D)$
 - c) $A * B * (CD)$
 - d) $A * B + C * D$

 [View Answer](#)

11. Which of the following is an important feature of the sum-of-products form of expressions?
- a) All logic circuits are reduced to nothing more than simple AND and OR operations
 - b) The delay times are greatly reduced over other forms
 - c) No signal must pass through more than two gates, not including inverters
 - d) The maximum number of gates that any signal must pass through is reduced by a factor of two

 [View Answer](#)

12. Which of the following expressions is in the product-of-sums form?
- a) $(A + B)(C + D)$
 - b) $(AB)(CD)$
 - c) $AB(CD)$
 - d) $AB + CD$

8. A basic multiplexer principle can be demonstrated through the use of a _____

- a) Single-pole relay
- b) DPDT switch
- c) Rotary switch
- d) Linear stepper

 [View Answer](#)

9. One multiplexer can take the place of _____

- a) Several SSI logic gates
- b) Combinational logic circuits
- c) Several Ex-NOR gates
- d) Several SSI logic gates or combinational logic circuits

 [View Answer](#)

10. The inputs/outputs of an analog multiplexer/demultiplexer are _____

- a) Bidirectional
- b) Unidirectional
- c) Even parity
- d) Binary-coded decimal

 [View Answer](#)

11. If enable input is high then the multiplexer is _____

- a) Enable
- b) Disable
- c) Saturation
- d) High Impedance

14. What does VLIW stands for?

- a) Very Long Instruction Width
- b) Very Large Instruction Word
- c) Very Long Instruction Width
- d) Very Long Instruction Word

 View Answer

15. In CISC architecture most of the complex instructions are stored in ____

- a) CMOS
- b) Register
-  Transistors
- d) Diodes

 View Answer

16. Both the CISC and RISC architectures have been developed to reduce the ____

- a) Time delay
-  Semantic gap
- c) Cost
- d) All of the mentioned

 View Answer

17. ____ are the different type/s of generating control signals.

- a) Hardwired
- b) Micro-instruction
- c) Micro-programmed
-  Both Micro-programmed and Hardwired

4. The observation that a bubbled input OR gate is interchangeable with a bubbled output AND gate is referred to as _____

- a) A Karnaugh map
- b) DeMorgan's second theorem
- c) The commutative law of addition
- d) The associative law of multiplication

 View Answer

5. The systematic reduction of logic circuits is accomplished by _____

- a) Symbolic reduction
- b) TTL logic
- c) Using Boolean algebra
- d) Using a truth table

 View Answer

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6. Each "1" entry in a K-map square represents _____

- A HIGH for each input truth table condition that produces a HIGH output
- b) A HIGH output on the truth table for all LOW input combinations
- c) A LOW output for all possible HIGH input conditions
- d) A DON'T CARE condition for all possible input truth table combinations

 View Answer

7. Each "0" entry in a K-map square represents _____

- a) A HIGH for each input truth table condition that produces a HIGH output
- b) A HIGH output on the truth table for all LOW input combinations
- c) A LOW output for all possible HIGH input conditions
- d) A DON'T CARE condition for all possible input truth table combinations

4. Which of the following is a type of architecture used in the computers nowadays?

- a) Microarchitecture
- b) Harvard Architecture
- c) Von-Neumann Architecture
- d) System Design

 View Answer

5. Which of the following is the subcategories of computer architecture?

- a) Microarchitecture
- b) Instruction set architecture
- c) Systems design
- d) All of the mentioned

8. How many select lines are required for a 1-to-8 demultiplexer?

- a) 2
- b) 3
- c) 4
- d) 5

 [View Answer](#)

9. How many AND gates are required for a 1-to-8 multiplexer?

- a) 2
- b) 6
- c) 8
- d) 15

1. What is computer architecture?

- a) set of categories and methods that specify the functioning, organisation, and implementation of computer systems
- b) set of principles and methods that specify the functioning, organisation, and implementation of computer systems
- c) set of functions and methods that specify the functioning, organisation, and implementation of computer systems
- d) None of the mentioned

 View Answer

2. What is computer organization?

- a) structure and behaviour of a computer system as observed by the user
- b) structure of a computer system as observed by the developer
- c) structure and behaviour of a computer system as observed by the developer
- d) All of the mentioned

 View Answer

3. Which of the following is a type of computer architecture?

- a) Microarchitecture
- b) Harvard Architecture
- c) Von-Neumann Architecture
- d) All of the mentioned

1. What is a multiplexer?

- a) It is a type of decoder which decodes several inputs and gives one output
- b) A multiplexer is a device which converts many signals into one
- c) It takes one input and results into many output
- d) It is a type of encoder which decodes several inputs and gives one output

 View Answer

2. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?

- a) Data Selector
- b) Data distributor
- c) Both data selector and data distributor
- d) DeMultiplexer

 View Answer

3. It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of _____

- a) Inputs
- b) Outputs
- c) Selection lines
- d) Enable lines

8. EEPROM stands for Electrically Erasable Programmable Read Only Memory.

- True
- b) False

 [View Answer](#)

9. The disadvantage of the EEPROM is/are _____

- The requirement of different voltages to read, write and store information
- b) The Latency read operation
- c) The inefficient memory mapping schemes used
- d) All of the mentioned

 [View Answer](#)

10. The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____

- a) Memory sticks
- b) Blue-ray devices
- c) Flash memory
- d) CMOS

 [View Answer](#)

11. The only difference between the EEPROM and flash memory is that the latter doesn't allow bulk data to be written.

- True
- b) False

 [View Answer](#)

12. The flash memories find application in _____

- a) Super computers
- b) Mainframe systems
- c) Distributed systems
- d) Portable devices

4. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is _____

- Ex-NOR gate
- OR gate
- Ex-OR gate
- NAND gate

 [View Answer](#)

5. What is the first thing you will need if you are going to use a macro-function?

- A complicated design project
- An experienced design engineer
- Good documentation
- Experience in HDL

 [View Answer](#)

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6. What is the major difference between half-adders and full-adders?

- Full-adders are made up of two half-adders
- Full adders can handle double-digit numbers
- Full adders have a carry input capability
- Half adders can handle only single-digit numbers

 [View Answer](#)

7. The binary subtraction of $0 - 0 = ?$

- Difference = 0, borrow = 0
- Difference = 1, borrow = 0
- Difference = 1, borrow = 1
- Difference = 0, borrow = 1

10. 3 bits full adder contains _____

- a) 3 combinational inputs
- b) 4 combinational inputs
- c) 6 combinational inputs
- d) 8 combinational inputs

1. In parts of the processor, adders are used to calculate _____

- a) Addresses
- b) Table indices
- c) Increment and decrement operators
- d) All of the Mentioned

 View Answer

2. Total number of inputs in a half adder is _____

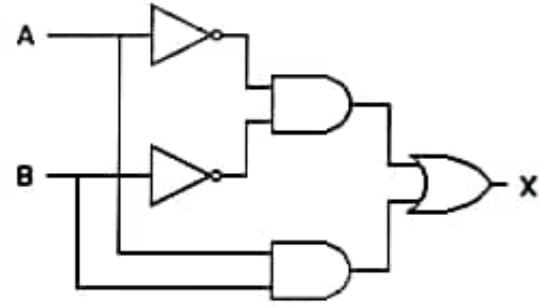
- a) 2
- b) 3
- c) 4
- d) 1

 View Answer

3. In which operation carry is obtained?

- a) Subtraction
- b) Addition
- c) Multiplication
- d) Both addition and subtraction

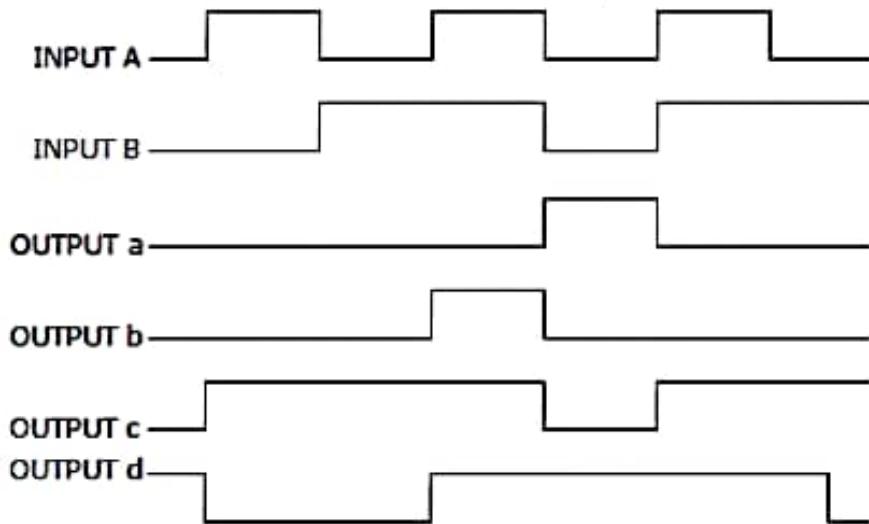
4. What type of logic circuit is represented by the figure shown below?



- a) XOR
- b) XNOR
- c) AND
- d) XAND

 View Answer

5. For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?



- a)
- b) c
- c) d
- d) b

4. In 1-to-4 demultiplexer, how many select lines are required?

- a) 2
- b) 3
- c) 4
- d) 5

 View Answer

5. In a multiplexer the output depends on its _____

- a) Data inputs
- b) Select inputs
- c) Select outputs
- d) Enable pin

 View Answer

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6. In 1-to-4 multiplexer, if $C1 = 0$ & $C2 = 1$, then the output will be _____

- a) Y0
- b) Y1
- c) Y2
- d) Y3

 View Answer

7. In 1-to-4 multiplexer, if $C1 = 1$ & $C2 = 1$, then the output will be _____

- a) Y0
- b) Y1
- c) Y2
- d) Y3

4. Which is the major functioning responsibility of the multiplexing combinational circuit?

- a) Decoding the binary information
- b) Generation of all minterms in an output function with OR-gate
- c) Generation of selected path between multiple sources and a single destination
- d) Encoding of binary information

 View Answer

5. What is the function of an enable input on a multiplexer chip?

- a) To apply Vcc
- b) To connect ground
- c) To active the entire chip
- d) To active one half of the chip

 View Answer

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6. One multiplexer can take the place of _____

- a) Several SSI logic gates
- b) Combinational logic circuits
- c) Several Ex-NOR gates
- d) Several SSI logic gates or combinational logic circuits

 View Answer

7. A digital multiplexer is a combinational circuit that selects _____

- c) One digital information from several sources and transmits the selected one
- b) Many digital information and convert them into one
- c) Many decimal inputs and transmits the selected information
- d) Many decimal outputs and accepts the selected information

4. In a sequential circuit, the output at any time depends only on the input values at that time.

- a) Past output values
- b) Intermediate values
- c) Both past output and present input
- d) Present input values

 View Answer

5. Procedure for the design of combinational circuits are:

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- A. From the word description of the problem, identify the inputs and outputs and draw a block diagram.
- B. Draw the truth table such that it completely describes the operation of the circuit for different combinations of inputs.
- C. Simplify the switching expression(s) for the output(s).
- D. Implement the simplified expression using logic gates.
- E. Write down the switching expression(s) for the output(s).

- a) B, C, D, E, A
- b) A, D, E, B, C
- c) A, B, E, C, D
- d) B, A, E, C, D

 View Answer

6. All logic operations can be obtained by means of _____

- a) AND and NAND operations
- b) OR and NOR operations
- c) OR and NOT operations
- d) NAND and NOR operations

1. If the transistor gate is closed, then the ROM stores a value of 1.

a) True

False

 View Answer

2. PROM stands for _____

 Programmable Read Only Memory

b) Pre-fed Read Only Memory

c) Pre-required Read Only Memory

d) Programmed Read Only Memory

 View Answer

3. The PROM is more effective than ROM chips in regard to _____

a) Cost

b) Memory management

c) Speed of operation

 Both Cost and Speed of operation

1. 4 to 1 MUX would have _____

- a) 2 inputs
- b) 3 inputs
- c) 4 inputs
- d) 5 inputs

 [View Answer](#)

2. The two input MUX would have _____

- a) 1 select line
- b) 2 select lines
- c) 4 select lines
- d) 3 select lines

 [View Answer](#)

3. A combinational circuit that selects one from many inputs are _____

- a) Encoder
- b) Decoder
- c) Demultiplexer
- d) Multiplexer

4. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is _____

- a) Ex-NOR gate
- b) OR gate
- c) Ex-OR gate
- d) NAND gate

 [View Answer](#)

5. What is the first thing you will need if you are going to use a macro-function?

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- b) An experienced design engineer
- c) Good documentation
- d) Experience in HDL

 [View Answer](#)

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6. What is the major difference between half-adders and full-adders?

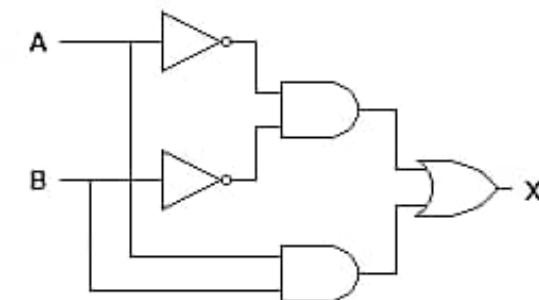
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- b) Full adders can handle double-digit numbers
- c) Full adders have a carry input capability
- d) Half adders can handle only single-digit numbers

 [View Answer](#)

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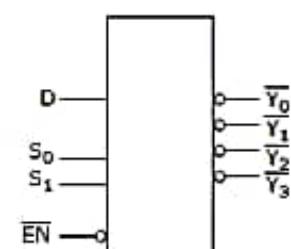
2. Which of the following logic expressions represents the logic diagram shown?



- a) $X=AB'+A'B$
- b) $X=(AB)'+AB$
- c) $X=(AB)'+A'B'$
- d) $X=A'B'+AB$

 View Answer

3. The device shown here is most likely a _____



- a) Comparator
- b) Multiplexer
- c) Inverter
- d) Demultiplexer

1. Why is a demultiplexer called a data distributor?

- a) The input will be distributed to one of the outputs
- b) One of the inputs will be selected for the output
- c) The output will be distributed to one of the inputs
- d) Single input gives single output

 View Answer

2. Most demultiplexers facilitate which type of conversion?

- a) Decimal-to-hexadecimal
- b) Single input, multiple outputs
- c) AC to DC
- d) Odd parity to even parity

 View Answer

3. In 1-to-4 demultiplexer, how many select lines are required?

- a) 2
- b) 3
- c) 4
- d) 5

22. Which of the following is the fullform of CISC?

- a) Complex Instruction Sequential Compilation
- b) Complete Instruction Sequential Compilation
- c) Computer Integrated Sequential Compiler
- d) Complex Instruction Set Computer

 View Answer

23. The reason for the cells to lose their state over time is _____

- a) Use of Shift registers
- b) The lower voltage levels
- c) Usage of capacitors to store the charge
- d) None of the mentioned

 View Answer

24. In order to read multiple bytes of a row at the same time, we make use of _____

- a) Memory extension
- b) Cache
- c) Shift register
- d) Latch

 View Answer

25. The difference in the address and data connection between DRAM's and SDRAM's is _____

- a) The requirement of more address lines in SDRAM's
- b) The usage of a buffer in SDRAM's
- c) The usage of more number of pins in SDRAM's
- d) None of the mentioned

1. The word demultiplex means _____

- a) One into many
- b) Many into one
- c) Distributor
- d) One into many as well as Distributor

 [View Answer](#)

2. Why is a demultiplexer called a data distributor?

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 [View Answer](#)

3. Most demultiplexers facilitate which type of conversion?

- a) Decimal-to-hexadecimal
- b) Single input, multiple outputs
- c) AC to DC
- d) Odd parity to even parity

i. 4 to 1 MUX would have _____

- 1 output
- 2 outputs
- 3 outputs
- 4 outputs

 [View Answer](#)

ii. Which of the following circuit can be used as parallel to serial converter?

- Multiplexer
- Demultiplexer
- Decoder
- Digital counter

 [View Answer](#)

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iii. A combinational circuit is one in which the output depends on the _____

- Input combination at the time
- Input combination and the previous output
- Input combination at that time and the previous input combination
- Present output and the previous output

 [View Answer](#)

iv. Without any additional circuitry an 8:1 MUX can be used to obtain _____

- Some but not all Boolean functions of 3 variables
- All function of 3 variables but none of 4 variables
- All functions of 3 variables and some but not all of 4 variables
- All functions of 4 variables

26. The chip can be disabled or cut off from an external connection using ____

- a) ACPT
- b) RESET
- c) LOCK
- d) Chip select

 [View Answer](#)

27. The controller multiplexes the addresses after getting the ____ signal.

- a) INTR
- b) ACK
- c) RESET
- d) Request

 [View Answer](#)

28. The data is transferred over the RAMBUS as ____

- a) Blocks
- b) Swing voltages
- c) Bits
- d) Packets

 [View Answer](#)

29. The memory devices which are similar to EEPROM but differ in the cost effectiveness is ____

- a) CMOS
- b) Memory sticks
- c) Blue-ray devices
- d) Flash memory

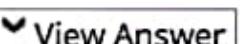
8. If A, B and C are the inputs of a full adder then the sum is given by _____

- a) A AND B AND C
- b) A OR B AND C
- c) A XOR B XOR C
- d) A OR B OR C

 View Answer

9. If A, B and C are the inputs of a full adder then the carry is given by _____

- a) A AND B OR (A OR B) AND C
- b) A OR B OR (A AND B) C
- c) (A AND B) OR (A AND B)C
- d) A XOR B XOR (A XOR B) AND C

 View Answer

10. How many AND, OR and EXOR gates are required for the configuration of full adder?

- a) 1, 2, 2
- b) 2, 1, 2
- c) 3, 1, 2
- d) 4, 0, 1

4. In a multiplexer the output depends on its _____

- a) Data inputs
- b) Select inputs
- c) Select outputs
- d) Enable pin

 [View Answer](#)

5. In 1-to-4 multiplexer, if $C_1 = 1$ & $C_2 = 1$, then the output will be _____

- a) Y_0
- b) Y_1
- c) Y_2
- d) Y_3

 [View Answer](#)

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6. How many select lines are required for a 1-to-8 demultiplexer?

- a) 2
- b) 3
- c) 4
- d) 5

 [View Answer](#)

7. How many AND gates are required for a 1-to-8 multiplexer?

- a) 2
- b) 6
- c) 8
- d) 16

18. If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation).

- a) 2
- b) -1
- c) -7
- d) 2

 View Answer

19. The small extremely fast, RAM's all called as _____

- a) Heaps
- b) Accumulators
- c) Stacks
- d) Cache

 View Answer

20. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?

- a) ANSA
- b) Super-scalar
- c) ISA
- d) All of the mentioned

 View Answer

21. What is the full form of ISA?

- a) Industry Standard Architecture
- b) International Standard Architecture
- c) International American Standard
- d) None of the mentioned

 View Answer

1. Controlled inverter is also known as _____

- a) Controlled buffer
- b) NOT gate
- c) Both controlled buffer and NOT gate
- d) Controlled gate

 [View Answer](#)

2. Why XOR gate is called an inverter?

- a) Because of the same input
- b) Because of the same output
- c) It behaves like a NOT gate
- d) It behaves like a AND gate

 [View Answer](#)

3. Controlled buffers can be useful _____

- a) To control the circuit's output into the bus
- b) In comparison of component's output with its input
- c) In increasing the output from its low input
- d) All of the Mentioned

8. In a multiplexer, the selection of a particular input line is controlled by _____

- a) Data controller
- b) Selected lines
- c) Logic gates
- d) Both data controller and selected lines

 View Answer

9. If the number of n selected input lines is equal to 2^m then it requires ____ select lines.

- a) 2
- b) m
- c) n
- d) 2^n

 View Answer

10. How many select lines would be required for an 8-line-to-1-line multiplexer?

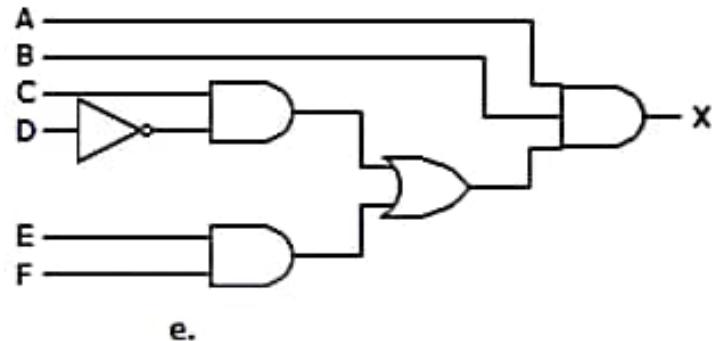
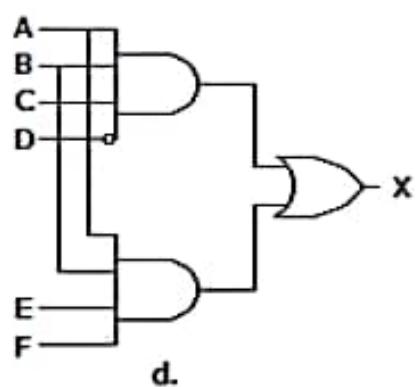
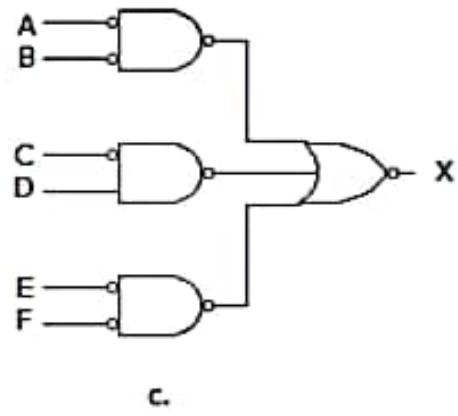
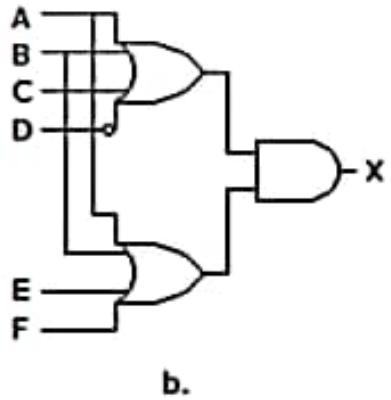
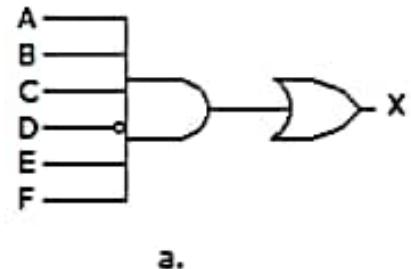
- a) 2
- b) 4
- c) 8
- d) 3

 View Answer

11. A basic multiplexer principle can be demonstrated through the use of a _____

- a) Single-pole relay
- b) DPDT switch
- c) Rotary switch
- d) Linear stepper

i. Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?



- i) a
- ii) b
- iii) c
- iv) d

12. What is data routing in a multiplexer?

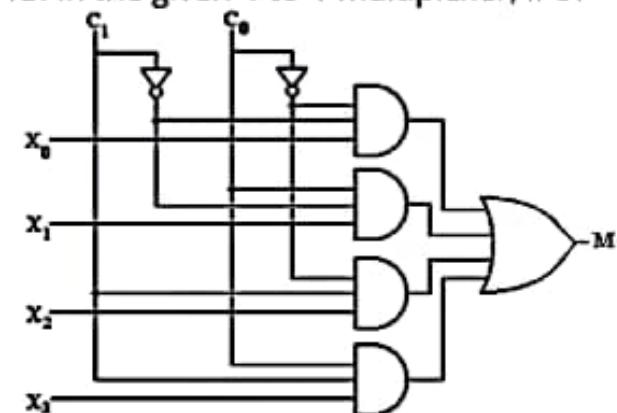
- a) It spreads the information to the control unit
 - b) It can be used to route data from one of several source to destination
 - c) It is an application of multiplexer
- It can be used to route data and it is an application of multiplexer

12. How many NOT gates are required for the construction of a 4-to-1 multiplexer?

- a) 3
- b) 4
- c) 2
- d) 5

 View Answer

13. In the given 4-to-1 multiplexer, if $c_1 = 0$ and $c_0 = 1$ then the output M is _____



- a) X0
- b) X1
- c) X2
- d) X3

 View Answer

14. The enable input is also known as _____

- a) Select input
- b) Decoded input
- c) Strobe
- d) Sink

3. Which of the following combinations of logic gates can decode binary 1101?

- a) One 4-input AND gate
- b) One 4-input AND gate, one inverter
- c) One 4-input AND gate, one OR gate
- d) One 4-input NAND gate, one inverter

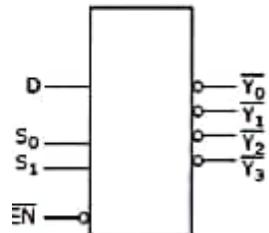
 View Answer

7. What is the indication of a short to ground in the output of a driving gate?

- a) Only the output of the defective gate is affected
- b) There is a signal loss to all load gates
- c) The node may be stuck in either the HIGH or the LOW state
- d) The affected node will be stuck in the HIGH state

 View Answer

8. For the device shown here, assume the D input is LOW, both S inputs are LOW and the EN input is LOW. What is the status of the Y' outputs?



- i) All are HIGH
- ii) All are LOW
- iii) All but Y0 are LOW
- iv) All but Y0 are HIGH

 View Answer

9. The carry propagation can be expressed as _____

- i) $C_p = AB$
- ii) $C_p = A + B$
- iii) All but Y0 are LOW
- iv) All but Y0 are HIGH

7. What does minuend and subtrahend denotes in a subtractor?

- a) Their corresponding bits of input
- b) Its outputs
- c) Its inputs
- d) Borrow bits

 [View Answer](#)

8. Full subtractor is used to perform subtraction of _____

- a) 2 bits
- b) 3 bits
- c) 4 bits
- d) 8 bits

 [View Answer](#)

9. The full subtractor can be implemented using _____

- a) Two XOR and an OR gates
- b) Two half subtractors and an OR gate
- c) Two multiplexers and an AND gate
- d) Two comparators and an AND gate

 [View Answer](#)

10. The output of a subtractor is given by (if A, B and X are the inputs).

- a) A AND B XOR X
- b) A XOR B XOR X
- c) A OR B NOR X
- d) A NOR B XOR X

1. Which statement below best describes a Karnaugh map?

- a) It is simply a rearranged truth table
- b) The Karnaugh map eliminates the need for using NAND and NOR gates
- c) Variable complements can be eliminated by using Karnaugh maps
- d) A Karnaugh map can be used to replace Boolean rules

 View Answer

2. Which of the examples below expresses the commutative law of multiplication?

- a) $A + B = B + A$
- b) $A \cdot B = B + A$
- c) $A \cdot (B \cdot C) = (A \cdot B) \cdot C$
- d) $A \cdot B = B \cdot A$

 View Answer

3. The Boolean expression $Y = (AB)'$ is logically equivalent to what single gate?

- a) NAND
- b) NOR
- c) AND
- d) OR

4. Let the input of a subtractor is A and B then what the output will be if $A = B$?

- a) 0
- b) 1
- c) A
- d) B

 View Answer

5. Let A and B is the input of a subtractor then the output will be _____

- a) A XOR B
- b) A AND B
- c) A OR B
- d) A EXNOR B

 View Answer

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6. Let A and B is the input of a subtractor then the borrow will be _____

- a) A AND B'
- b) A' AND B
- c) A OR B
- d) A AND B

11. The output of a full subtractor is same as _____

- a) Half adder
- b) Full adder
- c) Half subtractor
- d) Decoder

 [View Answer](#)

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