

- (١) حيازة التليفون المحمول مفتوحا داخل لجنة الامتحان يعتبر حالة غش تستوجب العقاب وإذا كان من الضروري الدخول بالمحمول فيوضع مغلق في الحقيبة .
 (٢) لا يسمح بدخول سماعة الاذن أو البلوتوث أو الآلة الحاسبة .
 (٣) لا يسمح بدخول كتب أو ملازم أو أوراق داخل اللجنة والمخالفة تعتبر حالة غش .
 (٤) يمكنك استخدام ظهر الورقة الاخير من ورق الاسئلة كمسودة لحل الاسئلة التي تحتاج الي مسودة لاختيار المناسب لها من الاجابات .

Question (1):

Choose the correct answer from A, B, C or D :

- The decoder is an example of which type of Boolean circuit ?
 A. Sequential B. Combinational C. Moore machine D. Analog
- An 9-input XOR circuit has an output $Y = 0$.Which input combination below is correct ?
 A. 110111100 B. 110111000 C. 111100111 D. 100011101
- If the decimal number is a integer then its octal equivalent is obtained by _____ the number continuously by 8 and collecting the remainders.
 A. Dividing B. Multiplying C. Subtracting D. Adding
- The representation of octal number $(410)_8$ in decimal is _____
 A. $(264)_{10}$ B. $(410)_{10}$ C. $(462)_{10}$ D. $(409)_{10}$
- The binary equivalent of the decimal number $(100)_{10}$ is _____
 A. $(1100100)_2$ B. $(0010011)_2$ C. $(0010111)_2$ D. $(1100101)_2$
- Representation of hexadecimal number (CE)₁₆ in decimal:
 A. $12 * 16^1 + 14 * 16^0$ B. $13 * 16^1 + 13 * 16^0$ C. $12 * 16^0 + 14 * 16^1$ D. $14 * 16^1 + 15 * 16^0$
- Convert binary to octal: $(111111100011)_2 = ?$
 A. $(6643)_8$ B. $(7743)_8$ C. $(5543)_8$ D. $(6634)_8$
- $(250)_{10}$ is equivalent to _____
 A. $(FD)_{16}$ B. $(DF)_{16}$ C. $(FA)_{16}$ D. $(AF)_{16}$
- The given hexadecimal number $(3C)_{16}$ is equivalent to _____
 A. $(740)_8$ B. $(74)_8$ C. $(47)_8$ D. $(35)_8$
- What is the addition result of the binary numbers 1100110011 and 1011100111?
 A. 0111001000 B. 11100011010 C. 11000011010 D. None

11. Perform binary subtraction by using 2's complement : $110111 - 100101 = ?$
 A. 110100 B. 1010100 C. 010100 ~~D. None~~
12. What is the addition result of the hexadecimal numbers 32FA and 1F1B = ?
~~A. 5215~~ B. 5125 C. 1255 D. None
13. Perform binary subtraction by using 10's complement : $3F - FF = ?$
 A. -192 B. +192 C. +291 ~~D. None~~
14. If we add -50 and +30 using 2's complement, we get _____
 A. -10100 B. -110100 C. 00101 D. None
15. In boolean algebra, the OR operation is performed by which properties?
 A. Associative properties C. Commutative properties
 B. Distributive properties D. All of the Mentioned
16. The decimal equivalent of the excess-3 number 101110000011 is _____
 A. 850 B. 1183 C. 580 D. 1150
17. The expression for Absorption law is given by _____
 A. $A + B = B + A$ B. $A + AB = B$ C. $AB + AA' = A$ D. $AB + ABCD = AB$
18. DeMorgan's theorem states that _____
 A. $A' + B' = A'B'$ B. $(AB)' = A' + B$ C. $(AB)' = A' + B'$ D. $(A + B)' = A' * B$
19. The boolean function $X + YZ$ is a reduced form of _____
 A. $XY + YZ$ B. $X'Y + XY'Z$ C. $(X + Y)(X + Z)$ D. $(X + Z)Y$
20. The expression $F = XY + YZ + XZ$ shows the _____ operation.
 A. SOP B. EX-OR C. POS D. NOR
21. The canonical sum of product form of the function $F(X, Y) = X + Y$ is _____
 A. $XY + YY + X'X$ B. $XY + XY' + X'Y$ C. $YX + YX' + X'Y'$ D. $XY' + X'Y + X'Y'$
22. The output of an EX-NOR gate is 0. Which input combination is correct?
 A. $A = 0, B = 0$ B. $A = 1, B = 1$ C. $A' = 1, B' = 1$ D. $A = 1, B = 0$
23. The number of full and half adders are required to add 18-bit number is _____
 A. 1 half adders, 17 full adders C. 18 half adders, 0 full adders
 B. 9 half adders, 9 full adders D. 4 half adders, 14 full adders
24. The following switching functions are to be implemented using a decoder: $f_1 = \sum m(1, 2, 4)$
 $f_2 = \sum m(2, 3)$ $f_3 = \sum m(2, 4, 5, 6, 7)$ The minimum configuration of decoder will be...
 A. 2 to 4 line B. 4 to 16 line ~~C. 3 to 8 line~~ D. 5 to 32 line
25. How many two-input OR and AND gates are required to realize $Y = CD + EF + G$?
 A. 3, 2 B. 3, 3 C. 2, 3 D. 2, 2
26. In Figure 4, the equation S in the numareical form is
 A. $S(x, y, z) = \sum(2, 4, 7)$ C. $S(x, y, z) = \sum(1, 2, 4, 5, 7)$
 B. $S(x, y, z) = \sum(1, 2, 4, 7)$ D. $S(x, y, z) = \sum(1, 2, 6, 7)$

27. If B and A are the inputs of a half adder, the sum is given by
 A. A AND B B. B OR A C. B XOR A D. A EX-NOR B
28. Which circuit in figure 1 (a to d) is the sum-of-products implementation?
 A. b B. a C. d D. c
29. For a two-input XNOR gate, with the input waveforms as shown in figure 2, which output waveform is correct?
 A. d B. c C. a D. b
30. Which of the following combinations of logic gates can decode binary 1001?
 A. (One 4-input AND gate) C. (One 4-input AND gate, two OR gate)
 B. (One 4-input AND gate, two inverter) D. (One 4-input NAND gate, two inverter)
31. In figure 3, which figure is Implement the following Boolean function with NAND gates:
 $F(x, y, z) = (1, 2, 3, 4, 5, 7)$
 A. a B. c C. b D. None
32. Simplify the following Boolean function F, together with the don't-care conditions d, when $F(A, B, C, D) = \sum(0, 6, 8, 13, 14)$ and $d(A, B, C, D) = \sum(2, 4, 10)$, the simplified function in sum-of-minterms form is-----
 A. $F = (B'D' + CD' + ABC'D)$ C. $F = (B'D' + CD' + AB'C'D)$
 B. $F = (B'D' + C'D' + ABC'D)$ D. $F = (B'D + CD' + ABC'D)$
33. In Figure 5, when $xy = ..$, output F is equal to z because $F = 0$ when $z = 0$ and $F = 1$ when $z = 1$
 A. 01 B. 11 C. 00 D. 10
34. In table (1), the simplified function in sum-of-minterms form is-----
 A. $F = (xz' + x'yz + yz)$ C. $F = (xz' + x'yz' + y'z')$
 B. $F = (xz' + x'yz + y'z')$ D. $F = (z' + x'yz + y'z')$
35. In table (1), the maxterm in numerical form is.....
 A. $F(x, y, z) = \pi(0, 2, 7, 5)$ C. $F(x, y, z) = \sum(0, 2, 7, 5)$
 B. $F(x, y, z) = \pi(0, 2, 7)$ D. $F(x, y, z) = \pi(1, 2, 7, 5)$
36. Any signed positive binary number is recognised by its _____
 A. MSB B. LSB C. Byte D. Nibble

Question (2):

Read the statements carefully and identify whether they are true or false

- 1's complement can be easily obtained by using inverter ()
- In boolean algebra, the AND operation is performed by Distributive properties only ()
- The logical sum of two or more logical product terms is called SOP ()
- A Karnaugh map (K-map) is an abstract form of Cycle diagram organized as a matrix of squares ()

5. It should be kept in mind that don't care terms should be used along with the terms that are present in Minterms ()
6. Half adder has two inputs and two outputs whereas Full Adder has 3 inputs and 2 outputs ()
7. AND gate means addition of two inputs, which outputs when any of the input is high ()
8. In EX-OR gate The output of a logic gate is 1 when all inputs are at logic 0 or all inputs are at logic 1 ()
9. In a combinational circuit, the output at any time depends only on the Input values at that time ()
10. A combinational circuit that selects one from many inputs are decoder ()

Question (3):

Find from column (2) the statement that matches the number in column (1):-

column (1)	column (2)
1. The output will be high if the two inputs are 00 for ... 2. Which input values will cause an AND logic gate to produce a HIGH output? 3. Which of the following logic families has the longest switching time 4. If A and B are the inputs of a half adder, the carry is given by	A. All inputs are HIGH B. NOR gate C. A AND B D. CMOS

$$\bar{x}\bar{y}z + \bar{x}yz + x\bar{y}z + x\bar{y}\bar{z}$$

Tables

Table 1

Truth Table of Function F

$$\bar{x}\bar{y}z + \bar{x}yz + x\bar{y}z + x\bar{y}\bar{z}$$

$$\bar{x}z + \bar{x}\bar{y}z + x\bar{y}z$$

x	y	z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

$$\bar{x}z + \bar{x}\bar{y}z + x\bar{y}z$$

000	001	010	011	100	101	110	111
0	1	0	0	1	0	0	0
1	1	1	1	0	0	0	0

$$\bar{x}z + \bar{x}\bar{y}z + x\bar{y}z$$

$$\bar{x}z + \bar{x}\bar{y}z + x\bar{y}z$$

$$\bar{x}z + \bar{x}\bar{y}z + x\bar{y}z$$

$$\bar{x}z + \bar{x}\bar{y}z + x\bar{y}z$$

Figures

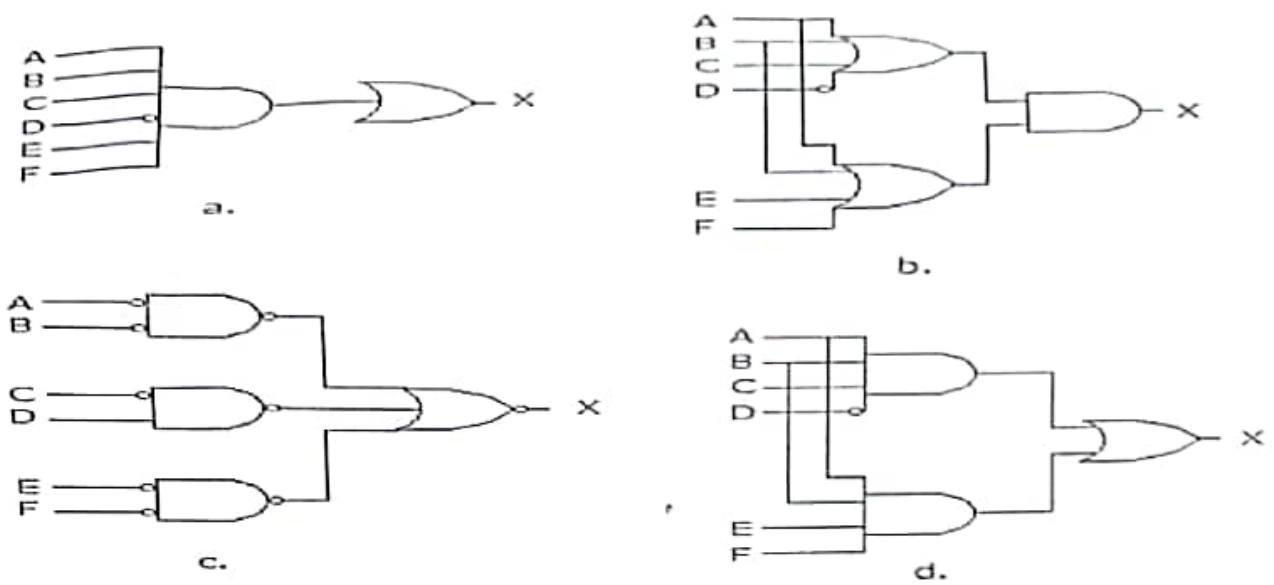


Figure 1

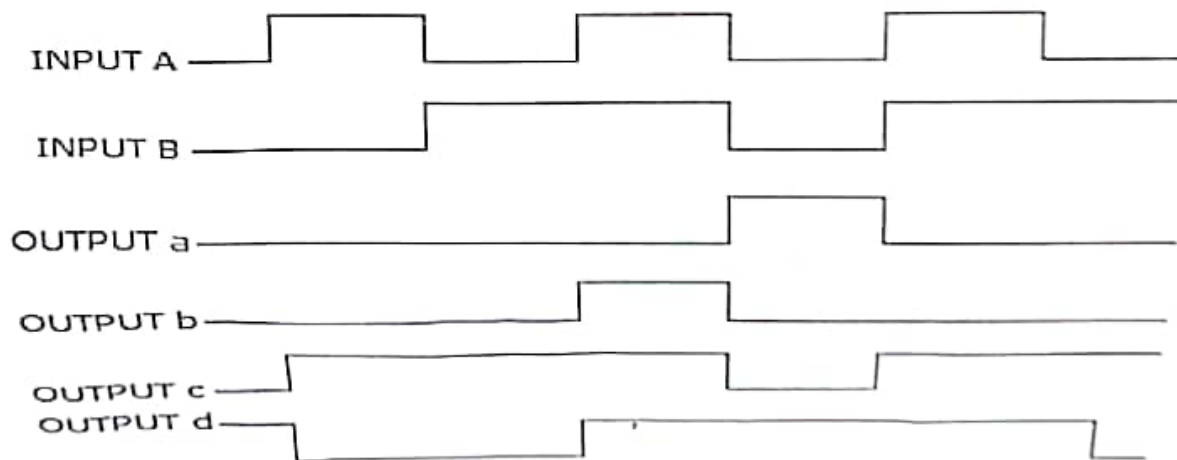
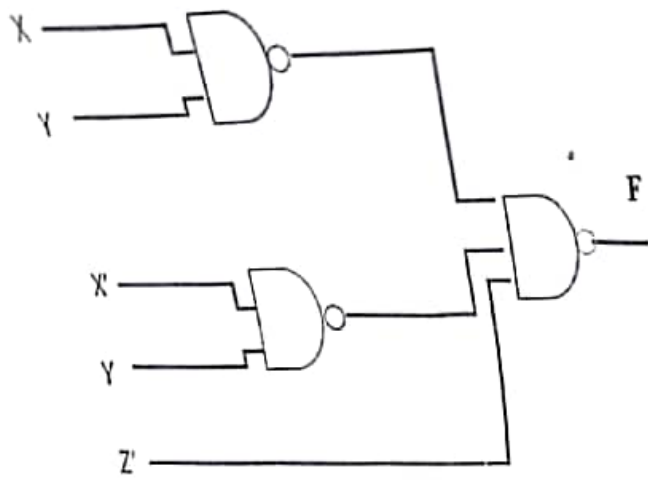
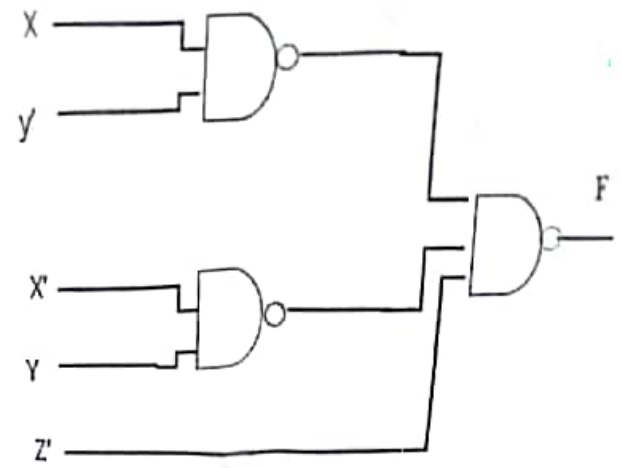


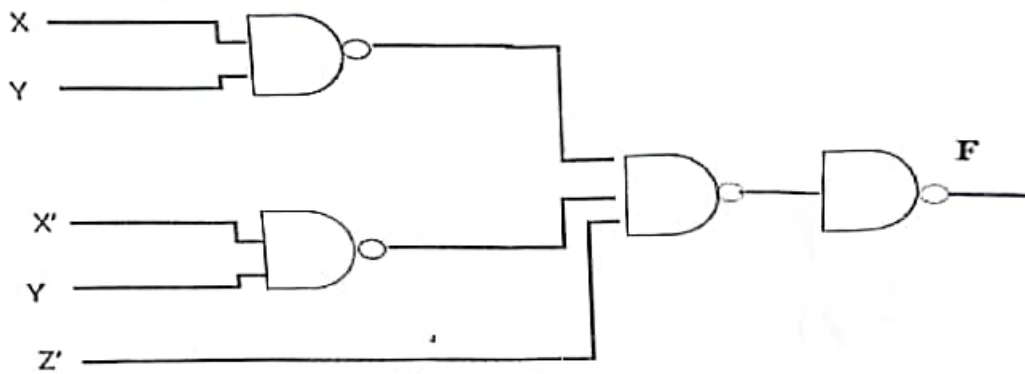
Figure 2



(a)



(b)



(c)

Figure 3

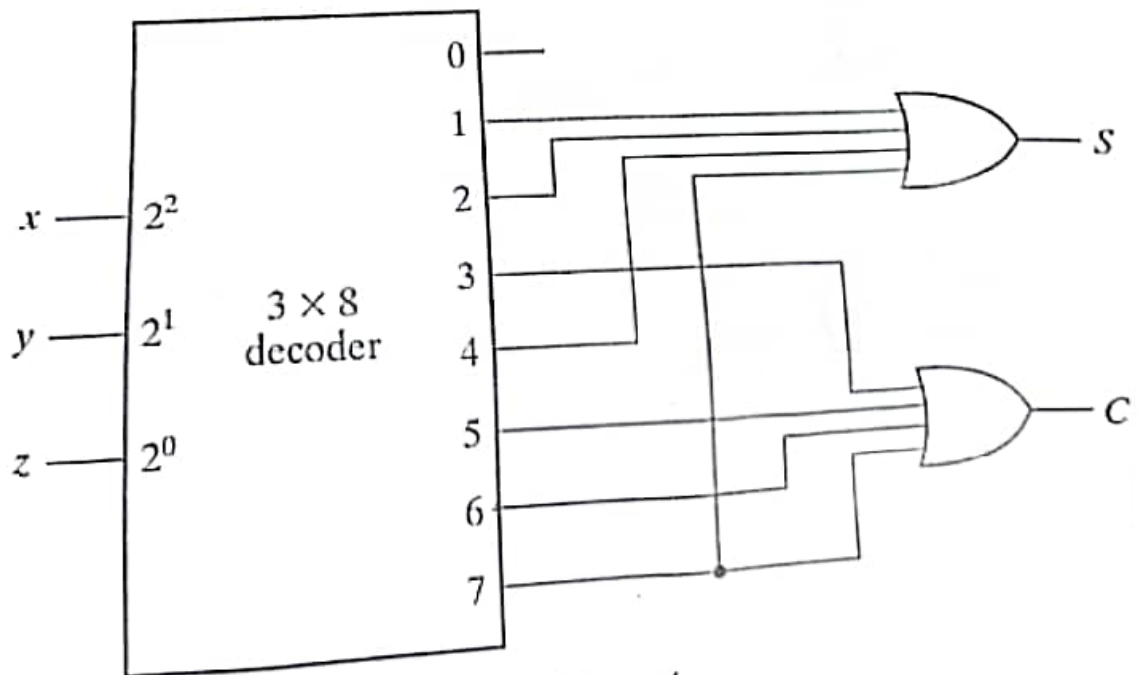
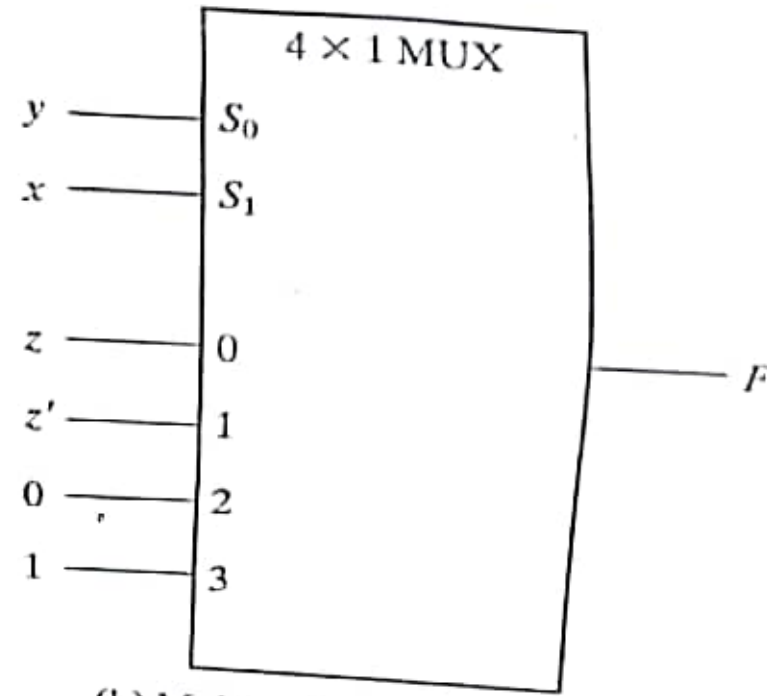


Figure 4

x	y	z	F	
0	0	0	0	$F = z$
0	0	1	1	
0	1	0	1	$F = z'$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	1	$F = 1$
1	1	1	1	

(a) Truth table



(b) Multiplexer implementation

Figure 5

Best wishes and good luck

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