Flip flop is at 'set' state when outputs Q and Q' are respectively

a) 1 and 0 b) 0 and 1 c) 1 and 1 d) 0 and 0

D flip flop contains output that are

a) complement b) similar c) infinite d) zero

D flip flop contains---------- clock input(s)

a) one b) two C) three d) four

Flip flop is at 'reset' state when outputs Q and Q' are respectively

a) 1 and 0 b) 0 and 1 c) 1 and 1 d) 0 and 0

Sequential circuits require a

a) timing motors b) timing transformers c) timing generators d) timing flips

Circuit which has a feedback is

a) combinational circuit b) sequential circuit c) systematic circuit d) correctional circuit

Circuit which has two stable states are termed as

a) combinational circuit b) bistable circuits c) unit stable circuits d) tri stable circuits

Flip flop is considered set when it stores

a) logic 1 b) logic x c) logic z d) logic 0

If we don't want to change the state of SR flip flop, S and R must be

a) 1 and 0 respectively b) 0 and 1 respectively c) 1 and 1 respectively d) 0 and 0 respectively

Logic circuits which don't have memory are

a) combinational circuit b) sequential circuit c) systematic circuit d) correctional circuit

Logic circuits that incorporate memory are called

a) combinational circuit b) sequential circuit c) systematic circuit d) correctional circuit

The term hold always means _____.

a) $Q = 0, \overline{Q} = 1$ **b)** $Q = 1, \overline{Q} = 0$ **c)** $Q = 0, \overline{Q} = 0$ **d) no change**

The signal used to identify edge-triggered flip-flops is _____.

a bubble on the clock input an inverted "L" on the output

the letter "E" on the enable input a triangle on the clock input

Whose operations are more faster among the following?

a) Combinational circuits b) Sequential circuits c) Latches d) Flip-flops

What is a trigger pulse?

a) A pulse that starts a cycle of operation b) A pulse that reverses the cycle of operation

c) A pulse that prevents a cycle of operation d) A pulse that enhances a cycle of operation

Sequential circuits require a

a) timing motors b) timing transformers c) timing generators d) timing flips

When the output of the NOR gate S-R flip-flop is in the HOLD state (no change), the inputs are _____.

a) $S = 1, R = 1$ **b)** $S = 1, R = 0$ **c)** $S = 0, R = 1$ **d)** $S = 0, R = 0$

The result "X + XY = X" follows which of these laws?

a) Consensus law b) Distributive law c) Duality law d) Absorption law

Which of the following options represent the correct reduction of XYZ + $\overline{X}$**YZ ?**

a) 0 b) YZ c) X + X b) 2YZ

The following hexadecimal number (1E.43)16 is equivalent to

(36.506)8 $(36.206)_8$ $(35.506)_8$ $(35.206)_8$

4) How many entries will be in the truth table of a 4-input NAND gate?

6 8 32 16

Convert the binary number 1001.0010_2 **to decimal**

a) 90.125 b) 9.125 c) 125 d) 12.5

Convert hexadecimal value C1 to binary

a) 11000001 b) 1000111 c) 111000100 d) 111000001

Convert the octal number 17_8 to decimal

a) 51 b) 82 c) 57 d) 15

Convert the binary number 010111100_2 to octal.

a) 172_8 b) 272_8 c)174_8 d) 274_8

1's complement of 1011001 is

0100111 0101100 0100110 0110110

2's complement of 1011011 is

0100011 0110101 0100011 0100101

The output of a NOR gate is HIGH if _____.

a) all inputs are HIGH b) any input is HIGH c) any input is HIGH d) all inputs are LOW

The format used to present the logic output for the various combinations of logic inputs to a gate is called a(n):

Boolean constant Boolean variable truth table input logic function

The Boolean expression for a 3-input AND gate is _____.

X = AB X = ABC X = AB+C X = A + B + C

If the input to a NOT gate is A and the output is X, then _____.

X = A X = 0 $X = \overline{A}$ none of them

The expressions, $\overline{A \cdot B} = \overline{A} + \overline{B}$, are equivalent

True False

Subtraction is commutative.

True False

The OR function is Boolean multiplication and the AND function is Boolean addition.

True False

In Boolean algebra, A + 1 = 1.

True False

The product-of-sums (POS) is basically the ORing of ANDed terms.

A flip-flop is in the CLEAR condition when $Q = 1, \overline{Q} = 1$.

a) True b) False

Some flip-flops have invalid states

a) True b) False

When the output of the NOR gate S-R flip-flop is $Q = 1$ and $\overline{Q} = 0$, the inputs are $S = 1, R = 1$.

a) True b) False

A TOGGLE input to a J-K flip-flop causes the *Q* and $\overline{Q}$ outputs to switch to their opposite state.

a) True b) False

Edge-triggered flip-flops can be identified by the triangle on the clock input.

a) True b) False