Digital Front End (DFE) Filter Array

Problem Design Statement

Design and implementation of a multistage Digital Front End (DFE) for radio/ADC preprocessing: fractional polyphase decimator (9 MHz → 6 MHz), dual 2nd-order IIR notch filters (2.4 MHz and 5 MHz), and a configurable CIC decimator chain (decimation factors 1,2,4,8,16).

Context & Motivation

An incoming digitized RF/intermediate-frequency stream is sampled at 9 MHz (or equivalent sample clock) but the downstream processing chain (demodulator/decoder) requires a 6 MHz sample rate and/or multiple lower-rate streams. The channel environment contains narrowband interferers centered at 2.4 MHz and 5 MHz that must be deeply suppressed. A multi-stage architecture—fractional polyphase decimation → narrowband IIR notches → CIC decimation—offers the best trade-off between computational cost, latency, and spectral performance.

High-Level Functional Requirements

1. Fractional Decimation (9 MHz → 6 MHz)
    - Implement a polyphase fractional decimator that converts a 9 MHz sampled stream to 6 MHz (i.e., decimation by factor 3/2) while meeting stringent aliasing requirements.
    - Must be streaming, fixed latency, and suitable for hardware (FPGA/ASIC) implementation.
2. Notch Filtering
    - Two cascaded 2nd-order IIR notch (biquad) filters to remove narrowband interferers at 2.4 MHz and 5.0 MHz (center frequencies relative to the 6 MHz sampling rate after fractional stage).
    - Notches shall be deeply attenuating and stable in fixed point.
3. CIC Decimation
    - Provide a CIC decimation stage with configurable decimation factor selectable among powers-of-two: 1, 2, 4, 8, 16.
    - The CIC output rate = 6 MHz / D, where $D \in \{1,2,4,8,16\}$.

- Include an optional compensation / final FIR stage if required to meet passband ripple requirements.

4. Control & Observability

- Run-time control registers to: enable/disable stages, set CIC decimation factor, bypass notches, set the coefficients, and read status (overflow, ready).
- Probe points or debug outputs

Numerical & Performance Requirements

• Fractional Decimator (9 → 6 MHz):

- Passband: 0 … 2.8 MHz (i.e., up to slightly below Nyquist at 3.0 MHz for 6 MHz rate)
- Passband ripple: ≤ ±0.25 dB
- Transition band: 2.8 MHz → 3.2 MHz (tight)
- Stopband attenuation (against aliased image energy): ≥ 80 dB beyond 3.2 MHz (relative to 9 MHz sampling).
- Group delay: known and constant across passband.

• IIR Notch Filters:

- Center frequencies: 2.4 MHz and 5.0 MHz (expressed in normalized frequency at the 6 MHz sample rate)
- Notch depth: ≥ 50 dB (goal: 60 dB) at center frequency
- Notch bandwidth (3 dB): narrow (e.g., < 50–100 kHz) to avoid damaging desired signals
- Stability: coefficient quantization must preserve pole radius < 1 (no ringing growth)
- Latency: minimal (1–2 sample periods for each biquad)

• CIC Decimator (variable D):

- Supported D: 1,2,4,8,16 (decimation in steps of 2)
- Passband ripple: after CIC (inherent droop) must be corrected by compensation FIR if ripple > 0.5 dB — final passband ripple spec ≤ 0.5 dB
- Stopband attenuation: deep enough to avoid aliased interferers → depending on chosen D, combine CIC + compensation FIR to reach ≥ 60 dB where required

- Word growth & saturation: internal bit growth must be sized to avoid overflow (accumulator bit width computed based on N stages and impulse sum).

- Overall System:
  - Throughput: must sustain continuous streaming at input rate (9 MHz) without dropped samples.
  - Fixed-point: all filters implemented in fixed-point arithmetic; choose coefficient widths and accumulator widths with analysis for SNR and dynamic range.
  - Latency budget: Overall maximum allowable end-to-end latency 200 μs

Interface & Data Format

- Input: streaming samples at Fs_in = 9 MHz
  - Data format: signed fixed-point (s16.15).
- Output(s): streaming sample(s) at Fs_mid = 6 MHz after fractional stage and then optionally at Fs_out = Fs_mid / D after CIC.
  - Output data format: signed fixed-point (s16.15).
- Control bus: register map over APB, CIC factor select, notch enable, bypass signals, filters coefficients.
- Status & debug: ready, overflow, tap coefficients (readback).

Implementation Notes & Recommended Architecture

1. Multistage approach (recommended):
   - Implement fractional decimation via polyphase FIR using interpolation/decimation ratio M/N (here 2/3 or 3/2 depending on direction). Since 9→6 is decimate-by-3/2, implement as interpolation by 2 then decimate by 3, or use direct fractional polyphase structure. Polyphase reduces computational cost dramatically vs single large FIR.
   - After fractional stage run coarse anti-alias filtering to suppress images.
2. Notch filters (IIR biquads):
   - Implement two cascaded fixed-coefficient biquads using direct-form II transposed for minimal state memory and good fixed-point behavior.

- Coefficients precomputed in high precision and quantized (e.g., s16.15 or s16.14) with pole radius chosen to meet notch depth and bandwidth.

3. CIC decimator:

- Implement N-stage integrator chain → downsample → N-stage differentiator comb. Choose number of stages and implement selectable decimation by power-of-two factors.
- Account for large bit growth in the integrator stage; add truncation/rounding before output.
- Implement optional compensation FIR (short fixed-point FIR) to correct CIC drop in the passband and meet final ripple/attenuation specs.

4. Fixed-point sizing:

- Compute accumulator widths to avoid overflow: accumulator bits = input_bits + ceil(log2(max_gain)), where max_gain depends on filter coefficients and CIC gain (for CIC gain = (R^N)).
- Use saturation where appropriate; prefer rounding (not truncation) to minimize bias.

Verification & Test Plan

1. Unit-level verification

- Verify fractional polyphase decimator frequency response vs golden floating-point reference (FFT of impulse/tones).
- Verify notch filter depth, bandwidth, and stability in fixed-point vs reference.
- Verify CIC gain, droop, and compensation performance.

2. System-level simulations

- Stimuli: single-tone sweeps, multi-tone with interferers at 2.4 & 5 MHz, wideband noise, worst-case channel impulsive interferers.
- Check aliasing: inject out-of-band tones prior to fractional decimator and ensure suppression meets spec.

3. Corner cases

- Overflow/stress tests with large input amplitudes; verify saturation behavior.
- Verify CIC decimation factor switching (run-time change) and transient behavior.

4. Hardware verification
    - RTL-level simulation

Deliverables

- System design on Python; double and quantized
- RTL (SystemVerilog, Verilog,VHDL) for: polyphase fractional decimator, two biquad IIR notches, configurable CIC decimator, optional compensation FIR, control/status register file.
- Fixed-point design report (coefficient quantization, accumulator widths, expected SNR).
- Testbench with golden-model float VS fixed comparisons, stimulus vectors, and automated regression scripts.
- Verification report: frequency responses, notch depths, aliasing tests, and functional results.

Success Criteria

- Fractional decimator meets passband ripple ≤ 0.25 dB and stopband attenuation ≥ 80 dB in simulation.
- Notch filters achieve ≥ 50 dB notch depth at 2.4 MHz and 5.0 MHz with minimal distortion to adjacent frequencies.
- CIC + compensation achieves final passband ripple ≤ 0.5 dB and overall stopband attenuation as required for system-level aliasing protection.
- Throughput, latency, and resource usage meet the system budget; no overflows in worst-case input scenarios; control registers work as specified.

Risks & Mitigations (Design Hints)

- Risk: Fractional decimation filter order becomes large to meet 80 dB stopband → resource heavy.
  Mitigation: Use multistage: short polyphase + small compensation FIR; explore interpolation then decimation (2× then 3×) to reduce FIR length.
- Risk: Quantized IIR poles become unstable or notch depth degrades.
  Mitigation: Use double-precision design to select robust pole radii, then carefully quantize with stability margin; use direct-form II transposed.

- Risk: CIC droop unacceptable at high decimation.
  Mitigation: Add short compensation FIR per decimation setting and/or select lower CIC stage count.