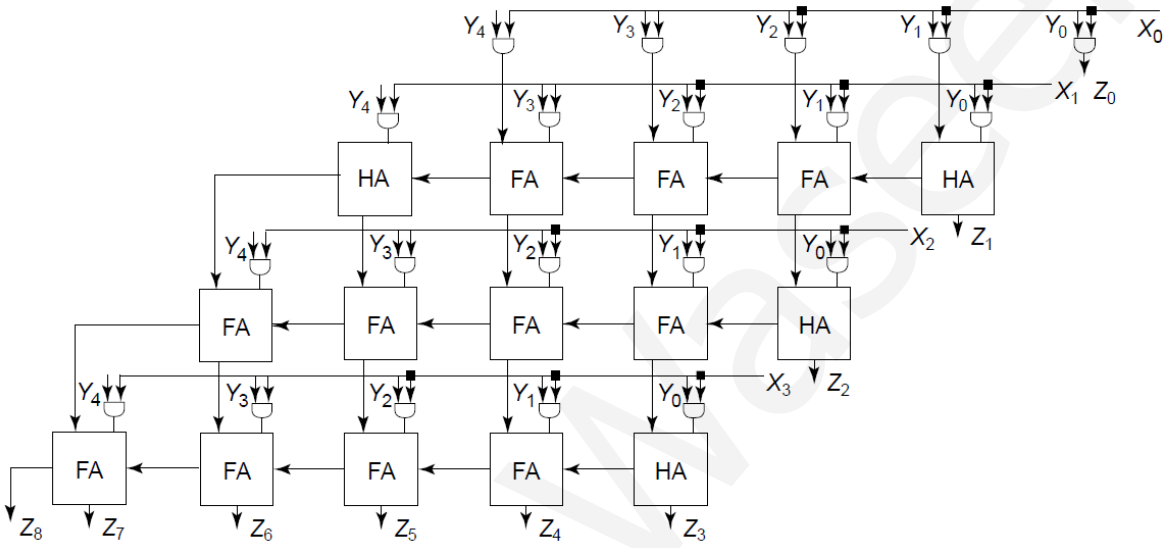
Project

Multiplication is now an essential operation in almost all machine learning algorithms. Different multiplier architectures are available. One of the most known architectures are the array multiplier. AND gates compute the partial products and the addition of partial products can be performed by using Full adders and Half-adders.

The 4×5 array multiplier shown has 9 inputs. The multiplication output Z has 9 bits.



The project is composed of two parts:

Design

1. Design a half adder and a full adder
2. Use the half adder and full adder as module instances to build the array multiplier

For the and gate, use the build-in primitive that models the and gate

and <instance_name> (and_output, and_in1, and_in2);

and and1 (x, a, b);

Verification

1. Test the design using the different Verification techniques learnt during the course
   - Directed test vectors
   - Randomized test vectors
   - Constrained-random test vectors

2. Add coverpoints and bins for the inputs and output
3. Report the statement, branch and toggle coverage for the multiplier

The project should run using do file compiling, simulating and displaying the coverage report.

To test the quality of the verification, we will measure a metric called omega, where omega equals to the toggle coverage of the multiplier divided by the number of test vectors. For example if the stimulus generator part of the testbench has 20 iterations and the toggle coverage is 90% then we have 90 divided by 20 test vectors resulting in an omega of 4.5

The project will be done in teams of two but you can choose to work by yourself. Please fill in the sheet here with your names. The project will be submitted by any of the team members on Microsoft teams.

Bonus

The team scoring highest omega will have 3 bonus marks for each team member. 2nd highest omega team will have 2 bonus marks for each team member. The following 3rd, 4th and fifth team will have 1 bonus mark for each member of the team.

100% toggle coverage is a must to receive the bonus marks.

Deliverables

One compressed file that has the following:

1) PDF file with this format <your_name>_Project. Snippets from the waveforms captured from Modelsim for the multiplier with inputs assigned values and output values visible is expected in the PDF
2) Verilog files for the designs and testbench
3) Do file to run the test case displaying the coverage at the end

Note that your document should be organized and neat.

Good luck.