Objectives

- To implement the basic circuits of DSP operation

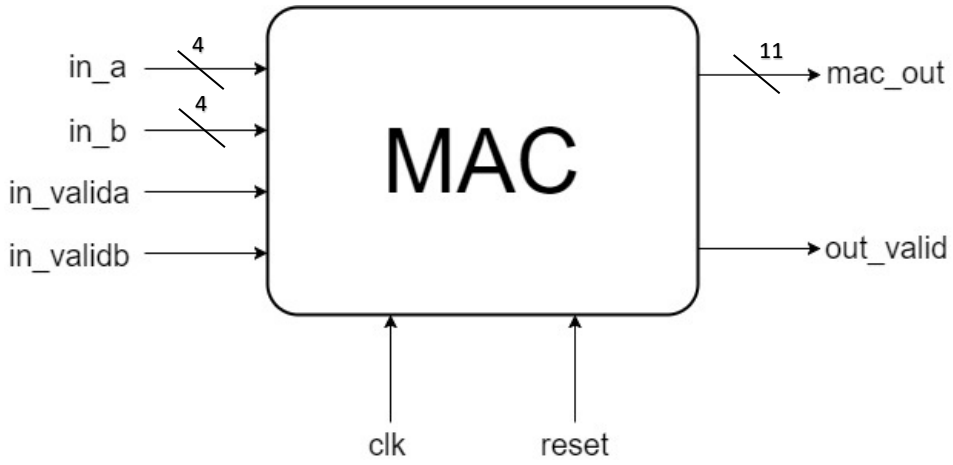
LAB contents

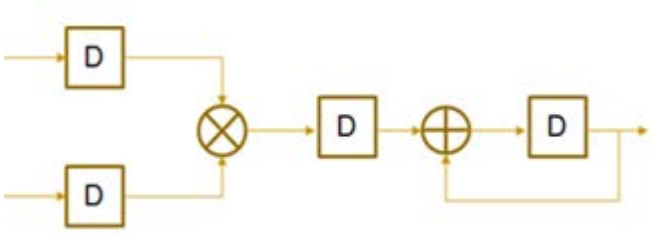
- LAB4: Multiply and Accumulation

Design Description

- Please design a Multiply and Accumulation(MAC) with two 4-bits inputs.

Block Diagram





Specifications

- Top module name : mac (File name: mac.v)
- Input pins: in_a[3:0], in_b[3:0], in_valida, in_validb, reset, clk
- Output pins: mac_out[10:0], out_valid,
- All inputs and outputs are synchronized at clock positive edge.
- It is synchronous-reset architecture, both outs become 0 when the reset equal to 1.
- Note that in_a, in_b are 4-bits signed integer number. Please design the circuit without overflow.
- The two operands are valid when the control signals “in_valida” and “in_validb” are 1, respectively.
- After 8 MACs, output the result and assert the “out_valid” signal
- Note that two control signals are in a “one-to-one” manner, so you do not have to buffer the operands.