|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| aluop | undifiend | regvalue | jump | memwrite | memsign | Regdst | Regwrite | S | alusrcb | alusrca | jr | Bl | Bge | Bne | Beq | Funct | Opcode | Instruction |
| 1000 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 | 000000 | 000000 | Sll |
| 1010 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 | 000010 | 000000 | srl |
| 1011 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 000011 | 000000 | sra |
| 1000 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 000100 | 000000 | sllv |
| 1010 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 000110 | 000000 | srlv |
| 1011 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 000111 | 000000 | srav |
| Xxxx | 0 | Xxxxx | 1 | 00 | x | xx | 0 | 0 | x | x | 1 | 0 | 0 | 0 | 0 | 001000 | 000000 | Jr |
| Xxxx | 0 | 001xx | 1 | 00 | x | 10 | 1 | 0 | x | x | 1 | 0 | 0 | 0 | 0 | 001001 | 000000 | jalr |
| 1111 | 0 | Xxxxx | 0 | 00 | x | xx | 0 | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 | 011001 | 000000 | multu |
| 0000 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 1 | 0 | 0 | x | 0 | 0 | 0 | 0 | 100000 | 000000 | add |
| 0000 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 | 100001 | 000000 | addu |
| 0001 | 0 | 000xx | 0 | 00 | X | 01 | 1 | 1 | 0 | 0 | X | 0 | 0 | 0 | 0 | 100010 | 000000 | sub |
| 0001 | 0 | 000xx | 0 | 00 | X | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 100011 | 000000 | subu |
| 0100 | 0 | 000xx | 0 | 00 | X | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 100100 | 000000 | and |
| 0101 | 0 | 000xx | 0 | 00 | X | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 100101 | 000000 | or |
| 0110 | 0 | 000xx | 0 | 00 | X | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 100110 | 000000 | xor |
| 0111 | 0 | 000xx | 0 | 00 | X | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 100111 | 000000 | nor |
| 0011 | 0 | 000xx | 0 | 00 | X | 01 | 1 | 1 | 0 | 0 | x | 0 | 0 | 0 | 0 | 101010 | 000000 | slt |
| 0011 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 101011 | 000000 | sltu |

**I Instructions**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| aluop | undifiend | regvalue | jump | Memwrite | memsign | Regdst | Regwrite | S | alusrcb | alusrca | jr | Bl | Bge | Bne | Beq | Opcode | Instruction |
| 0001 | 0 | 0xxxx | 0 | 00 | X | xx | 0 | 0 | 0 | 0 | X | 0 | 0 | 0 | 1 | 000100 | Beq |
| 0001 | 0 | 0xxxx | 0 | 00 | X | xx | 0 | 0 | 0 | 0 | X | 0 | 0 | 1 | 0 | 000101 | Bne |
| 0001 | 0 | 0xxxx | 0 | 00 | x | Xx | 0 | 1 | 0 | 0 | X | 0 | 1 | 0 | 0 | 000110 | Bge |
| 0001 | 0 | 0xxxx | 0 | 00 | X | Xx | 0 | 1 | 0 | 0 | X | 1 | 0 | 0 | 0 | 000111 | Bl |
| 0000 | 0 | 000xx | 0 | 00 | X | 00 | 1 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 | 001000 | addi |
| 0000 | 0 | 000xx | 0 | 00 | X | 00 | 1 | 0 | 1 | 0 | X | 0 | 0 | 0 | 0 | 001001 | addiu |
| 0011 | 0 | 000xx | 0 | 00 | X | 00 | 1 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 | 001010 | slti |
| 0011 | 0 | 000xx | 0 | 00 | X | 00 | 1 | 0 | 1 | 0 | X | 0 | 0 | 0 | 0 | 001011 | sltiu |
| 0100 | 0 | 000xx | 0 | 00 | X | 00 | 1 | 0 | 1 | 0 | x | 0 | 0 | 0 | 0 | 001100 | andi |
| 0101 | 0 | 000xx | 0 | 00 | X | 00 | 1 | 0 | 1 | 0 | x | 0 | 0 | 0 | 0 | 001101 | ori |
| 0110 | 0 | 000xx | 0 | 00 | X | 00 | 1 | 0 | 1 | 0 | X | 0 | 0 | 0 | 0 | 001110 | xori |
| Xxxx | 0 | 011xx | 0 | 00 | X | 00 | 1 | 0 | 0 | 0 | X | 0 | 0 | 0 | 0 | 001111 | lui |
| 1111 | 0 | 000xx | 0 | 00 | x | 01 | 1 | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 | 011100 | mul |
| 0000 | 0 | 10001 | 0 | 00 | 0 | 00 | 1 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 | 100000 | lb |
| 0000 | 0 | 10010 | 0 | 00 | 0 | 00 | 1 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 | 100001 | lh |
| 0000 | 0 | 10000 | 0 | 00 | 0 | 00 | 1 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 | 100011 | lw |
| 0000 | 0 | 10001 | 0 | 00 | 1 | 00 | 1 | 1 | 1 | 0 | x | 0 | 0 | 0 | 0 | 100100 | lbu |
| 0000 | 0 | 10010 | 0 | 00 | 1 | 00 | 1 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 | 100101 | lhu |
| 0000 | 0 | 000xx | 0 | 10 | X | Xx | 0 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 | 101000 | sb |
| 0000 | 0 | 000xx | 0 | 11 | X | Xx | 0 | 1 | 1 | 0 | X | 0 | 0 | 0 | 0 | 101001 | sh |
| 0000 | 0 | 000xx | 0 | 01 | x | xx | 0 | 1 | 1 | 0 | x | 0 | 0 | 0 | 0 | 101011 | sw |
| xxxx | 0 | 010xx | 0 | 00 | x | 00 | 1 | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 | 010000 | Mfc0 |

**J Instructions**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| aluop | undifiend | regvalue | jump | Memwrite | memsign | Regdst | Regwrite | S | alusrcb | alusrca | jr | Bl | Bge | Bne | Beq | Opcode | Instruction |
| xxxx | 0 | 0xxxx | 1 | 00 | x | xx | 0 | 0 | x | x | 0 | 0 | 0 | 0 | 0 | 000010 | J |
| xxxx | 0 | 001xx | 1 | 00 | x | 10 | 1 | 0 | x | x | 0 | 0 | 0 | 0 | 0 | 000011 | Jal |