Open Source Tools
Lab 7
5T OTA Design

1 OTA Desing

1.1 Specifications:

Technology	0.13 um CMOS	0.18 um CMOS
Supply Voltage	1.2V	1.8V
Load	5pF	5pF
Open Loop DC Voltage Gain	>= 34dB	>= 34dB
CMRR @ DC	>= 74dB	>= 74dB
Phase Margin	>= 70°	>= 70°
CM input range - low	<= 0.6V	<= 1V
CM input range - high	>= 1V	>= 1.5V
GBW	>= 10MHz	>= 10MHz

Figure 1. Specification Table

1.2 Input Pair Sizing

First Thing In Design OTA is to choose the INPUT pair NMOS or PMOS , this can be determined from CMIR spec. , as shown in figure 1 , CMIR closer to VDD , then NMOS is more suitable.

Now , Getting the value of g_m for the input pair form GBW spec GBW $= \frac{g_m}{C_L} = 10\text{MHz}$, form this $g_m \approx 317\,\mu S$, this can be got by choosing $\frac{g_m}{I_d} = 16$ and $I_D = 20\mu A$, but It was found that VGS in that case = 820mv , which in case of minimum CM input 1V , VDS for tail current source will be equal to 180mV taking a 50mV margin, $V^{\langle * \rangle} = 130\,\text{mv}$ which is small for the Current source, that's why $\frac{g_m}{I_d}$ is chosen to 17 for the Input pair which gives us $V_{\text{GS}} \approx 778\text{mv}$ (this is done with $V_{\text{sb}} = 220\,\text{mv}$), this gives us 220mv for the tail current source.

Input for SA	Value
g_{m/I_d}	17
V_{DS}	0.6V
V_{SB}	0.22V
g_m / g_{ds}	110
I_D	$20\mu A$

Table 1. Input Pair Sizing Input

The output form SA is shown in table 2

Paramter	Value
W	22.27μ
L	440n
V_{GS}	778m
r_o	311k
V_{dsat}	91.93m
$V^{\langle * \rangle}$	119m
V_{ov}	8.3m
I_d	20μ

Table 2. Input Pair Sizing Output

1.3 CM Load Sizing:

For the current mirror Load (PMOS CM) , the only things to consider is CM Input Maximum and r_o needs to match that of the input to get the required DC gain $\frac{g_m r_o}{2} \geqslant 50$.

Starting with CM Input Maximum $\geqslant 1.5V$

$$\begin{aligned} V_{\mathrm{GD}_{\mathrm{input\,pair}}} &\leqslant V_{\mathrm{GS}_{\mathrm{input\,pair}}} - V_{\mathrm{dsat}_{\mathrm{input\,pair}}} \\ 1.5 - (1.8 - V_{\mathrm{GS}_{\mathrm{CM}}}) &\leqslant V_{\mathrm{GS}_{\mathrm{input\,pair}}} - V_{\mathrm{dsat}_{\mathrm{input\,pair}}} \\ V_{\mathrm{GS}_{\mathrm{CM}}} &\leqslant 986\mathrm{mv} \end{aligned}$$

V_{GS} is chosen to be 950mv.

Paramter	Value
W	5.84μ
L	300n
V_{GS}	940m
r_o	311k
V_{dsat}	217.7m
$V^{\langle * \rangle}$	243.4m
V_{ov}	198m
I_d	20μ
g_m / I_d	8.216

Table 3. CM Load Sizing Output

1.4 Tail Current Source Sizing:

For Current Source tail , there are two specs that controls the sizing: CM Input Minimum and CMRR at DC , we chose that $V_{\mathrm{DS}_{\mathrm{min}}} = 220\mathrm{mV}$ as discussed previously.

For CMRR $\geqslant 74\mathrm{dB}$ at DC :

$$\begin{aligned} A_V\,(1 + 2(g_{m_{\mathrm{CM}}})R_{\mathrm{ss}}) &\geqslant 5011 \\ (g_{m_{\mathrm{CM}}})R_{\mathrm{ss}} &\geqslant 50 \\ R_{\mathrm{ss}} &\geqslant 300K \end{aligned}$$

r_o is chosen to be 300K, $V_{\mathrm{DS}} = 220\mathrm{mv}$ and $V^{\langle * \rangle} = 180\mathrm{mv}$ (50mv margin).

Paramter	Value
W	72.6μ
L	2.7μ
V_{GS}	787.4m
r_o	292.4k
V_{dsat}	137.3m
$V^{\langle * \rangle}$	182m
V_{ov}	124.7m
I_d	40μ
g_m/I_d	11

Table 4. Tail Current Source Sizing Output

1.5 Sizing Summary

Devices	W	L	I_d	g_m	$\frac{g_m}{I_d}$	V_{dsat}	$V^{\langle \rangle}$	V_{ov}
Input pair	22.27μ	440n	20μ	336.3μ	16.81	91.93m	119m	8.3m
CM load	5.84μ	300n	20μ	164.3μ	8.216	217.7m	243.4m	198m
Current Source	72.6μ	2.7μ	40μ	439.5μ	11	137.3m	182m	124m

Table 5. Sizing Summary

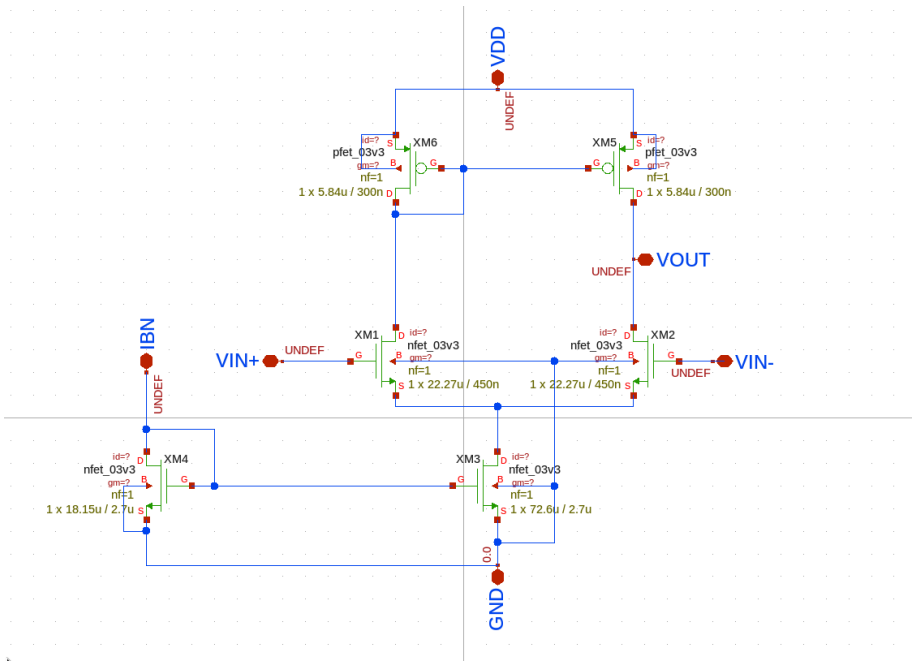


Figure 2. 5T OTA schematic

2 Simulation:

2.1 OP and AC simulation for V_{diff}

2.1.1 Operating point analysis

Using VICM = 1.25 V , Vout = 0.859 V , that's because for common mode input , V_{out} follows CM node which is equals to $1.8 - V_{\text{GS}} = 0.859V$.

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x9.xm6.m0	m.x9.xm5.m0	m.x9.xm3.m0
model	pfet_03v3.8	pfet_03v3.8	nfet_03v3.14
gm	0.000164599	0.000164599	0.000447876
gmbs	5.80529e-05	5.80529e-05	0.000176937
gds	3.1984e-06	3.1984e-06	1.05891e-06
vds	0.940782	0.940782	0.411416
vdsat	0.215992	0.215992	0.134862
vgs	0.940787	0.940787	0.78313
vth	0.744719	0.744719	0.663319
id	1.98544e-05	1.98544e-05	3.97088e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x9.xm4.m0	m.x9.xm2.m0	m.x9.xm1.m0
model	nfet_03v3.14	nfet_03v3.12	nfet_03v3.12
gm	0.000112588	0.000333659	0.000333659
gmbs	4.44853e-05	9.10594e-05	9.10594e-05
gds	1.92954e-07	3.38133e-06	3.38133e-06
vds	0.783129	0.447789	0.447789
vdsat	0.134862	0.0935572	0.0935572
vgs	0.78313	0.838581	0.838581
vth	0.663319	0.829473	0.829473
id	1e-05	1.98544e-05	1.98544e-05

Figure 3. OP Results

2.1.2 AC Simulation V_{diff}

Doing AC analysis where $v_{\text{cm}} = 0$ and $v_{\text{id}} = 1$, Results shows that BW = 206.6KHz , DC gain = 50.2 and GBW = 10.3M.

```
peak = 5.022535e+01
f2 = 2.066086e+05
gbw = 1.037699e+07
```

Figure 4. DC gain , BW and GBW

Analytical:

1. BW:
$$\text{BW} = \frac{1}{2\pi R_{\text{out}} C_L} = \frac{3.38 + 3.2}{2\pi\, 5} M = 209.4\text{KHz}$$
2. DC gain:
$$\text{DC gain} = g_m r_o / 2 = 333 / (3.38 + 3.2) = 50.6$$
3. GBW = 10.6M

	Simulation	Analysis
DC gain	50.2	50.6
BW	206.6KHz	209.4KHz
GBW	10.3M	10.6M

Table 6. BW , GBW and DC gain Simualtion Vs Analysis

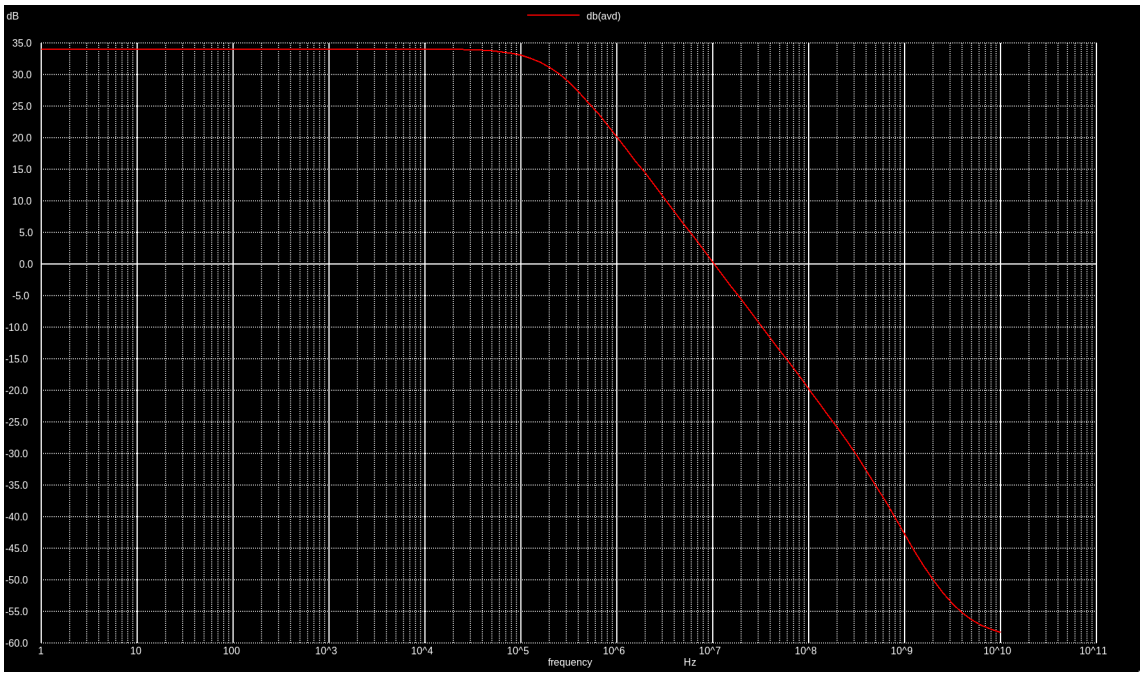


Figure 5. $V_{\text{out}_{\text{diff}}}$ bode plot in db

2.1.3 VICM vs Frequency:

Here $v_{\text{cm}} = 1$ and $v_{\text{id}} = 0$.

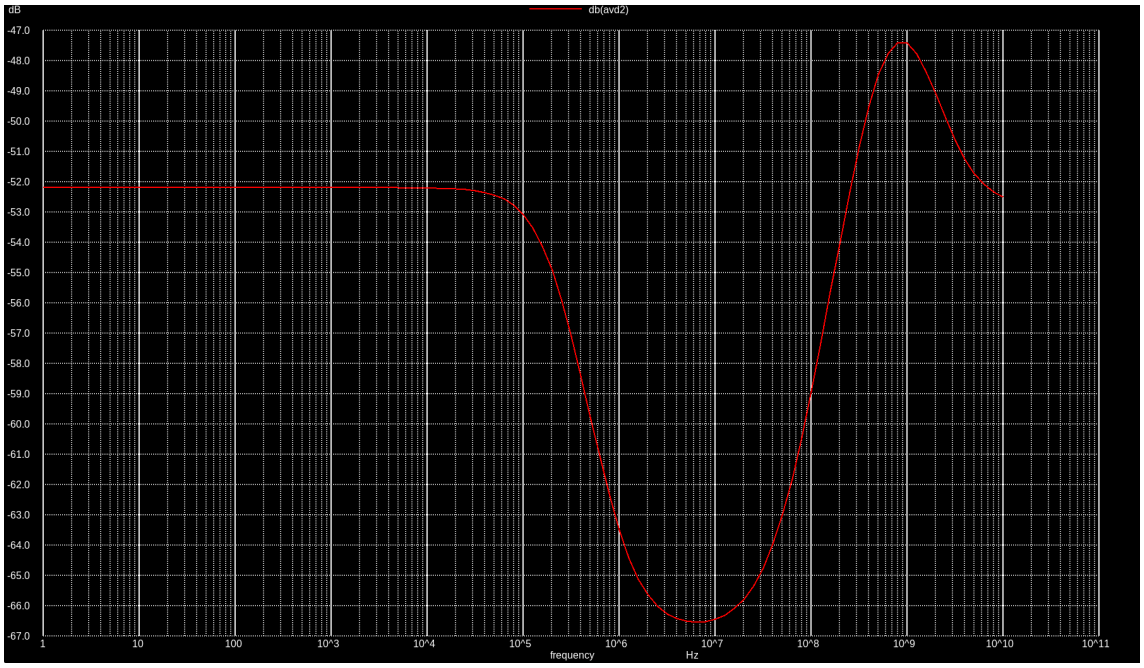


Figure 6. $V_{\text{out}_{\text{diff}}}$(Common Mode Input) bode plot in db

Simulation:

DC gain = -0.00245417

Peak = 0.0042545

pole : 216.5 KHz

zero : 5.77969e+07

second pole: 3.51603e+08

Analytical:

1. DC gain:

$$A_v = \frac{-1}{2g_m R_{\text{SS}}} = \frac{-1}{2\,164/1.06} = -3.2 \times 10^{-3}$$

2. Pole 1:

$$\frac{1}{2\pi(r_{o3}//r_{o2})C_L} = 204\text{KHz}$$

3. Zero: From ADT tail current source $C_{\text{db}} = 117.4\text{fF}$, $C_{\text{sb}}(\text{Input Pair}) = 17.39\text{fF}$

$$\frac{1}{2\pi(2r_o)(C_{\text{db}} + C_{\text{sb}})} = 62.58\text{MHz}$$

4. Pole 2:

$$\frac{(g_{m_3} + g_{\text{ds}_3} + g_{\text{ds}_{\text{input}}})}{2\pi(C_{\text{db}_{\text{input}}} + C_{\text{gd}_{\text{input}}} + C_{\text{db}} + C_{\text{gd}} + 2(C_{\text{gs}})} = 833\text{MHz}$$

5. Peak: This peak after occurs when R_{ss} becomes approximately zero abnd R_{out} is so small,

   R_{out} at 1GHz = $\frac{R_{\text{out}}}{1 + R_{\text{out}}\omega C_L} = 32\Omega$, $R_{\text{ss}} = \frac{R_{\text{ss}}}{1 + R_{\text{ss}}\omega(C_{\text{db}} + C_s b)} = 1.1K\Omega$

   Peak =

$$\frac{g_{m_{1,2}}}{1 + g_{m_{1,2}} R_{\text{ss}}} \left(\frac{g_{m_{3,4}}(R_{\text{out}})}{1 + g_{m_{3,4}}(R_{\text{out}})} - 1 \right) R_{\text{out}} \approx -4.64m$$

   This equation is an approximation but results is good

	Simulation	Analysis
DC gain	-2.45m	-3.2m
Pole 1	216.5KHz	204KHz
Zero(Due to R_{ss} Degradation)	57.7MHz	62.58MHz
Peak	-4.25m	-4.64m

Table 7. Pole, Zero ,DC gain and Peak Simulation Vs analysis

2.1.4 CMRR:

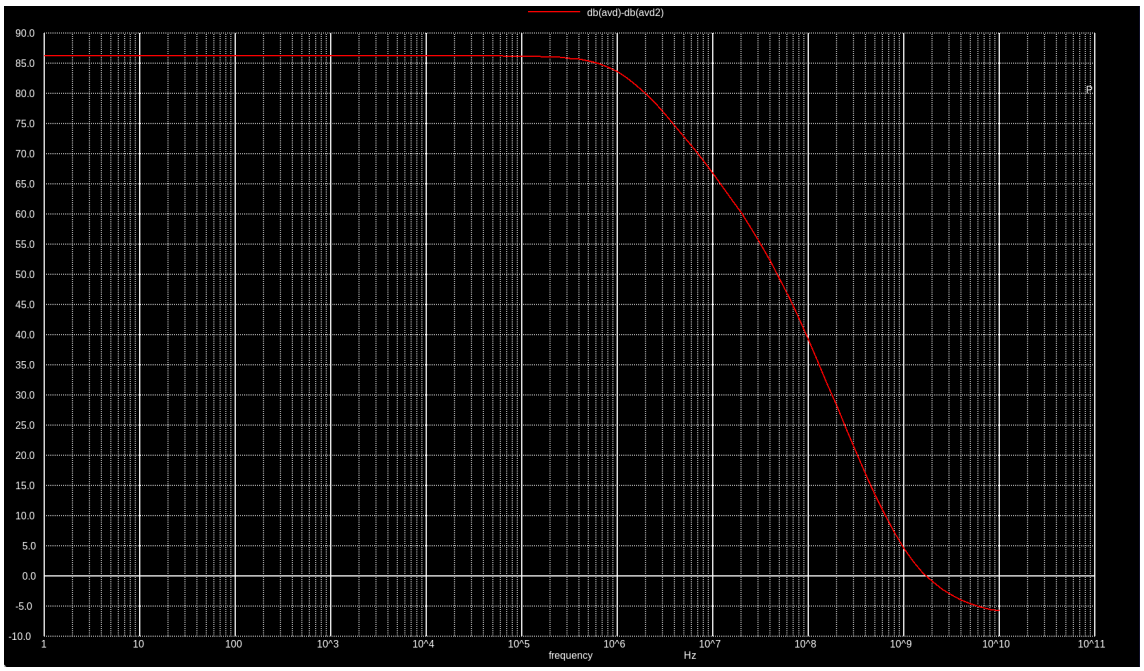


Figure 7. CMRR bode plot in (db)

As obivous form figure 7 that CMRR ≈86db at DC

DC CMRR = 20.418K

Analysis:

1. DC CMRR:

$$g_{m_{1,2}} r_{o1} // r_{o2} 2(g_{m_{3,4}} R_{\text{ss}}) = 15.625K$$

	Simulation	Analysis
DC CMRR	20.418K	15.625K

Table 8. DC CMRR Simulation Vs Analysis

2.2 Large Signal Analysis

2.2.1 Differential Mode

Sweeping V_{diff} from -VDD : 0.1m: VDD, the output is

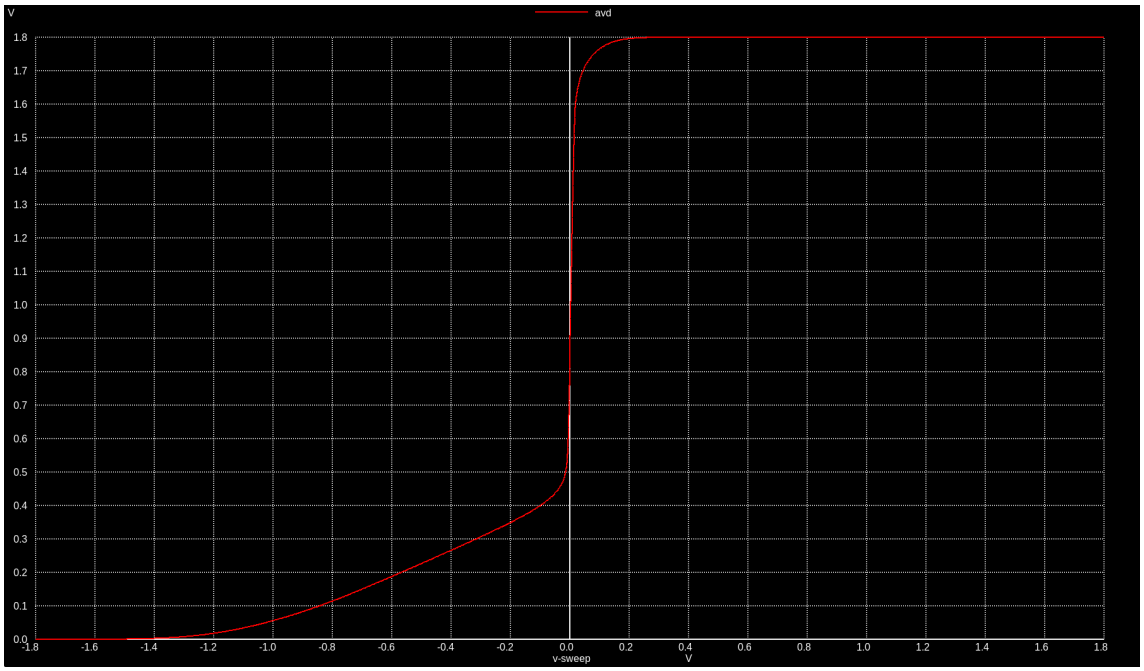


Figure 8. V_{out}Vs V_{id} Large Signal

V_{out} at $V_{\text{id}} = 0$ equals 0.859 V.

that's because at $v_{\text{id}} = 0$,V_{out} follows Current Mirror Node which equals VDD-V_{SG}=0.859V

Now for small signal gain:

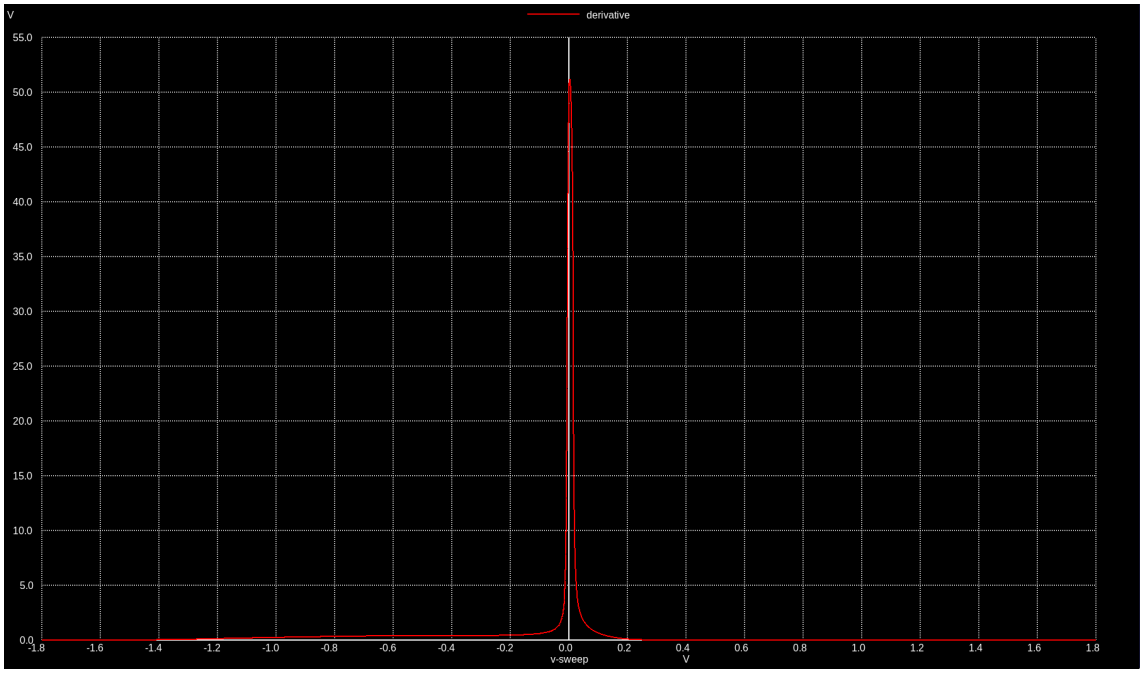


Figure 9. Small Signal Open Loop gain

Here gain at $V_{\text{id}} = 0$ equals 51.0345V, A_{vd}=50.2

2.2.2 Large Signal Common Mode:

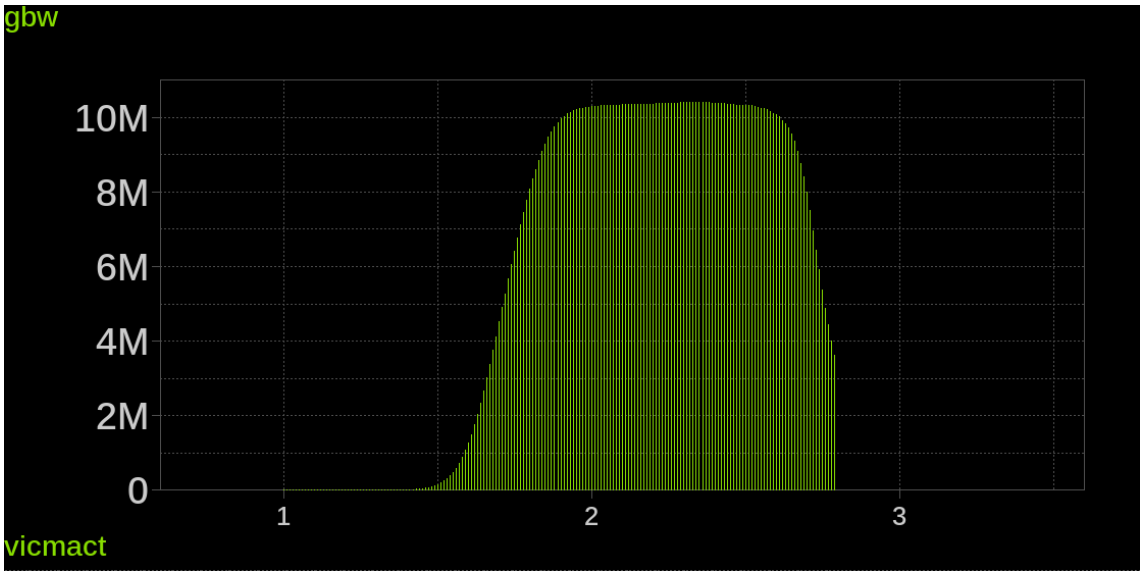


Figure 10. GBW Vs VICM

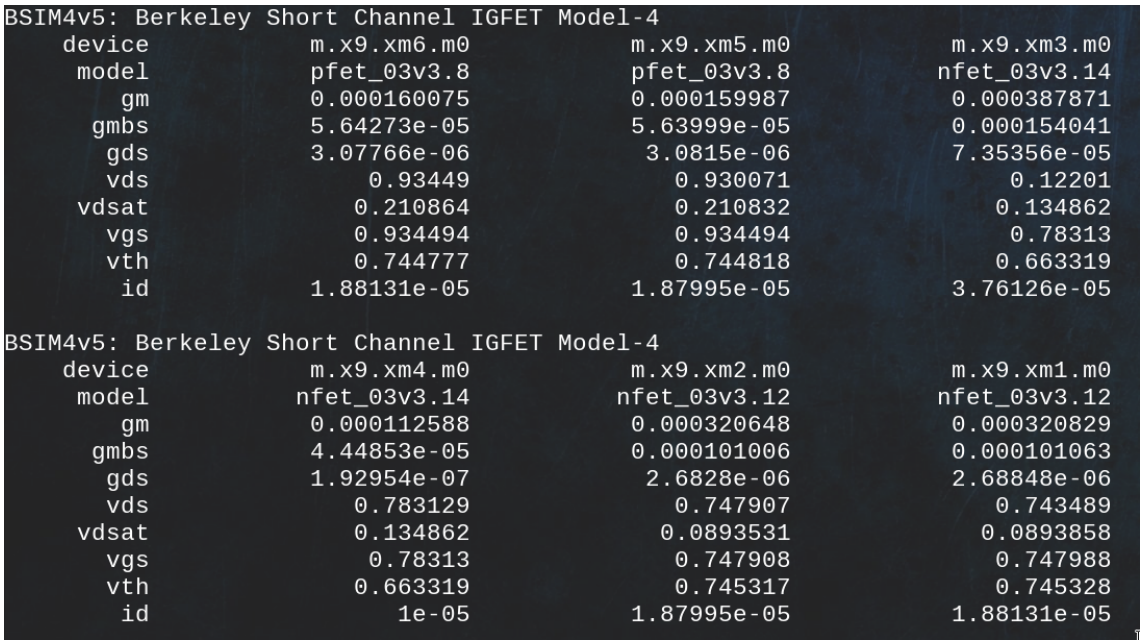
$\text{VICM}_{\text{min}} = 0.82V$ and $1.65V$

VICM is calculated for $90\langle\%\rangle$ GBW

3 Closed Loop OTA Simulation:

3.1 OP and Mismatch

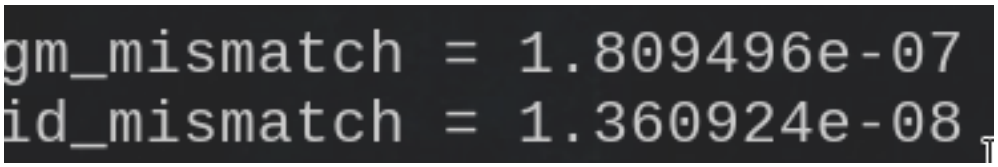
Operating Point analysis at VICM = 0.87 (CMIR Low + 50mv)



```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x9.xm6.m0          m.x9.xm5.m0          m.x9.xm3.m0
     model          pfet_03v3.8          pfet_03v3.8         nfet_03v3.14
        gm          0.000160075          0.000159987          0.000387871
      gmbs          5.64273e-05          5.63999e-05          0.000154041
       gds          3.07766e-06           3.0815e-06          7.35356e-05
       vds              0.93449              0.930071              0.12201
     vdsat             0.210864             0.210832             0.134862
       vgs             0.934494             0.934494              0.78313
       vth             0.744777             0.744818             0.663319
        id          1.88131e-05          1.87995e-05          3.76126e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device          m.x9.xm4.m0          m.x9.xm2.m0          m.x9.xm1.m0
     model         nfet_03v3.14         nfet_03v3.12         nfet_03v3.12
        gm          0.000112588          0.000320648          0.000320829
      gmbs          4.44853e-05          0.000101006          0.000101063
       gds          1.92954e-07           2.6828e-06          2.68848e-06
       vds             0.783129             0.747907              0.743489
     vdsat             0.134862            0.0893531             0.0893858
       vgs              0.78313             0.747908              0.747988
       vth             0.663319             0.745317              0.745328
        id                1e-05          1.87995e-05          1.88131e-05
```

Figure 11. Operating point results.



```
gm_mismatch = 1.809496e-07
id_mismatch = 1.360924e-08
```

Figure 12. Mismatch between Input Pair

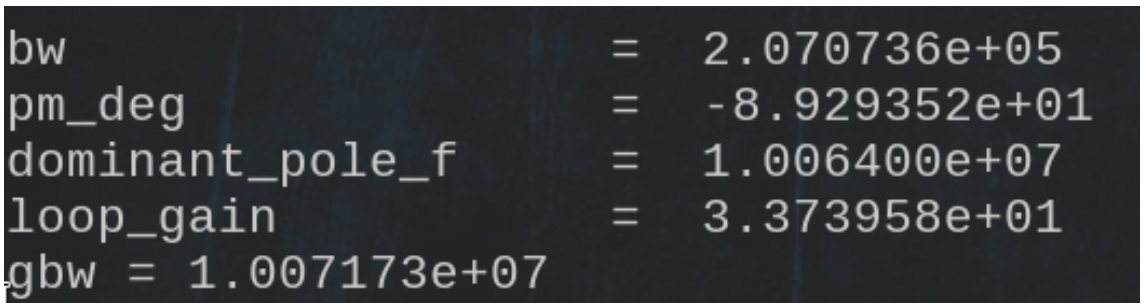
There is a mismatch between Input pair current because there is differential compoent v_{id}, Lets assume that's the output is the output at $v_{\text{id}} = 0$, then $V_{\text{out}_{\text{CM}}} = 0.8655$ (1.8-V_{GS}) shown previously but $v_+ = 0.87$, then $v_{\text{id}} = \frac{V_{\text{out}} - V_{\text{out}_{\text{CM}}}}{50}$, (since $V_{\text{CM}_{\text{min}}}$ is close to $V_{\text{out}_{\text{CM}}}$ the mismatch is so small).

Mismatch in $\Delta I_d = v_{\text{id}}\, g_{m_{1,2}} = 28n$.

$$\Delta g_m = g_{m_1} - g_{m_2} = \sqrt{2k_n(I_D + \Delta I_D)} - \sqrt{2k_n(I_D)} = \frac{\sqrt{2K_n(I_D) + 2K_n(\Delta I_D)}}{\sqrt{2K_n I_D}}\, g_m - g_m$$

$$\Delta g_m = \sqrt{1 + \frac{\Delta I_D}{I_D}}\, g_m - g_m = \sqrt{1 + \frac{28n}{18.8}}\, 320\mu - 320\mu = 0.23\mu = 2.3 \times 10^{-7}$$

3.2 Loop Gain



```
bw                    =  2.070736e+05
pm_deg                =  -8.929352e+01
dominant_pole_f       =  1.006400e+07
loop_gain             =  3.373958e+01
gbw = 1.007173e+07
```

Figure 13. Loop AC Paramters

DC gain Open Loop = 50.2 , DC gain closed loop = 48.4, GBW open loop = 10MHz = Closed Loop.

Analysis:

1. DC loop Gain = $\beta A_{\mathrm{OL}} = A_{\mathrm{OL}} = 50$
2. BW = 206.6KHz
3. Closed Loop Bandwidth = $\mathrm{BW}(1+\beta A_{\mathrm{OL}}) = 10.5\mathrm{MHz}$
4. GBW = BW (since $\beta = 1$) = 10.5MHz
5. PM : $-\tan^{-1}\frac{\omega_{p2}}{w_i} = -\tan^{-1}\frac{833M}{10.5} = -89.27$

	Analysis	Simulation
DC Loop Gain	50	48
BW	206.6KHz	207KHz
Dominant Pole (Close Loop BW)	10.5MHz	10MHz
GBW	10.5MHz	10MHz
PM	-89	-89

Table 9. Analysis Vs Simulation Closed Loop AC paramters

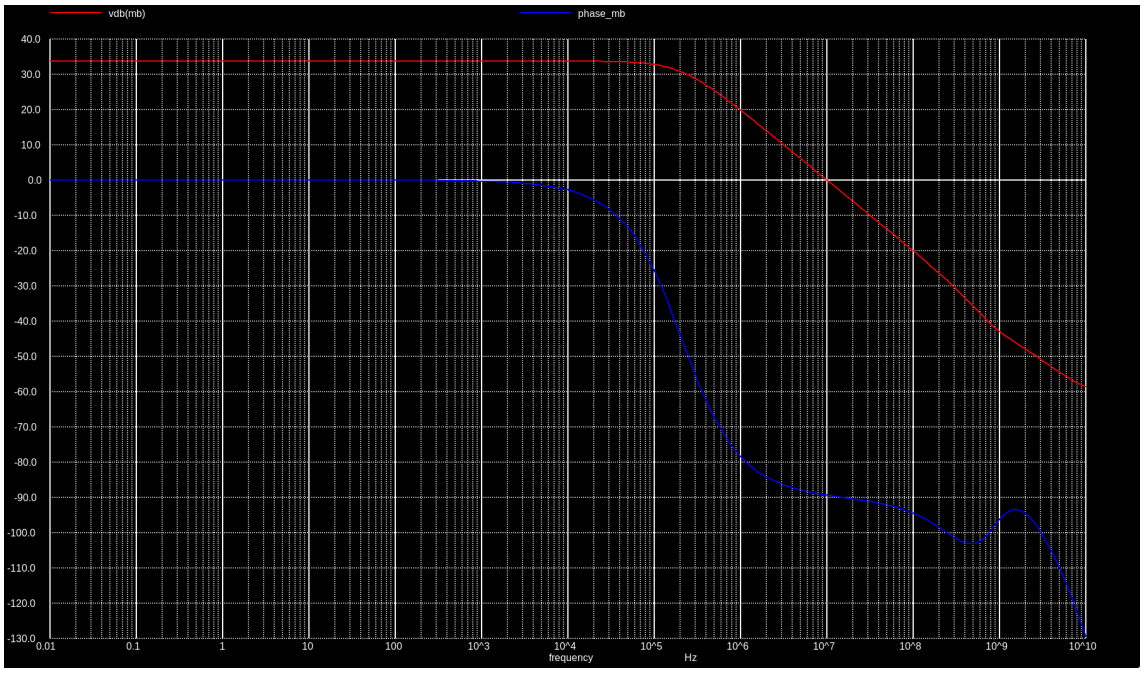


Figure 14. Loop Gain and Phase Margin

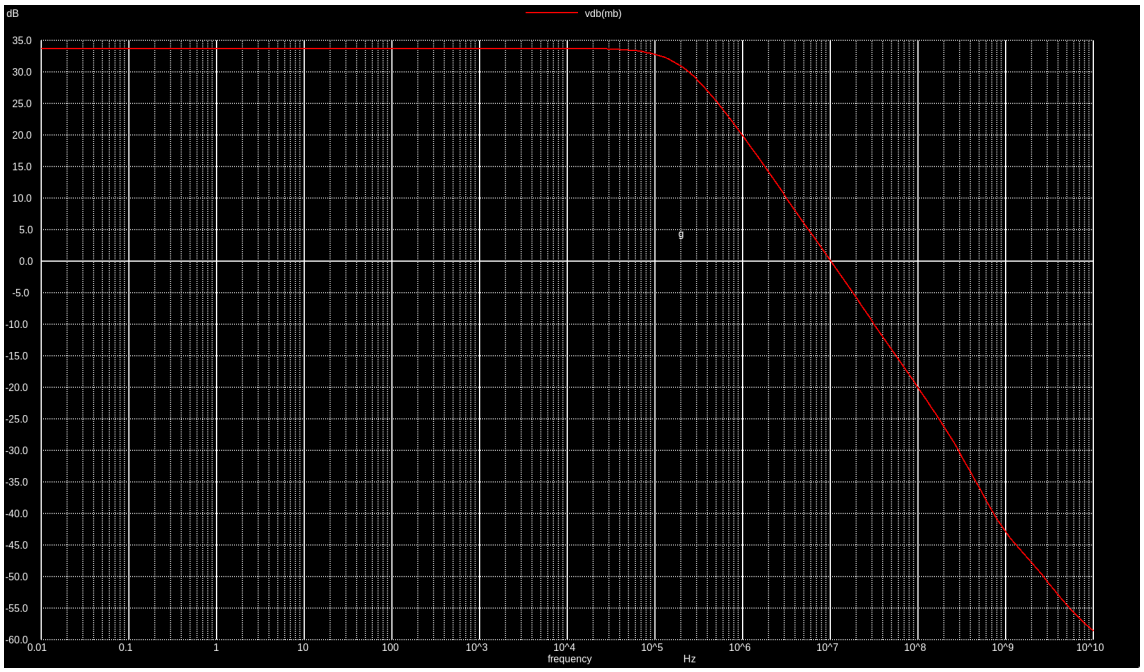


Figure 15. Loop Gain Bode plot

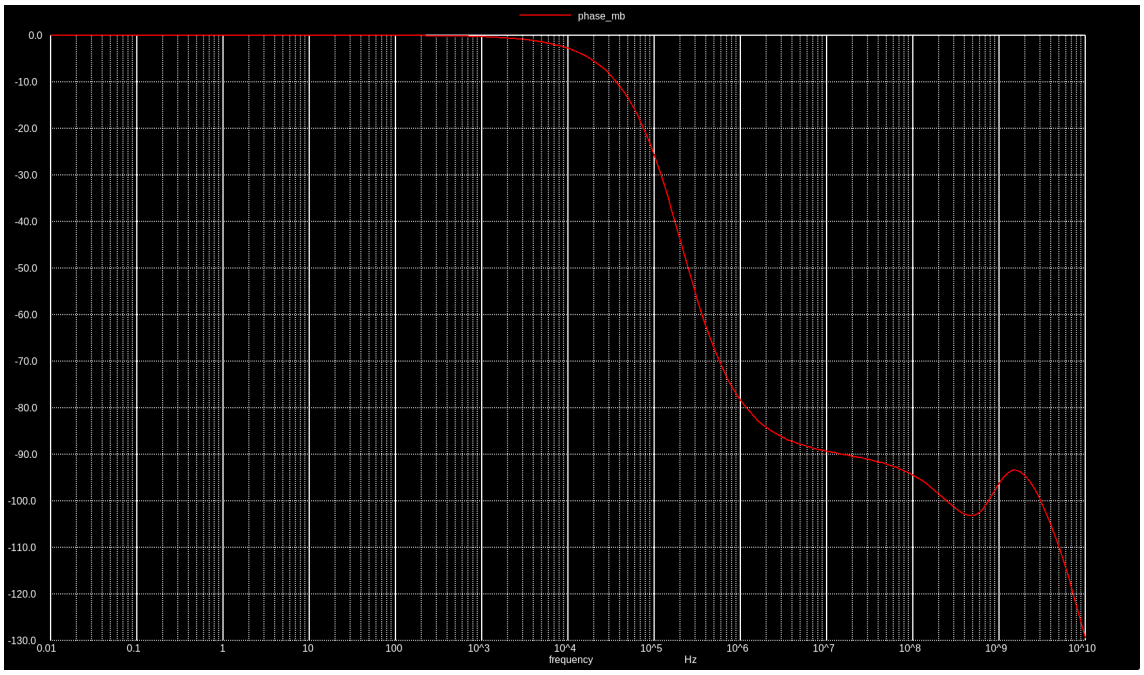


Figure 16. Loop Gain Phase plot.

Operating Point :

```
BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x9.xm6.m0          m.x9.xm5.m0          m.x9.xm3.m0
     model           pfet_03v3.8          pfet_03v3.8         nfet_03v3.14
        gm          0.000167482          0.000158384          0.000447859
      gmbs          5.90904e-05          5.62031e-05           0.00017693
       gds          3.27676e-06          3.93255e-06          1.06212e-06
       vds              0.94483             0.557565             0.409805
     vdsat             0.219295             0.216415             0.134862
       vgs             0.944834             0.944835              0.78313
       vth             0.744682             0.748255             0.663319
        id          2.05395e-05          1.91675e-05           3.9707e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4
    device           m.x9.xm4.m0          m.x9.xm2.m0          m.x9.xm1.m0
     model          nfet_03v3.14         nfet_03v3.12         nfet_03v3.12
        gm          0.000112588          0.000325194          0.000342494
      gmbs          4.44853e-05          8.87802e-05          9.35409e-05
       gds          1.92954e-07          2.67243e-06          3.48829e-06
       vds             0.783129             0.832618             0.445353
     vdsat             0.134862            0.0913452             0.094572
       vgs              0.78313             0.832619             0.840193
       vth             0.663319             0.828016             0.829047
        id                1e-05          1.91675e-05          2.05395e-05
```

Figure 17. Operating Point