Cadence Tools

Lab 11

Fully Differential Folded Cascode OTA

1 Design Charts

1.1 PMOS Design charts

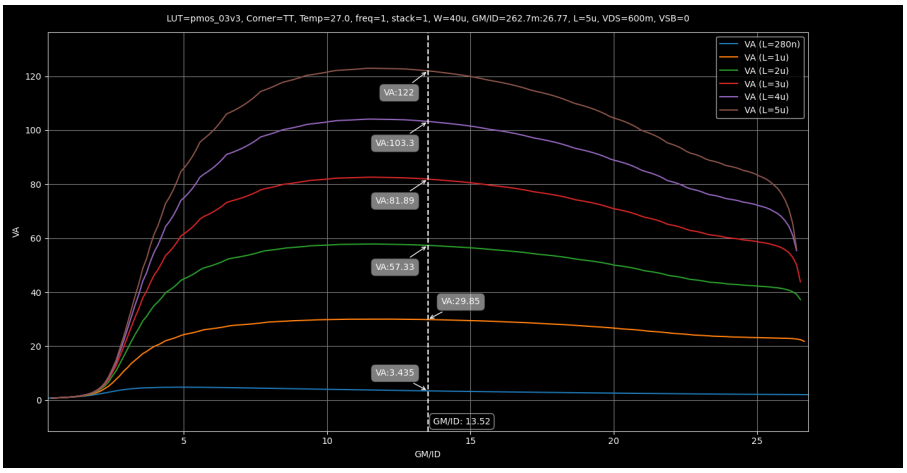

Figure 1: VA VS $\frac{g_m}{I_D}$

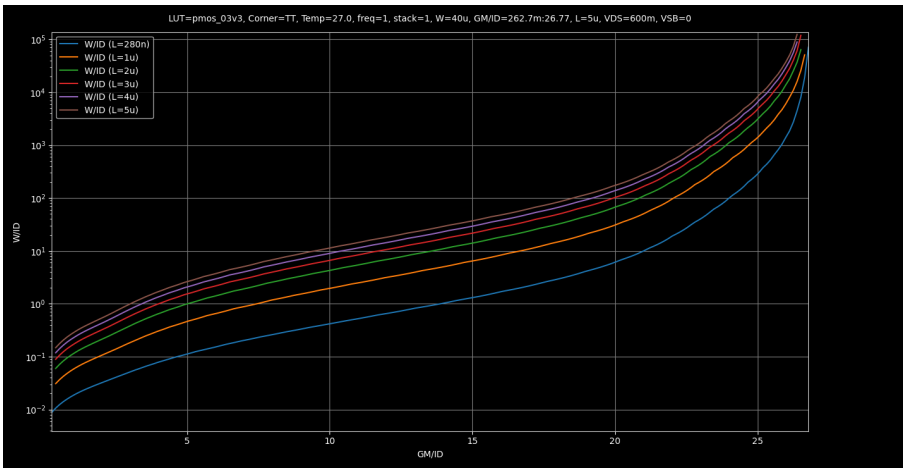

Figure 2: $\frac{W}{I_D}$ Vs $\frac{g_m}{I_D}$ (Log scale)

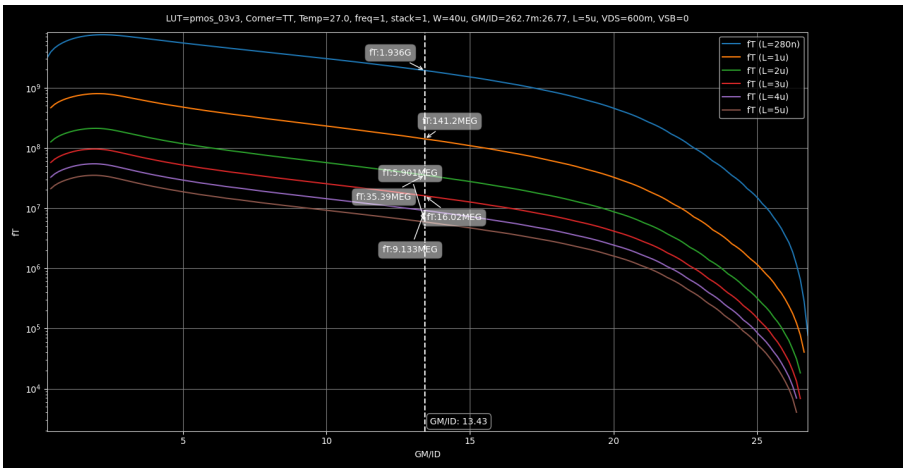

Figure 3: f_T Vs $\frac{g_m}{I_D}$ (log scale)

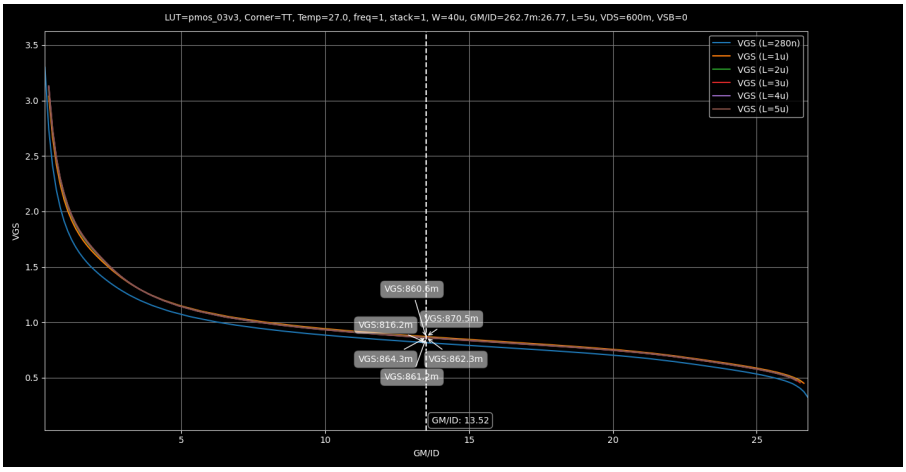

Figure 4: V_{GS} Vs $\frac{g_m}{I_D}$

1.2 NMOS

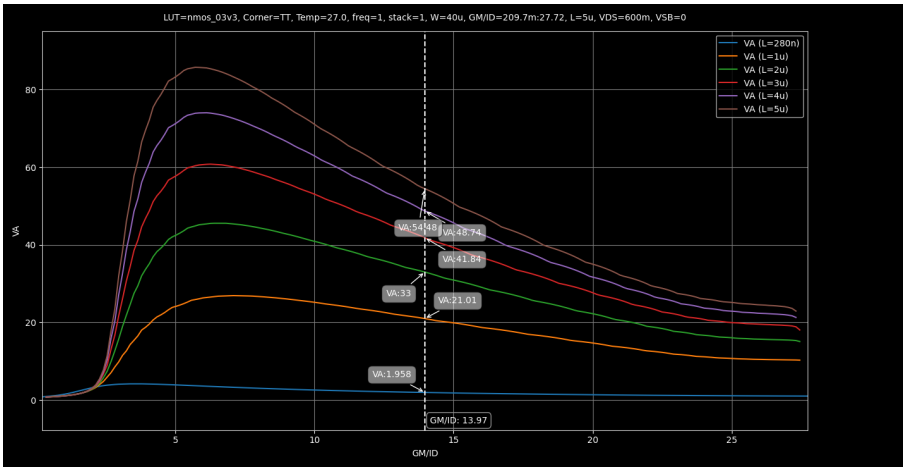

Figure 5: VA Vs $\frac{g_m}{I_D}$

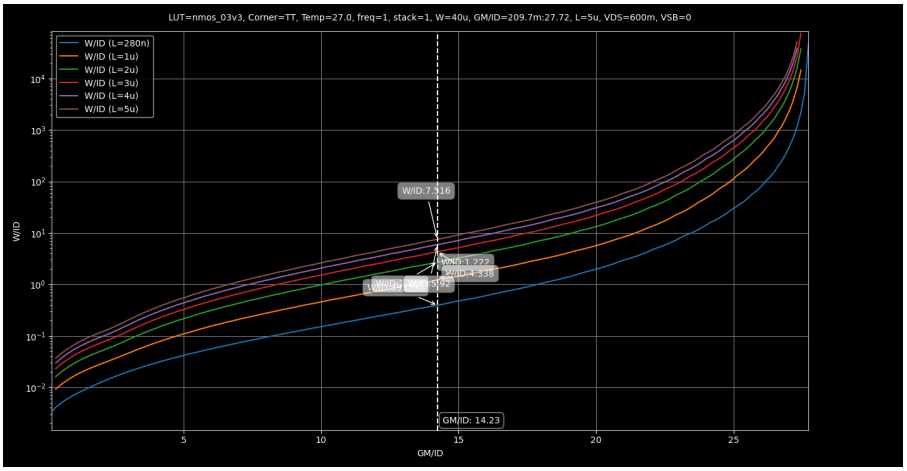

Figure 6: $\frac{W}{I_D}$ Vs $\frac{g_m}{I_D}$ (Log Scale)

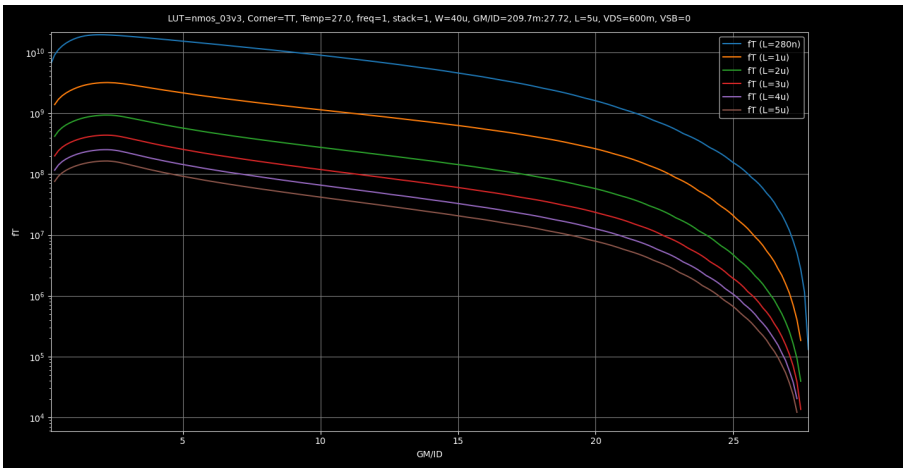

Figure 7: f_T Vs $\frac{g_m}{I_D}$ (Log scale)

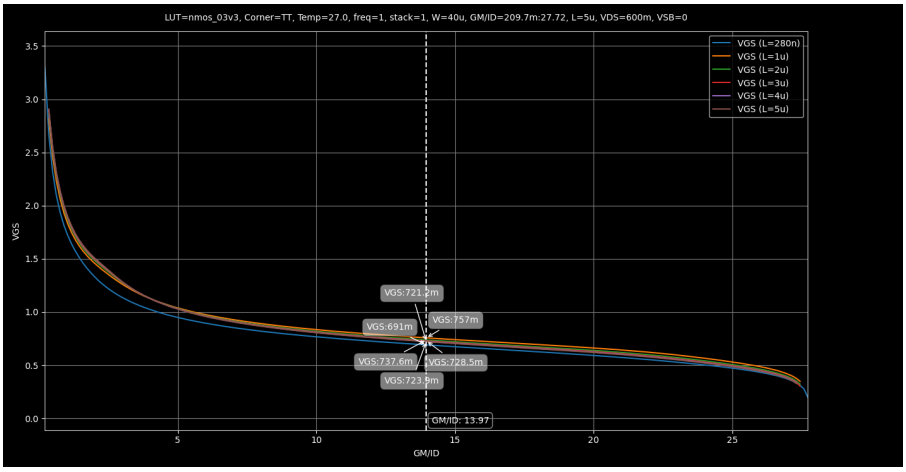

Figure 8: V_{GS} Vs $\frac{g_m}{I_D}$

2 Sizing

Technology	**0.13um**	**GF180MCU**
Supply voltage	1.2V	2.5V
Closed loop gain	2	2
Phase margin at the required ACL	$\geq 70^{\circ}$	$\geq 70^{\circ}$
CM input range – low	≤ 0	≤ 0
CM input range – high	≥ 0.6V	≥ 1V
Differential output swing	0.6Vpk-to-pk	1.2Vpk-to-pk
Load	500fF	500fF
DC Loop gain	50dB	60dB
CL settling time for 1% error	100ns	100ns

Table 1: Specifications table

2.1 Folded Cascode OTA sizing

2.1.1 Input pair Sizing:

First thing from the spec of setteling time 100ns for 1% error , we can get a spec on the closed loop bandwidth BW $\approx \frac{4.6}{2\pi t_r} = 7.32\,\text{MHz}$, since the Closed Loop DC gain = 2 ,then $\text{GBW}_{\text{CL}} = 14.6M$, now for open loop GBW must be larger to account for loading effects , $g_m > \text{GBW}_{\text{CL}}\, 2\pi \times (\sim 1.17p) = 107\,\text{uS}$, but we will take a big margin (because of parasitic caps and transient spikes) $g_m = 150\,\text{uS}$, now choosing $\frac{g_m}{I_D} = 20$for the input pair making $I_D = 7.5\,\text{uA}$ for the input pair, we will choose minimum L for the input pair to reduce it's area and capacitance, we will assume 500mv vdsat margin for the tail source making $V_{\text{sb}} = 500\,\text{mv}$.

Parameter	Value
ID	7.5u
IG	NaN
L	280n
W	41.5u
VGS	855.3m
VDS	500m
VSB	500m
gm/ID	19.77
Vstar	101.2m
fT	524.4M
gm/gds	42.64
VA	2.157
ID/W	180.7m
gm/W	3.572
AREA	11.62p
gm	148.3u
gmb	36.67u
gds	3.477u
ro	287.6k
VTH	875.4m
VDSAT	75.99m
cgg	44.99f
cgs	29.46f
cgd	6.266f
cgb	9.265f
cdb	-4.342f
csb	25.52f

Table 2: Input pair sizing

2.1.2 NMOS Current Source (Folding Node)

For the CG branch , we will use split ratio of 3 , meaning the current in this branch will equal 2.5uA, In that case the current in this Current source would equal to 10uA, Here We start by choosing W ,why? because of the bias branch that bais this source , we need the current in this branch to be minmum $\sim 1.25\,\text{uA}$, so it's reasonable to choose W=8u so that W/8=1u (reasonable width). aslo we have Choose L = 800n , to get a reasonable g_{ds} and $\frac{g_m}{I_D}$, we chose V_{ds} to be equal to 300mv

Parameter	Value
ID	10u
IG	NaN
L	800n
W	8u
VGS	772.8m
VDS	300.8m
VSB	0
gm/ID	13.2
Vstar	151.5m
ft	1.165G
gm/gds	9.778
VA	129.1
ID/W	16.5
gm/W	1.25
AREA	6.4p
gm	132u
gmb	49.67u
gds	1.023u
ro	977.8k
VTH	693.2m
VDSAT	126.7m
CGG	18.03f
CGS	1.615f
CGD	1.233f
Cgd	4.082f
Cdb	-5.771f
Csb	-5.771f
idnth2	1.606e-24
vgnth2	8.497e-24
idnfl2	92.19e-18
vgnfl2	6.069e-18

Table 3: Sizing of NMOS Current Source

2.1.3 Cascode NMOS

For the Cascode , the most important this is to get the required R_{out} , frrom the Loop gain Spec. we need LG = 1000 , meaning $A_{\text{OL}} > 3000$, from the previous sizing of input pair and NMOS source , we get that $g_{\text{ds}} \approx 4.5\,\text{uS}$, we $\frac{g_{m_{\text{input}}}}{g_{\text{ds}}} \frac{g_m}{g_{\text{ds}}}|_{\text{cascN}} \approx 4000 \sim 6000$ because of the other parrelle branch, $\frac{g_m}{g_{\text{ds}}} = 120$ sounds reasonable here ratio ~ 4000. Second thing what $\frac{g_m}{I_d}$ to choose ? as we will show later in the design of CMFB LOOP , $V_{\text{out}_{\text{min}}} < 600\,\text{mv}$, we take 300mv for the NMOS current source , we now have 300mv , we can choose $V^* = 200\,\text{mv}$, but the width was very small close to minimum so in the end $\frac{g_m}{I_D} = 15$.

Parameter	Value
ID	2.5u
IG	NaN
L	480n
W	1.79u
VGS	846.3m
VDS	600m
VSB	300m
gm/ID	14.77
Vstar	135.4m
FT	2.384G
gm/gds	118.4
VA	8.013
ID/W	1.397
gm/W	20.63
AREA	859.2f
gm	36.93u
gmb	10.99u
gds	312n
ro	3.205M
VTH	803.1m
VDSAT	111.5m
cgg	2.466f
cgs	1.5481
cgd	345.8e-18
cdb	572e-18
csb	1.41f

Table 4: NMOS Cascode Sizing

2.1.4 PMOS Cacode

Similarly, for PMOS we choose $\frac{g_m}{g_{\text{ds}}} = 120$,$\frac{g_m}{I_D} = 15$, $V_{\text{DS}} = 600\,\text{mv}$(it's should be 900mv but it's effect is small.

Parameter	Value
ID	2.5u
IG	NaN
L	410n
W	5.18u
VGS	956.2m
VDS	600m
VSB	300m
gm/ID	14.75
Vstar	135.6m
IT	737.3M
gm/gds	117.2
VA	7.943
ID/W	482.6m
gm/W	7.12
AREA	2.124p
gm	36.88u
gmb	12.98u
gds	314.7n
ro	3.177M
VTH	892.9m
VDSAT	115.3m
cgg	7.962f
cgs	5.72f
cgd	820.3e-18
cdb	1.421f
csb	-2.487f
idnth2	454.5e-27
vgnth2	334.1e-18
idnfl2	1.377e-18

Table 5: PMOS Cascode

2.1.5 PMOS Source CG branch

In this branch current is equal to 2.5uA , and for the bais branch $\sim 1.25\,\text{uA}$, using for this current source Vds = 400mv , we also chose W=2u , so that in the bais branch W=1u, also we need to get the required gain ~ 3000 , here we find that L=400n is reasonable ($A_{\text{OL}} = 3700$).

Parameter	Value
ID	2.5u
IG	NaN
L	400n
W	2u
VGS	915m
VDS	400m
VSB	0
gm/ID	10.71
Vstar	186.8m
FT	1.348G
gm/gds	72.3
VA	6.751
ID/W	1.25
gm/W	13.39
AREA	800f
gm	26.77u
gmb	11.09u
gds	370.3n
ro	2.701M
VTH	777.5m
VDSAT	163.1m
cgg	3.16f
cgs	2.273f
cgd	331.1e-18
cdb	556.3e-18
csb	-981.9e-18
idnth2	324.5e-27
vgnth2	452.7e-10
idnfl2	2.155e-18

Table 6: PMOS source CG branch sizing

2.1.6 Input Tail Current Source

for the tail current source , L is the same for the PMOS Current source and also V_{GS} is same, in fact it's size should equal 12u (since the current is 15uA)

Parameter	Value
ID	15u
IG	NaN
L	400n
W	11.79u
VGS	915m
VDS	400m
VSB	0
gm/ID	10.71
Vstar	186.7m
FT	1.348G
gm/gds	72.31
VA	6.751
ID/W	1.272
gm/W	13.63
AREA	4.716p
gm	160.6u
gmb	66.51u
gds	2.222u
ro	450.1k
VTH	777.5m
VDSAT	163.96m
cgg	18.64f
cgs	13.987f
cgd	1.987f
cdb	-3.338f
csb	5.892f
idnth2	10.947e-24
vgnth2	75.45e-18
idnfl2	12.936e-18

Table 7: Sizing of tail Current Source

2.2 Common Mode Feedback Loop

First we choose current for the input stage , since max Swing = 1.2V , meaning $V_{\text{out}}^{+} - V_{\text{out}}^{-} < 0.6$, Assume $R_{\text{sense}} = 100k$, then $I = 3\,\text{uA}$ for each branch.

2.2.1 Input pair (CD) (first stage)

the most important thing here is $V_{\text{out}_{\max}}$which we choose to be 1.2V , we need $V_{\text{out}_{\max}} < V_{\text{DD}} - V_{\text{GS}} - V_{\text{DS}}$, $V_{\text{out}_{\max}} = 2.5 - 0.9 - 0.4 = 1.2V$, so we choose $V_{\text{GS}} = 900\,\text{mv}$, we also chose minimum L.

Parameter	Value
ID	2.984u
IG	NaN
L	280n
W	900m
VGS	1.5
VDS	0
VSB	8.881
gm/ID	3.2m
Vstar	225.2m
FT	3.83G
gm/gds	51.37
VA	5.784
ID/W	3.315
gm/W	29.44
AREA	252f
gm	26.5u
gmb	8.685u
gds	515.8n
ro	1.939M
VTH	722.4m
VDSAT	203.3m
cgg	1.101f
cgs	765.8e-18
cgd	123.2e-18
cdb	-246.1e-18
csb	690.8e-18
idnth2	270.7e-27
vgnth2	385.5e-18
idnfl2	10.54e-18

Table 8: Sizing of Input pair (first stage)

2.2.2 PMOS current source (first stage)

for PMOS current source V_{gs} and L are the same for all PMOS sources , here the current 3uA.

Parameter	Value
ID	3.00u
IG	NaN
L	400n
W	2.36u
VGS	915m
VDS	400m
VSB	0
gm/ID	10.71
Vstar	186.7m
FT	1.348G
gm/gds	72.31
VA	6.751
ID/W	1.272
gm/W	13.63
AREA	944f
gm	56.1u
gmb	13.31u
gds	444.7n
ro	2.249M
VTH	777.5m
VDSAT	163.1m
cgg	3.796f
cgs	2.73f
cgd	397.7e-18
cdb	668.2e-18
csb	-1.179
idnth2	3.079e-27
vgnth2	376.9e-18
idnfl2	2.589e-18

Table 9: PMOS source (first stage) sizing

2.2.3 Current Mirror Load (Second stage)

We choose the current to be 1.25uA , as for all PMOS L and Vgs are the same.

2.2.4 Input pair (second stage)

here we want to get $g_m \sim 2g_{m_{\text{CM}}}$ since we want the DC gain to be approximatly 1 , we choose also minimum L and vsb=400mv (because it's NMOS).

Parameter	Value
ID	1.252u
IG	NaN
L	400n
W	930n
VGS	915m
VDS	0
VSB	10.66
gm/ID	187.7m
Vstar	1.429G
FT	119
gm/gds	1.347
VA	11.17
ID/W	372
gm/W	13.5
AREA	5.516u
gm	112.1n
gmb	8.918M
gds	776m
ro	164.2m
VTH	1.074f
VDSAT	486f
cgg	266e-18
cgs	504e-18
cgd	156.6e-18
cdb	819.5e-18
csb	667.8e-18
idnth2	1.271e-18

Table 10: CM Load (second stage) sizing

Parameter	Value
ID	1.25u
IG	NaN
L	280n
W	770n
VGS	724m
VDS	915m
VSB	400m
gm/ID	15.94
Vstar	125.5m
FT	4.01G
gm/gds	26.48
VA	1.662
ID/W	1.623
gm/W	25.87
AREA	215.6f
gm	19.92u
gmb	3.364u
gds	752.3n
ro	1.320M
VTH	714.5m
VDSAT	91.39m
cgg	790.7e-18
cgs	537.3e-18
cgd	122.4e-18
cdb	131.1e-18
csb	37.32e-18

Table 11: Input pair (second stage) sizing

2.3 Sizing Summary

Sizing	Input Pair	Current Source N	Cascode N	Cascode P	Current Source P
W	41.5u	8u	1.79u	5.18u	2u
L	280n	800n	480n	410n	400n
Sizing	Tail current source	CS Bais N	CS Bias P	CS Ref P	
W	11.79u	$W_{\text{source }N}/8$	$W_{\text{source }P}/2$	$W_{\text{source }P}$*4	
L	400n	800n	400n	400n	

Table 12: Sizing of Folded Cascode

Sizing	Input buffer	Current source (Input)	Input second stage	CM Load	Tail source
W	900n	2.36u	770n	930n	2u
L	280n	280n	280n	400n	800n

Table 13: Sizing of CMFB Loop

$V_{\text{ref}} = 1.8V$, $V_{\text{outCM}} = 0.9$, $V_{\text{cascN}} = 1.15V$, $V_{\text{cascP}} = 1.15V$.

$-0.58V < V_{\text{ICM}} <$1.44V

$0.44V < V_{\text{out}} < 1.4V$

We will use $VICM_{nominal} = 0.5V$ and $VOUT_{CM} = 0.9V$

2.4 Actual Sizing after simulation:

Sizing	Input Pair	Current Source N	Cascode N	Cascode P	Current Source P
W	41.5u	9.5u	1.79u	5.18u	2u
L	280n	800n	420n	280n	400n
Sizing	Tail current source	CS Bais N	CS Bias P	CS Ref P	
W	11.79μ	0.9μ	$W_{\text{source }P}/2$	$W_{\text{source }P}$*4	
L	400n	800n	400n	400n	

Table 14: Actual Sizes of OTA

Sizing	Input buffer	Current source (Input)	Input second stage	CM Load	Tail source
W	900n	2.36u	770n	930n	2u
L	280n	280n	280n	400n	800n

Table 15: Actual Sizes of CMFB Loop

FOM Calculation

Area of OTA =53.48p

Area of CMFB =4.6p

Total area = 58.08p

From fig-18 total current=$52\mu A$, subtracting $10\mu A$

$I_{total} = 42\mu A$.

From fig-21, UGF = 23.69M

$FOM = 9.712KHz/(\mu A * pm^2)$

3 Open Loop Analysis

3.1 OP and AC analyis:

3.1.1 Behavioral CMFB:

Using Behavioral model for Common Mode Feedback Loop in fig.11, Doing OP point analysis using $V_{\text{Ref}} = 1.25V$ to maximize swing (this only for behavioral) , results are anotated in fig-9, fig-10 and fig-11.

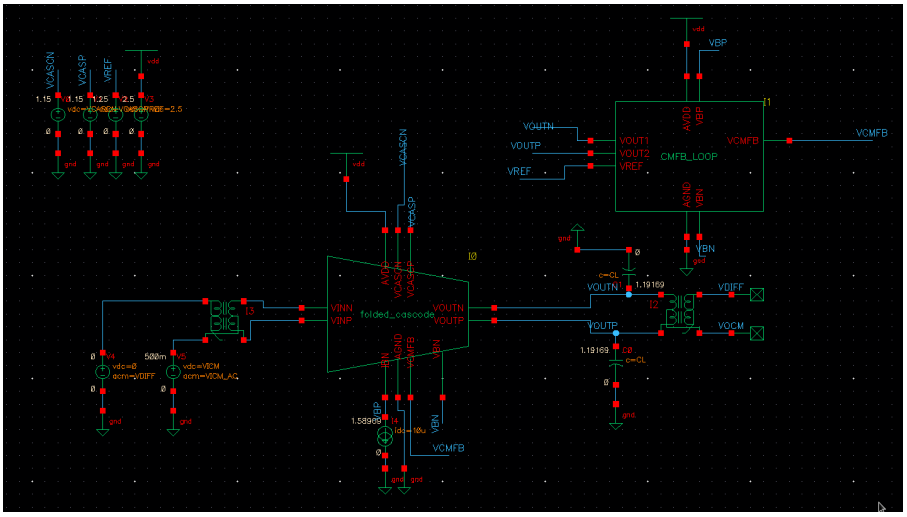

Figure 9: DC voltage Annotated (behavioral CMFB Loop)

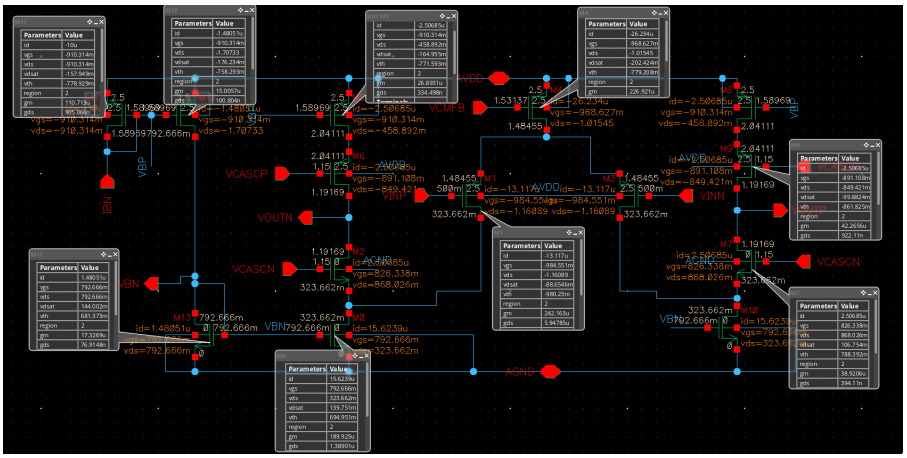

Figure 10: DC OP annotated for Folded Cascode

As Clearly shown in fig-11 $V_{\text{outCM}} = 1.19V$, $V_{\text{id}} = 58\,\text{mv}$,$\Delta V_{\text{out}} = 58\,\text{mv}$,meaning $A_v = 1$ as expected.

The error between $V_{\text{CM}_{\text{out}}}$ and V_{ref} is large , that's because the tail current source for the

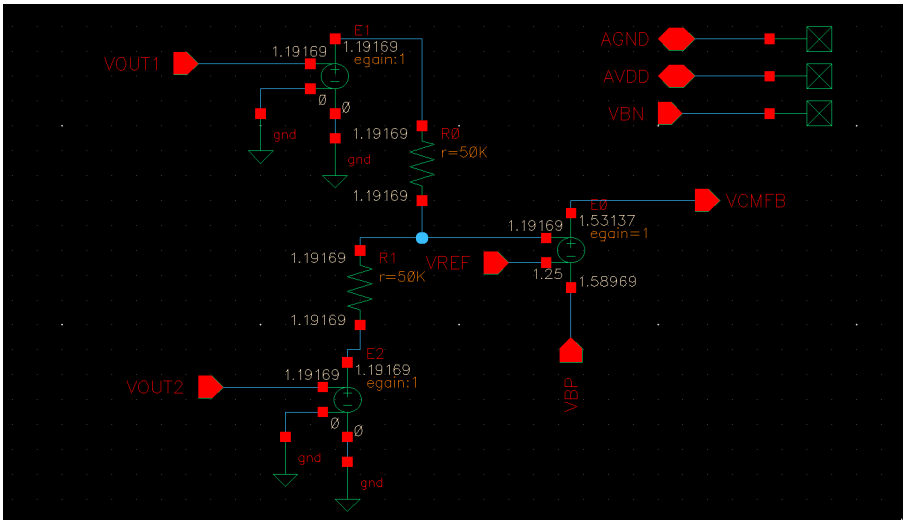

Figure 11: Op annotated CMFB Loop Behavioral

input stage of the OTA current is changed largely from the design step, without changing the sizing for the current source , this cahnged V_{gs} of this source from other PMOS current sources making it harder for the CMFB loop to minimize the error between V_{ref} and V_{outCM}, but this is not a big problem.

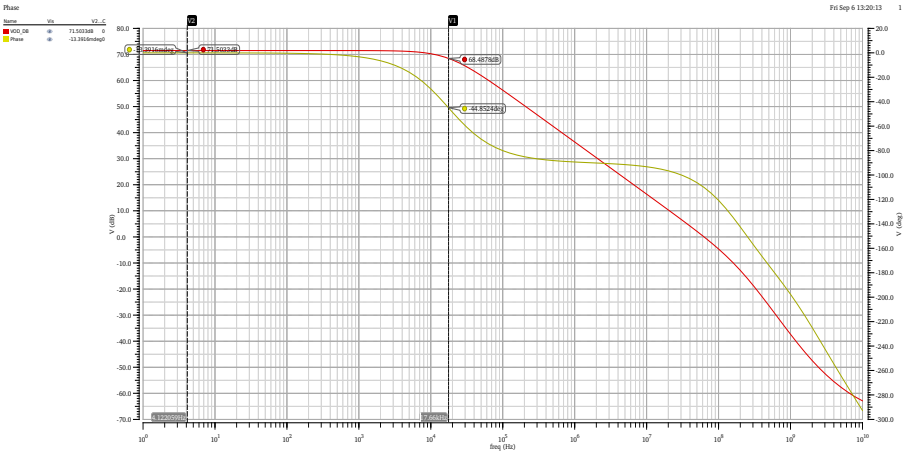

Figure 12: V_{OD} bode plot (DC gain = 71.5db)

AC Simulaion:

Analyis

- DC gain :

$$A_v = \frac{g_{m_{\text{input}}}}{(g_{\text{ds}_{\text{input}}} + g_{\text{ds}_{\text{Fold}}})\frac{g_{\text{ds}_{\text{cascN}}}}{g_{m_{\text{cascN}}}} + \frac{g_{\text{ds}_{\text{cascP}}}}{g_{m_{\text{cascP}}}}(g_{\text{ds}_{\text{current source }p}})} \approx 3200$$

Labs:lab11_folded_cascode:1	VOD_DB				
Labs:lab11_folded_cascode:1	DC_GAIN	3.76k			
Labs:lab11_folded_cascode:1	UGF	63M			
Labs:lab11_folded_cascode:1	GBW	66.54M			
Labs:lab11_folded_cascode:1	PM	69.81			
Labs:lab11_folded_cascode:1	Phase				
Labs:lab11_folded_cascode:1	BW	17.66k			

Figure 13: DC gain, UGF and GBW Behavioral CMFB Loop

- GBW $= \frac{g_{m_{\text{input}}}}{C_L 2\pi} = 76M$, more accurately $\frac{g_m \frac{g_{m_{\text{cascN}}}}{g_{\text{ds}_{\text{input}}} + g_{\text{ds}_{\text{fold}}} + g_{m_{\text{cascN}}}}}{C_L 2\pi} = 64.74M$
- BW $= \frac{\text{GBW}}{\text{DC gain}} = 20.2\,\text{KHz}$

	Simulation	Analysis
DC gain	3700	3200
GBW	66M	64M
UGF	63M	64M
BW	17.66kHz	20.2KHz

Table 16: DC gain , BW , GBW and UGF Comparison

3.1.2 With Actual CMFB LOOP

Here We use Actual CMFB Loop , there are Two Consideration, first $V_{\text{ref}} \approx V_{\text{OU}_{\text{CM}}} + V_{\text{GS}}$, second $\text{Vout}_{\text{max}} = 2.5 - V_{\text{GS}} - V_{\text{DS}} \approx 1.2V$, choosing minimum $V_{\text{out}_{\text{min}}} = 0.6$, $V_{\text{out}_{\text{CM}_{\text{Nominal}}}} = 0.9V$. now $V_{\text{ref}} = 1.8V$. Here OP results are anotatted in fig-14, fig-15 and fig-16.

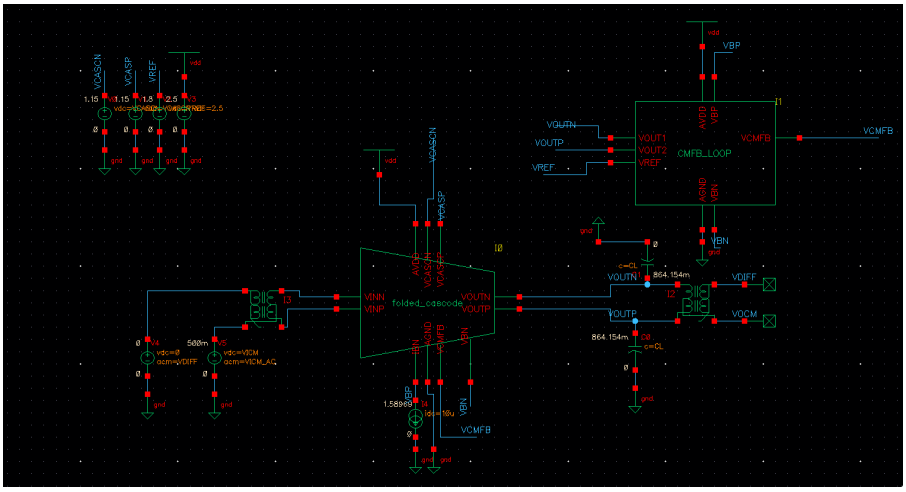

Figure 14: DC Voltage Anotatted

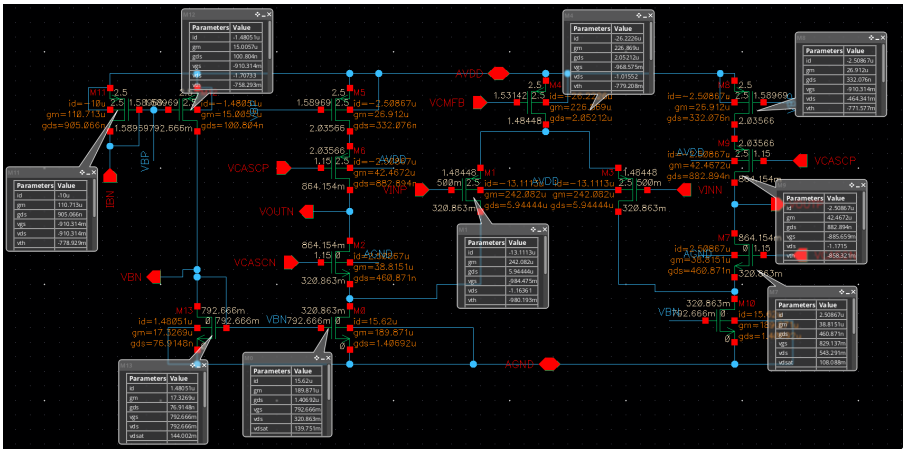

Figure 15: OTA OP point anotatted

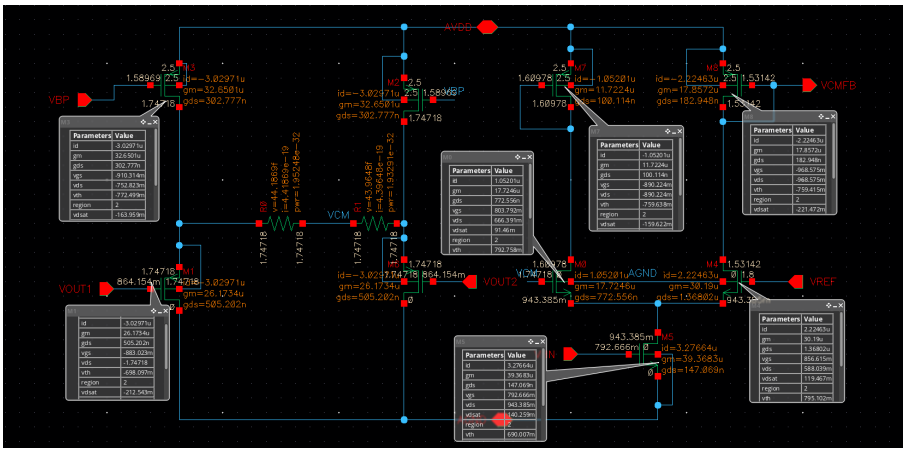

Figure 16: CMFB Loop OP annotated

As shown in fig-16 , $V_{\mathrm{OUT_{CM}}} = 0.864V$ less than expected that's beacuse V_{GS} of the input for CMFB Loop isn't exactly equal to 900mv it's equal to 883mv, also there's a finite error between V_{ref} and $V_{\mathrm{outCM}} + V_{\mathrm{GS}}$ also this error is small $\sim 53\,\mathrm{mv}$.

$V_{\mathrm{id}} = 53\,\mathrm{mv}$, $V_{\mathrm{OD}} = 78\,\mathrm{mv}$, which means $A_{\mathrm{ol}} = 1.47$,which is slightly larger than unity.

Labs:lab11_folded_cascode:2	PM	69.83			
Labs:lab11_folded_cascode:2	GBW	66.27M			
Labs:lab11_folded_cascode:2	VOD_DB				
Labs:lab11_folded_cascode:2	Phase				
Labs:lab11_folded_cascode:2	BW	20.23k			
Labs:lab11_folded_cascode:2	DC_GAIN	3.268k			
Labs:lab11_folded_cascode:2	UGF	62.92M			

Figure 17: DC gain ,GBW ,UGF and Phase Margin, using actual CMFB Loop

AC Simulation:

4 Closed Loop Simulaion

4.1 Operating Point Analysis

Now for Closed Loop Simulation, V_{CM} doesn't affect simulation results since $V_{\text{CM}_{\text{input}}} = V_{\text{CM}_{\text{out}}}$ regardless of V_{CM} that we choose, Here we will choose $V_{\text{CM}} = V_{\text{CM}_{\text{out}}} = 0.858V$ to make the offset of the graph is zero (to show the output clearly in Transient simulation).

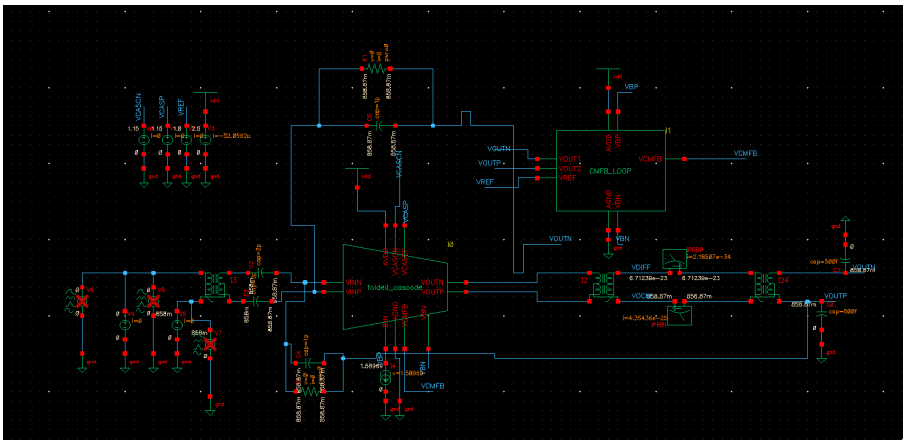

Figure 18: Schematic DC volatge annotated

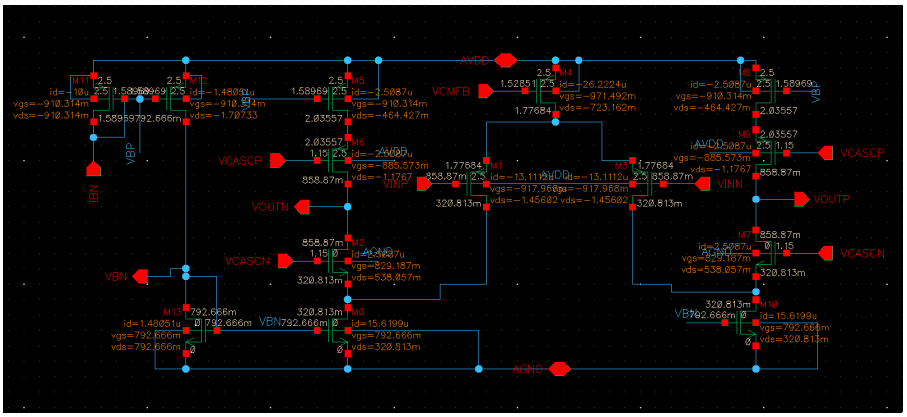

Figure 19: DC OP annotated OTA

as shown in fig-18 , $V_{\text{outCM}} = V_{\text{In}_{\text{CM}}} = 858.87\,\text{mv}$, always equal to each other becuase of the feedback, and because of CMFB Loop $V_{\text{out}_{\text{CM}}} \approx V_{\text{ref}} - 0.883$.

4.2 AC and STB analysis:

4.2.1 AC Closed Loop

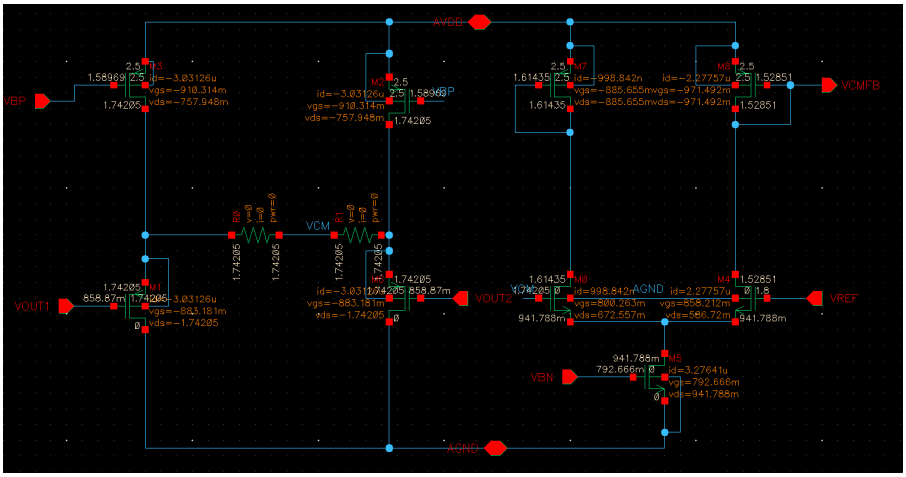

Figure 20: CMFB OP annotated

Labs:lab11_folded_cascode_Closed_Loop:1	GBW_CL	23.16M	
Labs:lab11_folded_cascode_Closed_Loop:1	PM_CL	72.75	
Labs:lab11_folded_cascode_Closed_Loop:1	VDIFF_CL		
Labs:lab11_folded_cascode_Closed_Loop:1	DC_GAIN_CL	1.998	
Labs:lab11_folded_cascode_Closed_Loop:1	BW_CL	11.71M	
Labs:lab11_folded_cascode_Closed_Loop:1	UGF_CL	23.69M	

Figure 21: GBW, BW and DC closed Loop gain

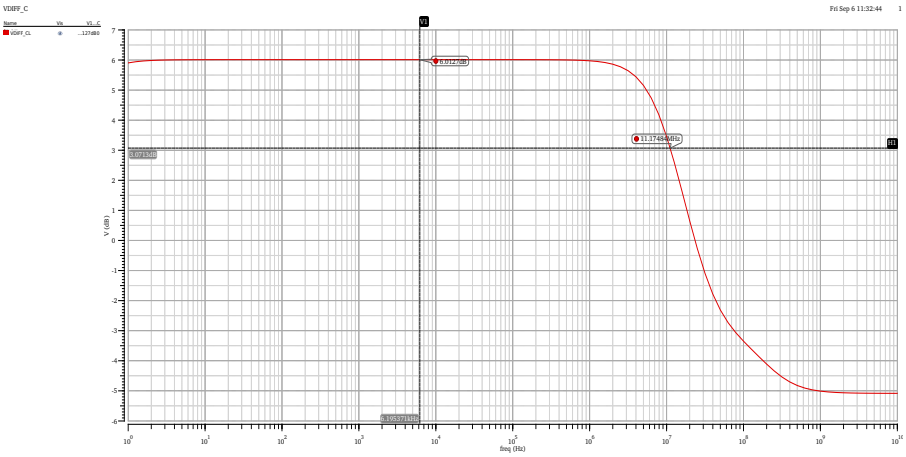

Figure 22: $V_{\text{out}_{\text{Diff}}}$ bode plot

4.2.2 STB Differential Loop gain

Now Doing STB analysis to get Loop gain and PM.

4.2.3 STB Common Mode Loop gain

Comments:

- DC loop gain for is Common Mode is larger than DC loop gain for Differential Mode ,

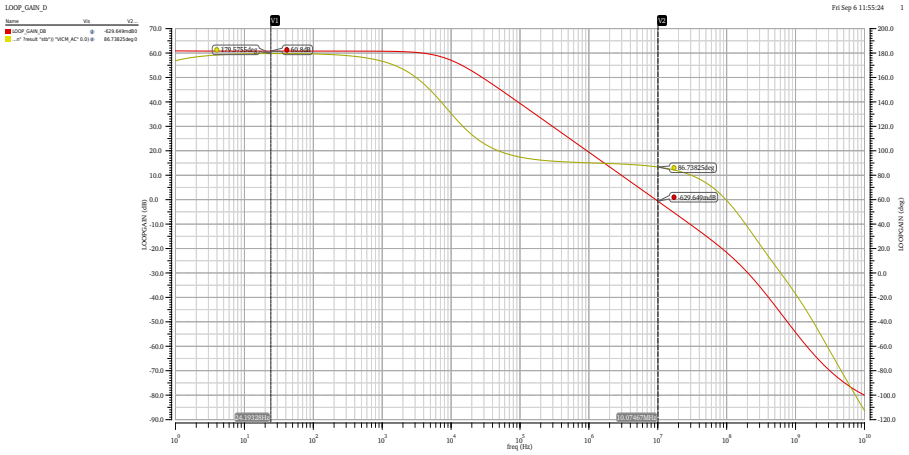

Figure 23: Differential Loop gain bode plot (mag. and phase)

Labs:lab11_folded_cascode_Closed_Loop:1	DC_LOOP_GAIN	1.109k			
Labs:lab11_folded_cascode_Closed_Loop:1	PM_LOOP_GAIN	-93.02			
Labs:lab11_folded_cascode_Closed_Loop:1	GBW_LOOP_GAIN	9.291M			

Figure 24: DC loop gain, PM and GBW

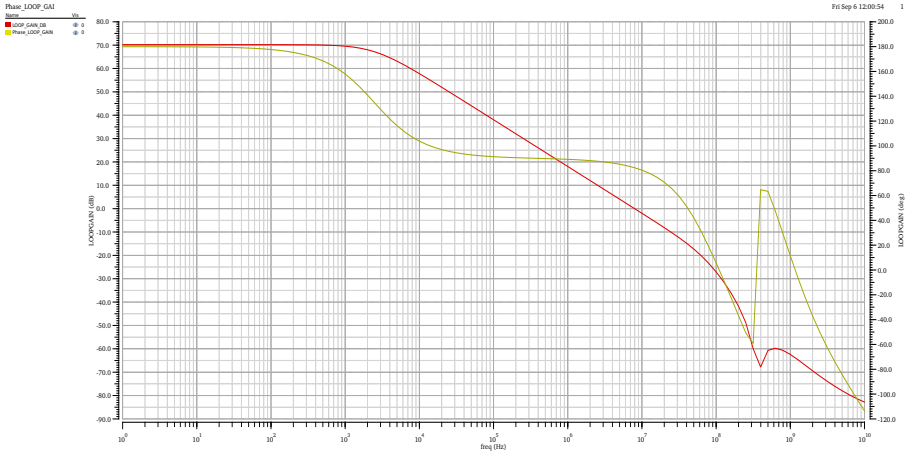

Figure 25: Common Mode Loop gain bode plot (mag. and phase)

Labs:lab11_folded_cascode_Closed_Loop:1	DC_LOOP_GAIN	3.248k			
Labs:lab11_folded_cascode_Closed_Loop:1	PM_LOOP_GAIN	-97.59			
Labs:lab11_folded_cascode_Closed_Loop:1	GBW_LOOP_GAIN	8.021M			

Figure 26: DC loop gain , PM , GBW

that's because for Differential Mode feedback circuit has $\beta \approx \frac{1}{3}$, and this not the case for Common Mode LG $\approx \frac{0.5 g_{m_{\text{tail source}}}}{g_{\text{ds}_{\text{source } P}} \frac{g_{\text{ds}_{\text{Cascp}}}}{g_{\text{mCascp}}} + g_{\text{ds}_{\text{folding source}}} \frac{g_{\text{ds}_{\text{CascN}}}}{g_{m_{\text{CascN}}}}} 0.5 A_{V_{\text{CMFB}}} \approx 3500.$

- GBW for Differential Mode is larger than GBW for Common Mode which is expected beacuse $\text{GBW}_{\text{CM}} = 0.5 g_{m_{\text{tail source}}} 0.5 A_{V_{\text{CMFB}}} / C_L \approx 7.6M$ and for $\text{GBW}_{\text{diff}} = \frac{G_m}{\beta C_L} \approx 10M$
- for PM both are Very Large because Capacitance are small and the dominant pole at the

output

- Comparing Open Loop Diff. with Closed Loop :

  DC LG : it's multiplied by the feedback factor $\approx \frac{1}{3}$,(Open Loop = 3200 , LG =1100)

  GBW: For GBW , C_L is higher for the feedback because of loading effects also GBW is muliplied by the feedback factor $\approx \frac{1}{3}$ (Open Loop = 66M , GBW Loop = 9.29M)

4.3 Transient Analyis:

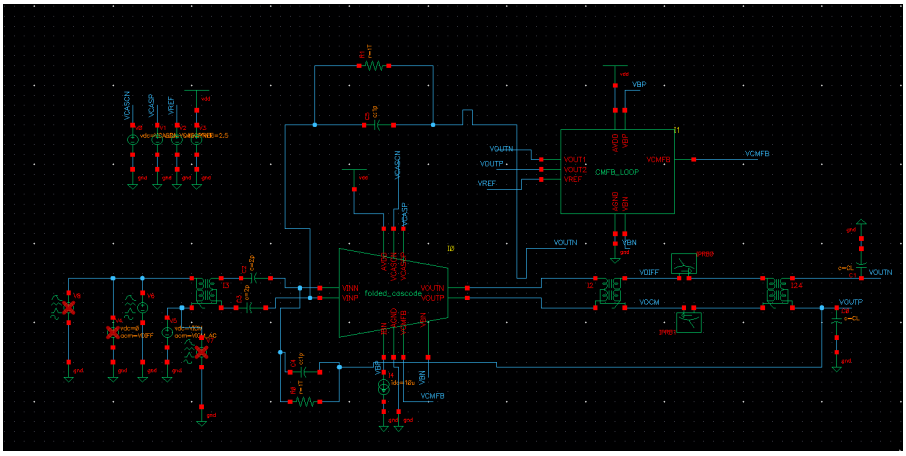

Figure 27: Schematic Diagram

4.3.1 Setteling Time and Differential Loop Stablity

Applying a differential pulse 100mv peak 10n rise time and 1u Pulse Width.

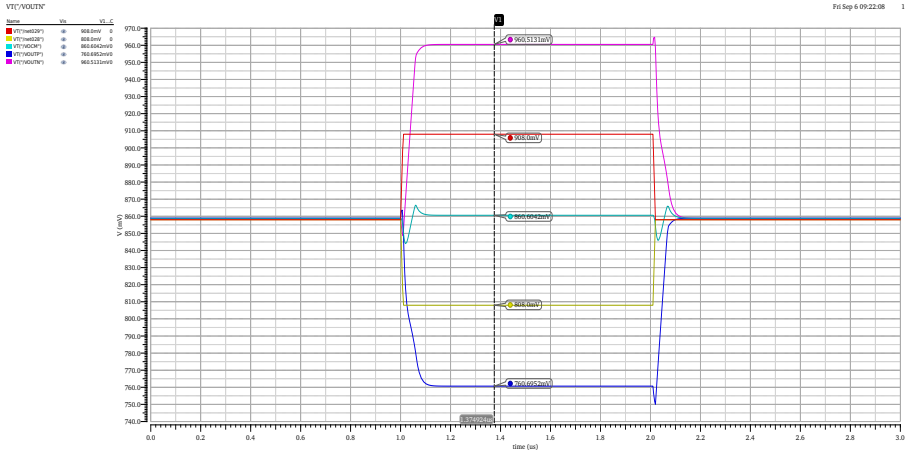

Figure 28: $V_{\text{in}}^{+}, V_{\text{in}}^{-}, V_{\text{out}}^{+}, V_{\text{out}}^{-}$ and $V_{\text{out}_{\text{CM}}}$ Vs time

From fig-28 , there is now differential ringing nor Common mode ringing except for a small spike, this is spike is due to capacitive coupling of the feedback loop (small $\frac{C_L}{C_s+C_f}$ ratio) and it's hard to avoid, maybe increasing the speed (GBW) of the Common mode may reduce or eleminate it, we need GBW $\approx \frac{1}{t_r 2\pi} \approx 16M$, beside that both Differential and Common mode feedback loops are stable with adequate PM.

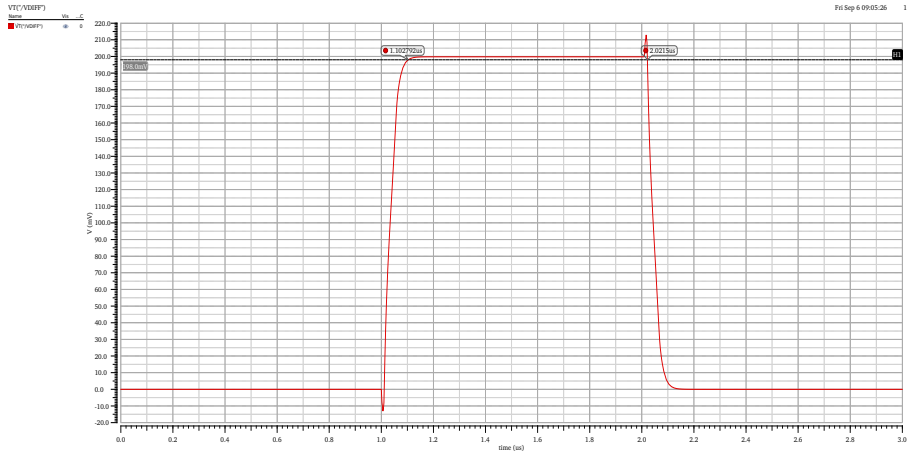

Figure 29: V_{OD} vs time (setteling time)

From fig-29 , the signal settles at 102ns , which again because of the small negative spike, Make it settle faster , we can Increase the current in the input pair or $\frac{g_m}{I_D}$, another solution is to increase the current of the CMFB Loop or $\frac{g_m}{I_D}$ of the tail source , this makes CMFB Loop faster and recover form the spike faster.

4.3.2 Common Mode Pulse

Applying Common mode pulse with the same amplitude and rise time as before.

As shown in fig-31 , CMFB Loop isn't fast enough to respond for high transient ($t_r = 10\,\text{ns}$) ,but the Loop is stable and there is no ringing in Differential nor common mode Loops.

4.3.3 Output Swing

Applying sinusoidal signal with frequenct = 100KHz and amplitude = 150mv.

From fig-33 , peak-to-peak Swing of $V_{\text{id}} = 299.87\,\text{mv}$ and for $V_{\text{out}_d} = 599.1\,\text{mv}$, Close loop gain =1.998.

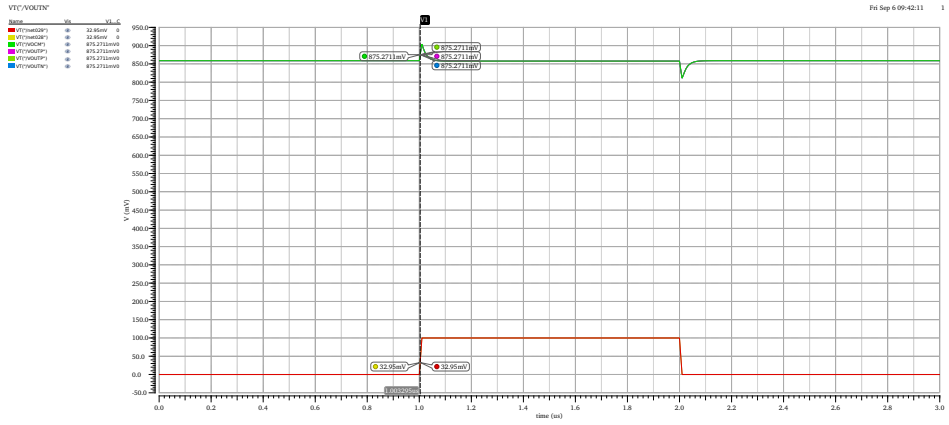

Figure 30: $V_{\text{in}}^{+}, V_{\text{in}}^{-}, V_{\text{out}}^{+}, V_{\text{out}}^{-}$ and $V_{\text{out}_{\text{CM}}}$ Vs time (Common Mode excitation)

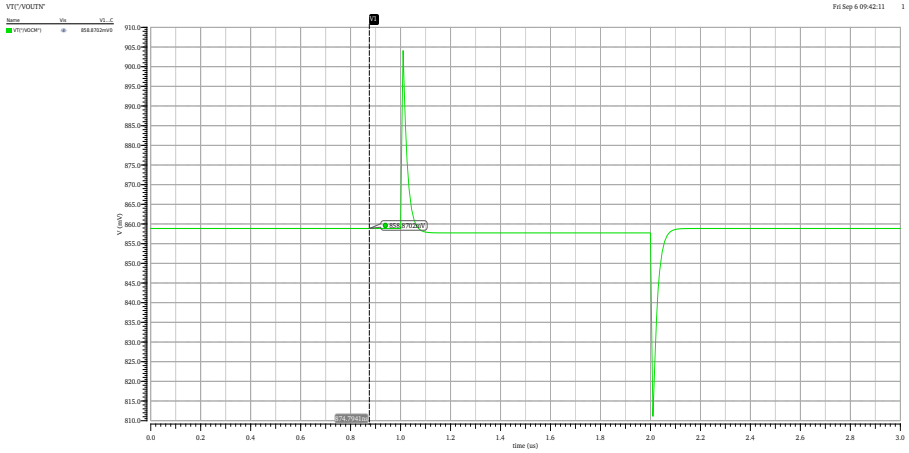

Figure 31: $V_{\text{out}_{\text{CM}}}$ Vs time

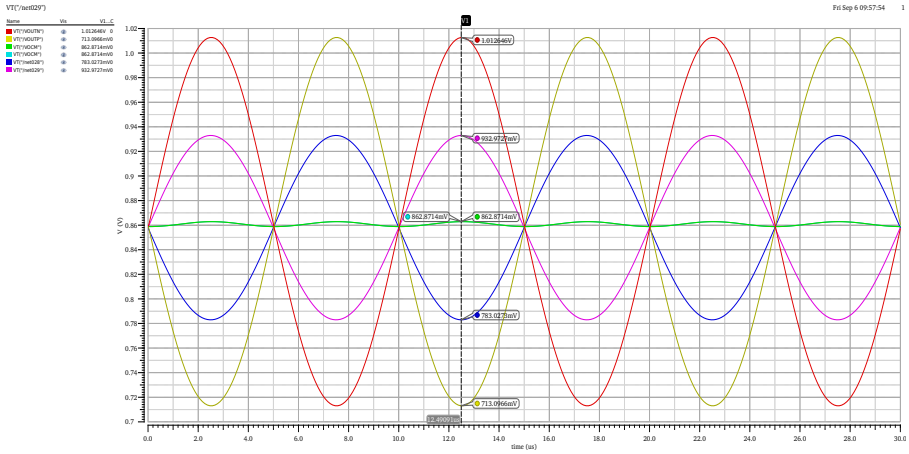

Figure 32: $V_{\text{out}}^{+}, V_{\text{out}}^{-}, V_{\text{out}_{\text{CM}}}, V_{\text{in}}^{+}$ and V_{in}^{-} Vs time

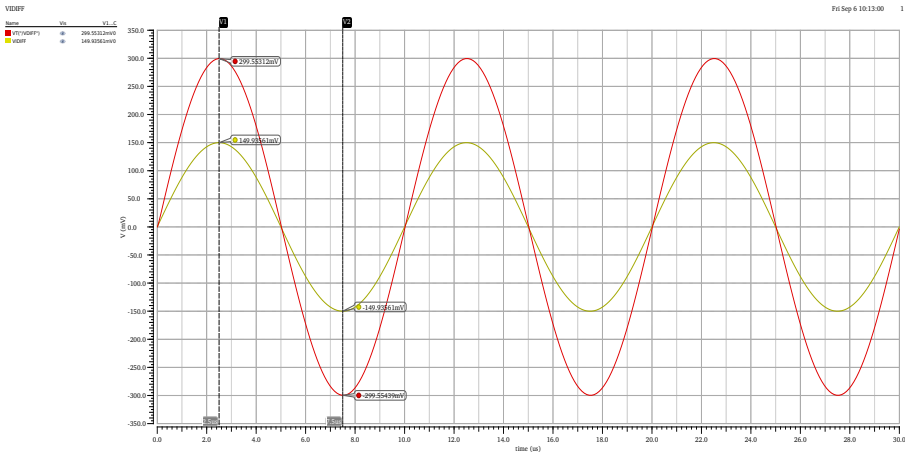

Figure 33: $V_{\mathrm{ou}_{\mathrm{diff}}}$ and V_{id} Vs time