Lab 04 and Lab 05

Mini project SAR ADC

1 Pre Lab 04 : Behavioral models

1.1 Inverter

1.1.1 Schematic

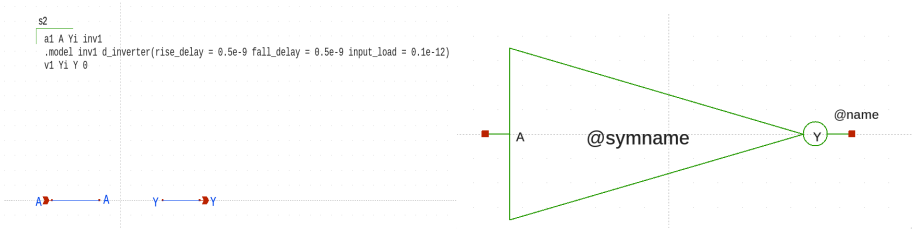

Figure 1. Schematic and symbol for an inverter

1.1.2 Simulation

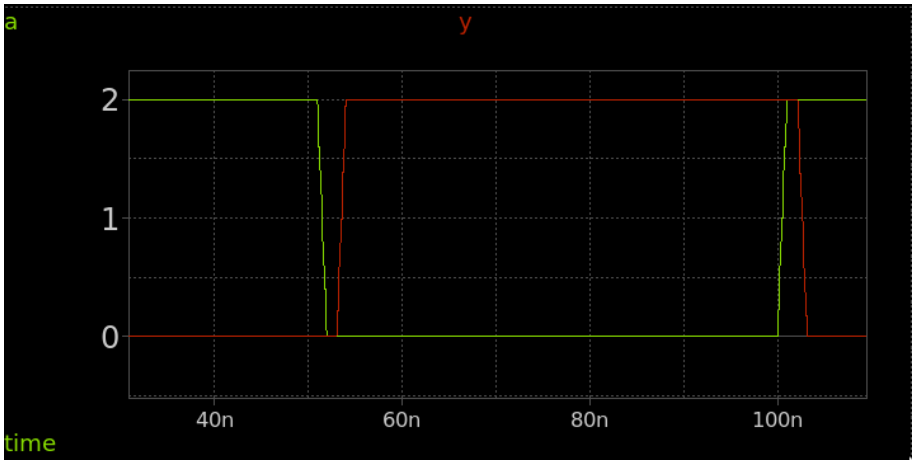

Figure 2. Inverter Transient Simulation output

1.2 Nand Gate

1.2.1 Schematic

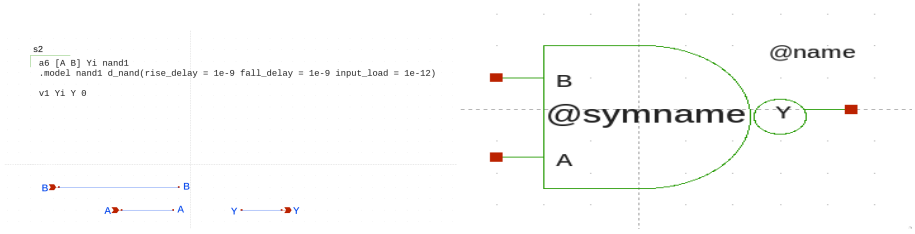

Figure 3. Nand gate schematic and symbol

1.2.2 Transient simulation

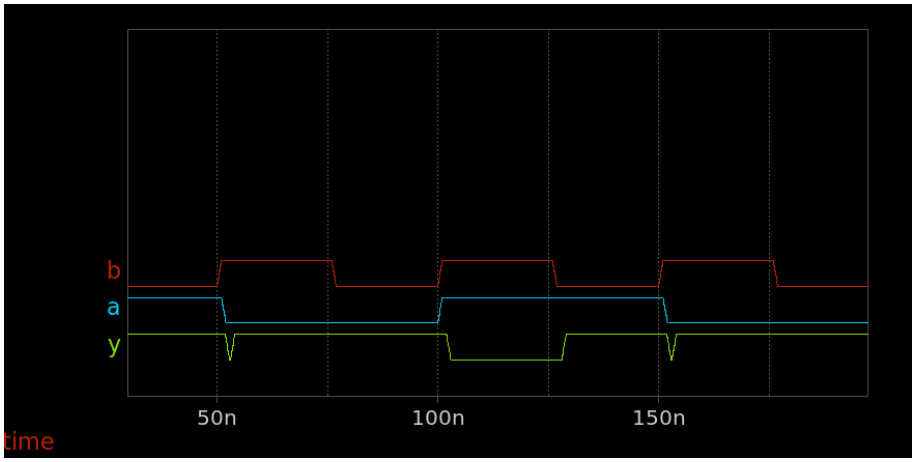

Figure 4. Nand gate transient simulation

1.3 Nor gate

1.3.1 Schematic

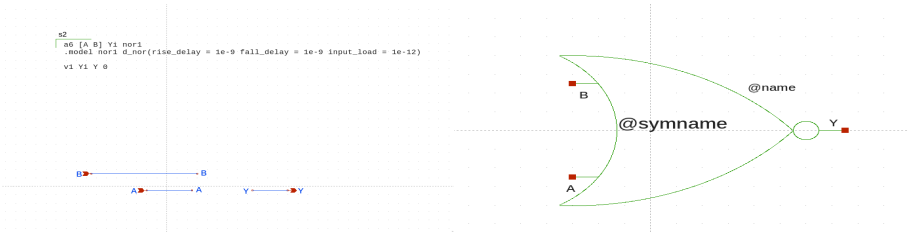

Figure 5. Schematic and symbol of Nor gate

1.3.2 Transient simulation

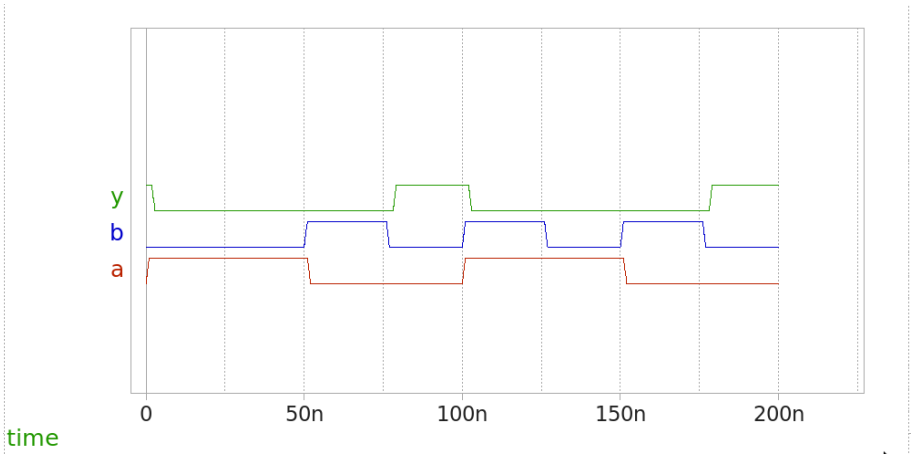

Figure 6. Nor Simulation

1.4 Comparator

1.4.1 Schematic and symbol

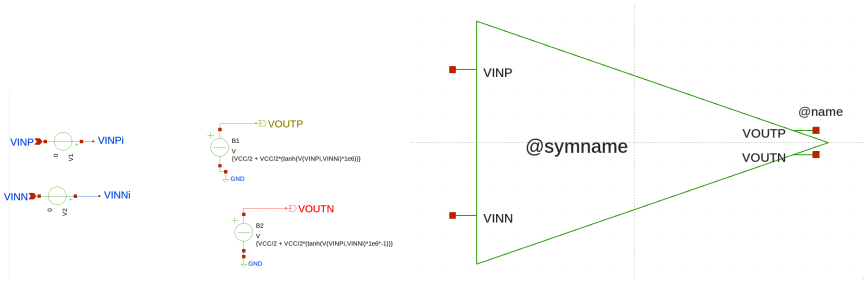

Figure 7. Schematic and symbol of comparator

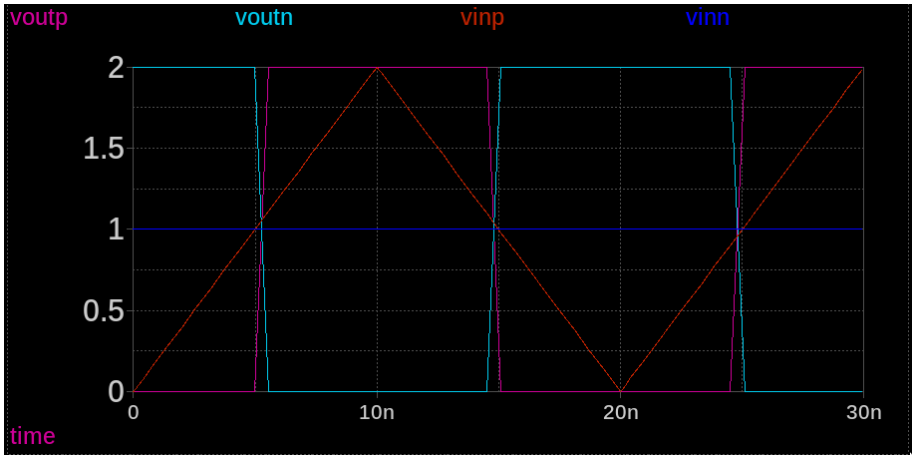

Figure 8. Comparator Transient Simulation

1.4.2 D-flip flop

1.4.3 Schematic

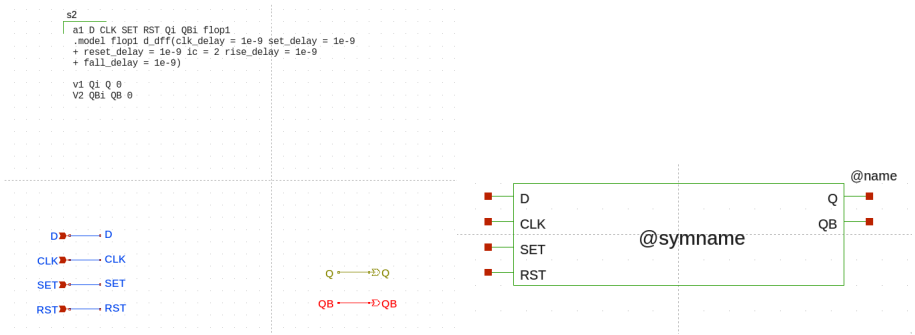

Figure 9. Schematic and symbol of D-flip flop

1.4.4 Transient simulation

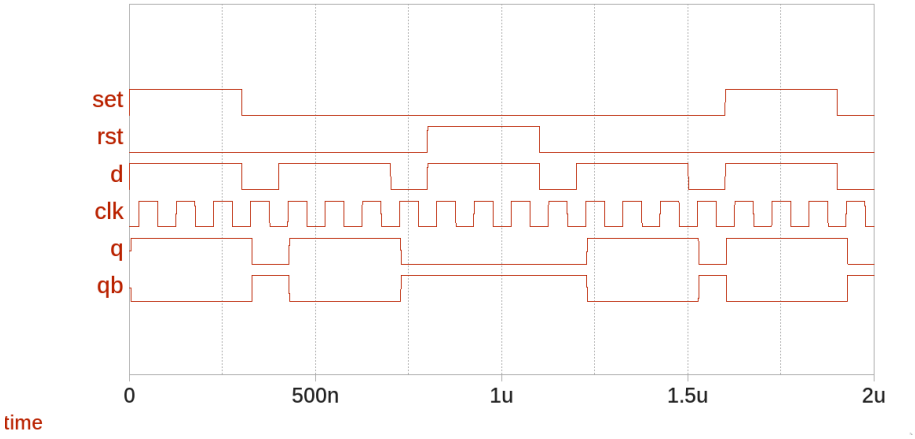

Figure 10. D flip flop transient simulation

2 SAR ADC

2.1 Schematic:

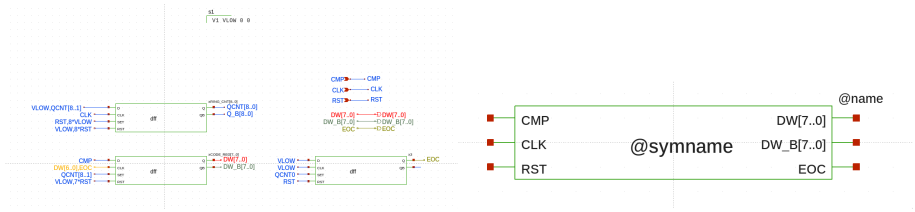

Figure 11. Schematic of SAR ADC

2.2 Simulation

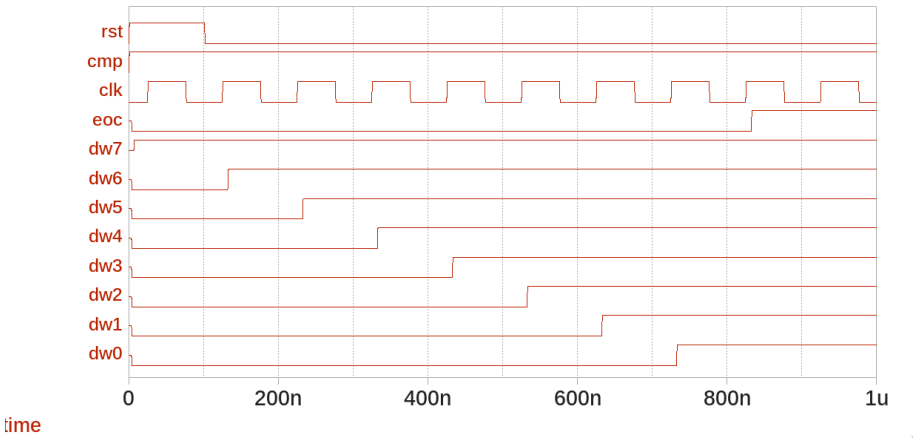

Figure 12. CMP all ones

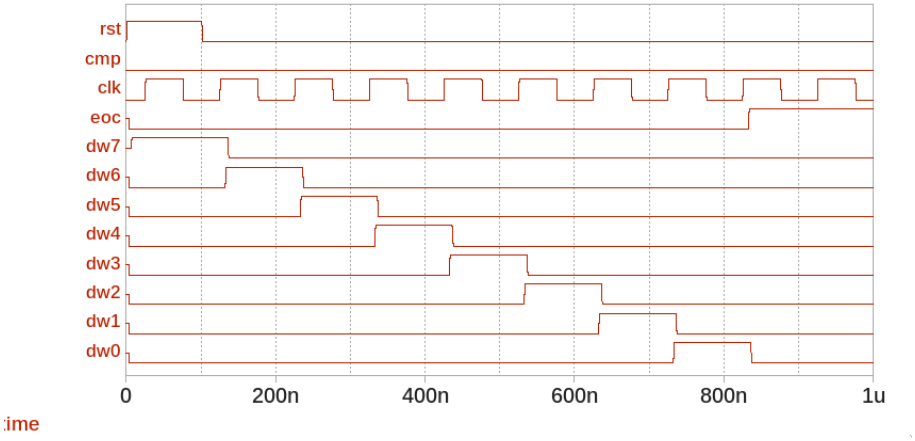

Figure 13. CMP all zeros

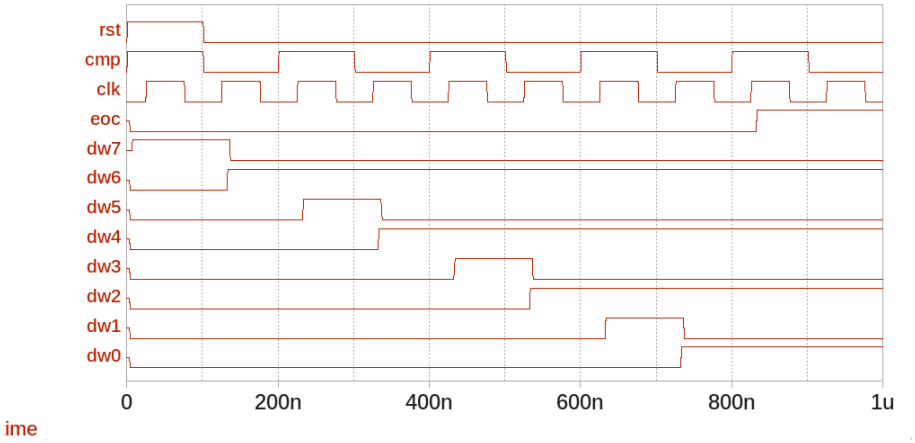

Figure 14. CMP signal alternating

2.3 Operation Explanation

Initially at reset (when RST is high), Counter is $Q_{\mathrm{CNT_8}}$ is set to start counting and DW_7 is set to one, after that the counter start counting and sets the bit in code register which to be compared a clock earlier before the actual comparison starts (That's because the code register uses the later data DW_{i+1} as a clock to choose which bit to be compared with CMP) , when the CMP is high the corresponding DW is high , when CMP is low DW is low , CMP signal should come from a comparator which compares the cumulative sum of the DAC output to the actual input.

Lastly, When counter sets the its last bit Q_{CNT_0} EOC is set and the Code register use the EOC rise as the last clk signal to compare its last bit.

CLK	DW<7>	DW<6>	DW<5>	DW<4>	DW<3>	DW<2>	D<1>	DW<0>	CMP
1 (reset)	1	0	0	0	0	0	0	0	X
2	B7	1	0	0	0	0	0	0	B7
3	B7	B6	1	0	0	0	0	0	B6
4	B7	B6	B5	1	0	0	0	0	B5
5	B7	B6	B5	B4	1	0	0	0	B4
6	B7	B6	B5	B4	**B3**	1	0	0	B3
7	B7	B6	B5	B4	B3	B2	1	0	B2
8	B7	B6	B5	B4	B3	B2	B1	1	B1
9	B7	B6	B5	B4	B3	B2	B1	B0	B0
10	B7	B6	B5	B4	B3	B2	B1	B0	

Table 1. State Table of SAR ADC

3 Transmission gate

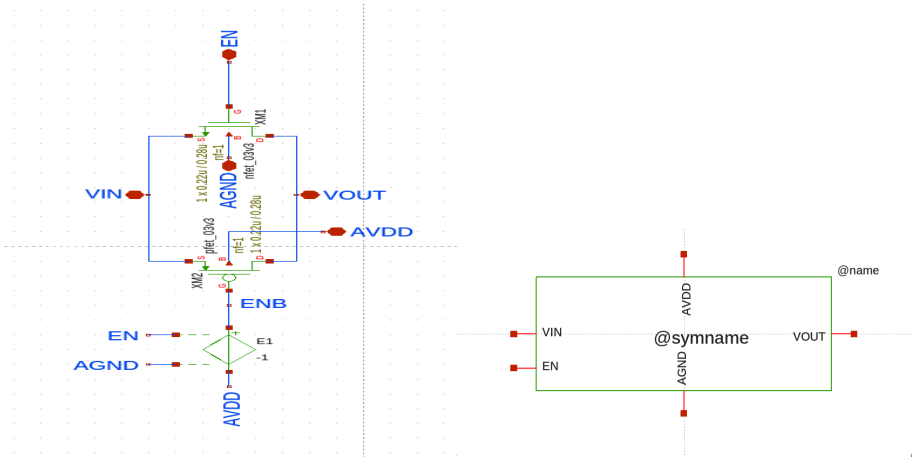

Figure 15. Schematic and symbol of Transmission gate

4 Bottom plate switch

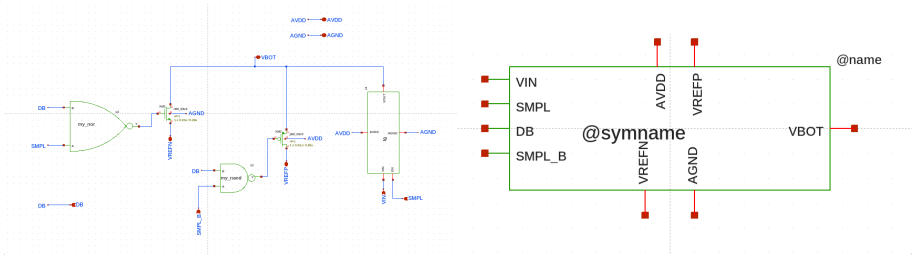

Figure 16. Schematic and Symbol of Bottom plate switch

5 Pre Lab 05

5.1 Capacitive DAC

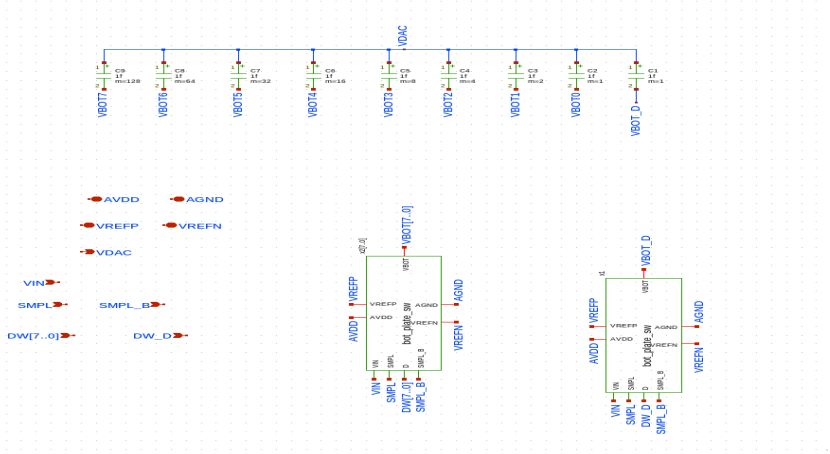

Figure 17. Schematic of Capacitive DAC

5.2 SAR ADC schematic

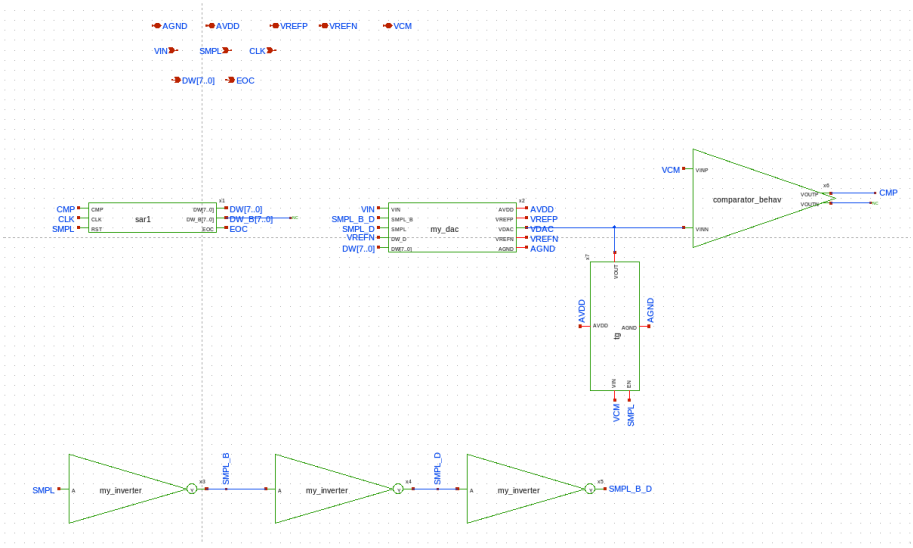

Figure 18. Schematic of SAR ADC

5.3 SAR ADC Testbench

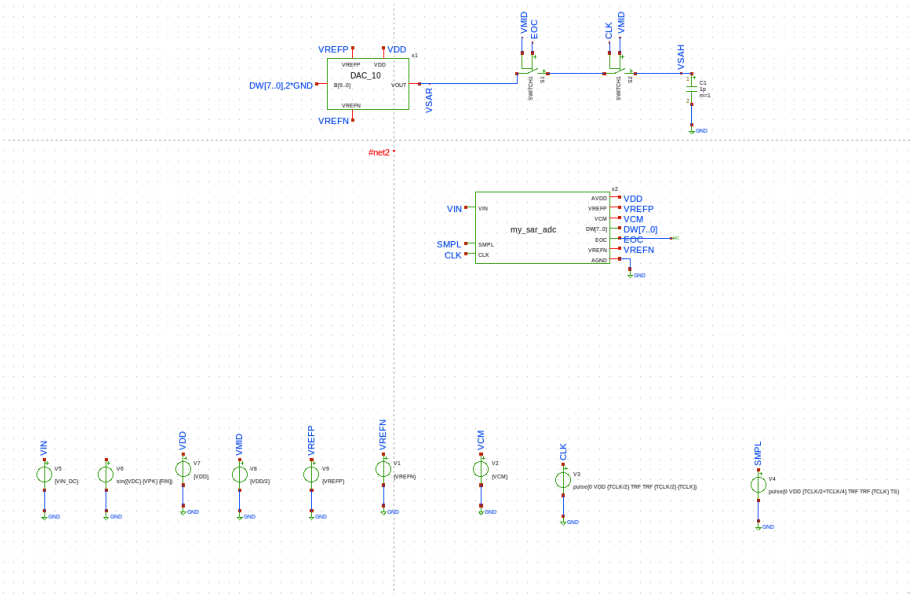

Figure 19. SAR ADC Testbench schematic

6 Part 2 DC functional test

Three tests are made,

1. $V_{\text{in}} = V_{\text{ref}_n}$
2. $V_{\text{in}} = V_{\text{ref}_p}$
3. $V_{\text{in}} = V_{\text{REF}_N} + (128 + 32 + 8 + 2 + 0.5)\, 2\,\text{VPK}/(2^8)$ (Alternating zeros and ones)

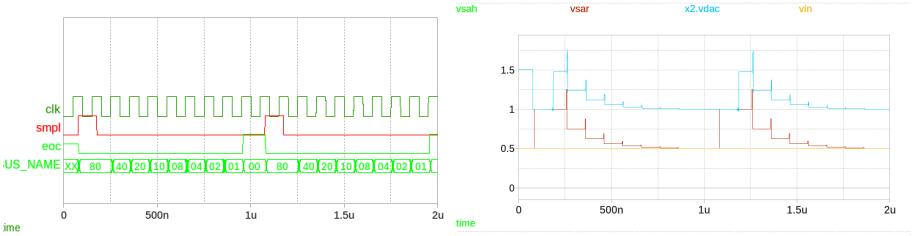

Figure 20. ADC output , V_{SAH} and V_{SAR} DC test input $= V_{\text{refn}}$

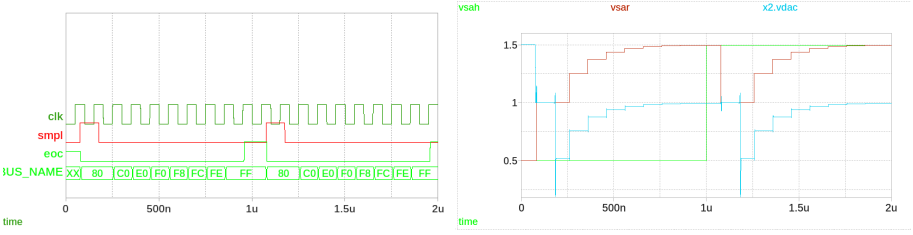

Figure 21. ADC output , V_{SAH} and V_{SAR} DC test input $= V_{\text{refp}}$

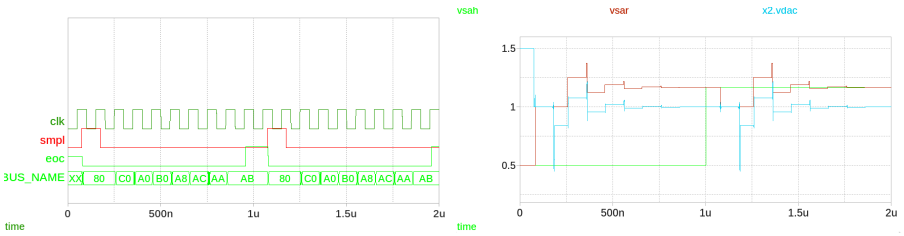

Figure 22. ADC output , V_{SAH} and V_{SAR} DC test input = Alternating

7 Sine Wave test

Here the input is sine wave with Number of cycles = 5 and Number of fft points = 256 points.

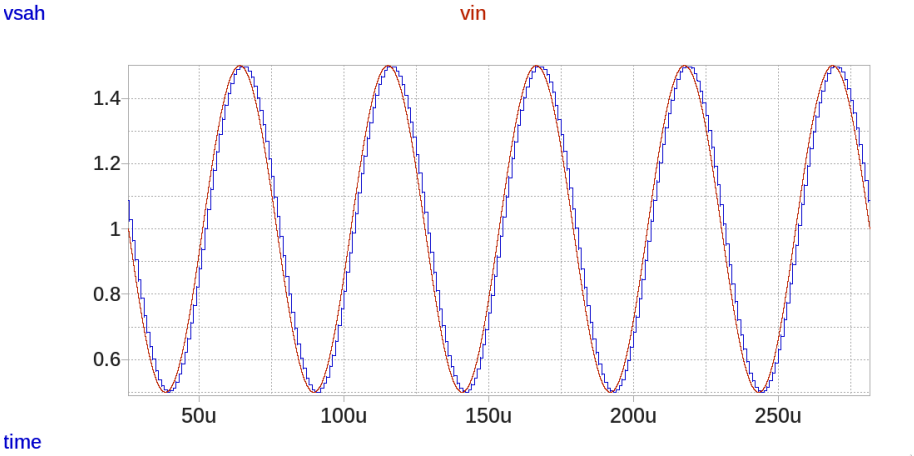

Figure 23. V_{SAH} and V_{in} waveforms Vs time

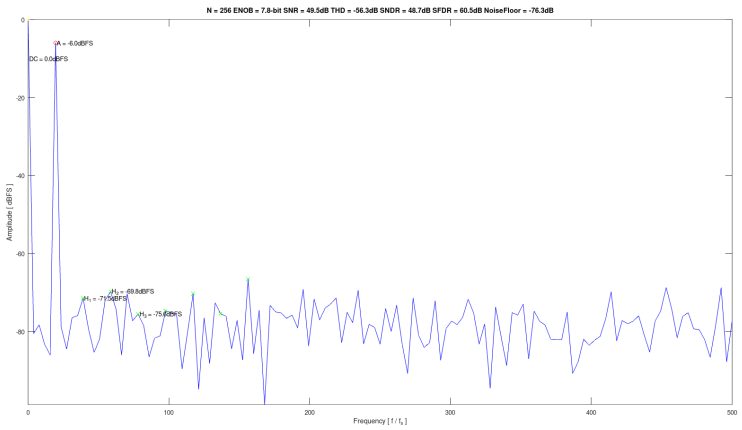

Figure 24. V_{SAH} frequency domain spectrum

FFT Results:

- ENOB = 7.8 bits
- SINAD = 48.7dB
- SNR = 49.5dB

- SFDR = 60.5dB
- THD = -56.3dB
- Signal power = -9dBFS (average power = peak power -3dB)
- DC power = 0dBFS

8 Differential Operation

8.1 Schematic

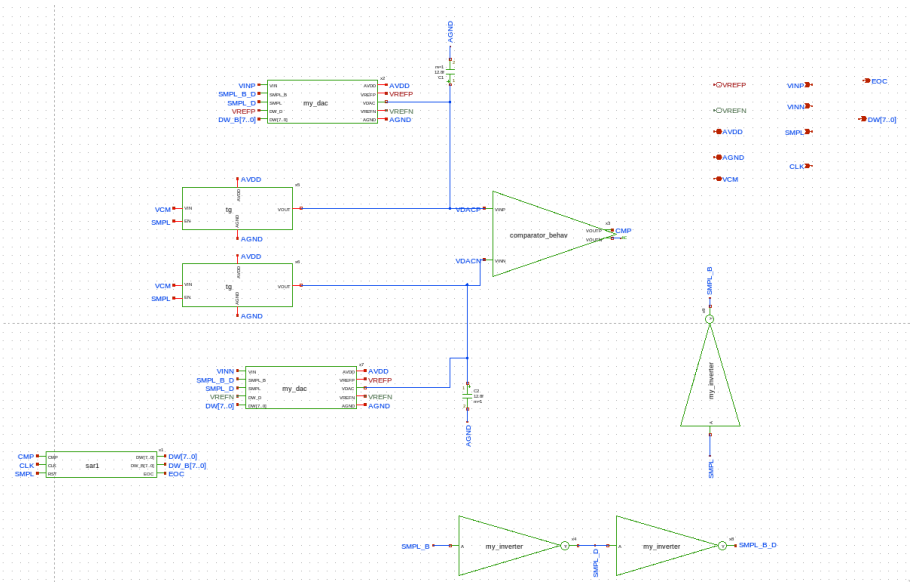

Figure 25. Schematic of differential SAR ADC

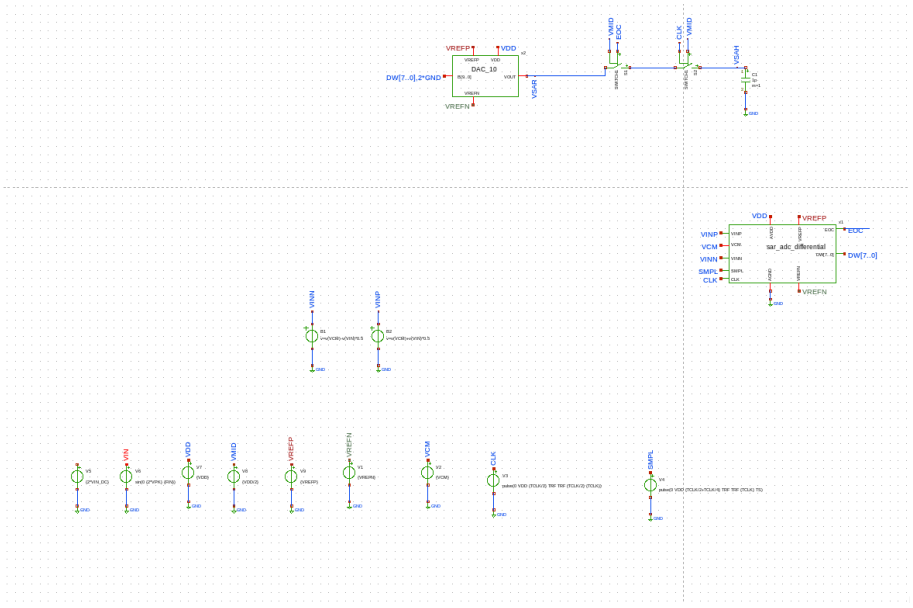

Figure 26. Testbench for Differential sar ADC

8.2 Simulation

Performing Transient simulation with Number of cycles = 5 cycles and 256 FFT points peak-to-peak voltage of 2V, as shown in fig-27 V_{out} is half of the peak-to-peak voltage, that's because we only take single output, also fig-28 shows that no increase in performance compared to single-ended.

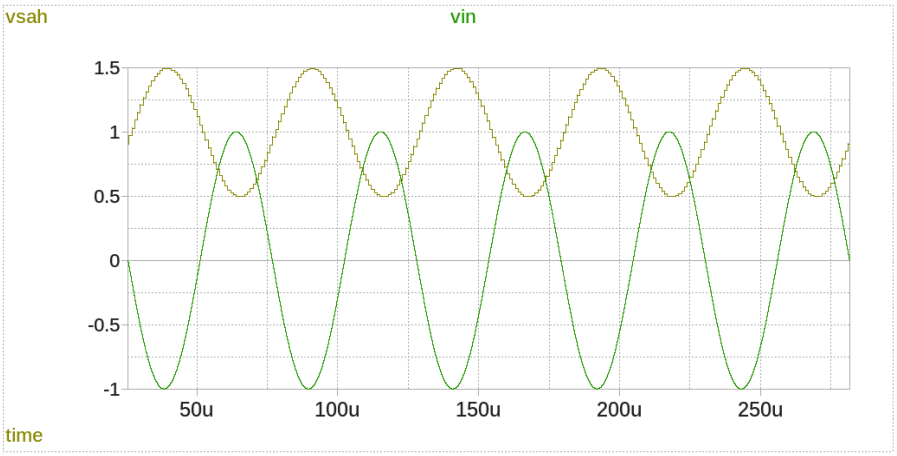

Figure 27. V_{SAH} and V_{in} vs time (differential operation)

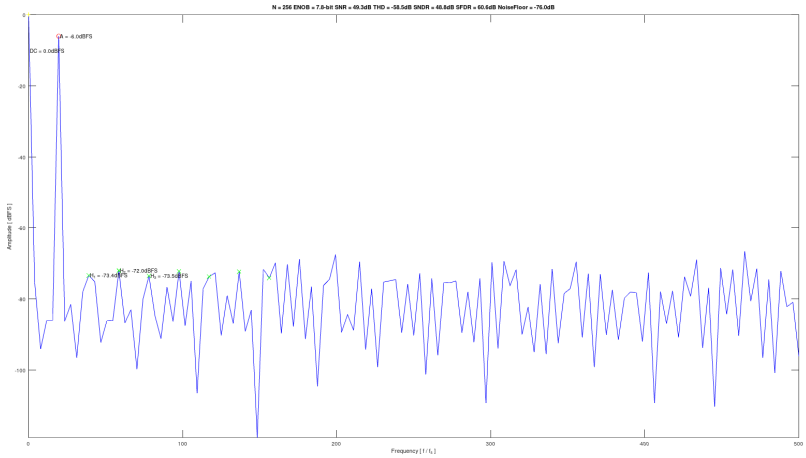

Figure 28. V_{SAH} frequency spectrum (differential operation)

Results and comments:

- ENOB = 7.8 bits
- SNR = 49.3dB
- SINAD = 48.8dB
- SFDR = 60.6dB
- THD = -58.6dB
- Signal power = -9dBFS
- DC power = 0dBFS

There is no increase in performance compared to single-ended operation that's because we only take single output.