Cadence Tools

Lab 9

Two Stage Miller OTA

1 Design Charts

PMOS:

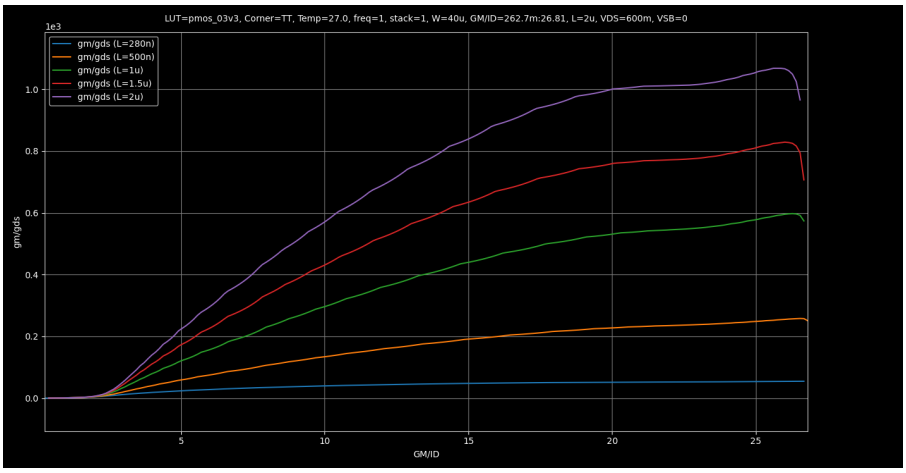

Figure 1: $\frac{g_m}{g_{\mathrm{ds}}}$ Design Chart for PMOS

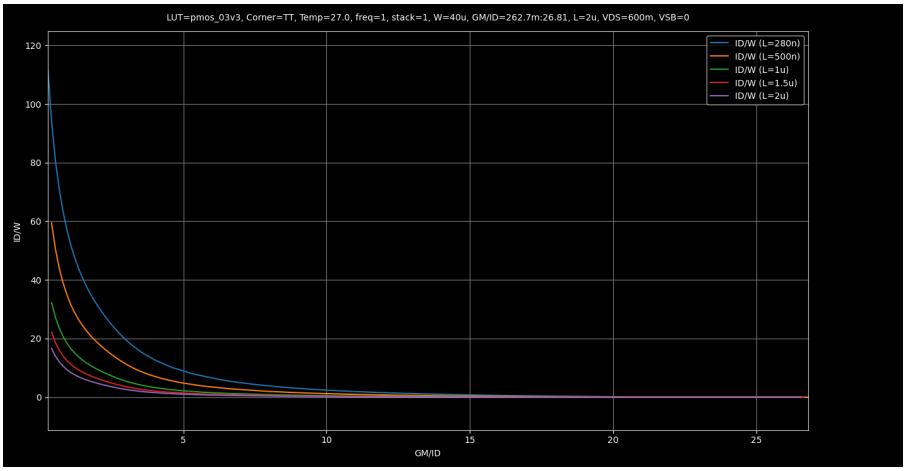

Figure 2: $\frac{I_D}{W}$ Desing Chart for PMOS

NMOS:

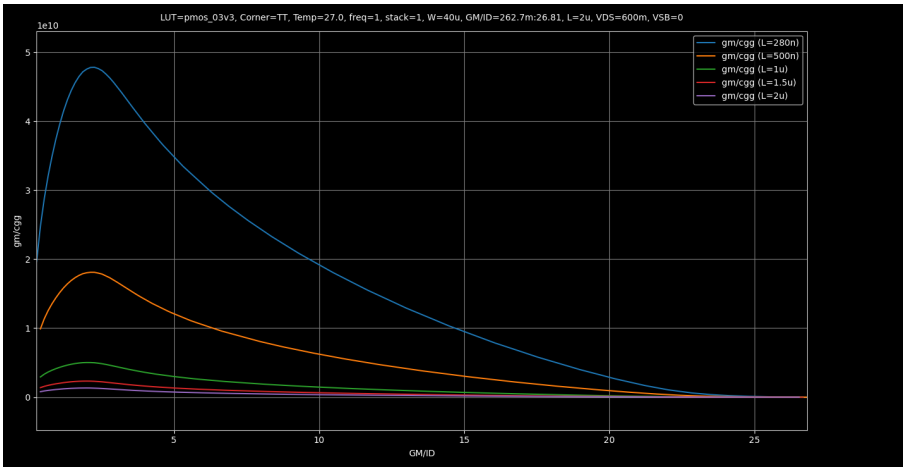

Figure 3: $\frac{g_m}{C_{\mathrm{gg}}}$ Design chart for PMOS

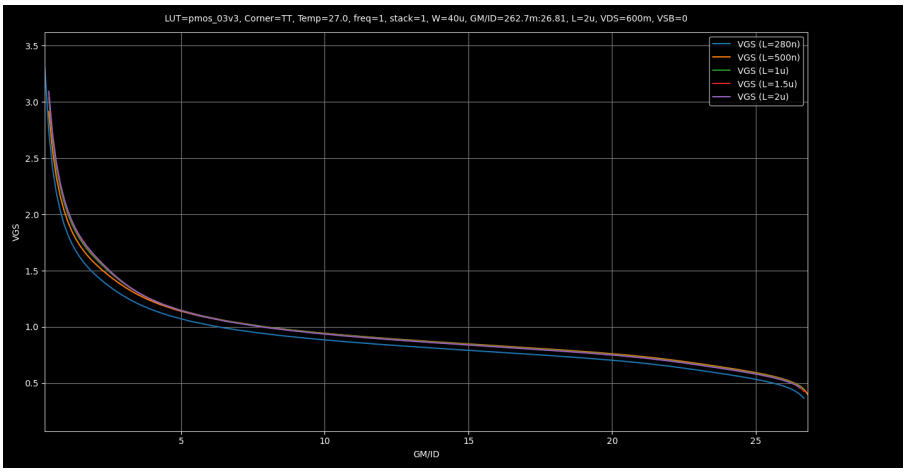

Figure 4: V_{GS} Design Chart for PMOS

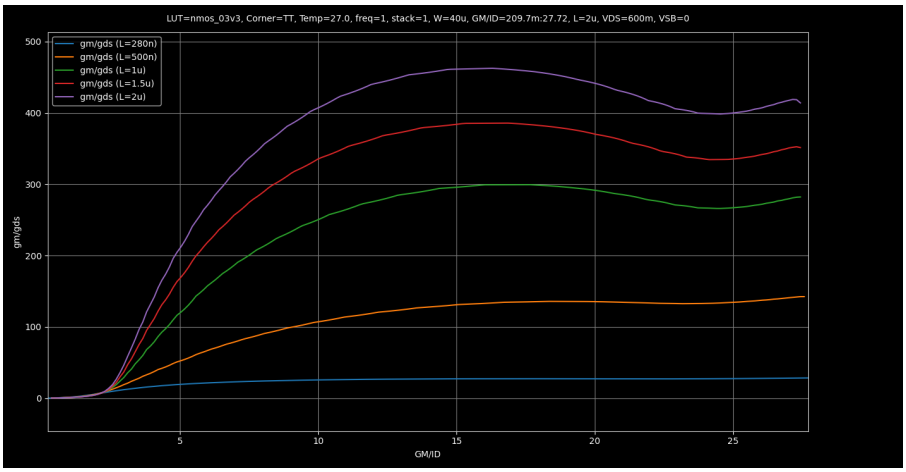

Figure 5: $\frac{g_m}{g_{\mathrm{ds}}}$ Design chart for NMOS

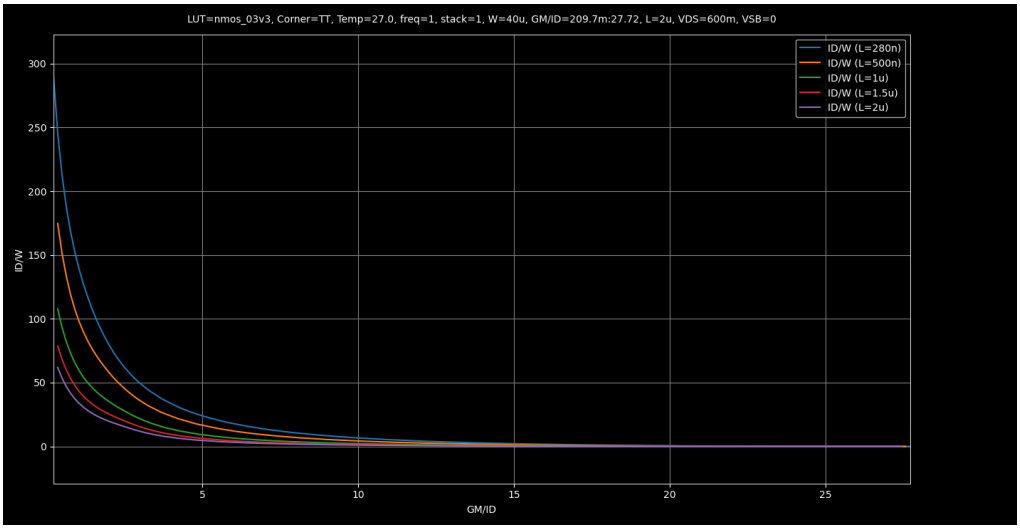

Figure 6: $\frac{I_D}{W}$ Desing chart for NMOS

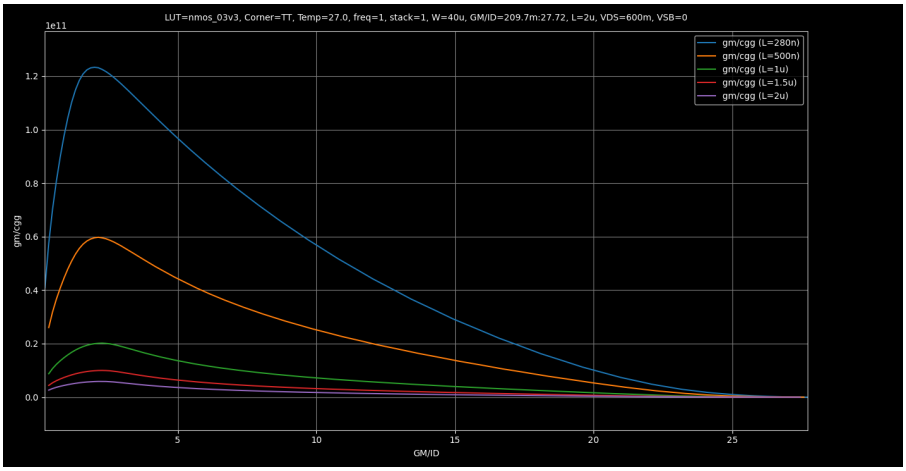

Figure 7: $\frac{g_m}{C_{\text{gg}}}$ Design cahrt for NMOS

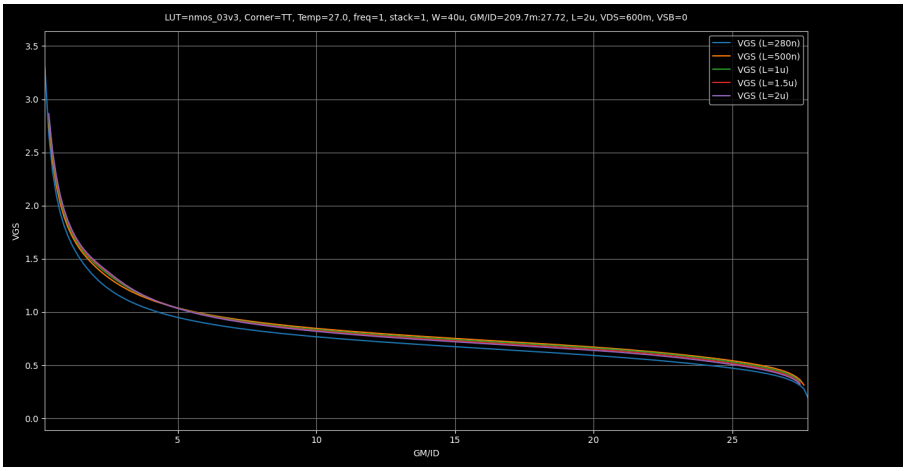

Figure 8: V_{GS} Design chart for NMOS

Technology	0.18um
Supply voltage	1.8V
Static gain error	$\leq 0.05\%$
CMRR @ DC	$\geq$ 74dB
Phase margin (avoid pole-zero doublets)	$\geq 70^{\circ}$
OTA current consumption	$\leq$ 60uA
CMIR – high	$\geq$ 1V
CMIR – low	$\leq$ 0.2V
Output swing	0.2 – 1.6V
Load	5pF
Buffer closed loop rise time (10% to 90%)	$\leq$ 70ns
Slew rate (SR)	$5\text{V}/\mu\text{s}$

Table 1: Specification Table

2 Design and Sizing:

2.1 Input Pair Sizing

We begin from VICM Range, since it's closer to 0 , then we use a PMOS input pair, VICM_{min} can be easily achieved 0.2V , in fact it's a negative number as we will show later, the problem is $\text{VICM}_{\text{high}}$= 1 , In fact it's not feasible for reasonable area , Here we design for $\text{VICM}_{\text{high}} = 0.8$ and we will connect the body of the PMOS to VDD, even if the design is made for $\text{VICM}_{\text{high}} = 0.8$ the actual range is higher because of the V_{dsat} margin.

- V_{GS}:

  Since $\text{VICM}_{\text{High}}$ is the hardest spec. , it's reasonable to start with choosing V_{GS} for the input pair ,since $\text{VICM}_{\text{high}} = 1.8 - V_{\text{ds}_{\text{current source}}} - V_{\text{GS}}$, a reasonable $V_{\text{ds}} = 180\,\text{mV}$ (it's small because smaller V_{GS} makes the area very large (deep subthreshold) , then $V_{\text{GS}} = 820\,\text{mv}$.

- I_{B1} :

  Since $V_{\text{GS}} = 820\,\text{mV}$, this means that this mosfet will be baised in MI/WI, hence it will not be a good Idea to use a higher current , choosing reasonable current comes from Speed spec ,whic is SR and Rise time, $\text{SR} = \frac{I_{B1}}{C_C}$, C_c is usually chosen to be $0.5C_L$ but here since

we need smaller current $C_C = 2$ will require $I_{B1} = 10\mu$, which is reasonable ,but we will use smaller $C_C = 1.8$ to account for second order effects (like $r_z$and Internal Capacitance).

- Choosing $\frac{g_m}{g_{\text{ds}}}$:

  This comes from DC gain spec (Error Spec. ¡ 0.05%) $A_{\text{vol}} \geqslant 2000$. this gain is achieved on the two stage, it's usually preferable to make the input stage gain larger, but since the V_{GS} for the input stage is small ($\frac{g_m}{I_D}$is high) , going for big $\frac{g_m}{g_{\text{ds}}}$ will make $\frac{g_m}{I_D}$ even higher and the device size will be bigger, also second stage gain is always large due to large r_{out} for the current source and large $g_{m_2} \sim 8g_{m1}$, in conclusion gain is split equally between the two stages, meaning $\frac{g_m}{g_{\text{ds}}} = 90$ for the input pair.

- V_{ds} : not very important , choosen to be 0.8.

- V_{sb}: Since V_{GS} is choosed for the case of $V_{\text{DS}} = 180\,\text{mv}$ for the tail source , $V_{\text{SB}} = 180\,\text{mv}$

2.2 CS stage:

Going now for the current source stage , since we need first to choose g_{m2} from PM spec > 70 , we will go with PM $= 72.3$,$\frac{\text{GM}_2}{\text{GM}_1} = 3\frac{C_L}{C_C}$, from sizing of Input stage we need $g_{m_2} \geqslant 750\mu$, $\text{I}_{B2} = 50\mu$, DC gain ≈ 45, since current source is usually has high r_{out} (it must have high VA since the same L is choosen with the current source at the input stage which must have high VA due to required high CMRR). $\frac{g_m}{g_{\text{ds}}} = 1.5 \times$ gain not $2 \times$ gain and ($g_{\text{ds}}$for current source at most $0.5 \times g_{\text{ds}_{\text{CS}}}$),$V_{\text{sb}} = 0$ and $V_{\text{DS}} = 0.6$.

Parameter	Value
ID	4.855 µA
L	340 nm
W	22.8 µm
VGS	820 mV
VDS	800 mV
VSB	180 mV
gm/ID	18.56
Vstar	107.7 mV
fT	479.7 MHz
gm/gds	82.62
VA	4.451
ID/W	212.9 nA μm^{-1}
gm/W	3.953
AREA	7.752 pm^2
gm	90.13 µS
gmb	30.35 µS
gds	1.091 µS
ro	916.7 kΩ
VTH	825.1 mV
VDSAT	79 mV
cgg	29.9 fF
cgs	19.9 fF
cgd	3.565 fF
cgb	6.442 fF
cdb	12.97 fF
csb	17.02 fF
cdd	14.16 fF

Table 2: Input Pair

2.3 Current Mirror Load:

Now for the current mirror load the most important thing is to tune V_{GS} to make it equal V_{GS} for the CS stage , second thing is to choose $g_{\text{ds}} \geqslant g_{\text{ds}_{\text{input pair}}}$, $I_D = 5\mu$, $V_{\text{GS}} = 728.6\,\text{mv}$, $g_{\text{ds}} = 998n$ and $V_{\text{DS}} = 728.6\,\text{mv}$.

2.4 Current Source first and second stage

Current Source cannot be desinged independantly since they have the same V_{GS} and L , inorder to choose proper V_{GS} it can be chosen from the first stage since it has minimum $V^* = 130\,\text{mv}$ to make $V_{\text{ds}_{\text{min}}} = 180\,\text{mv}$, so we first desing the Current Source of the first stage and if the sizing satsfies the condition on the second stage (r_{out} and $V_{\text{ds}_{\text{min}}} = 0.2$),then it's a valid size. to get the required r_o for Input stage current source , we can get it from CMRR spec. CMRR=$A_{\text{vd}} \times$

Parameter	Value
ID	50.73 µA
L	370 nm
W	26.66 µm
VGS	728.6 mV
VDS	600 mV
VSB	0
gm/ID	14.47
Vstar	138.2 mV
fT	3.475 GHz
gm/gds	61.39
VA	4.242
ID/W	1.903 µA µm^{-1}
gm/W	27.53
AREA	9.864 pm^2
gm	734.1 µS
gmb	217.3 µS
gds	11.96 µS
ro	83.62 kΩ
VTH	686.2 mV
VDSAT	108.8 mV
cgg	33.62 fF
cgs	21.77 fF
cgd	5.11 fF
cgb	6.737 fF
cdb	17.45 fF
csb	23.04 fF
cdd	20.47 fF
idnth2	8.303 nA
vgnth2	15.41 aF
idnf12	148.8 aF
vgnfl2	276.2 aF
idmis	1.523 µA
vgmis	2.074 mV

Table 3: CS (second stage)

$g_{m_{\text{load}}} \times 2r_o$, $r_o \geqslant 700k$, we chose $r_o = 900k$, to account for VAdegradation.

Second Stage Current Source. Moving to the second stage current Source using the same L and V_{GS} we see that r_o is valid $g_{\text{ds}} < 6\mu$. then this solution is valid.

Parameter	Value
ID	5.156 µA
IG	N/A
L	390 nm
W	3.05 µm
VGS	728.6 mV
VDS	728.6 mV
VSB	0
gm/ID	14.81
Vstar	135.1 mV
fT	3.116 GHz
gm/gds	76.5
VA	5.166
ID/W	1.69 µA µm^{-1}
gm/W	25.03
AREA	1.19 pm^2
gm	76.35 µS
gmb	23.54 µS
gds	998.1 nS
ro	1.002 MΩ
VTH	691.1 mV
VDSAT	106.2 mV
cgg	3.9 fF
cgs	2.502 fF
cgd	564.4 fF
cgb	833.6 fF
cdb	1.959 fF
csb	2.655 fF
cdd	2.271 fF
idnth2	864.7×10^{-27} A
vgnth2	148.3 aF
idnf12	13.01 aF
vgnfl2	2.231 nV
idmis	449.2 nA
vgmis	5.883 mV

Table 4: Current Mirror Load

2.5 Choosing r_z

Lastly first we choose r_z to move the zero to infinity $r_z = 1.36k$ (this will be changed later to improve PM).

2.6 Sizing Summary:

Total Area = 118p

Area = 118.5617p

Parameter	Value
ID	11.2 µA
L	510 nm
W	32.6 µm
VGS	844.8 mV
VDS	400 mV
VSB	0
gm/ID	15.15
Vstar	132 mV
fT	438.5 MHz
gm/gds	152.4
VA	10.06
ID/W	343.5 mA μm^{-1}
gm/W	5.204
AREA	16.63 pm^2
gm	169.6 µS
gmb	75.69 µS
gds	1.113 µS
ro	898.4 kΩ
VTH	786.1 mV
VDSAT	104.5 mV
cgg	61.57 fF
cgs	44.06 fF
cgd	5.458 fF
cgb	12.05 fF
cdb	24.16 fF
csb	31.31 fF
cdd	22.21 fF

Table 5: Current Source Input

3 Open Loop Simulation:

Note that both C_C and r_z are change to achieve Slew Rate $\geqslant 5V/\mu$s and PM $\geqslant 70^o$, $C_c = 1.55p$ and $r_z = 2k$.

3.1 DC Operating point:

Comments:

- Both Current and g_m for the input pair is equal because there is only a common mode signal
- DC voltage of first stage = 725.953mv equals V_{GS} of the currrent source (for common mode input V_{out} follows mirror node

Parameter	Value
ID	50.01 µA
L	510 nm
W	143.1 µm
VGS	844.8 mV
VDS	600 mV
VSB	0
gm/ID	15.14
Vstar	132.1 mV
fT	446.7 MHz
gm/gds	196.8
VA	13
ID/W	349.5 mA μm^{-1}
gm/W	5.29
AREA	72.98 pm^2
gm	757 µS
gmb	337.7 µS
gds	3.846 µS
ro	260 kΩ
VTH	785.9 mV
VDSAT	104.6 mV
cgg	269.7 fF
cgs	193.2 fF
cgd	23.38 fF
cgb	53.11 fF
cdb	102.9 fF
csb	137.3 fF
cdd	93.9 fF

Table 6: Current Source Second Stage

	W	L	I_D	g_m	V_{GS}	$\frac{g_m}{I_D}$	V_{dsat}	V_{ov}	V^*
Input pair	22.8μ	340n	5μ	90μ	820m	18	79m	-5.1m	107.7m
CM Load	3.05μ	390n	5μ	76.35μ	728.6m	15.27	107.2	37.5m	135.1m
Current Source (Input)	32.6μ	510n	10μ	152.8μ	844.8m	15.28	104m	58.7m	132m
CS	26.66μ	370n	50μ	723μ	728.6m	14.46	108.8m	42.4m	138.2m
Current Source (CS)	5*32.6μ	510n	50μ	756.8μ	844.8m	15.136	104.6m	58.9m	132m

Table 7: Final Sizing

- DC voltage of the second stage (output) = 823mV it's not eqaul to 0.9V because of mismatch betweem CM load and CS and mismatch between Current sources

3.2 AC analysis

3.2.1 Differential Analysis

Analysis

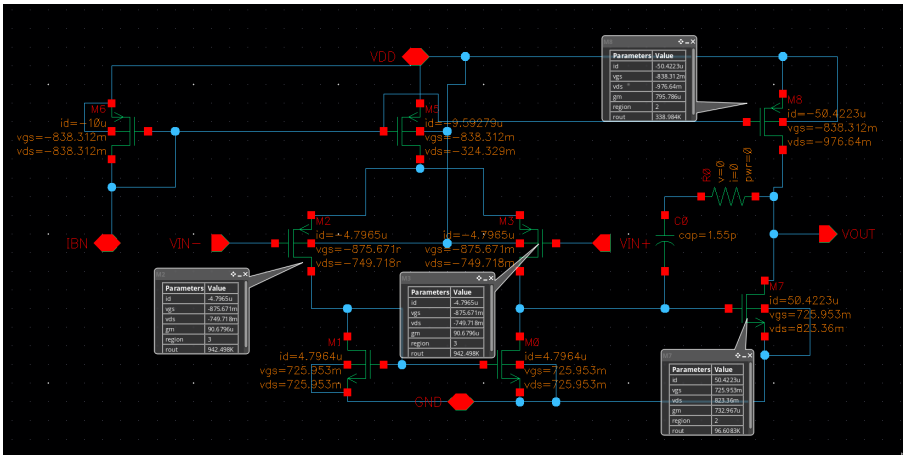

Figure 9: OP annotated

Test	Output	Nominal	Spec	Weight	Pass/Fail
Labs:5T_OTA_miller_lab9:1	A0	2.513k			
Labs:5T_OTA_miller_lab9:1	A0_DB	68.01			
Labs:5T_OTA_miller_lab9:1	BW	3.533k			
Labs:5T_OTA_miller_lab9:1	UGF	8.371M			
Labs:5T_OTA_miller_lab9:1	GBW	8.901M			

Figure 10: DC gain , BW , UGF and GBW

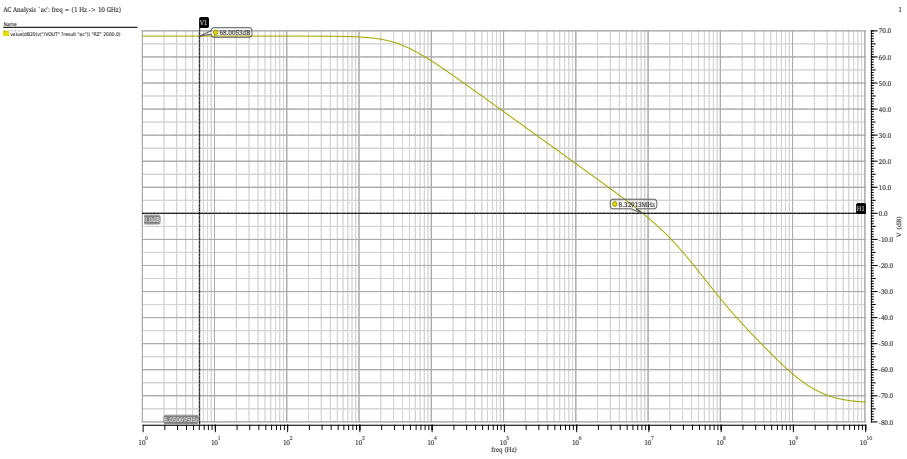

Figure 11: V_{out} Bode plot

- $A_0 = g_{m2}(r_{o1}||r_{o2}) \times g_{m7}(r_{o7}||r_{o8}) \approx 2400$
- $\text{GBW} = \text{UGF} = \frac{g_{m2}}{C_c \times 2\pi} = 9.24\,\text{MHz}$
- $\text{BW} = \frac{1}{(r_{o1}||r_{o2})(g_{m2}(r_{o7}||r_{o8}))C_C \times 2\pi} = 3.86\,\text{KHz}$

3.2.2 Common Mode Analysis

Analysis

	Analysis	Simultaion
DC gain	2400	2513
GBW	9.24M	8.901M
UGF	9.24M	8.371M
BW	3.86KHz	3.533KHz

Table 8: DC gain , GBW,UGF and BW Analysis Vs Simulation

Test	Output	Nominal	Spec	Weight	Pass/Fail
Labs:5T_OTA_miller_lab9:1	A0	310.2m			
Labs:5T_OTA_miller_lab9:1	A0_DB	-10.17			
Labs:5T_OTA_miller_lab9:1	BW	3.533k			
Labs:5T_OTA_miller_lab9:1	UGF	eval err			
Labs:5T_OTA_miller_lab9:1	GBW	1.098k			
Labs:5T_OTA_miller_lab9:1	VOUT_DB				

Figure 12: AC paramters

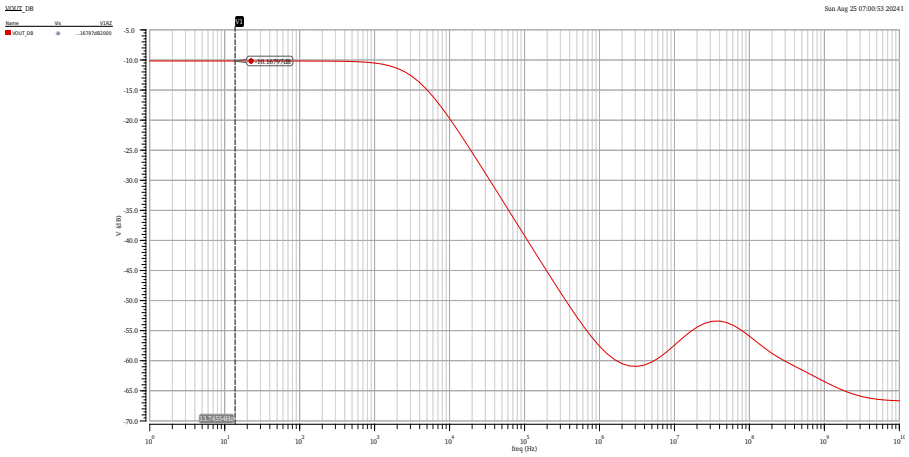

Figure 13: CMR bode plot

- CMR $= \frac{1}{1+2g_{m_1}r_{o_5}} \times g_{m_7}(r_{o_7}||r_{o_8}) = 396m$
- $\text{CMR}_{\text{DB}} = -8.04\,\text{db}$

	Analysis	Simulation
CMR	396m	310.2m

Table 9: CMR analysis Vs Simultion

3.2.3 CMRR

CMRR Simulation = 88.73 db

Analysis:

- $\text{CMRR} = \frac{A_{v_d}}{\text{CMR}} = \frac{2400}{0.396} = 6.06K = 75.65\,\text{db}$

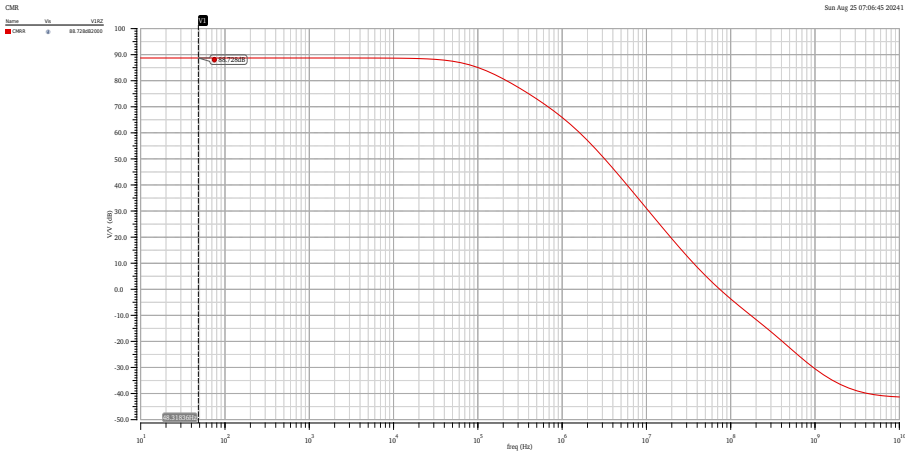

Figure 14: CMRR Bode plot

	Analysis	Simulation
CMRR	75.65db	88.73db

Table 10: CMRR analysis Vs Simulation

3.2.4 Differientail Large Singal

Test	Output	Nominal	Spec	Weight	Pass/Fail
Labs:5T_OTA_miller_lab9:1	GAIN				
Labs:5T_OTA_miller_lab9:1	GAIN_MAX	2.52k			
Labs:5T_OTA_miller_lab9:1	VOUT_DC				

Figure 15: Maximum DC gain (step = 0.0001V)

Using finer step size results in more accurate DC gain , when step size was 1m DC gain was 900 which is very small compared to AC simulation, $V_{\text{out}} = 823\,\text{mv}\,\text{at}\,V_{\text{id}} = 0$,which is equal to DC OP result.

3.2.5 Common Mode Large Signal

$\text{VICM}_{\text{max}} = 0.9V$, $\text{VICM}_{\text{min}} = 0V$

Analysis: $\text{VICM}_{\text{high}} = 1.8 - V_{\text{dsat}\,\text{Current Source}} - V_{\text{GS}_{\text{input}}} = 1.8 - 0.104 - 0.82 = 0.876$, $\text{VICM}_{\text{low}} = V_{\text{GS}_{\text{CM}}} - V_{\text{GS}_{\text{input}}} + V_{\text{dsat}} = -0.013V$. results are a little bit different because of body effect makes

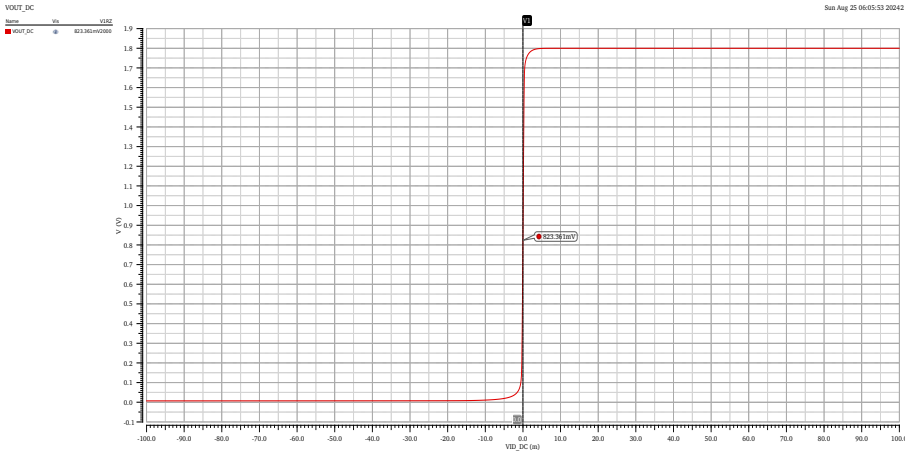

Figure 16: V_{out} Vs V_{ID} $V_{\text{out}} = 823\,\text{mv}$ at $V_{\text{id}} = 0$

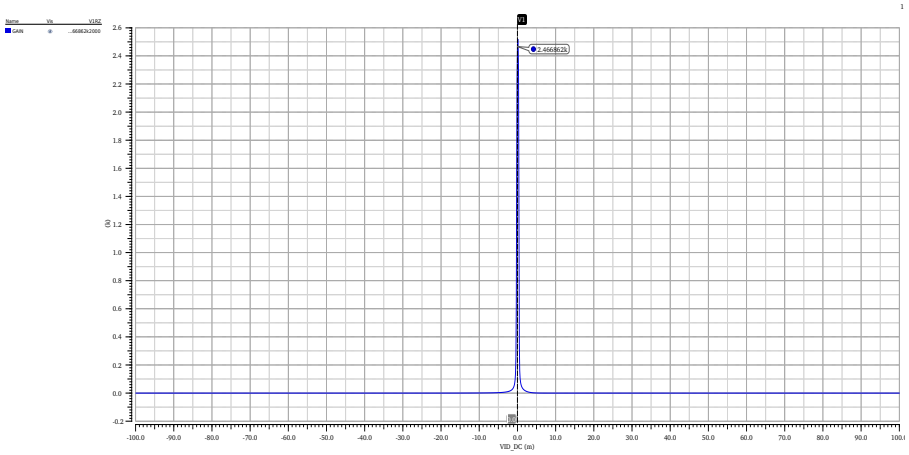

Figure 17: DC gain Vs V_{ID}

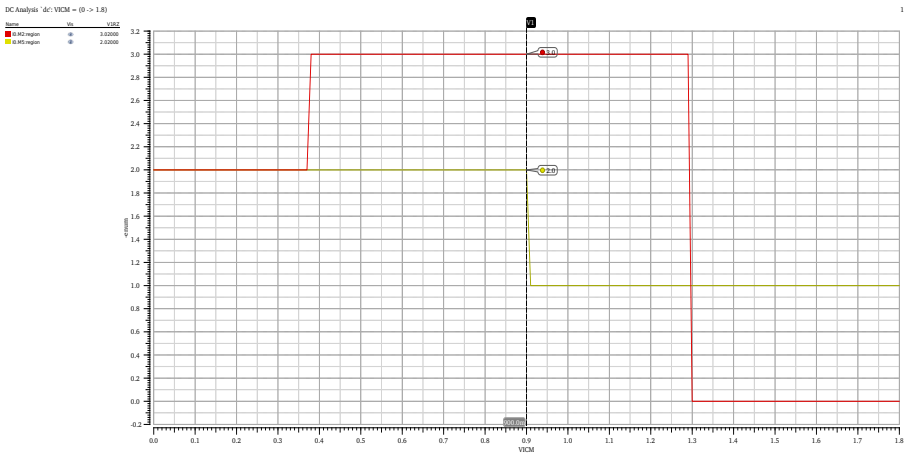

Figure 18: VICM Region M_3 is the input pair

$V_{\text{GS}_{\text{input}}}$ smaller When VICM is high and makes it Larger for when VICM is small.

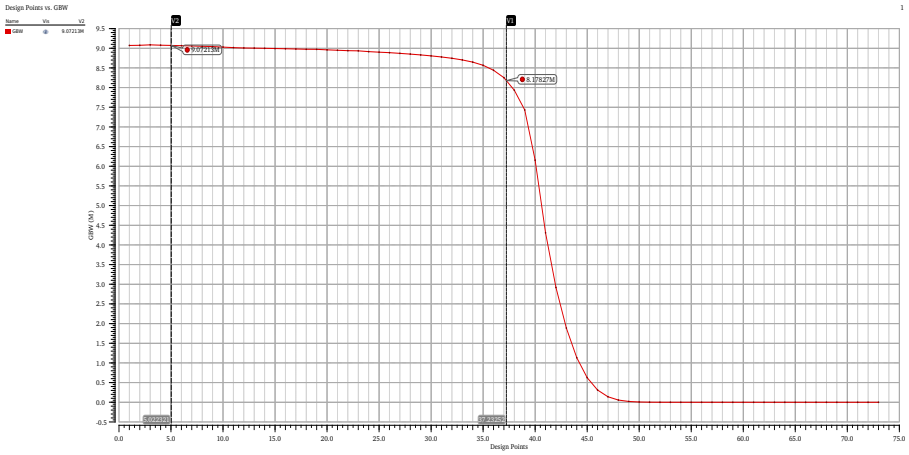

Figure 19: GBW Vs VICM ($\mathrm{VICM_{max}} = 925\,\mathrm{mv}$)

	Analysis	Simulation
$\mathrm{VICM_{HIGH}}$	0.876	0.9
$\mathrm{VICM_{Low}}$	0	0

Table 11: ICMR Simulation Vs Analysis

4 Closed Loop analysis

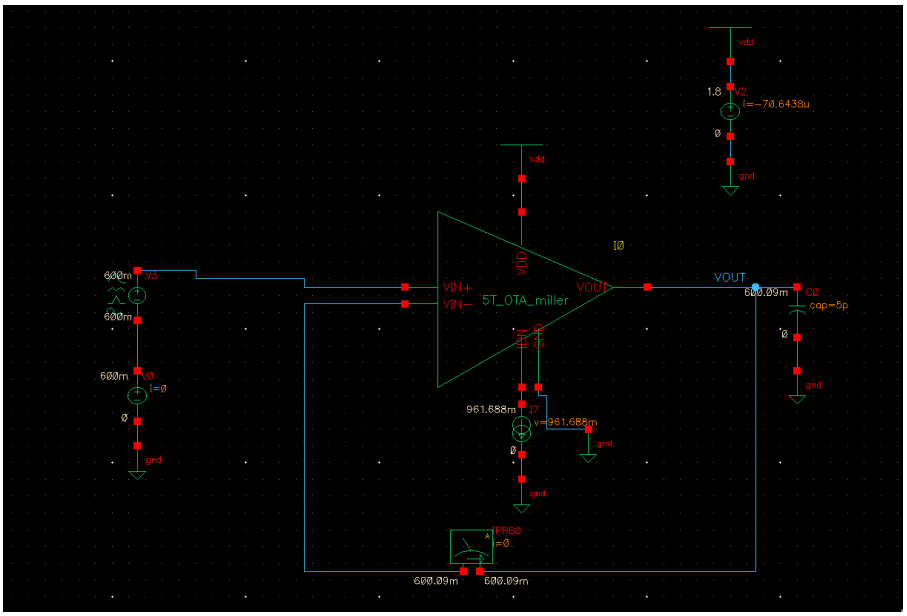

Figure 20: Schematic Diagram

4.1 Operating Point

Comments:

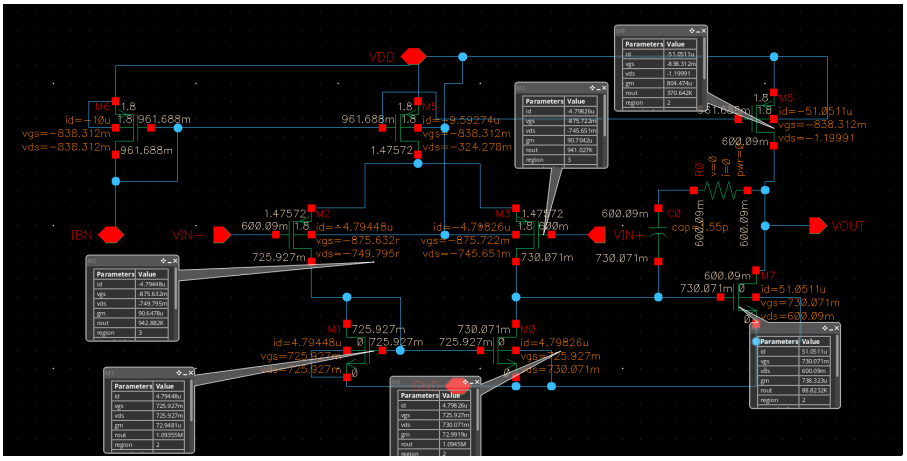

Figure 21: Operating point Annotated (r_z and C_c adjusted)

- Input Voltage at the input terminal are not exactly equal $v_{\text{id}} = 0.09\,\text{mv}$, this is due to the finite Gain of the OTA
- DC Voltage output of the first stage here is not equal to the value from Open Loop analysis ,that's because of the existance of v_{id}=0.09mv , making $V_{\text{out}_1} = V_{\text{CM}} + v_{\text{id}} g_{m2}(r_{o_1} || r_{o2}) \approx$730mv
- I_d and g_m of the input pair is not equal , that's again because of v_{id} which steeres the current.

4.2 Stability Analysis:

PM = 71.1 $>$ 70.

Test	Output	Nominal	Spec	Weight	Pass/Fail
Labs:miller_OTA_lab9_closed_loop:1	PM	-108.9			
Labs:miller_OTA_lab9_closed_loop:1	DC_Loop_gain	2.477k			
Labs:miller_OTA_lab9_closed_loop:1	Phase				
Labs:miller_OTA_lab9_closed_loop:1	UGF	8.336M			
Labs:miller_OTA_lab9_closed_loop:1	GBW	8.865M			
Labs:miller_OTA_lab9_closed_loop:1	dB20(getData("loopGain" ?resul...				

Figure 22: Phase Margin,GBW,UGF and DC loop gain ($C_C = 1.55p$, R = 2K)

Loop gain is less than Open Loop gain, this maybe becasue of $V_{\text{out}_{\text{CM}}}$ is different making r_o for output stage is different also mismatch due to v_{id} ,GBW and UGF are close to that of open loop.

Analysis: Calculating Phase margin , $\text{PM} = \tan^{-1}\left(\frac{\text{GM}_2}{G_{M1}} \times \frac{C_C}{C_L}\right) = 68.38$, PM from simulation is larger due to r_z

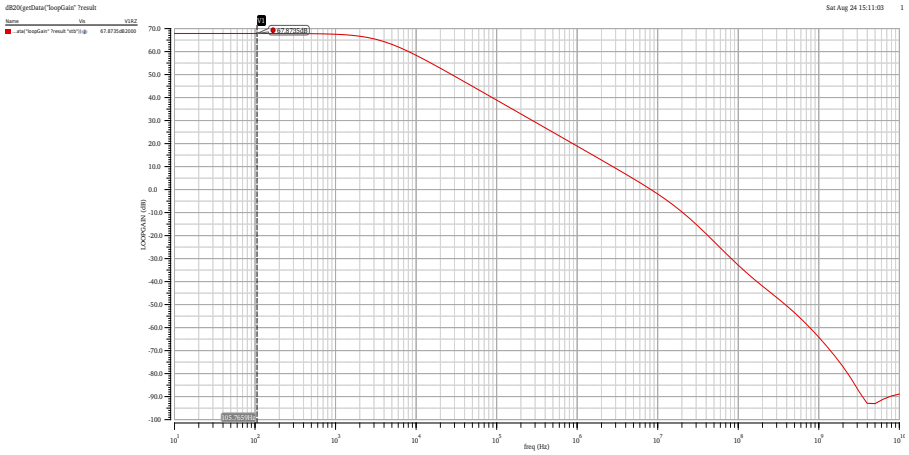

Figure 23: Loop gain bode plot

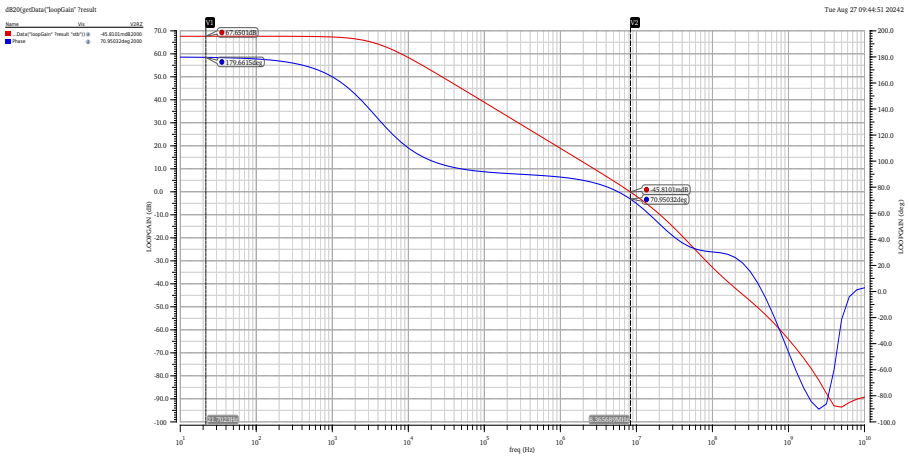

Figure 24: Bode Plot and Phase plot for Loop gain

	Analysis	Simulation
PM	68.38	71.1
DC Loop gain	2400	2477
GBW	9.2M	8.86M
UGF	9.2MHz	8.33MHz

Table 12: Loop gain Analysis Vs Simulation

4.3 Transient Analysis

4.3.1 SR

$V_{\text{Low}} = 50\,\text{mv}$, $V_{\text{High}} = 890\,\text{mv}$,

	RZ	slewRate..."time")
1	2.000E3	5.404E6

Figure 25: Slew Rate (50mv to 890mv)

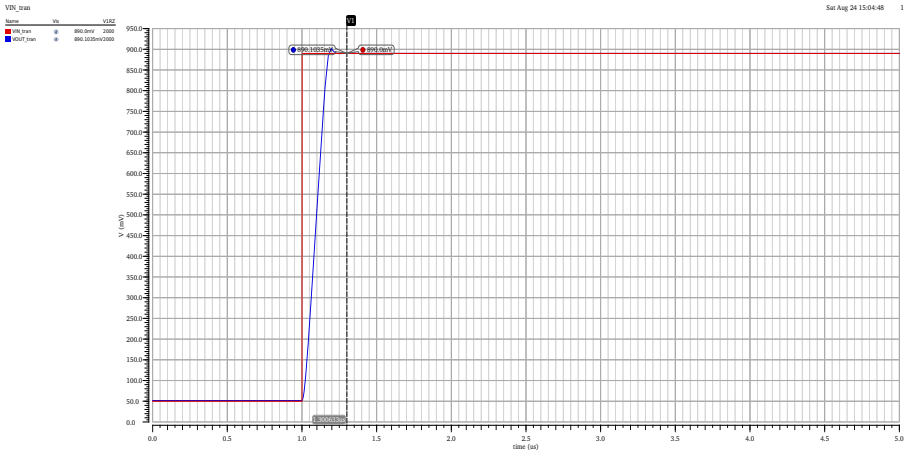

Figure 26: V_{out} and V_{in} Vs time

Analysis: SR $= \frac{I_{B1}}{C_C} = 6.45V/\mu s$, this deviation because of r_z.

	Analysis	Simulation
Slew Rate	6.45V/μs	5.4$V/\mu s$

Table 13: Slew rate Analysis Vs Simulation

4.3.2 Setteling Time

Test	Output	Nominal	Spec	Weight	Pass/Fail
Labs:miller_OTA_lab9_closed_loop:1	VOUT_tran				
Labs:miller_OTA_lab9_closed_loop:1	VIN_tran				
Labs:miller_OTA_lab9_closed_loop:1	trise	27.92n			

Figure 27: Rise Time

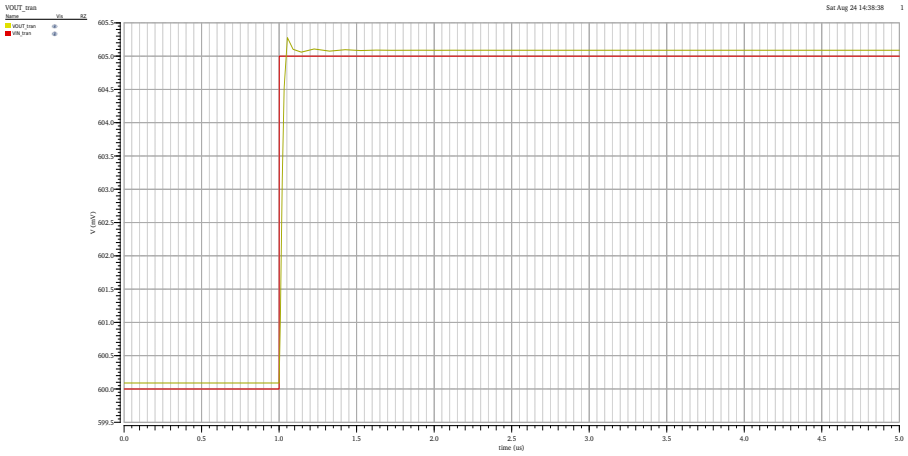

Figure 28: V_{out} and V_{in} Vs time

Analysis: rise time for first order system $= 2.2\tau = 2.2\frac{C_c}{g_{m_{\text{input}}}} = 37.89\,\text{ns}$, rise time from simulation is smaller since it's a second order system.

Comments: There exists time domain ringing becasue PM < 72.4

	Analysis	Simulation
t_{rise}	37.89ns	27.92ns

Table 14: t_{rise} Analysis Vs Simulation

5 DC Closed Loop AC Open Loop

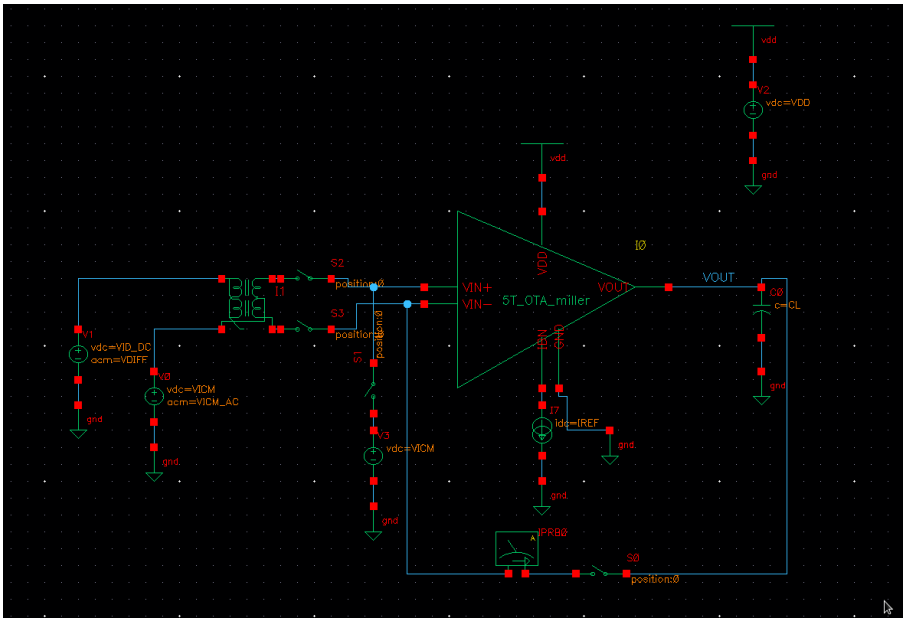

Figure 29: Schematic Diagram

5.1 Operating Point Analysis

For Operating Point Analyis Feedback switches are On and the Operating point is similar to Closed Loop.

5.2 AC analysis

Now For AC Simulaton Feedback switches will be off and results aresimilar to open Loop Simulation.

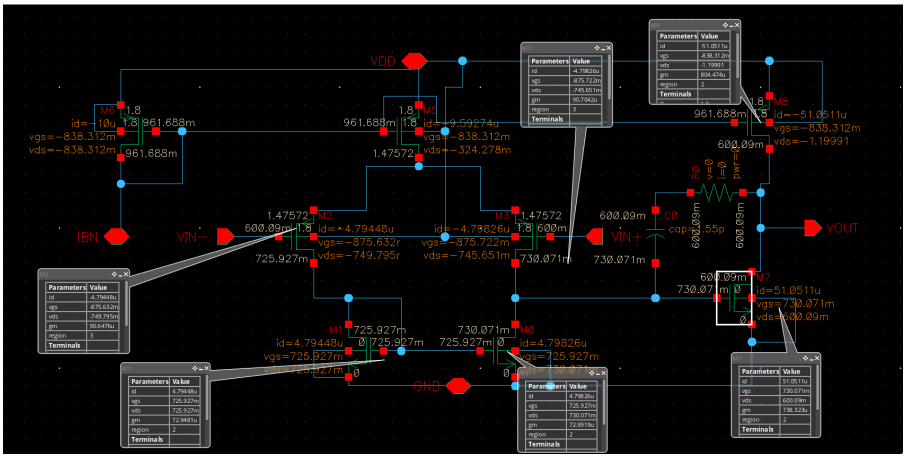

Figure 30: Operating Point Annotated

5.2.1 Differential Mode

First we begin by Differential Mode Analyis:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Labs:miller_OTA_lab9_Open_Loop:1	GBW	8.889M			
Labs:miller_OTA_lab9_Open_Loop:1	UGF	8.376M			
Labs:miller_OTA_lab9_Open_Loop:1	A_V_db				
Labs:miller_OTA_lab9_Open_Loop:1	A_V0	2.413k			

Figure 31: Differential Gain , GBW and UGF

Here A_v bode plot:

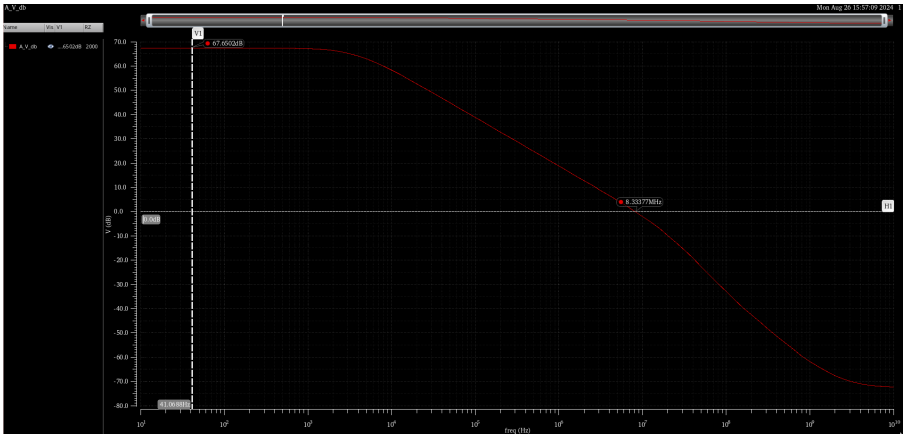

Figure 32: Differential Gain Bode plot

5.2.2 Common Mode

Now For Common Mode:

Test	Output	Nominal	Spec	Weight	Pass/Fail
Labs:miller_OTA_lab9_Open_Loop:1	GBW	902.2			
Labs:miller_OTA_lab9_Open_Loop:1	UGF	eval err			
Labs:miller_OTA_lab9_Open_Loop:1	A_V_db				
Labs:miller_OTA_lab9_Open_Loop:1	A_V0	244.9m			

Figure 33: CMR

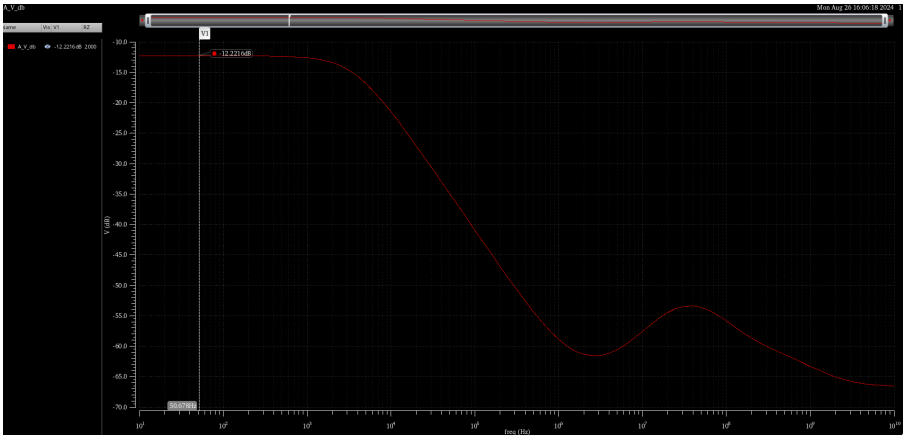

Figure 34: CMR bode plot

6 Achieved Specification

Technology	0.18um	Achieved Specs
Supply voltage	1.8V	1.8V
Static gain error	$\leq$ 0.05%	0.015%
CMRR @ DC	$\geq$ 74dB	88.73dB
Phase margin (PM)	$\geq$ 70°	71.1°
OTA current consumption	$\leq$ 60uA	60uA
CMIR – high	$\geq$ 1V	0.925V
CMIR – low	$\leq$ 0.2V	0
Output swing	0.2 – 1.6V	0.108 – 1.696V
Load	5pF	5pF
Buffer closed loop rise time (10% to 90%)	$\leq$ 70ns	27.92ns
Slew rate (SR)	5V/μs	5.4V/μs

Table 15: Required Specifications and Achieved Specifications