DESIGN OF OPERATIONAL AMPLIFIER FOR BIO-SIGNALS

ABDOLRAOUF RAHMANI

DEPARTMENT OF ELECTRICAL ENGINEERING

FACULTY OF ENGINEERING

UNIVERSITY OF MALAYA

KUALA LUMPUR

2021

1. Abstract

Continuous measurement of patient parameters such as heart rate and rhythm, respiratory rate, blood pressure, blood-oxygen saturation, and many other parameters have become a common feature of the care of critically ill patients. These parameters are known as bio signals. When accurate and immediate decision-making is crucial for effective patient care, electronic monitors frequently are used to collect and display physiological data. The electronic circuit for measurement must be designed specifically for these low voltage and low varying bio-signals. This paper proposes a design of bio-signal amplifier circuit to achieve a given transfer function whose inputs are temperature, heart rate, blood oxygen and respiratory rate.

2. Design Requirements

This section points out the design requirements as well as considerations to be taken for designing the amplifier circuit.

Requirements: for the circuit are given as below.

- Amplifier circuit must amplify voltages of **10 microvolts to 100 mV**
- Circuit must consider a noise reduction method
- Resistor values are limited to less than **10k Ω**
- Circuit achieves the transfer function below:

$$V_0 = -4\left(V_t + 1.5V_{hr} + 3V_{bo} + V_{rr}\right)$$

Where V_t , V_{hr} ,V_{bo} ,V_{rr} are the temperature, heart rate, blood oxygen, respirator rate sensor signal outputs.

- Operational Amplifiers:
  a. Input impedance of 4M Ω
  b. Output impedance of 50 Ω
  c. Open loop gain of 200,000

d. Operating with supply voltage of -+12V
e. No capacitor should be used
f. Gain of NPN must be considered as 200 while PNP as 150

Design Considerations: Due to the low voltage values of bio-sensors, it is of utmost importance to reduce the loading throughout all stages of the amplifier circuits. Furthermore, the quality of output is prioritized over cost optimization.

3. Introduction

To obtain the summation of input signals the use of operational amplifiers is essential. Practical operational amplifiers are made up of three major stages: Differential input stage, the gain stage and the output stage. To design a practical operational amplifier with given characteristics, a basic operational amplifier is first proposed (see Fig. 1), and its components explained. This will introduce the background of amplifiers as well as the design procedure used.

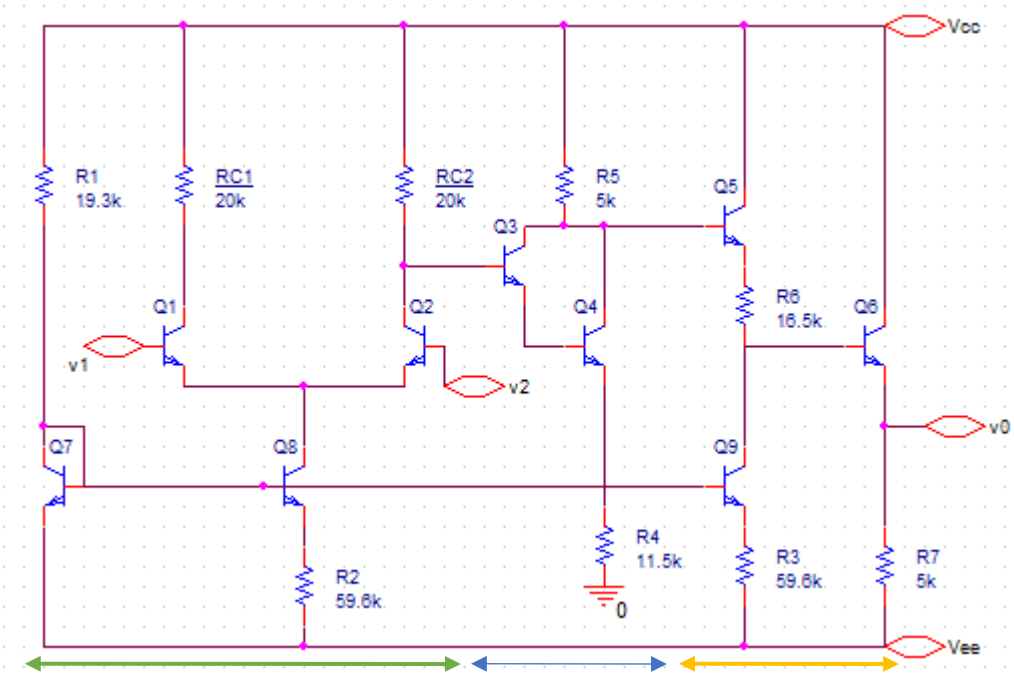


Figure 1: basic Op-amp with 3 stages, Differential input stage (green arrow), Gain stage (Blue arrow) and output stage (yellow arrow)

1.1.Differential input stage

Operational amplifiers require a differential input, and this is provided by a differential pair in the input stage. Differential pair amplifiers have characteristics that achieves the requirements for an input stage (see Table 1).

Characteristics	*Input stage requirement achieved*
High common-mode rejection ratio	Low noise in the output by providing more differential gain
High input impedance	Low loading effect
High differential voltage gain	Voltage gain for signal amplification
Single-ended output	The op-amp is expected to have a single output so a conversion at input stage is carried out which also allows other stages to be single-input single-output amplifiers.
Low output impedance	Low loading for the next stage
Use of npn transistors or CC or CB amplifiers in design	Good Frequency response

The voltage gain in input is desirable since the noise and offset voltage associated with the later stages are divided by this gain when referred to the input. Another notable input stage requirement is level shifting to maximize the range of output voltages. In 741 this is carried out by use of pnp transistors whose emitter is near input voltage and collector near negative supply.

1.2.Gain and Output Stage

The second op-amp stage, or gain stage, is often a Darlington pair connected to the diff-amp output, and a simple emitter-follower. Darlington pairs contribute to the overall gain of the amplifier and they also ensure that no loading is caused with later or prior stages. The current gain provided is high as the base current is magnified twice as it goes to the emitters. Furthermore, the input impedance is high due to reflection of base resistor of second resistor. Lastly the output impudence is high as the resistance seen is that of r_0.

Direct coupling of amplifier stages, not using coupling capacitor, is essential in IC design to ensure that space and size is saved. However, this results in dc level to buildup throughout the stages. To level shift, or level translate this DC value, level shifters are used. This is usually a common collector configuration which is made up of npn for level down and pnp for level up. Common collectors are used as they have a ac gain of 1 while a DC shift of about 0.7V.

4. Proposed Schematic and Design Approach

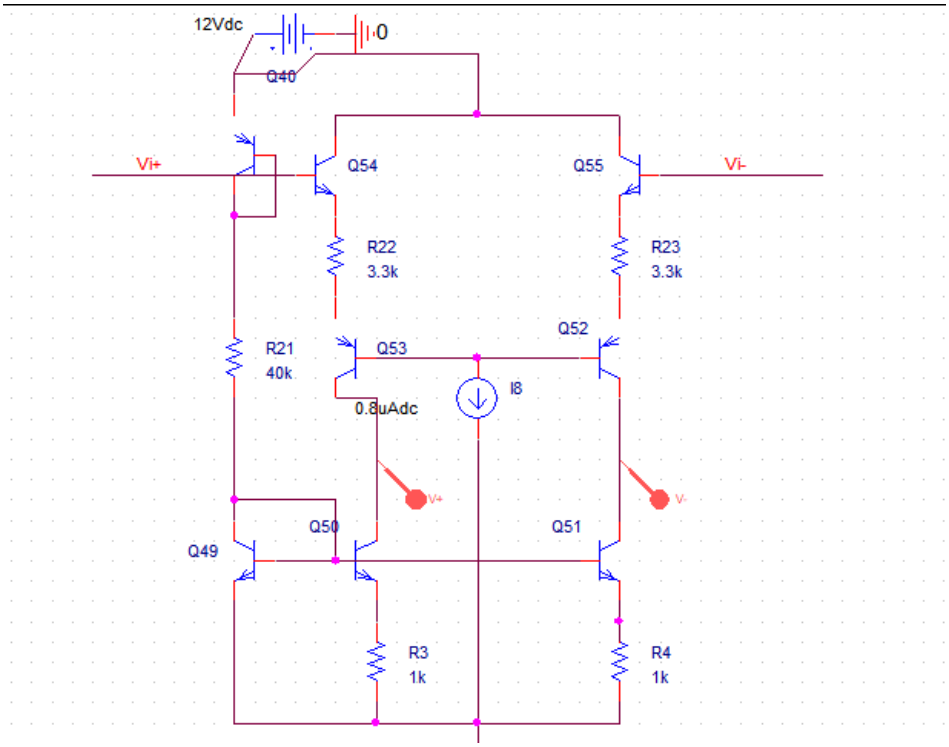


Figure 2: The main focus of design was to add the above additional stage.

Designing Op-amps makes use of the aforementioned stages. 741 op-amps are very good multistage operational amplifiers based on BJTs. It already achieves most criteria except the 4M ohm input impedance. To solve this another stage will be used as input where it provides the input impedance, as well as a bit of gain. Adding another stage to differential amplifier will increase the dc level in the output so in order to be efficient with time and utilize 741 fully, the input stage will have its own level shifting. This way no DC level is sent to 741.

This stage must be made up of differential pair and produce a balanced output. To provide a portion of the input impedance the input will see the similar resistance as that of 741, giving $2r_{pi}$. As this is not sufficient two resistors are added between the pnp and npn transistors. The value must provide the remaining resistance. Admittedly as was pointed out during presentation, a Darlington pair would add the additional resistance. This was wrongly shrugged off because of the assuming that the value of r_{pi} is small.

Furthermore, in order to ensure the gain of amplifier is high, active loads are added. Unlike unbalanced diff-amps, active loading balanced amplifier was proof to be difficult. In the end it was decided that the only sufficient resistance on a transistor is that of r_0 and so the collector must see this. Furthermore, since active loads are self-biased the current mirror was selected. The current mirror used must be driven (follow the reference current) from an external transistor. This contrasts with current mirrors for unbalanced diff-amps that utilize an internal driving transistor. Furthermore, an additional resistor was added to the emitter of active loads to allow for biasing of the transistors.

Unlike in 741, the pnp transistor does not form a complex feedback loop. Instead, a simple biasing is done at the base. After several unsuccessful attempts to form feedback, it was decided that the preferred choice would be to use normal biasing as it makes design simpler, and the behavior more easily understood.

Free simulators readily available allow a limited number of transistors for simulation. To allow for simulation current sources are used instead of current mirrors. However, the isolated stages will be simulated with current mirrors to showcase how the currents are achieved. Despite using current sources using the above input stage could not be done as it holds many transistors. For purpose of simulating the entire op-amp a simpler design of this stage that doesn’t make use of active load is used. However isolated simulations and gains of the active load design will be explored in the appendix.

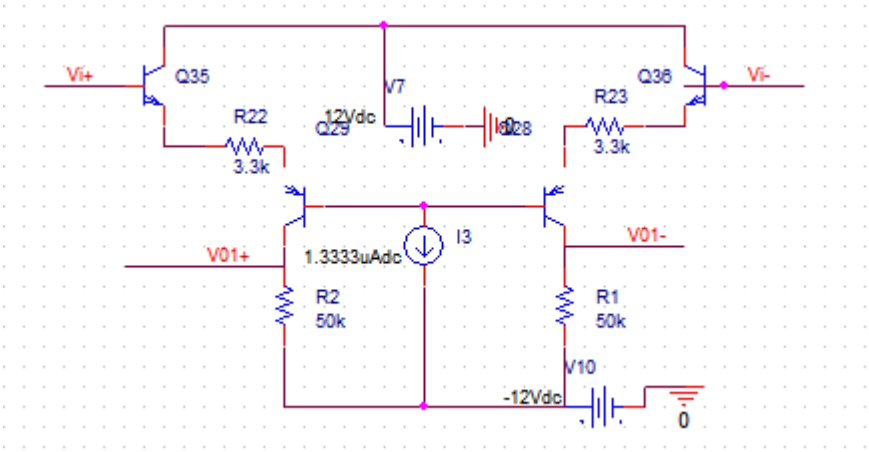


Figure 3: Input stage without active loading.

The complete circuit is given as below

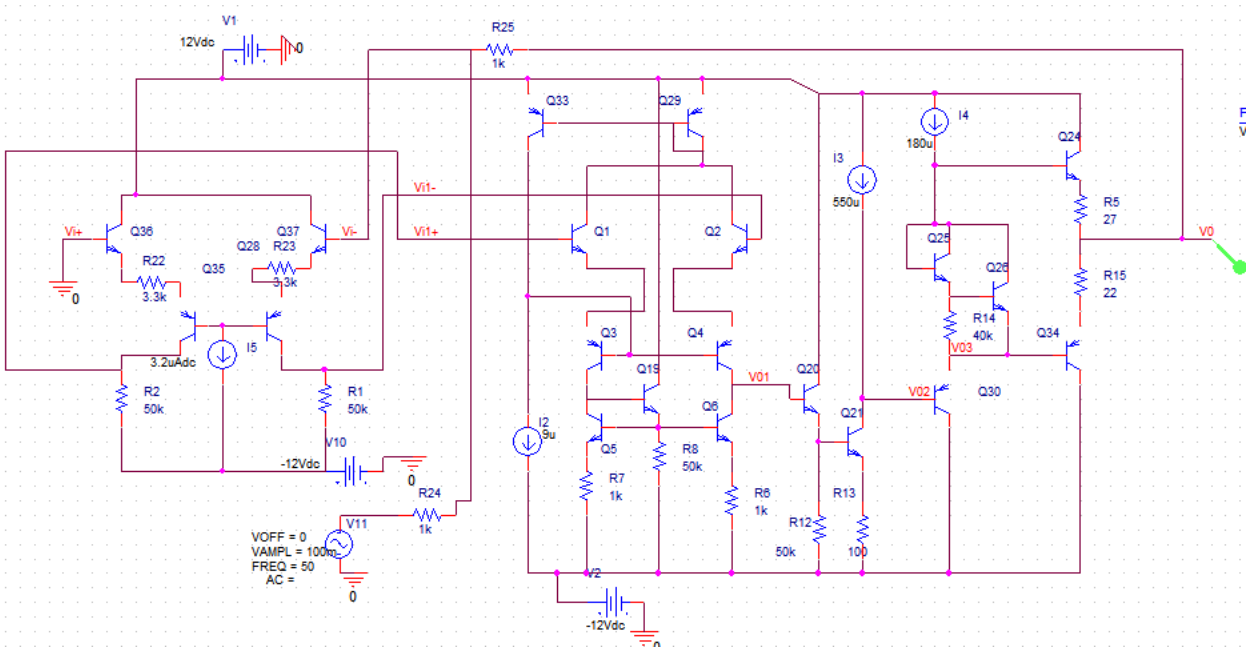


Figure 4: Complete schematic of Op-amp. the op-amp is being used as inverting amplifier of gain 1.

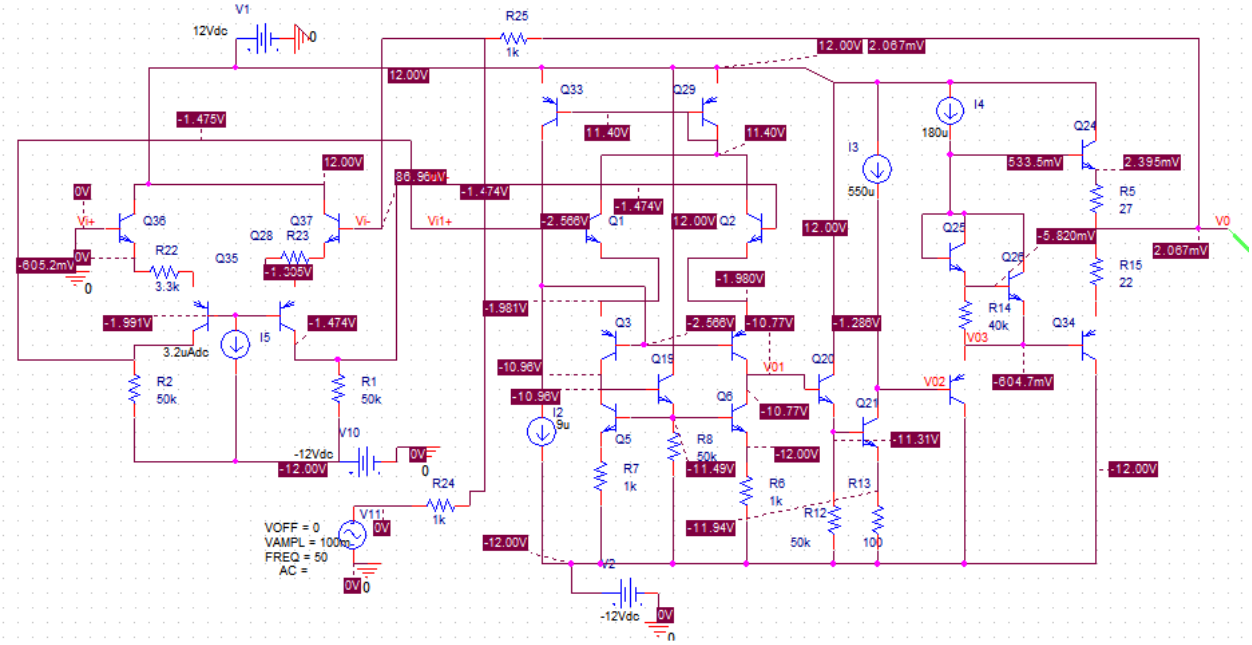


Figure 5: Schematic with bias voltages.

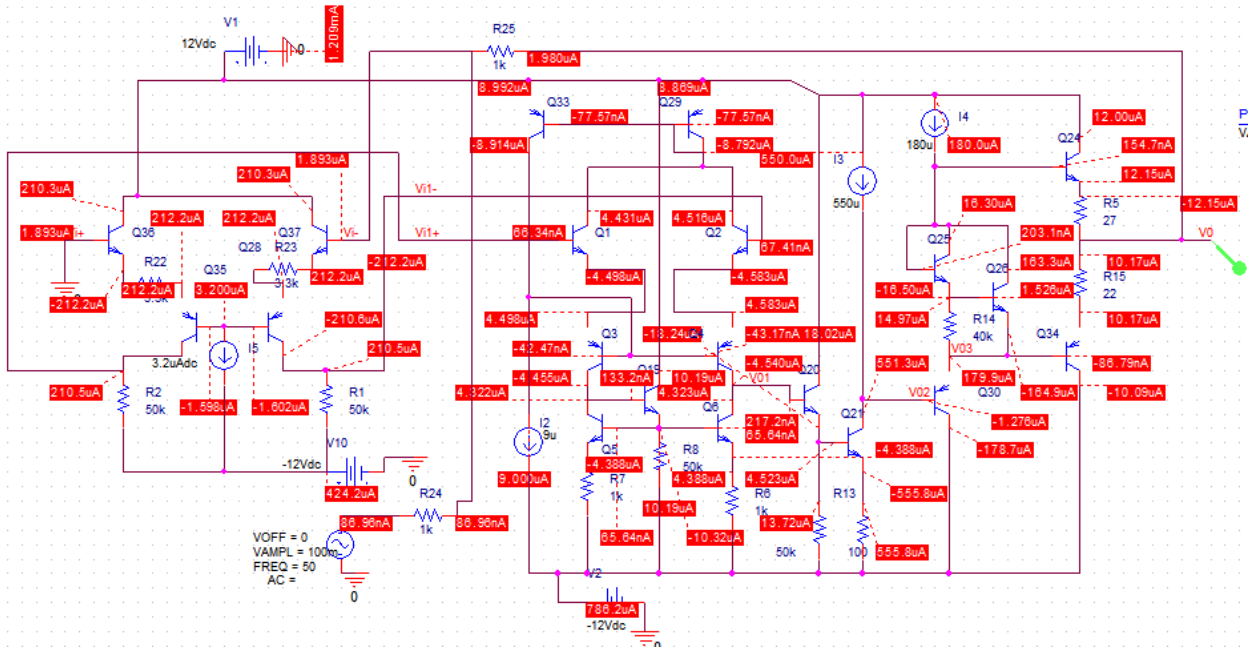


Figure 6: schematic with bias currents.

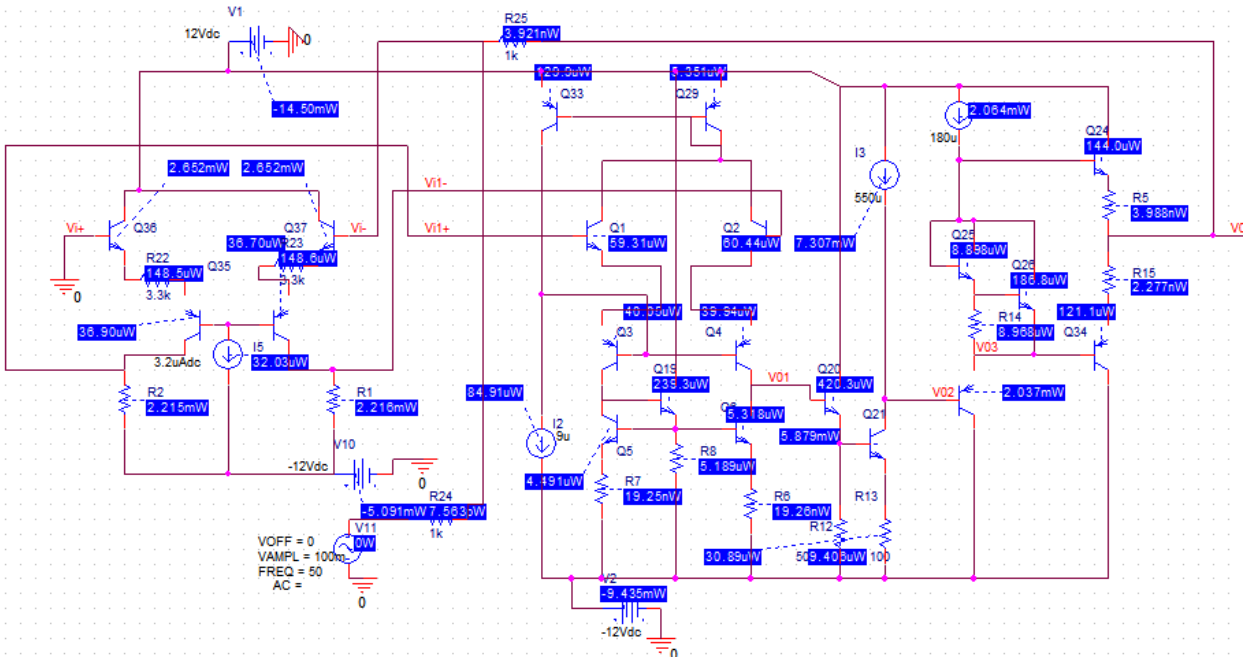


Figure 7: schematic showing power consumption.

5. Qualitative Analysis of Op-Amp

The first stage has been fully discussed in the previous section. Next the qualitative analysis of the 741 stages is discussed. The 741 circuit consists of three stages: an input differential stage, an intermediate single ended high-gain stage, and an output-buffering stage. Transistors Q1 and Q2 act as emitter followers, causing the input resistance to be high and delivering the differential input signal to the differential common-base amplifier formed by Q3 and Q4. Transistors Q5, Q6 and Q19 and resistors R7, R6, and R8 form the load circuit of the input stage. This is an elaborate current-mirror load circuit. It will be shown that this load circuit not only provides a high-resistance load but also converts the signal from differential to single-ended form with no loss in gain or common-mode rejection. The output of the input stage is taken single-endedly at the collector of Q6.

741 also includes a level shifter whose function is to shift the dc level of the signal so that the signal at the op-amp output can swing positive and negative. In the 741, level shifting is done in the first stage using transistors

Q3 and Q4. The use of transistors Q3 and Q4 in the first stage results in an added advantage: protection of the input-stage transistors Q1 and Q2 against emitter-base junction breakdown. Since the emitter-base junction of an npn transistor breaks down at about 7 V of reverse bias, regular npn differential stages suffer such a breakdown if the supply voltage is accidentally connected between the input terminals. Pnp transistors, however, have high emitter-base breakdown voltages (about 50 V); and because they are connected in series with Q 1 and Q2 they provide protection of the 741 input transistors, Q1 and Q2. Furthermore, due to use of quite a number of common base emitters the frequency response of this stage should be quite good.

The second stage is as simple as that of Darlington pair used in the introduction section where it provides a decent gain as well as level shifting.

The output stage provides the amplifier with a low output resistance. In addition, the output stage is able to supply relatively large load currents without dissipating large amount of power in the IC. The 741 uses an efficient output circuit known as a class AB output stage. This class avoids the downfall of Class A and B in terms of distortion and power consumption. Furthermore, the power transistors are maintaining on by use of 2 transistors.

6. Use of Standard Resistors

The standard resistors shown in the table are expected to be used for design. These standard values can be added in series, parallel or in T network to give the desired resistance. The use of T network resistor is demonstrated in the summing amplifier section.

Resistance Tolerance (±%)

0.1% 0.25% 0.5%	1%	2% 5%	10%	0.1% 0.25% 0.5%	1%	2% 5%	10%	0.1% 0.25% 0.5%	1%	2% 5%	10%	0.1% 0.25% 0.5%	1%	2% 5%	10%	0.1% 0.25% 0.5%	1%	2% 5%	10%	0.1% 0.25% 0.5%	1%	2% 5%	10%
10.0	10.0	10	10	14.7	14.7	—	—	21.5	21.5	—	—	31.6	31.6	—	—	46.4	46.4	—	—	68.1	68.1	68	68
10.1	—	—	—	14.9	—	—	—	21.8	—	—	—	32.0	—	—	—	47.0	—	47	47	69.0	—	—	—
10.2	10.2	—	—	15.0	15.0	15	15	22.1	22.1	22	22	32.4	32.4	—	—	47.5	47.5	—	—	69.8	69.8	—	—
10.4	—	—	—	15.2	—	—	—	22.3	—	—	—	32.8	—	—	—	48.1	—	—	—	70.6	—	—	
10.5	10.5	—	—	15.4	15.4	—	—	22.6	22.6	—	—	33.2	33.2	33	33	48.7	48.7	—	—	71.5	71.5	—	—
10.6	—	—	—	15.6	—	—	—	22.9	—	—	—	33.6	—	—	—	49.3	—	—	—	72.3	—	—	—
10.7	10.7	—	—	15.8	15.8	—	—	23.2	23.2	—	—	34.0	34.0	—	—	49.9	49.9	—	—	73.2	73.2	—	—
10.9	—	—	—	16.0	—	16	—	23.4	—	—	—	34.4	—	—	—	50.5	—	—	—	74.1	—	—	—
11.0	11.0	11	—	16.2	16.2	—	—	23.7	23.7	—	—	34.8	34.8	—	—	51.1	51.1	51	—	75.0	75.0	75	—
11.1	—	—	—	16.4	—	—	—	24.0	—	24	—	35.2	—	—	—	51.7	—	—	—	75.9	—	—	—
11.3	11.3	—	—	16.5	16.5	—	—	24.3	24.3	—	—	35.7	35.7	—	—	52.3	52.3	—	—	76.8	76.8	—	—
11.4	—	—	—	16.7	—	—	—	24.6	—	—	—	36.1	—	36	—	53.0	—	—	—	77.7	—	—	—
11.5	11.5	—	—	16.9	16.9	—	—	24.9	24.9	—	—	36.5	36.5	—	—	53.6	53.6	—	—	78.7	78.7	—	—
11.7	—	—	—	17.2	—	—	—	25.2	—	—	—	37.0	—	—	—	54.2	—	—	—	79.6	—	—	—
11.8	11.8	—	—	17.4	17.4	—	—	25.5	25.5	—	—	37.4	37.4	—	—	54.9	54.9	—	—	80.6	80.6	—	—
12.0	—	12	12	17.6	—	—	—	25.8	—	—	—	37.9	—	—	—	56.2	—	—	—	81.6	—	—	—
12.1	12.1	—	—	17.8	17.8	—	—	26.1	26.1	—	—	38.3	38.3	—	—	56.6	56.6	56	56	82.5	82.5	82	82
12.3	—	—	—	18.0	—	18	18	26.4	—	—	—	38.8	—	—	—	56.9	—	—	—	83.5	—	—	—
12.4	12.4	—	—	18.2	18.2	—	—	26.7	26.7	—	—	39.2	39.2	39	39	57.6	57.6	—	—	84.5	84.5	—	—
12.6	—	—	—	18.4	—	—	—	27.1	—	27	27	39.7	—	—	—	58.3	—	—	—	85.6	—	—	—
12.7	12.7	—	—	18.7	18.7	—	—	27.4	27.4	—	—	40.2	40.2	—	—	59.0	59.0	—	—	86.6	86.6	—	—
12.9	—	—	—	18.9	—	—	—	27.7	—	—	—	40.7	—	—	—	59.7	—	—	—	87.6	—	—	—
13.0	13.0	13	—	19.1	19.1	—	—	28.0	28.0	—	—	41.2	41.2	—	—	60.4	60.4	—	—	88.7	88.7	—	—
13.2	—	—	—	19.3	—	—	—	28.4	—	—	—	41.7	—	—	—	61.2	—	—	—	89.8	—	—	—
13.3	13.3	—	—	19.6	19.6	—	—	28.7	28.7	—	—	42.2	42.2	—	—	61.9	61.9	62	—	90.9	90.9	91	—
13.5	—	—	—	19.8	—	—	—	29.1	—	—	—	42.7	—	—	—	62.6	—	—	—	92.0	—	—	—
13.7	13.7	—	—	20.0	20.0	20	—	29.4	29.4	—	—	43.2	43.2	43	—	63.4	63.4	—	—	93.1	93.1	—	—
13.8	—	—	—	20.3	—	—	—	29.8	—	—	—	43.7	—	—	—	64.2	—	—	—	94.2	—	—	—
14.0	14.0	—	—	20.5	20.5	—	—	30.1	30.1	30	—	44.2	44.2	—	—	64.9	64.9	—	—	95.3	95.3	—	—
14.2	—	—	—	20.8	—	—	—	30.5	—	—	—	44.8	—	—	—	65.7	—	—	—	96.5	—	—	—
14.3	14.3	—	—	21.0	21.0	—	—	30.9	30.9	—	—	45.3	45.3	—	—	66.5	66.5	—	—	97.6	97.6	—	—
14.5	—	—	—	21.3	—	—	—	31.2	—	—	—	45.9	—	—	—	67.3	—	—	—	98.8	—	—	—

NOTE: These values are generally available in multiples of 0.1, 1, 10, 100, 1 k, and 1 M.

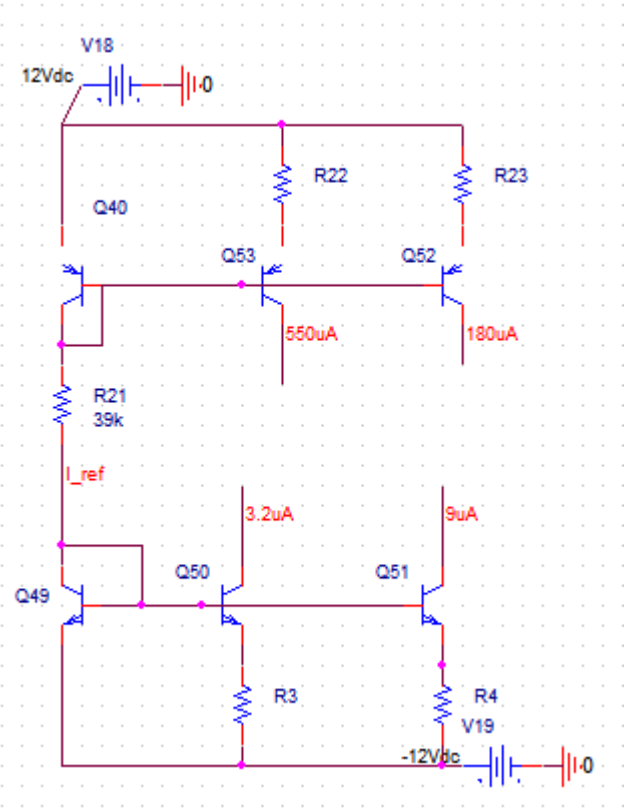
Figure 8: standard resistor table showing both normal and precision resistors. Precision resistors can even provide 1ohm resistance.

7. DC Analysis

This section will cover the evaluation of dc currents and voltages to find transistor parameters. The analysis will involve discussing the logic in finding major currents and voltages. Since the other values are obtained in similar manner they are not mentioned. To evaluate the particular transistor parameter, the simulated results can be used as they are close to expected theoretical values.

1.3. Bias Circuit

Although the biasing in the schematic is done using current sources, the biasing in IC design is done using current mirrors. Here the current mirrors that are to replace current sources are shown:



$$I_{ref}=\frac{V_{cc}-V_{ee}-2V_{be(on)}}{39k}=0.73m$$

To get the resistor values the equation below is used:

$$V_T \ln\left(\frac{I_{ref}}{I}\right) = R * I$$

Where R is the resistor at emitter, V_T is 0.025, and I is the bias current desired. Hence, we obtain for the resistors:

Bias Current (I)/ uA	***Emitter Resistor / Ω***
3.2	42.4k
9	12.2 k
550	13
180	195

Instead of using the low emitter resistors, alternatively transistors with different saturation values can be selected. In this case there is no emitter resistance, and the current relationship is that of natural log.

1.4.Input Stage

The bias current 3.2uA is split between the two base currents evenly as both are matched and their emitter base voltage is same. Furthermore, this current is amplified by B to give the collector currents.

$$I_b = \frac{3.2u}{2} = 1.6\,uA$$

$$I_c = I_b * B = 1.6\,u * 150 = 240\,uA$$

This collector is equivalent to current across the resistor R1 as it can be assumed that base current is negligible. Hence voltage is given by:

$$V_{R1} = I_c * R_1 = 10.53\,V$$

Using the bottom rail voltage, the input dc voltage to 741 can be calculated. This DC voltage can be altered by changing the values of R and I_Q (bias current at the base). However, the values must retain within a certain range to allow active forward operation of transistors, so current bias can't be reduced too much. The values I_Q and R_1 are selected based on this information.

1.5. 741 Diff Stage

Due to matching of both halves of the differential stage both will take the same current from the 9uA bias. This current can be used to evaluate the voltage at the emitter of the active load of this stage.

$$I_Q = 9\,uA$$

$$I_c = \frac{9}{2} = 4.5\,uA$$

$$V = I_c * R_6 = 4.5\,mV$$

This voltage is about negligible so the node voltage at the top can be assumed to be as -12V. This allows us to obtain the base voltage at the active loads. To evaluate the other voltage values, the voltage from the previous stage must be considered. This allows us to evaluate the remainder of the nodal voltages by simple subtracting the $V_{be\ (on)}$, 0.586V in simulation which is assumed to be 0.7 for simplicity of calculation.

1.6. 741 Gain Stage

For the dc offset at output to be zero, the current through collector of Q21 must be equivalent to that of current source 550uA. This allows us to get the base voltage of Q21 by using the emitter resistor and base-emitter voltage formula.

$$V_{B21} = 550u * 100 + V_T \ln \frac{550u}{10^{-14}} = 697mV$$

Where 10^{-14} is the saturation current. The base current is then obtained using gain:

$$I_{B21} = \frac{550uA}{200} = 2.75uA$$

And adding the base current to current through 50k resistor we obtain for $I_{C20:}$

$$I_{C20} = \frac{697mV}{50k} + 2.75u = 16u$$

1.7. 741 Output Stage

Since for dc analysis the output is assumed to be zero with no current flowing through it, current in collector of Q34 and Q24 is equal. Furthermore, the current through 40k resistor is given by:

$$I_{40} = \frac{0.7}{40k} = 17.5u$$

Using KCL at junction of Q26's collector the collector current is obtained as:

$$I_{C26} = 180u - 17.5u = 162.5u$$

The above steps can be done in iteration by reevaluating the resistor current I_{40} but the result will only change slightly so the current values are taken.

Lastly, to evaluate the current in the other two transistors, the equation below is used:

$$I_{24} = -I_{34} = \sqrt{I_{C25} I_{C26}} \sqrt{\frac{I_{S14} I_{s34}}{I_{S25} I_{S26}}} = \sqrt{162.5\,u * 17.5\,u} * 3 = 159.98\,uA$$

The multiplication by 3 is because the standard root of ratio of the saturations gives 3.

8. AC Analysis

This section will cover the ac analysis in order to evaluate the gain of each stage, overall voltage gain, input and output impedance and Frequency response. The frequency response will be simulated for the whole op-amp. The transistor parameters will be calculated based on the dc bias schematic as the values there are very close to the calculated values. Early voltage is assumed to be 100.

1.1. Input Stage

The differential input resistance is very similar to that of 741 except there is 2 series resistors. The total resistance is then given by:

$$R_i = 4r_{pi} + (B+1) * 3.3k = 716{,}126$$

To get the gain it must be understood that the base of pnp becomes a ac differential ground. Furthermore, the collector of Q3 and Q4 become ac grounds due to differential input as well as the small resistance contribution

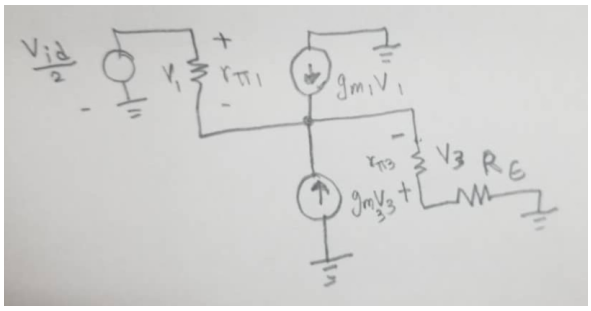


Figure 9: ac equivalent circuit of Q1 and Q3

when compared to r_0. The equivalent half circuit will then be:

Using KCL at the emitter junction as well as KVL from source to ground at emitter of Q3, the collector currents are obtained as:

$$i_{c3} = \frac{-v_{id}}{4\left(r_{pi3} + R_e(B+1)\right)}$$

$$i_{c4}=\frac{+v_{id}}{4\left(r_{pi3}+R_e\left(B+1\right)\right)}$$

Since output current is ic3 – ic4, then the transconductance becomes:

$$G_1=\frac{-1}{2\left(r_{pi3}+R_e\left(B+1\right)\right)}=0.736\,u$$

Output resistance is equivalent to parallel of 50k resistor with resistance seen from the collector of Q28:

$$R_o=50\,k\vee\left(r_{028}*\left(1+R_{eq}*g_m\right)\right)R_{eq}=r_{pi}\vee\left(R_E+\frac{r_{pi}}{B+1}\right)=2768.57 g_m=8.4\,m$$

$$R_o=50\,k\vee 11.6\,M=49784$$

1.2.741 Diff Stage

The resistance seen looking into the emitter of Q3 is given by:

$$R_{eq}=\frac{1}{g_{m3}\left(1+\frac{1}{B_3}\right)}$$

$$R_{id}=2\left(r_{pi1}+\left(B_1+1\right)R_{eq}\right)$$

$$R_{id}=2\left(2\,r_{pi1}\right)=4*376{,}846=1.5\,M$$

To get the gain it must be understood that the base of pnp becomes ac differential ground. Furthermore, the collector of Q3 and Q4 become ac grounds due to differential input as well as the small resistance contribution when compared to r_0. These are similar steps to previous stage but now we get for gain as:

$$G_2=\frac{g_{m1}}{2}=88.62u$$

The output resistance is obtained by getting equivalent resistance resulted from parallel of resistor seen by output into Q4 and Q6.

$$R_{o2}=\left(r_{04}*\left(1+R_{eq4}*g_m\right)\right)\vee ¿\left(r_{06}*\left(1+R_{eq6}*g_m\right)\right)$$

Taking approximation knowing Beta is a lot more than 1 and more than g_m(1k). Furthermore, given early voltage of 100 the resistor is obtained:

$$R_{02}=2\,r_{04}\vee 1.36\,r_{06}=2*22\,M\vee 1.36*23.256\,M=18.4\,M$$

1.3. 741 Gain Stage

First lets get resistance seen from base of Q21.

$$R_{eq}=r_{pi21}+\left(B+1\right)100=115101+20100=25627$$

Then input resistance is given by:

$$R_i=r_{pi20}+\left(B+1\right)\left(R_{eq}\vee ¿\,50\,k\right)$$

$$R_i=3{,}520{,}675$$

Transconductance is obtained by assuming emitter follower to have unity gain:

$$G_3=\frac{g_{m21}}{1+g_{m21}R_E}=\frac{7.148\,m}{7.148\,m*100+1}=4.168\,m$$

Output resistance is given by the parallel of current mirror to the top with the collector of Q21:

$$R_o = r_{o-bias} \vee ¿ \left(r_{021} \left(1 + R_{eq} * g_m \right) \right)$$

$$R_0 = 181818 \vee ¿ 311{,}046 = 114{,}745$$

1.4. 741 Output Stage

Assuming current is flowing out with 2mA into load of 2k ohm, the resistance of Q24 from base is obtained as:

$$R_{eq\,1} = r_{pi\,24} + \left(B + 1 \right) \left(2\,k \right) = 590051$$

$$R_i = r_{pi30} + \left(B + 1 \right) \left(r_{0\,-bias} \vee R_{eq\,1} \right) = 290395$$

$$A_{V\,4} = 1$$

1.5.Total Gain

$$A_T = G_1 * \left(R_{01} \middle| R_{i2} ¿ * G_2 * \left(R_{02} \middle| R_{i3} ¿ * G_3 \left(R_{03} \middle| R_{i4} ¿ = 0.736\,u * \left(49784 \vee 1.5\,M \right) * 88.62\,u * \left(18.4\,M \vee 3{,}520{,}675 \right) * 4. \right. \right. \right.$$

$$A_T = 0.736\,u * 48387 * 88.62\,u * 2955220 * 4.168\,m * 82246.5673$$

$$A_T = 0.03561 * 261.89 * 342.8036 = 3196.95$$

1.6.Frequency Response

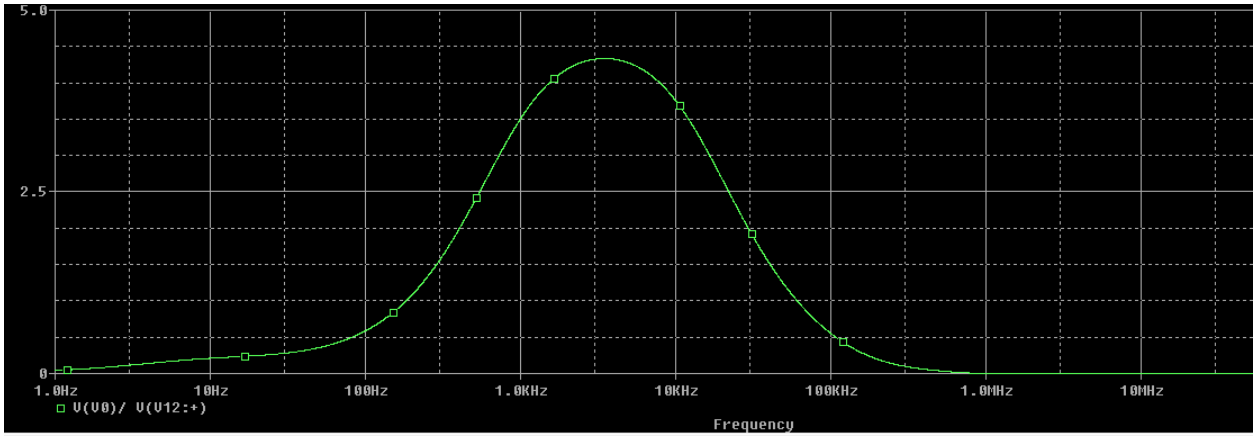


Figure 10: Frequency Response showing that the transistor acts as a band pass.

The design shows that the op-amp has low gains at low frequencies. This makes it unsuitable for use.

9. Application as Summing Amplifier

To achieve the bio signal transfer function the following circuit is used:

$$V_0 = -4\left(V_t + 1.5V_{hr} + 3V_{bo} + V_{rr}\right)$$

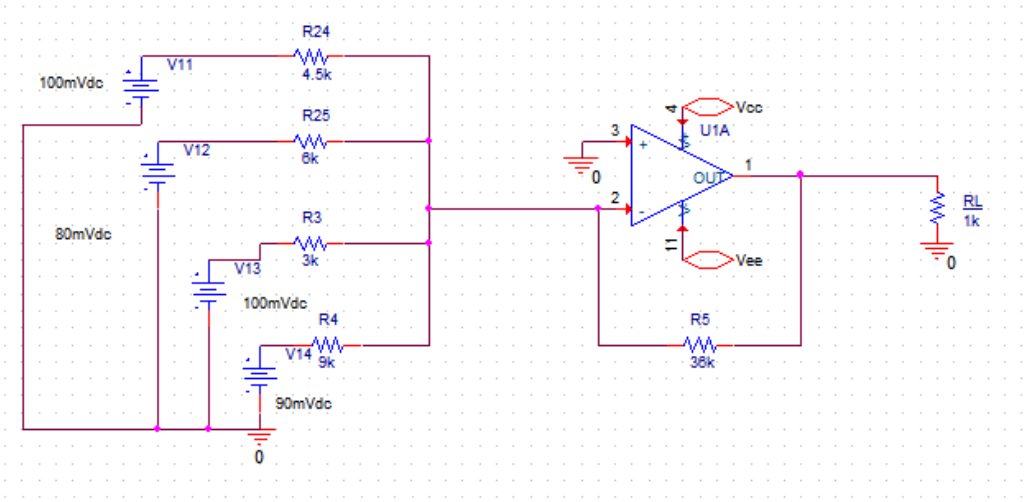


Figure 11: Summing amplifier to achieve the given function. Take note that the op-amp model shown is merely for presentation, For the purpose of simulation the designed op-amp was used.

The 36k ohm can be achieved using the T network below:

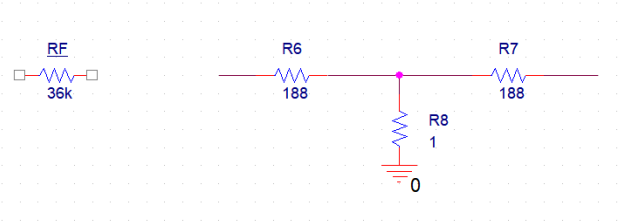


Figure 12: T resistor network to obtain 36k ohms with use of resistors less than 10k

Simulation results for the circuit gives the below graph:

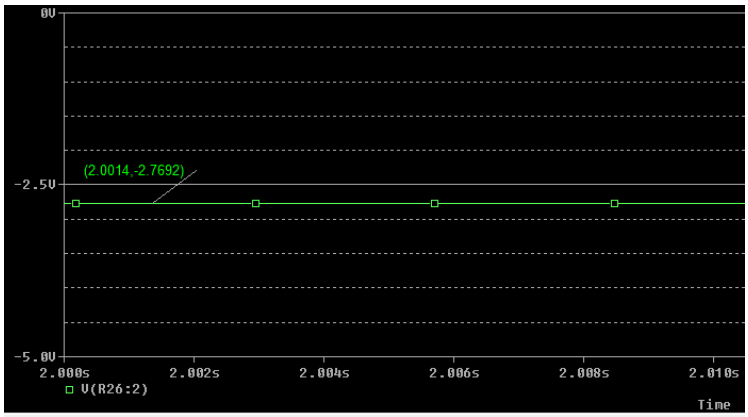


Figure 13: The Op-amp produces a dc signal of -2.7692V.

The theoretical value is -2.84V. This is only a 2.4% difference.

10. Op-amp Performance

The table below summarizes the performance of the op-amp.

Table 1: Table showing the design criteria achieved vs desired.

Criterion	Achieved	Desired
Gain (theoretical)	3196.95	200,000
DC offset (when used as inverting) / V	2.06 mV	0 V
Input Impedance (Theoretical) / Ohm	716,126	4M
Output Impedance (Theoretical) / Ohm	49	50
Power / mW	29.026	8
Frequency Trend	Band Pass	Low Pass

Throughout my design the sufficiency of gain was measured in two ways. Firstly the op-amp stages were simulated without any coupling. Secondly the multistage op-amps where simulated and they were used as inverting amplifier. The degree of closeness was considered to be proportional to the gain. This has resulted in wrong assumptions in the gain of the amplifier. Gains should be either measured by inputting extremely low voltage signals and then observe the output, or to theoretical approximate the gain. To improve the gain the first stage should not be used. The initial design with active load is more suitable but the resistors at the emitter should be removed.

The DC offset is relatively low but when compared to the lowest input signal (10uV) the offset voltage is seen as significant. This offset is determined by the dc level that each stage contributes as well as the quality of level shifter. Changing the resistor values at the emitter of Darlington pair can adjust the offset slightly. Attempts was made to redesign the level shifter by changing the resistor values as well as the configuration. The configurations that were attempted were firstly a pnp voltage divider (for leveling up) and secondly active load pnp (for level up). Both were placed instead of the second transistor in the Darlington pair. Both configurations failed as the current supplied by the current source was also going into the base of the output stage transistor. Furthermore, using pnp active load or voltage divider would mean that the 100ohm emitter resistor could not be there and this meant that the first transistor of Darlington pair should be biased somehow else. The second downside to this solution was that the output resistance of gain stage would drop. Looking back at it, a possible solution could be to have the current source change bias direction and simply use a voltage divider.

The input impedance is not enough due to the high dc currents. From the start of design it was assumed that the input impedance would be roughly

similar to an op-amp of 15V. This was a terrible assumption and lead to series of other bad assumptions. Darlington pair should have been used at the inputs. Such pairs can be easily added without much alteration to the rest of the stage.

Output resistance of a class AB power amplifier provided 49 ohms.

The power loss is 3 times more due to usage of the current sources. I would like to point out that current sources would have been replaced with current mirrors if transistor limit was not exceeded in simulation. Lastly, and the source of major concern, is the behavior of op-amp at lower frequencies. The gain variation with frequencies is essential specially when using summing point amplifier with signals from various frequencies. Nevertheless, the gain is sufficient to allow the op-amp to work as inverting amplifier at frequency of 50.

Overall, when the op-amp is used for it's closed loop gain, the results are very satisfactory as was demonstrated with the summing amplifier.

11. Application as Differentiator and Integrator

The op-amp was further used as integrator and differentiator. The circuits used, and the simulation results are shown below:

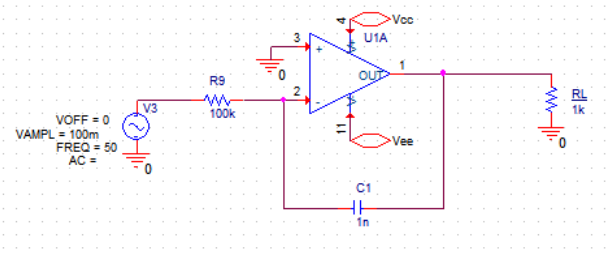


Figure 14: integrator circuit

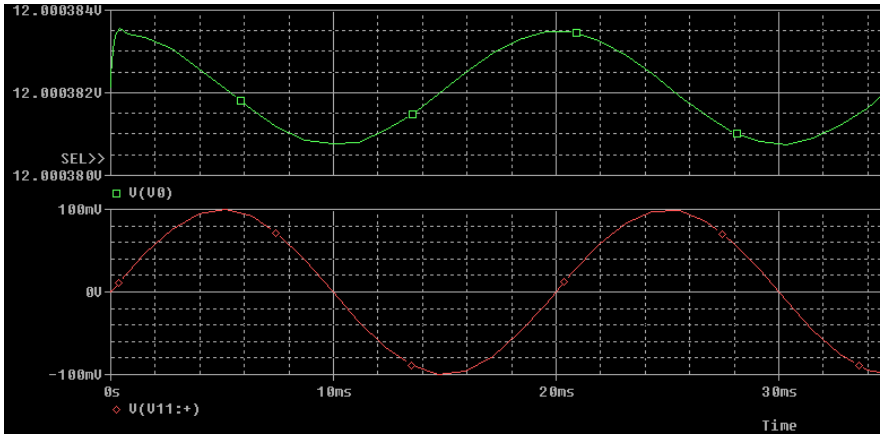


Figure 15: results of integration. V11 is the sine source.

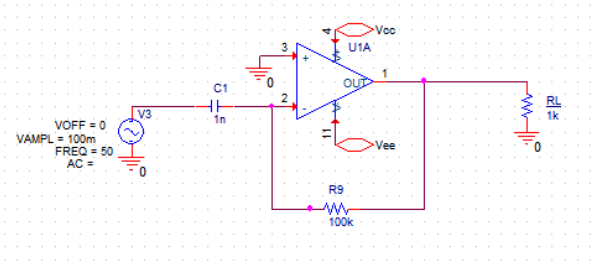


Figure 16: differentiator circuit

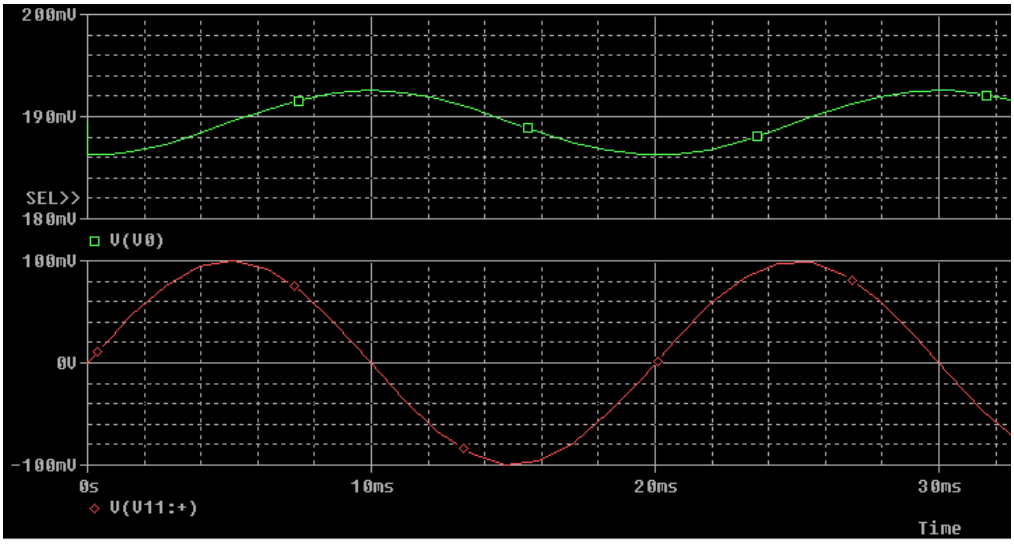


Figure 17: Result of differentiation. V11 is the sine source.

$$v_0 = -RC\frac{dv_i}{dt} v_0 = \frac{-1}{RC}\int_0^t v_i\,dt$$

Integration results aligns with theory as the double negative of integration of sine is positive cosine. Furthermore, the differentiation result aligns with theory as well since the negative of differentiation of sine is negative cosine.

12. Conclusion

Operational amplifiers have evolved from general functions, such as 741, to specific functions. Electronic engineers make use of the simple transistors to make task specific op-amps. The design proposed for bio signal does not achieve the engineering requirements. On the other hand, the op amp operates well when used for it’s closed loop gain.