DESIGN AND IMPLEMENTATION OF A CONSTANT-GM CIRCUIT USING CURRENT MIRROR IN 0.13 μM STANDARD CMOS TECHNOLOGY

KIE4019 ANALOG VLSI CIRCUIT DESIGN

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ABSTRACT

Reference current generator circuits must be designed so that they provide a constant current regardless of supply voltage variation. This document will provide the systematic approach in design of such circuit using theory and aid from Mentor Graphic. By the end of this document, a circuit design is proposed, and its supply voltage sensitivity is studied.

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LIST OF SYMBOLS AND ABBREVIATIONS

For examples:

MOSFET	:	Enhancement model metal oxide semiconductor field effective transistor
PMOS	:	p-channel MOSFET
NMOS	:	n-channel MOSFET
M4	:	Transistor labeled as 4

LIST OF APPENDICES

CHAPTER 1: INTRODUCTION

In an analog integrated circuit, many subcircuits work together to generate all the various dc voltages and currents. These include bias circuits, reference circuits, and regulators. A *bias* circuit generates the dc voltages required to keep transistors near some desired operating point; of course, as transistor parameters change, either due to process or with changes in temperature, so must the bias voltages. A *reference* circuit generates a voltage and/or current of a known fixed absolute value (for example, one micro amp). Finally, a *regulator* circuit improves the quality of a dc voltage or current, usually decreasing the noise. Figure 1-1 shows how these circuits may work together to support the analog circuits on a large mixed analog-digital chip.

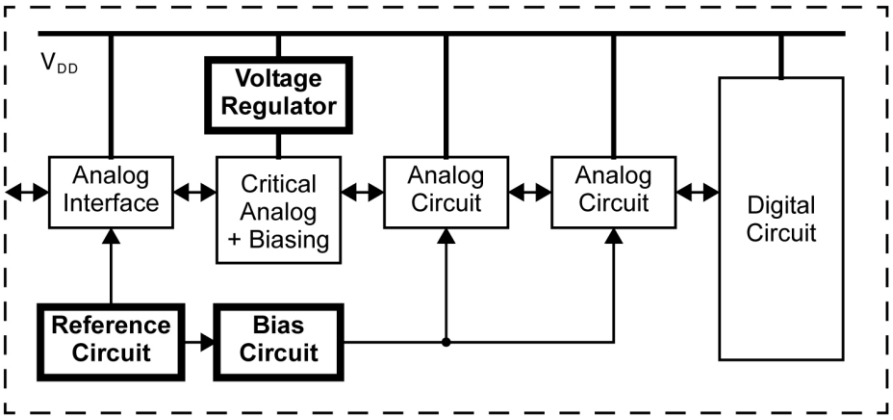

Figure 1-1: large mixed analog–digital integrated circuit emphasizing the role of biasing, references, and regulators

This chapter will focus on the technical backgrounds to design a reference current source where the current is independent of the supply voltage. In section 1.1 the general considerations in IC design are provided. After which the subcircuits of reference current generators, a current mirror and a current source, is studied in sections 1.2 and 1.3 respectively.

1.1 Reference Circuit Design Considerations in IC Design

The objective of reference generation is to establish a constant dc current that is independent of the supply, process, and temperature variations. Additionally, several other critical parameters are output impedance, output noise, and power dissipation. Some of these parameters will be addressed in the coming sections.

1.2 Current Mirror

The two-transistor current source, also called a current mirror, is the basic building block in the design of integrated circuit current sources. Figure 1-2 shows the basic current-source circuit, which consists of two NMOS transistors.

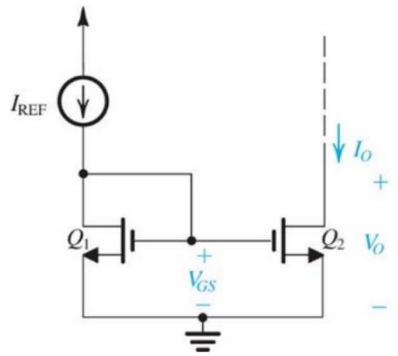

Figure 1-2: Basic 2-transistor NMOS current source

The drain and the source of the enhancement-mode transistor Q1 are connected, which means that Q1 is always biased in the saturation region (as long as I_{D1} is more than zero). Assuming $\lambda=0$ [1], we can write the reference current as equation (1).

$$I_{REF} = \frac{\beta_1}{2}(V_{GS} - V_{TN1})^2 \qquad (1)$$

[1] For sake of simplicity and ease of understanding the concept, assumptions are used in this chapter. Note that the practical relationship will not be exactly same as theory. Furthermore, note that theoretical relationship serves as guidelines for initial design and the practical relationship obtained via simulation will be used for finalized design.

Substituting for V_{GS} yields

$$V_{GS} = V_{TN1} + \left(\frac{2I_{REF}}{\beta_1}\right)^{0.5} \quad (2)$$

For the drain current of Q2 to be independent of the drain-to-source voltage (given that λ=0), transistor Q2 should always be biased in the saturation region. The load current is then obtained by substituting V_{GS} into the current equation of Q2:

$$I_O = \frac{\beta_2}{2}\left(V_{TN1} + \left(\frac{2I_{REF}}{\beta_1}\right)^{0.5} - V_{TN2}\right)^2 \quad (3)$$

If Q1 and Q2 are identical transistors, then $V_{TN1} \cong V_{TN2}$ and $\beta_1 \cong \beta_2$, and equation (3) becomes:

$$I_{REF} = I_{OUT} \quad (4)$$

Note that here we have assumed the drain current is independent of V_{DS} as there is no channel length modulation. In reality we cannot assume this. However, circuit designers make use of cascoding to match the V_{DS} of master to salve[2].

1.3 Widlar Current Source

Widlar current sources are used in supply-independent biasing circuits as their I_{OUT} is not dependent on I_{IN} for a particular current range (roughly speaking). To understand this behavior let us analyze the Widlar current source in Figure 1-3.

[2] Refer to Effect of Cascoding in Reducing CLM Effect in appendices for the full explanation.

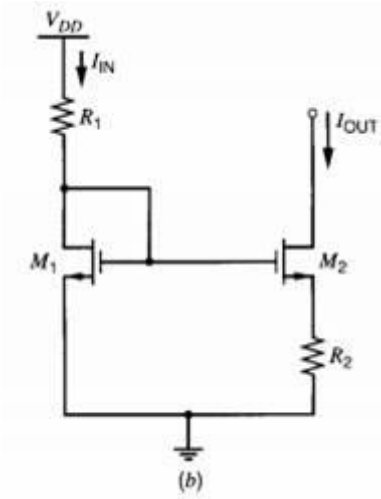

Figure 1-3: nMOS Widlar current source.

If $I_{IN} > 0$, *M1* operates in the active region because it is diode connected. Assume that *M2* also operates in the forward active region. KVL around the gate-source loop gives:

$$V_{GS1} - V_{GS2} - I_{OUT}R_2 = 0 \tag{5}$$

If we ignore the body effect, the threshold components of the gate-source voltages cancel and (5) simplifies to:

$$I_{OUT}R_2 + V_{ov2} - V_{ov1} = 0 \tag{6}$$

If the transistors operate in strong inversion and $V_A \to \infty$,

$$I_{OUT}R_2 + \left(\frac{2I_{OUT}}{k_n'\left(\frac{W}{L}\right)_2}\right)^{0.5} - V_{ov1} = 0 \tag{7}$$

The quadratic equation can be solved for $I_{OUT}^{0.5}$:

$$I_{OUT}^{0.5} = \frac{-\left(\frac{2}{k_n'\left(\frac{W}{L}\right)_2}\right)^{0.5} \pm \left(\frac{2}{k_n'\left(\frac{W}{L}\right)_2} + 4R_2V_{ov1}\right)^{0.5}}{2R_2} \tag{8}$$

Where $V_{ov1} = \left(\frac{2I_{IN}}{k_n'\left(\frac{W}{L}\right)_1}\right)^{0.5}$. Furthermore, we have $I_{OUT}^{0.5}$ as:

$$I_{OUT}^{0.5} = \left(\frac{k_n'}{2}\left(\frac{W}{L}\right)_2\right)^{0.5}(V_{GS2} - Vt) \tag{9}$$

Equation (9) applies only when *M2* operates in the active region, which means that $V_{GS2} > V_t$. As a result, $I_{OUT}^{0.5} > 0$ and the potential solution where the second term in the numerator of Equation (8) is subtracted from the first, cannot occur in practice. Therefore,

$$I_{OUT}^{0.5} = \frac{-\left(\frac{2}{k'\left(\frac{W}{L}\right)_2}\right)^{0.5} + \left(\frac{2}{k'\left(\frac{W}{L}\right)_2} + 4R_2V_{ov1}\right)^{0.5}}{2R_2} \tag{10}$$

Equation (10) shows that a closed-form solution for the output current can be written for a Widlar current source that uses MOS transistors operating in strong inversion. The graph in Figure 1-4 shows that as the I_{IN} increases, it's effect on I_{OUT} is reduced.

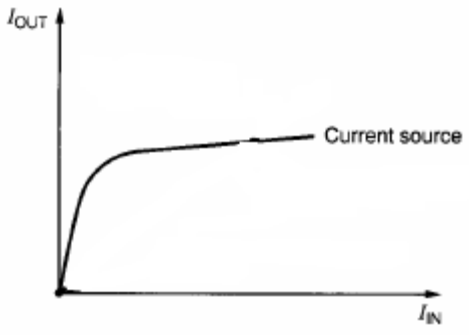

Figure 1-4: Relationship between input and output current of Widlar current source

This current source should be made to operate in strong inversion (where r_o is infinite) and bulk effect is zero for the relationships above to become valid.

The relationship is very similar if we use the PMOS Widlar current source as given in Figure 1-5.

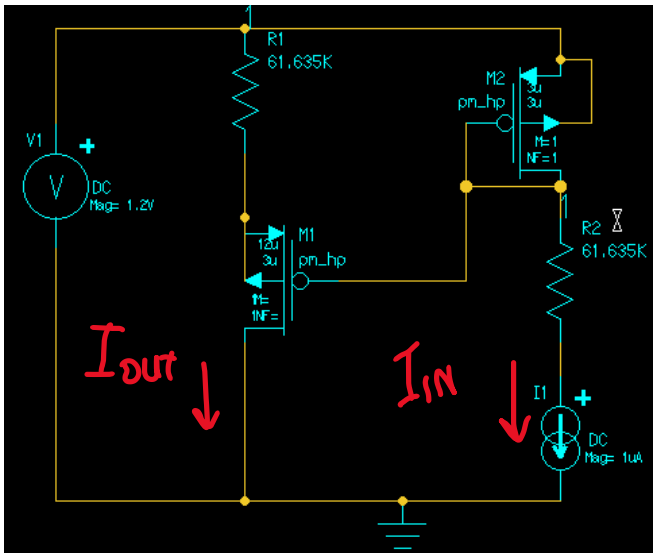

Figure 1-5: PMOS Widlar current source.

The current relationship for PMOS Widlar current source is given as:

$$I_{OUT}^{0.5} = \frac{-\left(\frac{2}{k_p'\left(\frac{W}{L}\right)_1}\right)^{0.5} + \left(\frac{2}{k_p'\left(\frac{W}{L}\right)_1} + 4R_1V_{ov2}\right)^{0.5}}{2R_1} \quad (11)$$

Where $V_{ov2} = \left(\frac{2I_{IN}}{k_p'\left(\frac{W}{L}\right)_2}\right)^{0.5}$.

Do note that the point of interest for our design of current reference generation circuit is where I_{out} and I_{in} are equal. Section 1.5.1 will showcase the derivation for this scenario where we obtain for the W/L and R values.

1.4 Supply-Independent Reference Current

In the Analog VLSI Design (KIE4019) so far made use of "golden" reference current to bias current sources and current mirrors. This I_{REF} is assumed to provide a constant current regardless of V_{DD} (supply voltage). To design for I_{REF} we can make use of self-

biasing (or bootstrap bias) circuits where I_{REF} must be driven from I_{OUT}. These types of circuits are made up of two blocks: (1) current source and (2) current mirror as shown in Figure 1-6 (a).

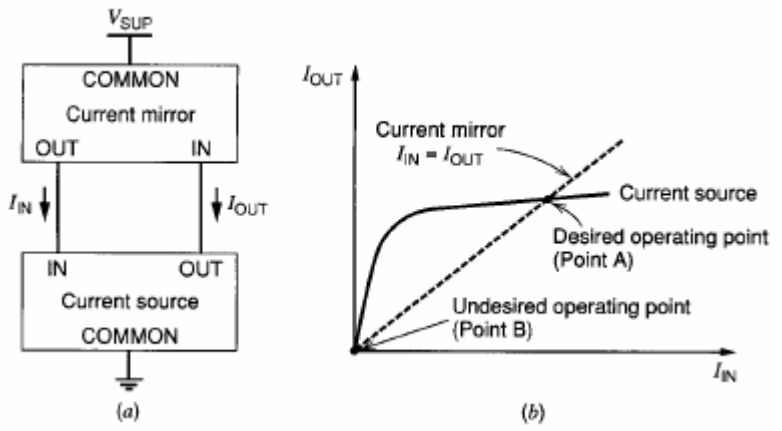

Figure 1-6: (a) Block diagram of a self-biased reference, (b) Determination of operating point.

The block connection in Figure 1-6 (a) has a current feedback loop and with the aid of the loop, the currents are not dependent on the power supply and only dependent on each other. To understand the loop let us consider the two key variables I_{IN} and I_{OUT}. The relationship between these variables is governed by both the current source and the current mirror and their respective current gains. From the standpoint of the current mirror, I_{IN} is set equal to I_{OUT}, assuming that the gain of the current mirror is unity (seen in Figure 1-6 (b) as a straight line). From the standpoint of the current source, the output current is almost independent of the input current for a wide range of input currents (seen in Figure 1-6 (b) as a line that reaches a plateau). The operating point of the circuit must satisfy both constraints and hence is at the intersection of the two characteristics.[3] The

[3] We have two methods to analyze circuits. Both involve the development of relationship between 2 parameters for the subcircuits involved and then the evaluation of operating point based on the points of intersection. One example of graphical analysis is the load line analysis where the parameters are I_D and V_{DS}. The second method is mathematical analysis where operating point is evaluated by simultaneous equations.

circuit for this assignment is made up of a PMOS Widlar current source and a simple 2 NMOS current mirror, both of which were studied in section 1.3 and 1.2 respectively.

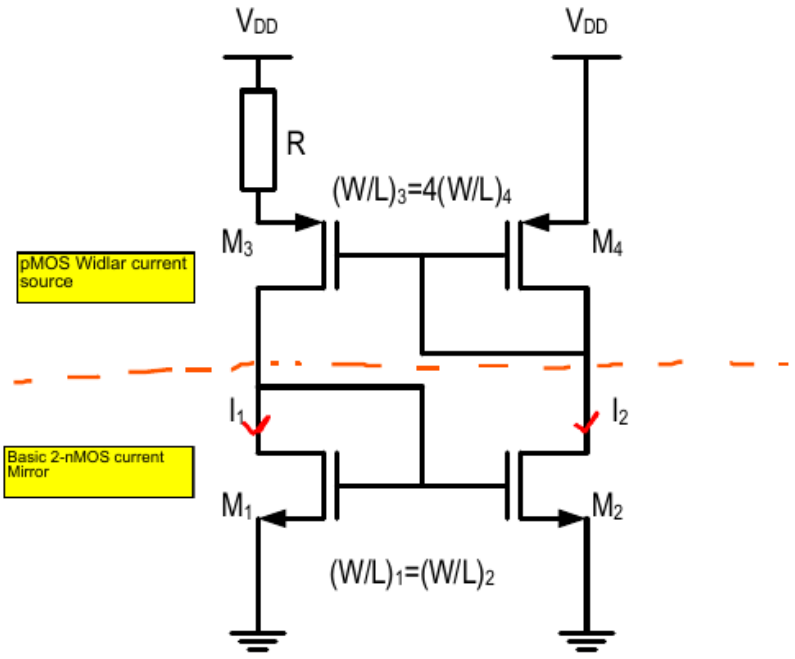

Figure 1-7: Supply independent current reference using PMOS Widlar current source and basic NMOS current mirror.

In the plot of Figure 1-6(b), two intersections or potential operating points are shown. Point **A** is the desired operating point, and point B is an undesired operating point because $I_{OUT} = I_{IN} = 0$.

If the output current in Figure 1-6(a), increases for any reason, the current mirror increases the input current by the same amount because the gain of the current mirror is assumed to be unity. As a result, the current source increases the output current by an amount that depends on the gain of the current source. Therefore, the loop responds to an initial change in the output current by further changing the output current in a direction that reinforces the initial change. In other words, the connection of a current source and a current mirror forms a positive feedback loop, and the gain around the loop is the gain of the current source. At point ***A,*** the gain around the loop is quite small because the output current of the current source is insensitive to changes in the input current around point ***A.*** On the other hand, at point ***B***, the gain around the feedback loop is deliberately

made greater than unity so that the two characteristics intersect at a point away from the origin. As a result, this simplified analysis shows that point ***B*** is an unstable operating point in principle, and the circuit would ideally tend to drive itself out of this state.

In practice, however, point ***B*** is frequently a stable operating point because the currents in the transistors at this point are very small, often in the picoampere range. At such low current levels, leakage currents and other effects reduce the current gain of MOS transistors, usually causing the gain around the loop to be less than unity. As a result, actual circuits of this type are usually unable to drive themselves out of the zero-current state. Thus, unless precautions are taken, the circuit may operate in the zero-current condition. For these reasons, self-biased circuits often have a stable state in which zero current flows in the circuit even when the power-supply voltage is non-zero. Start-up circuit is usually required to prevent the self-biased circuit from remaining in the zero-current state. Due to nature of simulators, the startup circuit is not required (see explanation in 4.3 of appendices). Furthermore, startup circuits are studied in 4.2 of appendices.

1.5 Deriving for Transconductance Gain and Supply Sensitivity

As per requirement for assignment, expression for transconductance gain in terms of R and sensitivity of the circuit to supply voltage will be driven in sections 1.5.1 and 1.5.2 respectively.

1.5.1 Transconductance Gain of M4 in terms of R

This section will analyze for the specific case where the I_{out} and I_{in} of Widlar current source are equal. This scenario results in simple relation between g_{m4} and R for the circuit in Figure 1-7.

For sake of calculation let us assume λ=0 and that all the MOSFETs are in saturation. Hence due to matched current mirror of M1 and M2, I_1 is equal to I_2. Hence, we can equate the drain current of M4 and M3 as below:

$$\frac{\beta_3}{2}(V_{SG3} - |V_{THp}|^2) = \frac{\beta_4}{2}(V_{SG4} - |V_{THp}|^2) \quad (12)$$

Furthermore, using KVL at the gate source voltages of top loop we obtain:

$$V_{SG3} = V_{SG4} - I_{out}R \quad (13)$$

Substituting (12) into (13) and simplifying the equation we obtain:

$$I_{out}R = (V_{SG4} - |V_{THp}|)\,(1 - \sqrt{\frac{\beta_4}{\beta_3}}\,) \quad (14)$$

Knowing $(V_{SG4} - |V_{THp}|) = \sqrt{\frac{2I_{out}}{\beta_4}}$ and $g_{m4} = \sqrt{2\beta_4 I_{out}}$ we can express (14) as:

$$R = \frac{2}{g_{m4}}(1 - \sqrt{\frac{\beta_4}{\beta_3}}) \quad (15)$$

From equation (15) we can see that I_{out} and hence the transconductance gain, g_{m4}, is independent of the supply voltage at this operating point. Furthermore, if we use the width to length ratio as given in Figure 1-7 we obtain for g_{m4} as:

$$g_{m4} = \frac{1}{R} \; or \; \sqrt{2\beta_4 I_{out}} = \frac{1}{R} \quad (16)$$

1.5.2 Supply Sensitivity

One measure of bias-circuit performance is the fractional change in the bias current that results from a given fractional change in supply voltage. The most useful parameter for describing the variation of the output current with the power-supply voltage is the sensitivity S. The sensitivity of the output current to small variations in the power-supply voltage gives:

$$S_x^y = \frac{V_{SUPP}}{I_{OUT}} \frac{\delta I_{OUT}}{\delta I_{SUP}}$$

To obtain for the supply sensitivity of Figure 1-7 we first draw the small signal equivalent circuit as Figure 1-8.

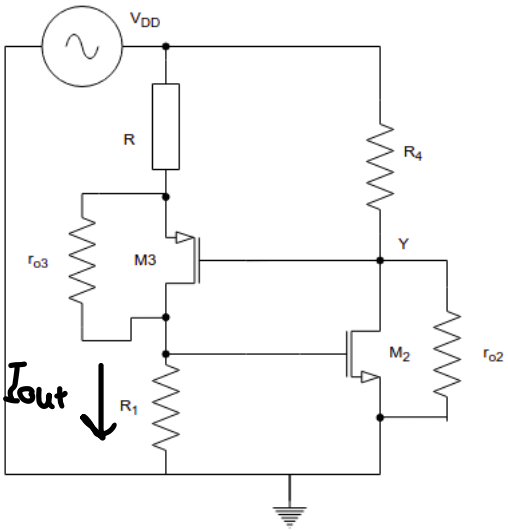

Figure 1-8: Small signal equivalent used to obtain for supply sensitivity.

Obtaining for KCL at node Y:

$$\frac{V_y}{r_{02}} + g_{m2} I_{out} R_1 = \frac{V_{DD} - V_y}{R_4} \tag{17}$$

Where R_1 and R_4 are given as:

$$R_{1|4} = \frac{1}{g_{m1|4}} || r_{o1||o4} \tag{18}$$

Differentiating equation 17 with respect to I_{out} will give:

$$\frac{\delta V_y}{\delta I_{out}} * \frac{1}{r_{02}} + g_{m2} R_1 = \frac{1}{R_4} \left(\frac{\delta V_{DD}}{\delta I_{out}} - \frac{\delta V_y}{\delta I_{out}} \right) \tag{19}$$

Given that $\frac{\delta V_y}{\delta I_{out}} = G_{m3}$, we obtain for $\frac{\delta V_{DD}}{\delta I_{out}}$ as:

$$\frac{\delta I_{out}}{\delta V_{DD}} = \frac{1}{R_4}\left(\frac{1}{G_{m3}\,(r_{02}||R_4)} + g_{m2}R_1\right)^{-1} \tag{20}$$

Where G_{m3} is the gain of common source M3 with degeneration due R_1 given as:

$$G_{m3} = \frac{g_{m3}r_{o3}}{R_1 + (1 + (g_{m3} + g_{mb3})R_1)r_{03}} \tag{21}$$

As we can observe in (20), the sensitivity is much lower than one, and so we can consider this circuit as supply independent current source.

We will use the theoretical understanding gained thus far to design for our reference current generator. However, before that we must evaluate the practical (simulated) behavior of the subcircuits as we have used assumptions in relationship derivation. This will be carried out in sections 2.2 and 2.4.

CHAPTER 2: DESIGNING CURRENT REFERENCE CIRCUIT

This chapter discusses the steps to design the supply independent current reference circuit by Mentor graphics with 0.13um Siltera technology. Section 2.1 will showcase the simulation involved to evaluate the (approximate) process parameters of Siltera 0.13um technology. After which the practical relationship between the input and output currents of current mirror is studied to obtain for a suitable initial L in sections 2.2. Section 2.3 will also involve studying practical current relationship of Widlar current source, from which W/L_4 and R values are selected.

2.1 Process Parameter for Silteta 0.13um

To design for the biasing circuit, we must first evaluate the approximate process parameters so we can use it in our calculation. The schematic in Figure 2-1 was used to evaluate for NMOS and PMOS process parameters.

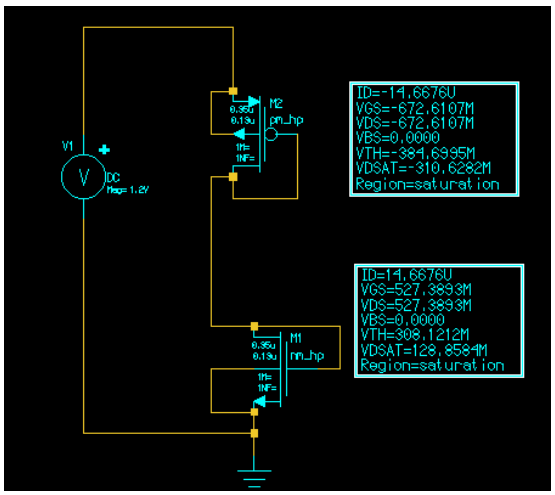

Figure 2-1: Schematic used to evaluate the process parameters (k'_p and k'_n).

Process parameter for NMOS and PMOS can be approximated as:

$$\mu_n C_{ox} = \frac{2I_{Dn}\left(\frac{L}{W}\right)_n}{(V_{GS1} - V_{THn})^2} \tag{22}$$

$$\mu_p C_{ox} = \frac{2I_{Dp}\left(\frac{L}{W}\right)_p}{\left(V_{GS2} - V_{THp}\right)^2} \tag{23}$$

The OP simulation gave the results as in Figure 2-1. Using these results, we obtain for process parameters as below:

$$\mu_n C_{ox} = \frac{2(14.667u)\left(\frac{0.13u}{0.35u}\right)}{(527.39m - 308.12m)^2} = 2.266 * 10^{-4} \tag{24}$$

$$\mu_p C_{ox} = \frac{2(14.667u)\left(\frac{0.13u}{0.35u}\right)}{(672.61m - 384.69m)^2} = 1.314 * 10^{-4} \tag{25}$$

Note that the values obtained are only estimates (since we ignored the CLM and other effects). This process parameter will be used for the initial design of our reference current generator. After initial design we are expected to tune the circuit to compensate for the error in process parameter value.

2.2 Current Mirror Simulation: Obtaining L for Sufficiently High r_o

As was highlighted in the derivation of transconductance gain of the circuit, the modulation effect must be negligible for the equation to work. Hence by selecting a suitable L value we must obtain for significant inversion. Furthermore, as we are using the current mirror with current gain of unity, we must ensure that current gain of this subcircuit will be about unity.

To evaluate the right L value the circuit in Figure 2-2 was used and effect of different L (=L_p=L_n) values was studied. Our intention here is to select an L that would give I_{out} equal to 1uA through the voltage range of 0.2 to 1.2V. This range is an estimation of V_{DS} voltage range across the current mirror NMOSFETs in Figure 1-7.

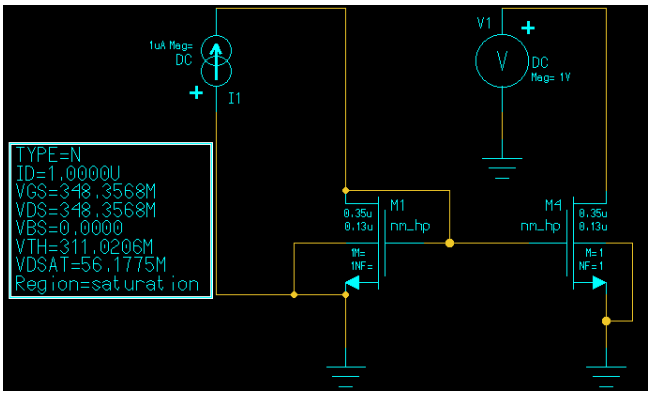

Figure 2-2: schematic of current mirror to produce I_{in}=I_{out}=1uA. W is retained as 0.35u as this is (near) minimum value.

To evaluate the appropriate L, I_{out} against V_{DS} is obtained by sweeping V1 from 0V to 1.6V for different L values. Graph in Figure 2-3 provides this relationship for the whole current range while Figure 2-4 shows the variation around 1uA (the nominal current).

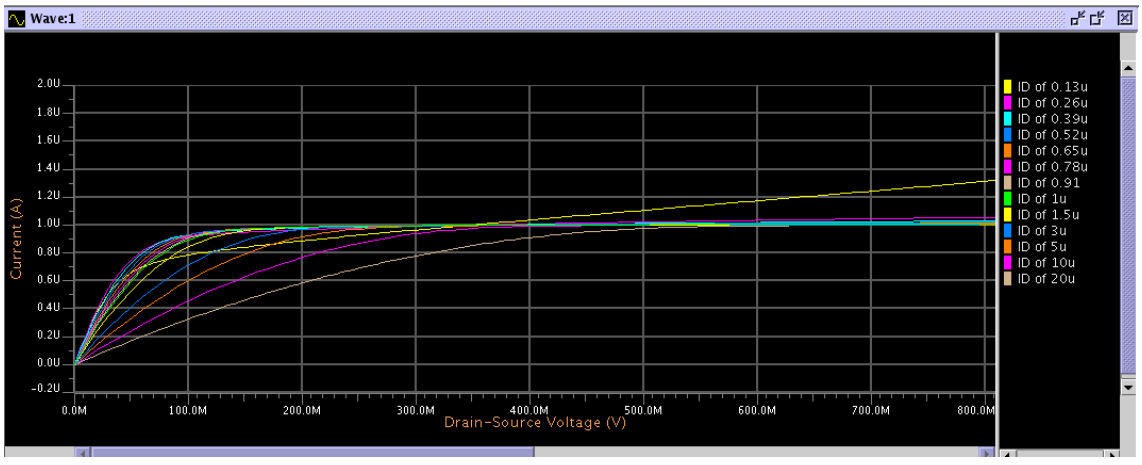

Figure 2-3: Output Characteristic of current mirror slave NMOS

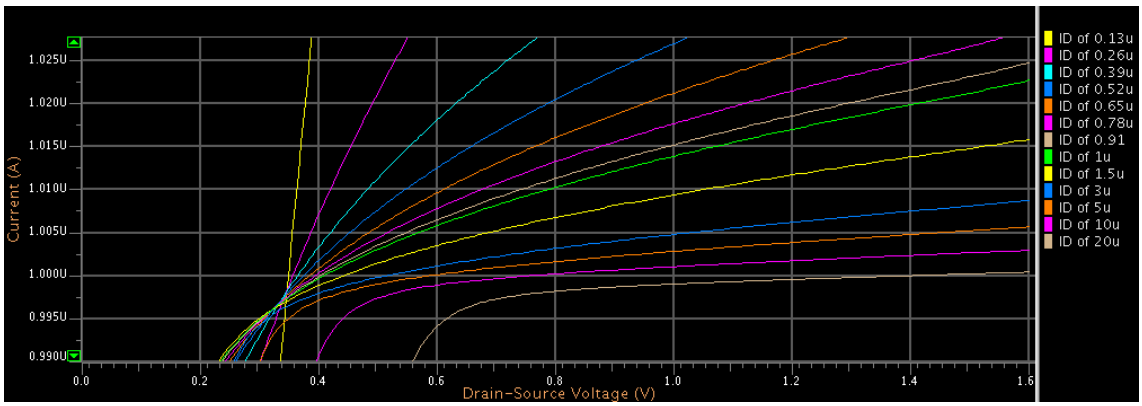

Figure 2-4: Output IV Characteristic of M4 (zoomed at 1uA)

The effect of L on the current gain of the current mirror was also studied and the results are provided in Figure 2-5. The gain graph was also zoomed to give Figure 2-6.

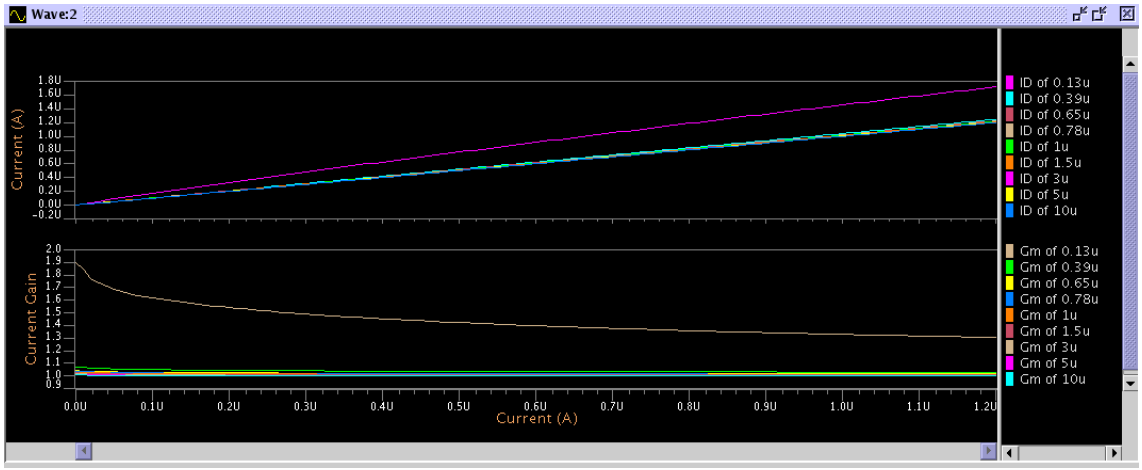

Figure 2-5: Top graph shows the relation between current of M1 and M4 for different lengths and the bottom graph shows the current gain against M1 current for different L values.

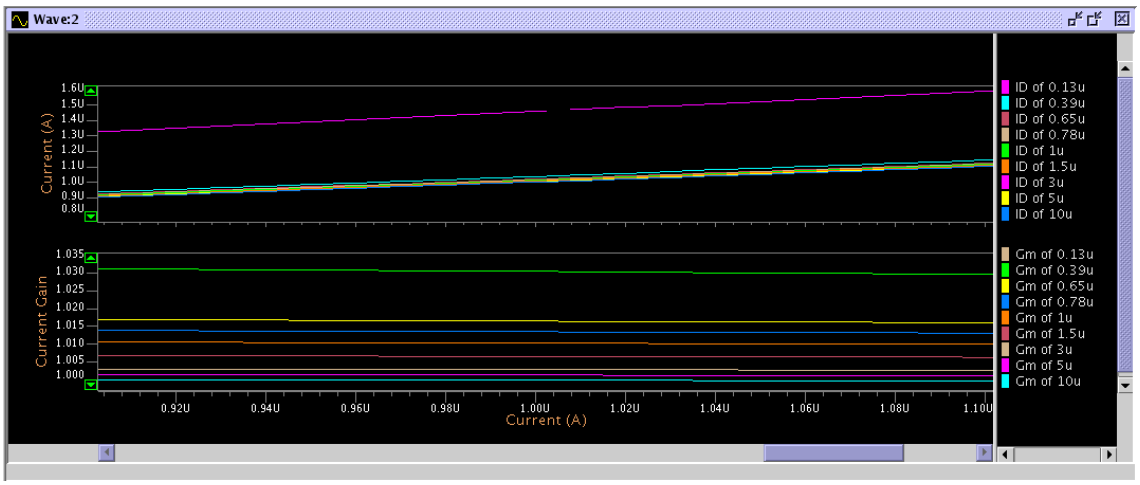

Figure 2-6: same graph as above but here we zoomed near 1uA region. We can see that L=3u is very close to G_m=1.

The right selection of L involves selecting length that is not too high (as more space would be required and hence chip cost would be higher) and not too low (where the r_o is too small and so V_{DS} affects the current significantly).

3u seems to be the best L value. Higher values than this requires higher voltage values to reach 1uA while lower L values have higher error from the nominal value (1uA) with lower r_0 values.

This selected L value will serve as the guide for design of the reference current generator circuit. Furthermore, this L value will be used for the L of Widlar current source.

2.3 Determining R and Width to Length ratio

Using the process parameter obtained as well as the L selected (3u), we design for the circuit to give 1uA at 1.2V.

Using equation (16) we obtain the graph of R against $\left(\frac{W}{L}\right)_4$ where the relationship is given as equation (26):

$$(1.6211 * 10^{-5})\sqrt{\left(\frac{W}{L}\right)_4} = \frac{1}{R} \tag{26}$$

The graph obtained is given in Figure 2-7:

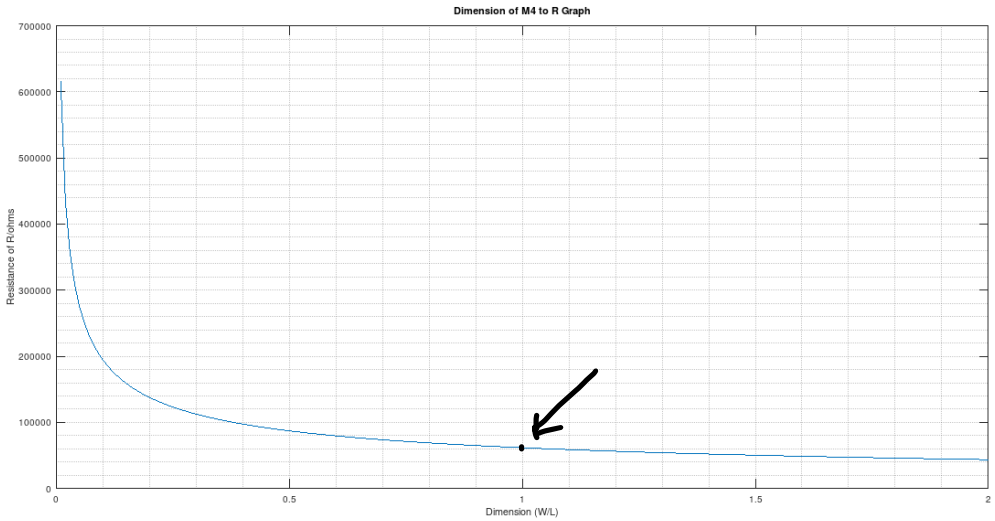

Figure 2-7: Relationship between R and W/L of M4.

Note that we expect the resistance to be provided by an external precision resistor as this seems to be the practice in research papers. Using the graph, we must select for an R that is available as external precision resistance (furthermore resistance can't be too high as this would mean higher power consumption) and length to width ratio that is not too high (higher values would mean higher device size). Furthermore, we must consider that the process parameter may vary with temperature and process and so we must select a resistance and dimension pair that has smaller slope. With such considerations we select nominal value for R as 61.635$k\Omega$ and for $(\frac{W}{L})_4$ as 1. This pair has small slope and the resistance value as well as the dimension ratio is more readily available.

It is important to note that the relationship driven is only an estimate (with assumption that the process parameter used is valid and that there is no CLM and bulk effect) and so simulation must be carried out to evaluate the adjusted/tuned R and $(\frac{W}{L})_4$ value.

2.4 Widlar Current Source Simulation

In the previous section we have used theory to evaluate the R and $(\frac{W}{L})_4$ values with assumptions that our process parameter is accurate and that there is no CLM and bulk effects. In this section we will verify and tune these values using simulation. The circuit in Figure 2-8 is used to first study the effect of CLM and process parameter errors on the Widlar current source.

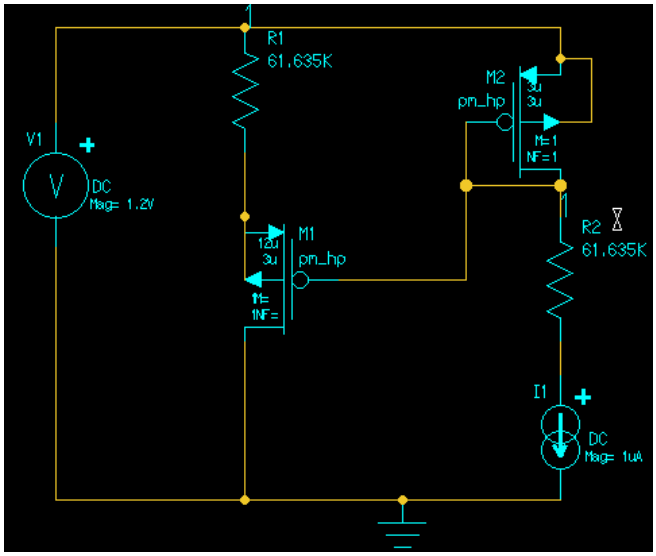

Figure 2-8: Widlar current source without bulk effect.

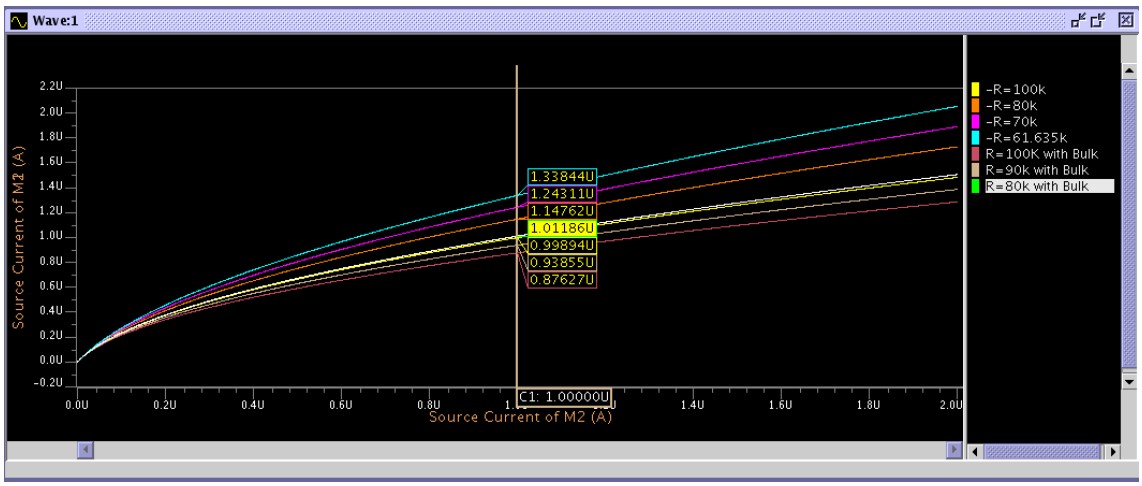

Figure 2-9: Current relations for different resistance values. Note that the ones with "Bulk" entails that the circuit is one that the bulk is connected to V_{DD} instead of source.

A current sweep using I_1 source was carried out to evaluate the accuracy of theoretical gain with simulation. Figure 2-9 shows that using the theoretical R (even without bulk effect) there is a large difference with nominal current (1uA) when I_1 is supplying 1uA. This is mainly because small inaccuracy of process parameter ($\Delta\mu_p C_{ox} \cong 10 * 10^{-5}$) would have major effect on the R value obtained ($\Delta R = 15k\Omega$). We could have reduced this error if we simply used a dimension that is a lot higher than 1 which would mean smaller slope in graph of Figure 2-7. Instead of doing that we instead tune the R value so that we can reduce the current. The optimum R value when there is no bulk effect is $100k\Omega$ as shown in Figure 2-9. However, with bulk effect the results become different (since the assumption where overdrive voltages are equal for obtaining equation 14 is no longer valid). With bulk effect we evaluate that best R value is $80k\Omega$.

We must note that for fabrication there will be variation in mobility of carriers and to avoid this it would have been optimum design if larger dimension value (W/L) was selected for M4.

2.5 First Draft of Design

Now that we have the required parameters for design, we can simulate the circuit. Figure 2-10 shows the circuit simulated.

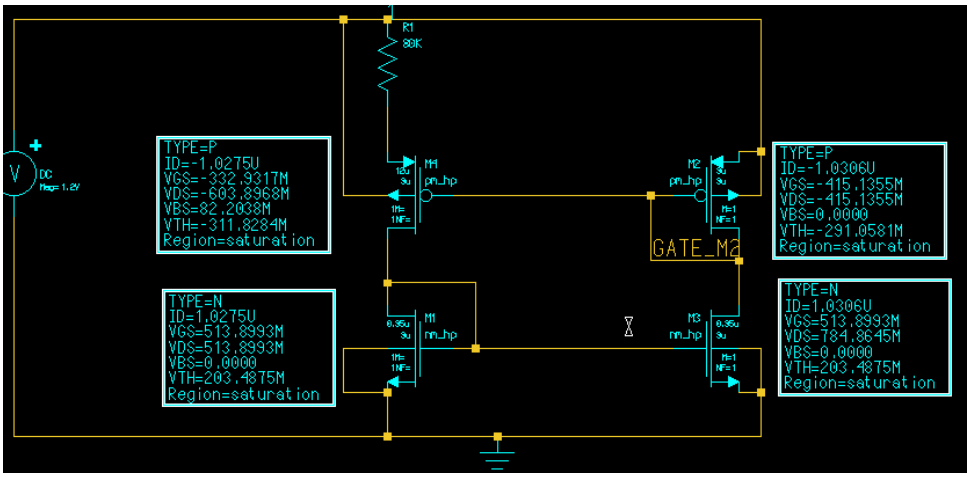

Figure 2-10: Constant g_m circuit.

As was expected the current in circuit is very close to nominal current ($1uA \cong 1.0275uA$).

2.6 Assessing the design

The circuit designed thus far has operated well at 1.2V. Here we will study the effect of change in V_{DD} on the current developed. Figure 2-11 shows the DC voltage sweep from 0.8V to 1.5V.

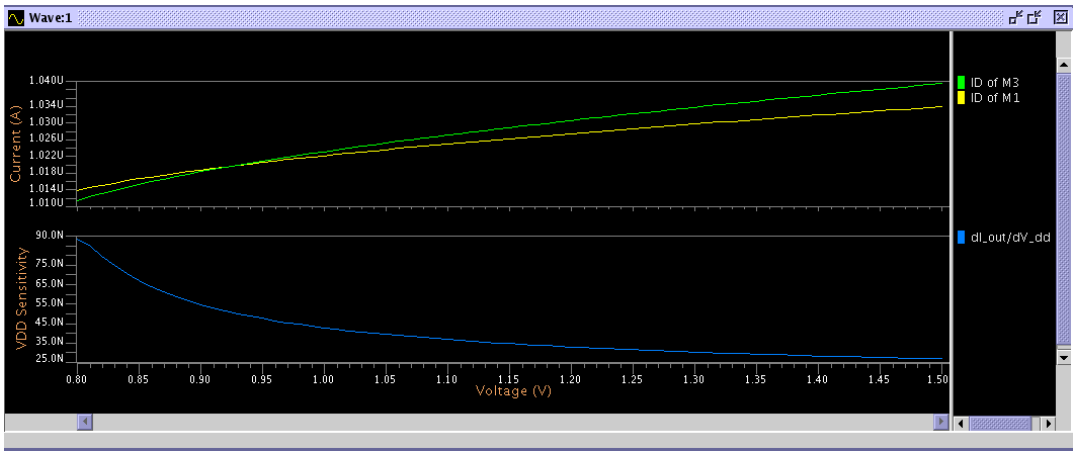

Figure 2-11: Upper graph shows the variation of current against the supply voltage and lower graph shows the derivative of the top graph (supply voltage sensitivity of M1 current).

The DC analysis was used as opposed to AC or transient as the operating point is established by V_{DD}, and for AC and transient this will remain constant (refer to section 4.3 of appendices). Furthermore, AC and transient analysis are useful for noise analysis from V_{DD}.

As it can be observed in Figure 2-11, the output current (through M1) sensitivity towards voltage is at nano meter level (at 1.2V we have 0.035u) and so we can conclude that the current reference generator is indeed supply independent.

2.7 Optimizing the Design

The design should be further optimized for minimizing error due to temperature and process variation. This assignment however will not cover this topic.

CHAPTER 3: CONLCUSION

Supply independent current reference generators are simple circuits made up of current mirror and a current source. This report has showed the systematic approach to design such circuit using theory as well as simulation. The designed reference current circuit provides 1uA current with 0.035u sensitivity to supply at V_{DD} of 1.2V.

CHAPTER 4: APPENDIX

4.1 Effect of Cascoding in Reducing CLM Effect

One of the reasons for cascoding is the reduction of V_{DS} difference between master's and slave's. This in turn will ensure that the current mirror operates as intended when ignoring CLM effect.

To understand this benefit let us first consider the effect of ΔV_{DS} on ΔI_D. Figure 4-1 shows the circuits without (a) and with cascoding (b).

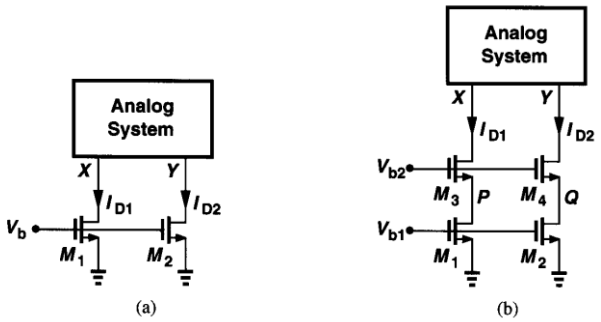

Figure 4-1 Current mirrors without cascoding (a) and with cascoding (b). Given M1 and M2 are same size.

M_1 and M_2 are used as constant current sources in a system. However due to internal circuitry of system V_x is higher than V_y by ΔV. This difference will result in difference in I_{D1} and I_{D2} if $\lambda \neq 0$ due to channel length modulation (CLM) effect. We analyze the circuit in Figure 4-1 (a) we obtain for ΔI_D as:

$$\Delta I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_b - V_{th})^2(\lambda \Delta V) \tag{27}$$

On the other hand, for circuit in Figure 4-1 (b) we obtain for ΔI_D as:

$$\Delta V_{PQ} = \Delta V \frac{r_{o1}}{(1 + (g_{m3} + g_{mb3})r_{o3})r_{o1} + r_{o3}} \tag{28}$$

$$\Delta I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_b - V_{th})^2\left(\frac{\lambda \Delta V}{(1+(g_{m3}+g_{mb3})r_{o3})}\right)^4 \qquad (29)$$

As we can see from comparing equations [27] and [29], we can conclude that addition of cascoding reduces the channel length modulation effect. The circuit in Figure 4-2 is an example use of cascoding in design of supply independent current reference circuit.

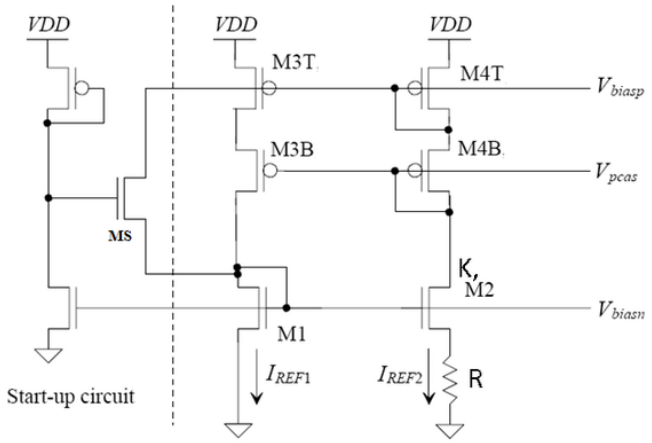

Figure 4-2: self-biased circuit with cascoding transistors (M3B and M4B). Note that there is a start-up circuit used to allow self-bias to exit the zero current operation point.

[4] r_{o3} in equation [36] has been ignored to give equation [37] as it is a lot smaller than the other denominator component.

4.2 Startup Circuits for the Self-biased MOS

In general, the following two things are expected from a startup circuit:

- Must push the circuit from undesired operating point to desired operating point.
- Must not interfere with the circuit once it reaches the desired operating point.

Usually, all the self-bias circuits like current and voltage reference generators require a startup circuit. Let's take a β Multiplier based current biasing circuit as shown in Figure 4-3.

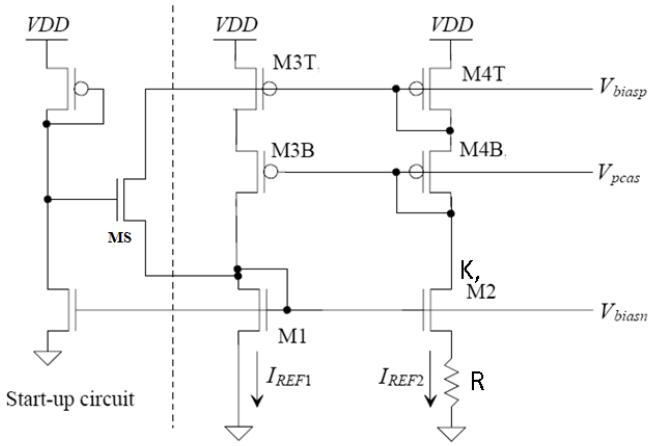

Figure 4-3: β Multiplier based current biasing circuit using MOSFETs

The above circuit has two stable operating points, first one when I_{REF1}, I_{REF2} = 0, other when I_{REF1} and I_{REF2} are at a desired positive current.

During '0' current situation, V_{biasp} is at V_{DD}, V_{biasn} is at GND causing the device MS to be in saturation. MS allows a small amount of current through it, pushing the whole circuit from its stable '0' current point to the desired stability point. In the positive current stable point V_{biasp} changes to V_{DD} - (V_{tp} + V_{Dsat}) and V_{biasn} changes to V_{tn} + V_{Dsat}. The device MS should be biased in such a way that its V_{GS} is positive during '0' current situation and negative during the positive current situation. This -VGS makes the device MS to be in cuttoff during the positive current operation.

Depending on the circuit, startup can be implemented by checking the number of stable operating points and which operating point is desired.

Alternative startup circuits are shown in Figure 4-4 and Figure 4-5.

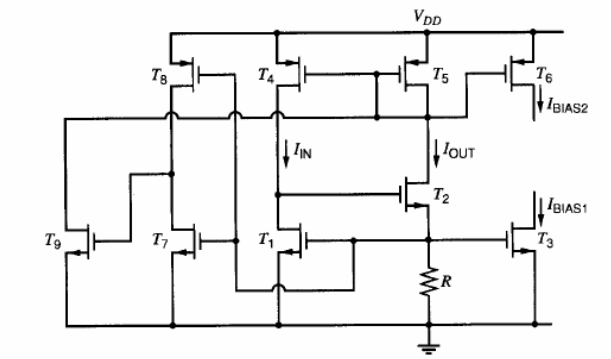

Figure 4-4: T8, T7 and T9 form the startup circuit. T8 and T7 are an inverter where they are sized so that they will provide a 1 to gate of T9 only at low voltages of T1 gate. At this point T9 will make V_{SG6} and V_{SG4} to be active.

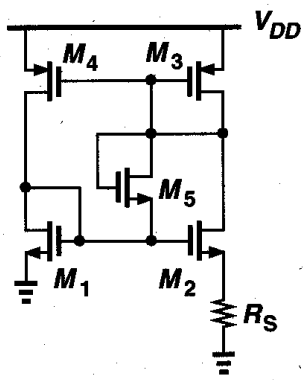

Figure 4-5: simple startup circuit made up of M5 only. This diode is to short gate of M3 and M4 at zero current conditions.

4.3 Simulators and Startup Conditions

As was discussed, self-bias circuits have two operating points and so the question is which point is given by the simulator.

To understand this, we must first understand that all simulations start at time t=0. Whatever DC conditions are applied to the simulation at t=0 is considered to have been

present for all time t<0. Even though an AC Analysis has no time duration associated with it, the DC operating point is calculated at t=0.

If there are no .IC SPICE statements included in a simulation and the Startup and UIC modifiers are not used, then the initial DC conditions of a circuit are completely defined by the initial levels or DC offsets of any sources present in the circuit and these are treated as having been present at those levels for all time prior to t=0. So, for example, the voltages across all capacitors and the currents through all inductors in the circuit will have reached their DC steady state values prior to the simulation starting at t=0.

For our reference current circuit, the operating point (where $I_{in}=I_{out}$) is reached by the time the results are recorded. This means that the region of operation of the MOS transistors will be the case when the feedback loop has reached a steady state.