HOCHSCHULE
RHEIN-WAAL
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of Applied Sciences

LABORATORY

Microcontroller

3

EXPERIMENT:

Seven Segment Counter & I²C Bus: EEPROM

Write your name in every sourcefile you edit and compile the code with your matriculation number (variable in the template). All files should contain all names of the persons who made changes. Do use the @author tag for this (as available in the headline of template files).

1 Seven Segment Display

A seven-segment display is a cheap method to display numbers (0-9), using only 7 LEDs (or light bulbs). The segments are named A to G (with an eighth segment DP “decimal point” sometimes added). See Figure 1.

For displaying a zero, the segments must to be set to: **A=1, B=1, C=1, D=1, E=1, F=1, G=0**.

1.1 The "breadboard"

In this lab you will use a so called “breadboard” for plugging the circuits without soldering, see Figure 2.

A breadboard is often used for prototyping of small circuits. The bread board is broken up into positive (+) and negative (-) “power rails”, which span the height of the board. The positive rails are coloured in Red, while the negative rails are coloured in Blue. These rails are internal and vertically connected. In the middle of the bread board are multiple groups of holes organized in vertical columns and numbered in a sequence of 5s (for reference). Each group consists of 5 pin sockets wired together horizontally. These groups are not connected over the middle horizontal break of the board, nor do they connect vertically.

1.2 Kingbright Sx39-11

You would use a is a Kingbright Sx39 (i.e., SA39 or SC39) as a seven-segment display. Some snippets from the datasheet are shown in Figure 3 and Figure 4.

Please note: We have the SA39 and the SC39 in the lab. Check what device you get, these two devices are different!

Read the data sheet! We want to operate the LEDs at a maximum of 6 mA. Since you attended the analog electronics lab, you should know how to limit the current through an LED. Calculate with an LED forward voltage from 2V. The data sheet is appended to this document on page 9. The resistors in the boxes are good to limit the current for the used LED segments.

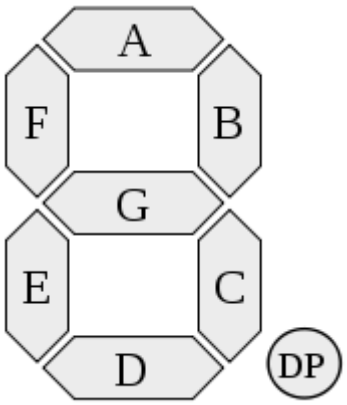


Figure 1: Seven Segment Indicator with decimal point.

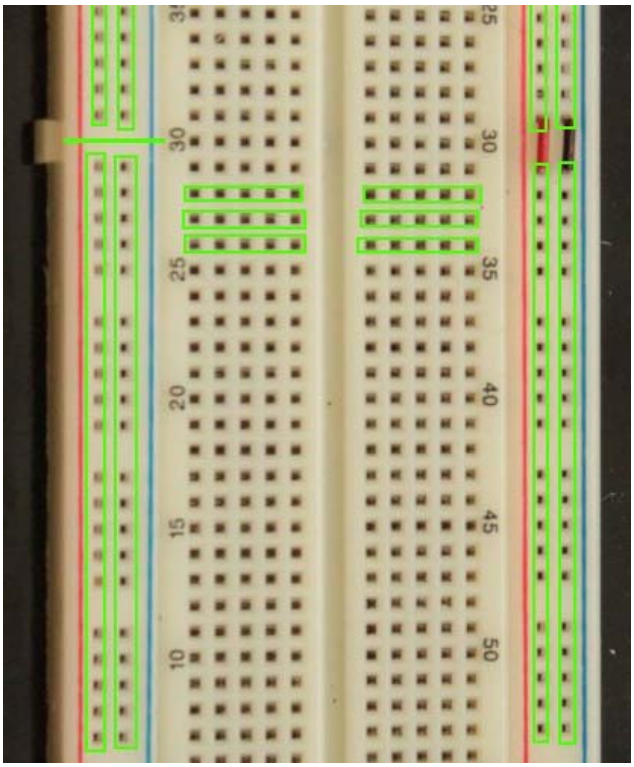


Figure 2: "Breadboard"

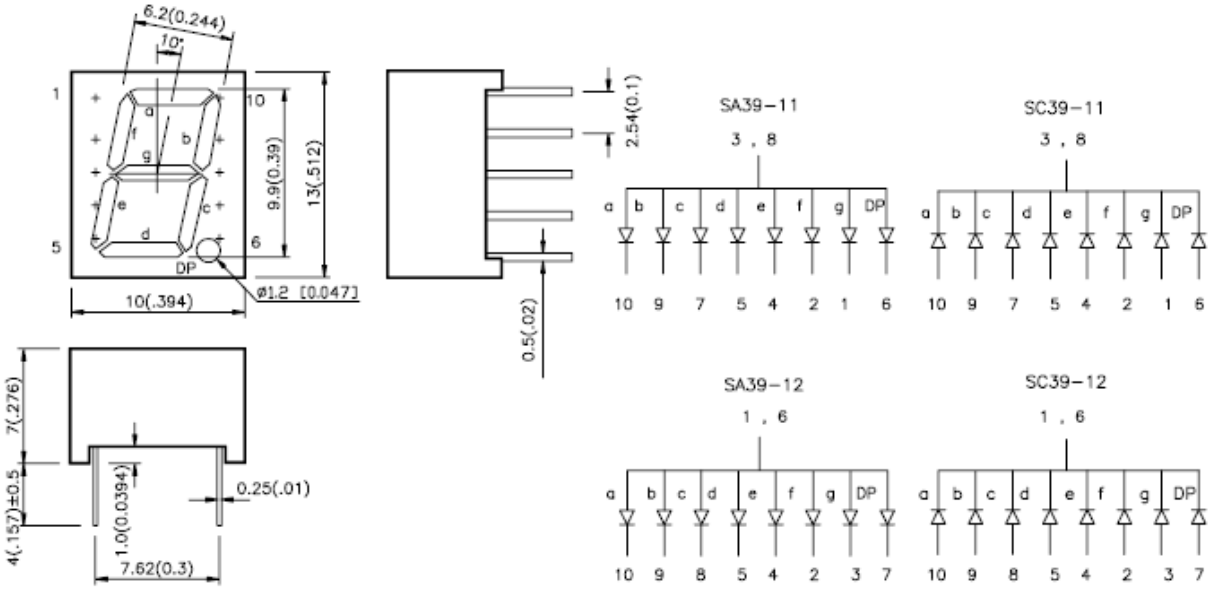


Figure 3: SC39-11 and SA39-11 seven segment indicators.

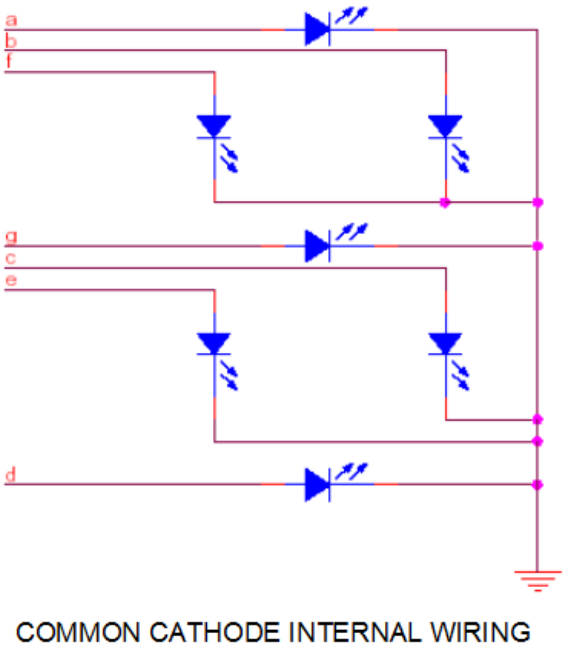


Figure 4: Internal circuitry of a SC39-11.

2 Seven Segment Counter

Task 1:
What we want at the end of this task is a working “counter”, see Figure 5.

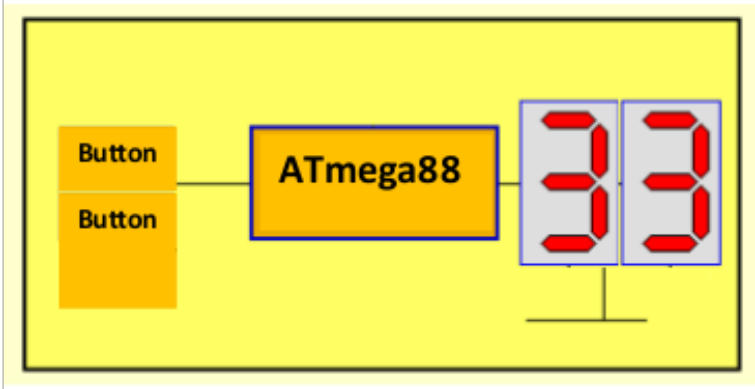


Figure 5: A counter with seven segment display.

First, there should be a button used as an input and a seven segment display (consisting of two seven-segment indicators) showing the decimal numbers from 0 to 99. This looks very simple, but you will get a few typical problems like:

- key contact bouncing,
- signal edge evaluation,

- bit manipulations,
- counting / limits.

The seven segment displays will be mounted on a breadboard. You can find a short explanation of a breadboard in 1.1. Please try to become familiar with this device. If the provided information is not sufficient, use additional material from the Internet.

If the counter with one button works fine, add a second button for counting up (first key) and down (second key). If both buttons are pressed, the counter should reset to zero.

There is a template, read this program first, understand and complete it.

You have to write/complete a function to set the outputs. Please use the following connections for the inputs:

- **Key 1 (up):** pin PC2,
- **Key 2 (down):** pin PC3.

and for the output (see Figure 6):

	MyAVR	Sx39-11 Pin
A	PD7	10
B	PD6	9
C	PD5	7
D	PB4	5
E	PB5	4
F	PC0	2
G	PC1	1
A	PD4	10
B	PD3	9
C	PD2	7
D	PB0	5
E	PB1	4
F	PB2	2
G	PB3	1
	Hi/Lo	3,8

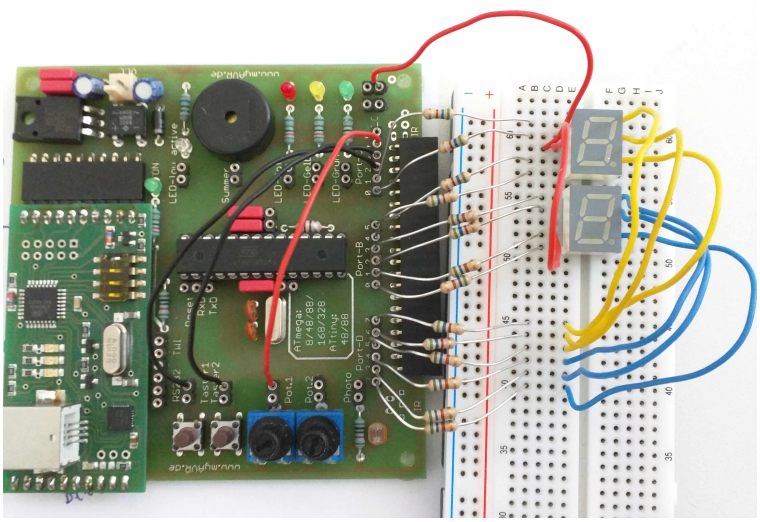


Figure 6: Dual sevensegment counter

Task 2 (Optional):
Use one ADC channel to create a simple voltmeter. Measure the voltage from a potentiometer. The output over the seven segment can only show two digits, so only display a rounded value ($0.1V$ steps). Do not forget to activate the DP on the first seven segment indicator. Please use the pin PC4 as the **analog input**.

3 The I²C Bus

The I²C Bus (Inter-Integrated Circuit) was developed in 1982 to realize the communication between integrated circuits. It uses serial data transfer.

A microcontroller has normally memory, inputs/outputs, timers, and so on. Sometimes it is necessary to add additional memory, more inputs/outputs, ... to a microcontroller. This is the typical application area for the I²C Bus:

- **A short distance:** No error check or error correction,
- **The devices are on the same board:** It uses only two wires to make the layout design simpler and more efficient,
- **"Active parts" like microcontroller and "passive" parts like memory and other peripheral devices:** Master/Slave structure.

A typical implementation is one master and multiple slave devices. Multiple master devices are also possible, however, this structure would not be used in this lab.

3.1 Electrical part

Only two signal wires are used for the I²C Bus:

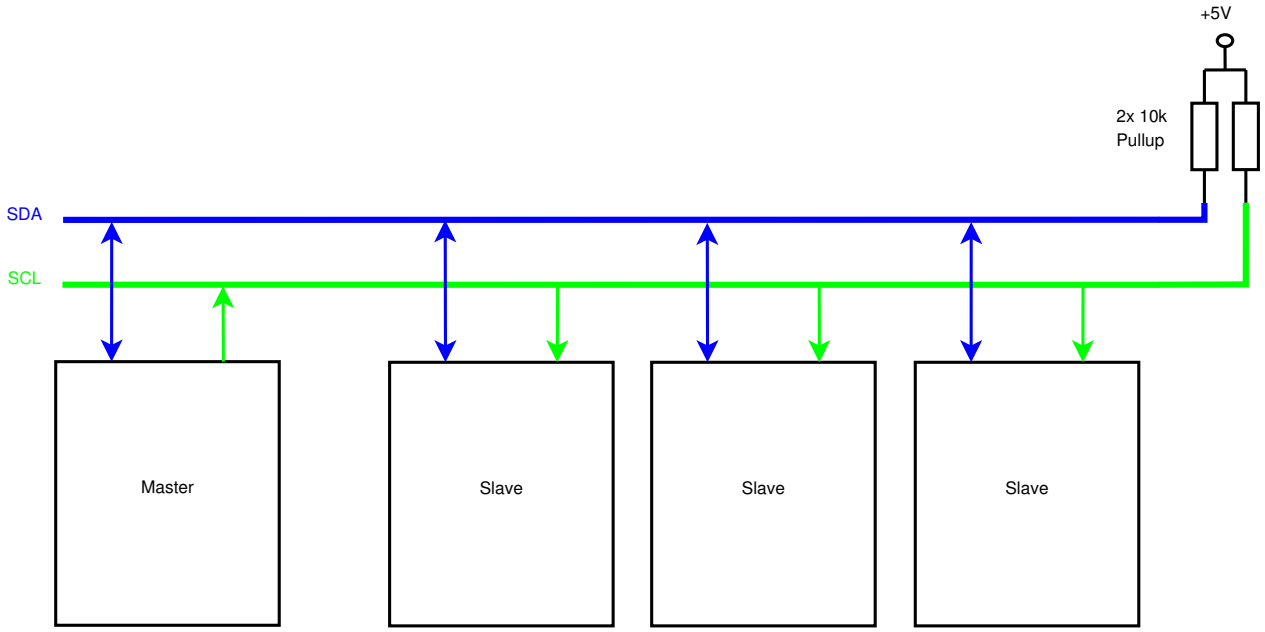


Figure 7: Typical I^{2}C Bus circuit.

- **SDA:** For the data,
- **SCL:** For the clock signal.

Because the I^{2}C Bus is designed for the communication inside one circuit and not for a data transfer to different machines, a global ground is a natural consequence for the I^{2}C Bus.

The master generates the clock signal and has the control over the whole bus. A slave only sends data when the master requests this. To see how the devices are connected, see Figure 7.

The I^{2}C Bus has the following typical speeds:

- **Standard Mode:** 100 kBit/s,
- **Fast Mode:** 400 kBit/s,
- **Fast Mode Plus:** 1 MBit/s.

The speed is controlled by the master device. This device generates the clock signal, that is global for the whole bus. So the devices do not need a precise clock generator for the serial communication.

In Figure 7, you can see that there are pullup resistors for both signals. The bus subscribers have open collector connections to the two bus signals, see Figure 8.

3.2 I^{2}C Bus on the Atmel ATmega88PA

In the lab we use a microcontroller from Atmel. Atmel devices use the name TWI (Two Wire Interface) for I^{2}C Bus. There is only a licence problem with the name I^{2}C Bus, the technical part is exactly the same. Some newer Atmel datasheets use the name 2-wire Serial Interface.

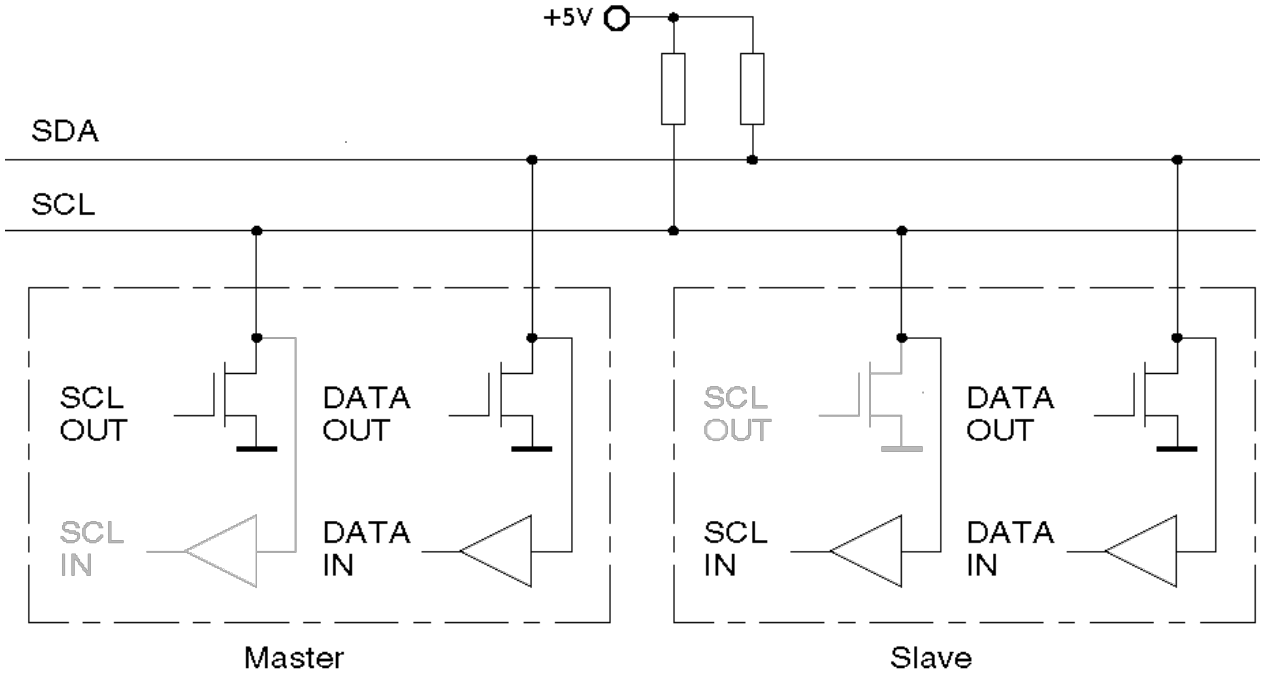


Figure 8: I^{2}C Bus driver structure.

To use the TWI, there is a prepared library in the template:

- i2c_master.c
- i2c_master.h

The .c file is incomplete and you have to complete it by using the datasheet (you have to find the relevant bits).

In the lab, we work with “memory like” devices. Every device has an internal position pointer. To write or read data, it is important to read from the right position inside the memory, from the right device.

When the I^{2}C Bus is opened, the first byte from the master is the device address. The device that has this address will be activated while all other devices, will ignore the following bus traffic. In this lab, the second step is to set the position of the pointer inside the memory device. From now on, it is possible to read or write data. The pointer increases automatically.

To read data with this library via I^{2}C Bus:

1. i2c_master_open_write(adr); //Device address, open to write
2. i2c_master_write(pos); //Set the position pointer of the device
3. i2c_master_open_read(adr); //Re-Open the same device to read
4. x = i2c_master_read_next(); //Read a byte
5. y = i2c_master_read_next(); //Read a byte

6. z = i2c_master_read_last(); //Read last byte
7. i2c_master_close(); //Close the device access

To write data with this library via I^{2}C Bus:

1. i2c_master_open_write(adr); //Device address, open to write
2. i2c_master_write(pos); //Set the position pointer of the device
3. i2c_master_write(x); //Write a byte
4. i2c_master_write(y); //Write a byte
5. i2c_master_close(); //Close the device access

4 EEPROM

EEPROM (Electrically Erasable Programmable Read-Only Memory) is a memory, that can save data without any power source. This is a good memory to save e.g. a system configuration. For example a hand calculator can store settings on an EEPROM. So, if you change the battery, it is not necessary to re-enter all settings again.

In the Lab we will use an ST 24C02. This integrated circuit can have different addresses depending of the state of three input pins. The hardware used in this lab has jumpers to select the values for these pins.

4.1 Task EEPROM

Connect the LCD display and the myTWI EEPROM board and complete the template. Use the wires to connect:

- Key1 to pin PB0,
- Key2 to pin PB1,
- Poti1 to pin PC0.

Read the template and understand the code before you edit it. The template has different .c files. Read all files, except the LCD files. Hint: You can use the search function of the editor and search for "TODO". You need to use datasheets of the microcontroller and the EEPROM for this lab.

Task 3:
Your program should do the following:

- Show current potentiometer value (0 to 1023) on the LCD,
- Enable the buttons to save and load the values to/from the EEPROM,
- Handle the potentiometer value as a 16 bit value.

To test your program, perform the following checks:

- Set any value with the potentiometer,
- Press key 1 (save),
- Press key 2 (load),
- Check that the value is now shown on the LCD on the second line,
- Disconnect the USB wire, wait a few seconds and reconnect the USB wire,
- Press key 2 (load) and check the value.

Task 4 (Optional):
Expand the program in a way that the values are stored in the EEPROM (512 bytes) of the microcontroller.

Task 5 (Optional):
Expand the program in a way that it is possible to store and load more than one value. Make this possible with only the two buttons and the one potentiometer.

5 Appendix

Datasheet: Kingbright® Sx39

Kingbright®

9.9mm (0.39INCH) SINGLE DIGIT NUMERIC DISPLAYS

SA39-11 SC39-11

SA39-12 SC39-12

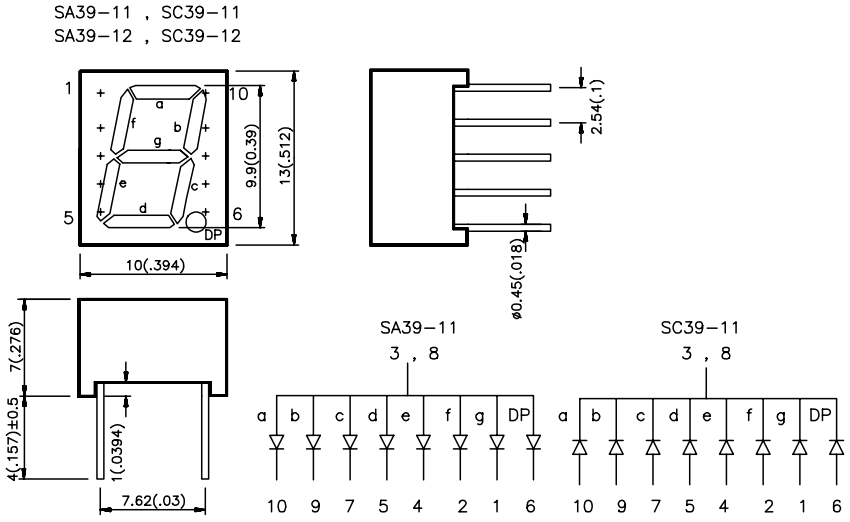
Features

- ●0.39 INCH DIGIT HEIGHT.
- ●LOW CURRENT OPERATION.
- ●EXCELLENT CHARACTER APPEARANCE.
- ●EASY MOUNTING ON P.C. BOARDS OR SOCKETS.
- ●I.C. COMPATIBLE.
- ●CATEGORIZED FOR LUMINOUS INTENSITY,
- ●YELLOW AND GREEN CATEGORIZED FOR COLOR.
- ●MECHANICALLY RUGGED.
- ●STANDARD : GRAY FACE, WHITE SEGMENT.

Description

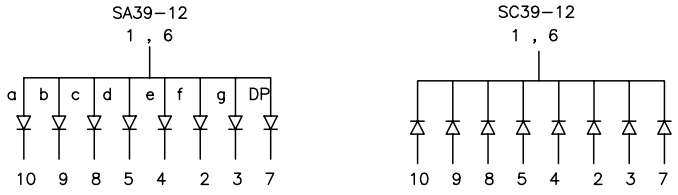
The Bright Red source color devices are made with Gallium Phosphide Red Light Emitting Diode.
The Green source color devices are made with Gallium Phosphide Green Light Emitting Diode.
The High Efficiency Red source color devices are made with Gallium Arsenide Phosphide on Gallium Phosphide Orange Light Emitting Diode.
The Yellow source color devices are made with Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diode.
The Super Bright Red source color devices are made with Gallium Aluminum Arsenide Red Light Emitting Diode.

Package Dimensions & Internal Circuit Diagram



Notes:
1. All dimensions are in millimeters (inches), Tolerance is ±0.25(0.01")unless otherwise noted.
2. Specifications are subjected to change whitout notice.

Internal Circuit Diagram



Selection Guide

Part No.	Dice	Iv (ucd) @ 10 mA		Description
		Min.	Max.	
SA39-11HWA SA39-12HWA	BRIGHT RED (GaP)	560	2200	Common Anode
SC39-11HWA SC39-12HWA				Common Cathode
SA39-11EWA SA39-12EWA	HIGH EFFICIENCY RED (GaAsP/GaP)	2200	9000	Common Anode
SC39-11EWA SC39-12EWA				Common Cathode
SA39-11GWA SA39-12GWA	GREEN (GaP)	1400	5600	Common Anode
SC39-11GWA SC39-12GWA				Common Cathode
SA39-11YWA SA39-12YWA	YELLOW (GaAsP/GaP)	1400	5600	Common Anode
SC39-11YWA SC39-12YWA				Common Cathode
SA39-11SRWA SA39-12SRWA	SUPER BRIGHT RED (GaAlAs)	9000	31000	Common Anode
SC39-11SRWA SC39-12SRWA				Common Cathode

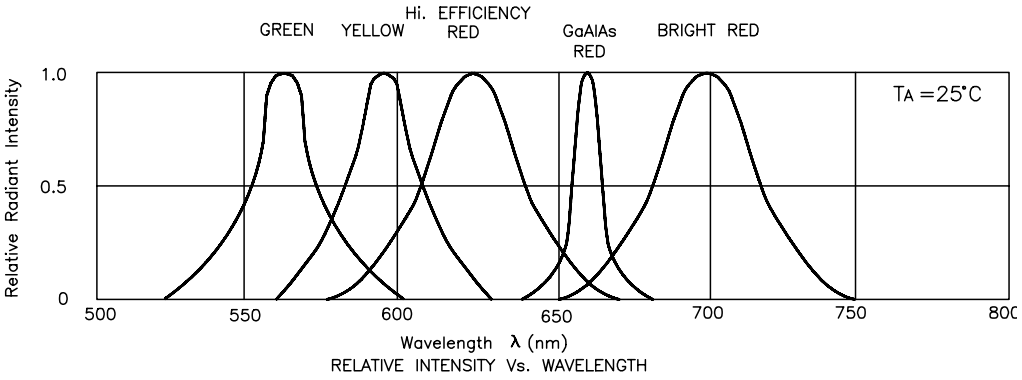
Electrical / Optical Characteristics at T_A=25°C

Symbol	Parameter	Device	Typ.	Max.	Units	Test Conditions
λ_{peak}	Peak Wavelength	Bright Red High Efficiency Red Green Yellow Super Bright Red	700 625 565 590 660		nm	IF=20mA
$\Delta\lambda_{1/2}$	Spectral Line Halfwidth	Bright Red High Efficiency Red Green Yellow Super Bright Red	45 45 30 35 20		nm	IF=20mA
C	Capacitance	Bright Red High Efficiency Red Green Yellow Super Bright Red	40 12 45 10 95		pF	VF=0V;f=1MHz
V_F	Forward Voltage	Bright Red High Efficiency Red Green Yellow Super Bright Red	2.0 2.0 2.2 2.1 1.85	2.5 2.5 2.5 2.5 2.5	V	IF=20mA
I_R	Reverse Current	All	10		uA	VR = 5V

Absolute Maximum Ratings at T_A=25°C

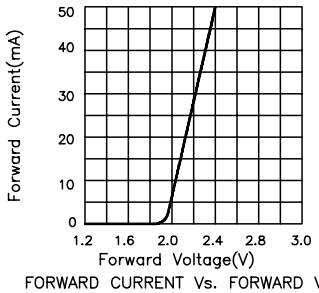
Parameter	Bright Red	High Efficiency Red	Green	Yellow	Super Bright Red	Units
Power dissipation	120	105	105	105	100	mW
DC Forward Current	25	30	25	30	30	mA
Peak Forward Current [1]	150	150	150	150	150	mA
Reverse Voltage	5	5	5	5	5	V
Operating/Storage Temperature	-40° C To +85 ° C					
Lead Soldering Temperature [2]	260° C For 5 Seconds					

Notes:
1.1/10 Duty Cycle, 0.1ms Pulse Width.
2. 4mm below package base.

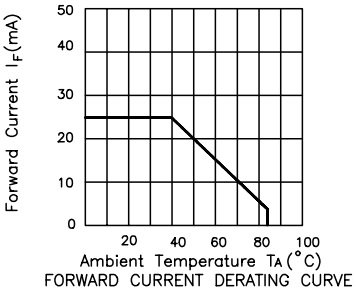


RELATIVE INTENSITY Vs. WAVELENGTH

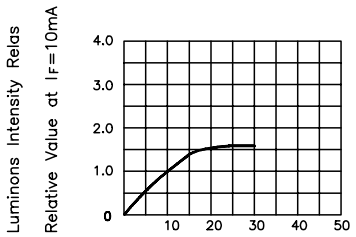
Bright Red



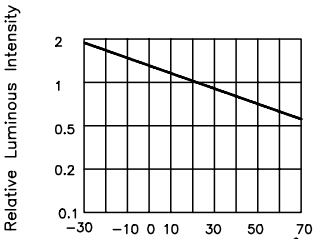
FORWARD CURRENT Vs. FORWARD VOLTAGE



FORWARD CURRENT DERATING CURVE

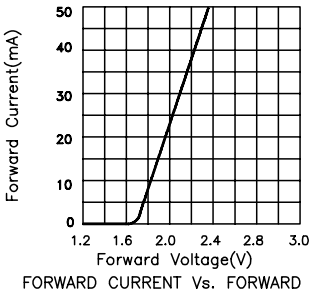


LUMINOUS INTENSITY Vs. FORWARD CURRENT

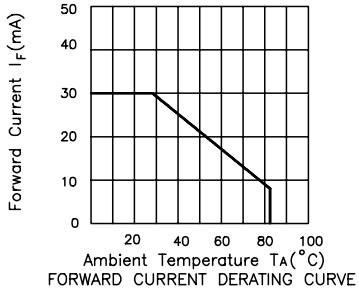


LUMINOUS INTENSITY Vs. AMBIENT TEMPERATURE

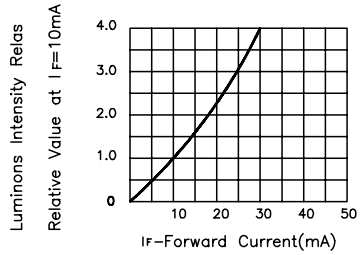
High Efficiency Red



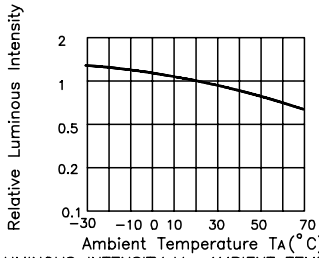
FORWARD CURRENT Vs. FORWARD VOLTAGE



FORWARD CURRENT DERATING CURVE

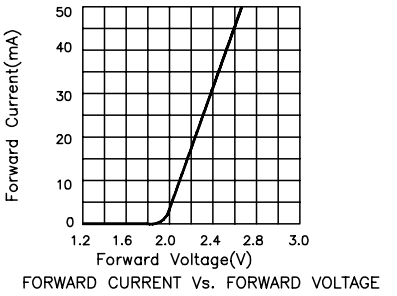


LUMINOUS INTENSITY Vs. FORWARD CURRENT

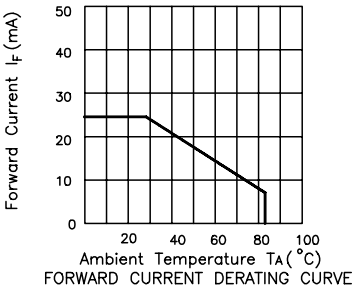


LUMINOUS INTENSITY Vs. AMBIENT TEMPERATURE

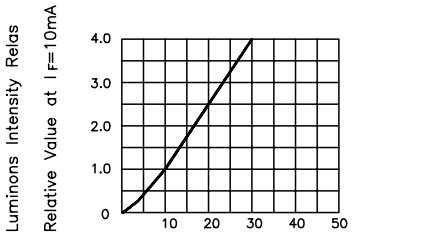
Green



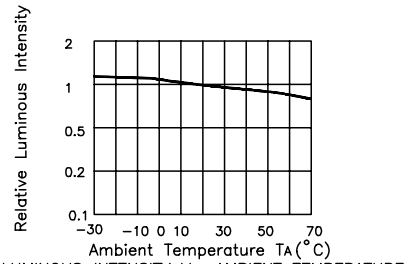
FORWARD CURRENT Vs. FORWARD VOLTAGE



FORWARD CURRENT DERATING CURVE

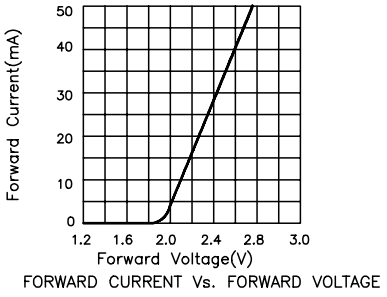


LUMINOUS INTENSITY Vs. FORWARD CURRENT

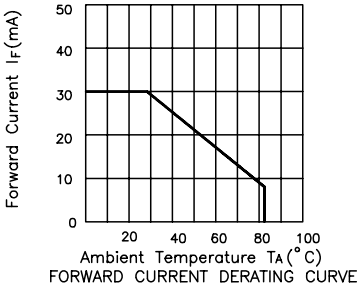


LUMINOUS INTENSITY Vs. AMBIENT TEMPERATURE

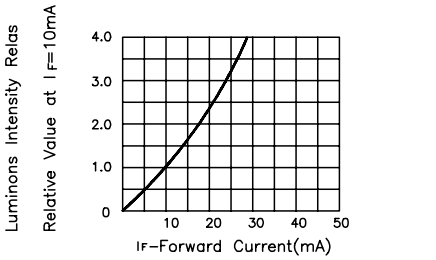
Yellow



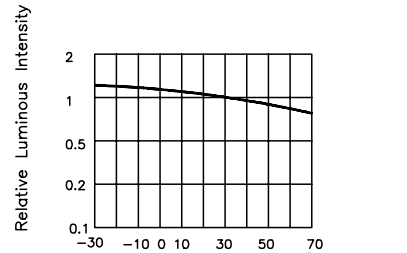
FORWARD CURRENT Vs. FORWARD VOLTAGE



FORWARD CURRENT DERATING CURVE

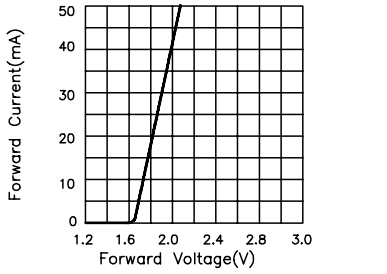


LUMINOUS INTENSITY Vs. FORWARD CURRENT



LUMINOUS INTENSITY Vs. AMBIENT TEMPERATURE

Super Bright Red



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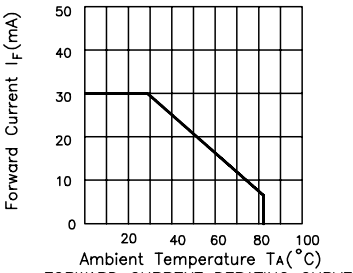
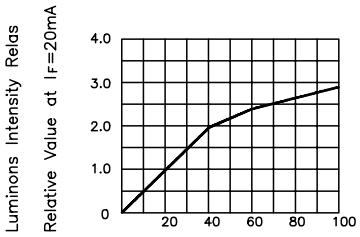
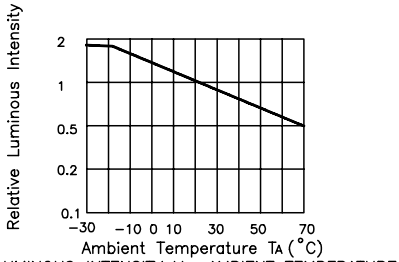


FORWARD CURRENT DERATING CURVE



LUMINOUS INTENSITY Vs. FORWARD CURRENT



LUMINOUS INTENSITY Vs. AMBIENT TEMPERATURE

Datasheet: ST24C02 EEPROM

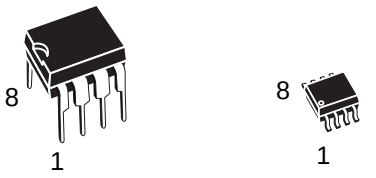
SGS-THOMSON MICROELECTRONICS

ST24/25C02, ST24C02R ST24/25W02

SERIAL 2K (256 x 8) EEPROM

NOT FOR NEW DESIGN

- 1 MILLION ERASE/WRITE CYCLES with 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE:
  - 3V to 5.5V for ST24x02 versions
  - 2.5V to 5.5V for ST25x02 versions
  - 1.8V to 5.5V for ST24C02R version only
- HARDWARE WRITE CONTROL VERSIONS: ST24W02 and ST25W02
- TWO WIRE SERIAL INTERFACE, FULLY I^2C BUS COMPATIBLE
- BYTE and MULTIBYTE WRITE (up to 4 BYTES)
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH-UP PERFORMANCES
- ***ST24C/W02 are replaced by the M24C02***
- ***ST25C/W02 are replaced by the M24C02-W***
- ***ST24C02R is replaced by the M24C02-R***



PSDIP8 (B)
0.25mm Frame

SO8 (M)
150mil Width

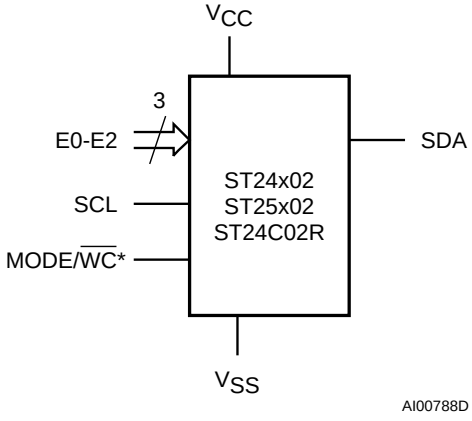
DESCRIPTION

This specification covers a range of 2K bits I^2C bus EEPROM products, the ST24/25C02, the ST24C02R and ST24/25W02. In the text, products are referred to as ST24/25x02, where "x" is: "C" for Standard version and "W" for hardware Write Control version.

Table 1. Signal Names

E0-E2	Chip Enable Inputs
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multibyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram



Note: $\overline{WC}$ signal is only available for ST24/25W02 products.

This is information on a product still in production but not recommended for new design

Figure 2A. DIP Pin Connections

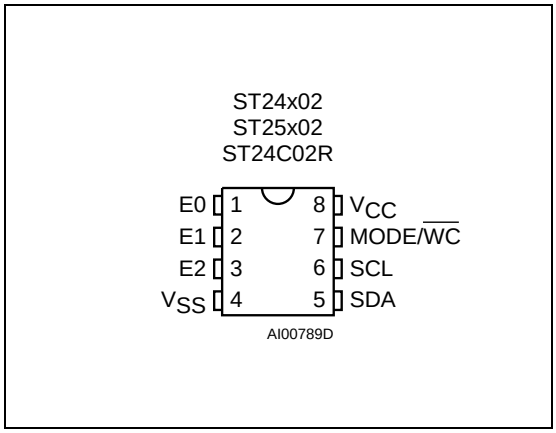


Figure 2B. SO Pin Connections

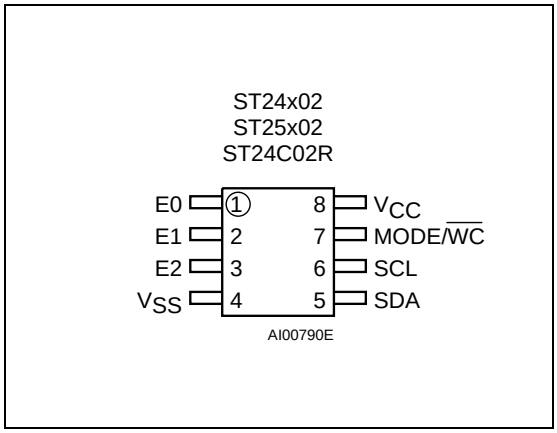


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		–40 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V_{IO}	Input or Output Voltages		–0.6 to 6.5	V
V_{CC}	Supply Voltage		–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)		4000	V
	Electrostatic Discharge Voltage (Machine model) (3)		500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500 Ω).
3. EIAJ IC-121 (Condition C) (200pF, 0 Ω).

DESCRIPTION (cont'd)

The ST24/25x02 are 2K bit electrically erasable programmable memories (EEPROM), organized as 256 x 8 bits. They are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The memories operate with a power supply value as low as 1.8V for the ST24C02R only.

Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

The memories are compatible with the I^2C standard, two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I^2C bus definition. This is used together with 3 chip enable inputs (E2, E1, E0) so that up to 8 x 2K devices may be attached to the I^2C bus and selected individually. The memories behave as a slave device in the I^2C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 bits (identification code 1010), plus one read/write bit and terminated by an acknowledge bit.

Table 3. Device Select Code

	Device Code				Chip Enable			RW
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	E2	E1	E0	RW

Note: The MSB b7 is sent first.

Table 4. Operating Modes (1)

Mode	RW bit	MODE	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, RW = '1'
Random Address Read	'0'	X	1	START, Device Select, RW = '0', Address,
	'1'			reSTART, Device Select, RW = '1'
Sequential Read	'1'	X	1 to 256	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, RW = '0'
Multibyte Write (2)	'0'	V_{IH}	4	START, Device Select, RW = '0'
Page Write	'0'	V_{IL}	8	START, Device Select, RW = '0'

Notes: 1. X = V_{IH} or V_{IL}
2. Multibyte Write not available in ST24/25W02 versions.

When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition.

Power On Reset: V_{CC} lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active, all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTIONS

Serial Clock (SCL). The SCL input pin is used to synchronize all data in and out of the memory. A resistor can be connected from the SCL line to V_{CC} to act as a pull up (see Figure 3).

Serial Data (SDA). The SDA pin is bi-directional and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A resistor must be connected from the SDA bus line to V_{CC} to act as pull up (see Figure 3).

Chip Enable (E2 - E0). These chip enable inputs are used to set the 3 least significant bits (b3, b2, b1) of the 7 bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Mode (MODE). The MODE input is available on pin 7 (see also WC feature) and may be driven dynamically. It must be at V_{IL} or V_{IH} for the Byte Write mode, V_{IH} for Multibyte Write mode or V_{IL} for Page Write mode. When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode).

Write Control (WC). An hardware Write Control feature (WC) is offered only for ST24W02 and ST25W02 versions on pin 7. This feature is usefull to protect the contents of the memory from any erroneous erase/write cycle. The Write Control signal is used to enable (WC = V_{IH}) or disable (WC = V_{IL}) the internal write protection. When unconnected, the WC input is internally read as V_{IL} and the memory area is not write protected.

SIGNAL DESCRIPTIONS (cont'd)

The devices with this Write Control feature no longer support the Multibyte Write mode of operation, however all other write modes are fully supported.

Refer to the AN404 Application Note for more detailed information about Write Control feature.

DEVICE OPERATION

I²C Bus Background

The ST24/25x02 support the I²C protocol. This protocol defines any device that sends data onto the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master will always initiate a data transfer and will provide the serial clock for synchronisation. The ST24/25x02 are always slave devices in all communications.

Start Condition. START is identified by a high to low transition of the SDA line while the clock SCL is stable in the high state. A START condition must precede any command for data transfer. Except during a programming cycle, the ST24/25x02 continuously monitor the SDA and SCL signals for a START condition and will not respond unless one is given.

Stop Condition. STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the ST24/25x02 and the bus master. A STOP condition at the end of a Read command, after and only after a No Acknowledge, forces the standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK). An acknowledge signal is used to indicate a successfull data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 bits of data.

Data Input. During data input the ST24/25x02 sample the SDA bus signal on the rising edge of the clock SCL. Note that for correct device operation the SDA signal must be stable during the clock low to high transition and the data must change ONLY when the SCL line is low.

Memory Addressing. To start communication between the bus master and the slave ST24/25x02, the master must initiate a START condition. Following this, the master sends onto the SDA bus line 8 bits (MSB first) corresponding to the device select code (7 bits) and a READ or WRITE bit.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I²C Bus

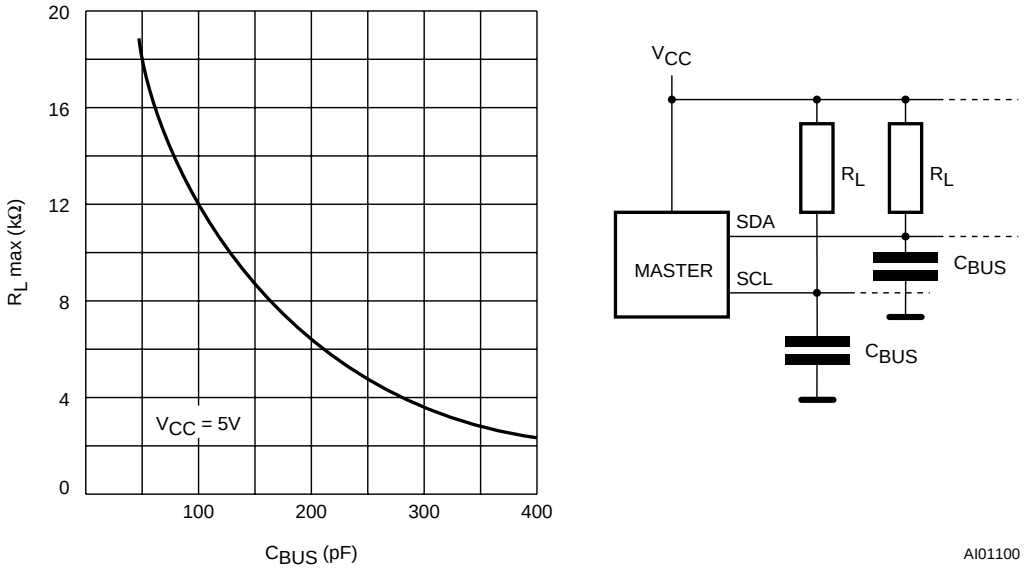


Table 5. Input Parameters (1) (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance (ST24/25W02)	$V_{IN} \le 0.3\ V_{CC}$	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance (ST24/25W02)	$V_{IN} \ge 0.7\ V_{CC}$	500		kΩ
t_{LP}	Low-pass filter input time constant (SDA and SCL)			100	ns

Note: 1. Sampled only, not 100% tested.

Table 6. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±2	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$ SDA in Hi-Z		±2	µA
I_{CC}	Supply Current (ST24 series)	V_{CC} = 5V, f_C = 100kHz (Rise/Fall time < 10ns)		2	mA
	Supply Current (ST25 series)	V_{CC} = 2.5V, f_C = 100kHz		1	mA
I_{CC1}	Supply Current (Standby) (ST24 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V		100	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5V, f_C = 100kHz		300	µA
I_{CC2}	Supply Current (Standby) (ST25 series)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V		5	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5V, f_C = 100kHz		50	µA
I_{CC3}	Supply Current (Standby) (ST24C02R)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 3.6V		20	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 3.6V, f_C = 100kHz		60	µA
I_{CC4}	Supply Current (Standby) (ST24C02R)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V		10	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8V, f_C = 100kHz		20	µA
V_{IL}	Input Low Voltage (SCL, SDA)		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (E0-E2, MODE, $\overline{WC}$)		–0.3	0.5	V
V_{IH}	Input High Voltage (E0-E2, MODE, $\overline{WC}$)		V_{CC} – 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage (ST24 series)	I_{OL} = 3mA, V_{CC} = 5V		0.4	V
	Output Low Voltage (ST25 series)	I_{OL} = 2.1mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (ST24C02R)	I_{OL} = 1mA, V_{CC} = 1.8V		0.3	V

Table 7. AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C or –40 to 85°C; V_{CC} = 3V to 5.5V, 2.5V to 5.5V or 1.8V to 5.5V)

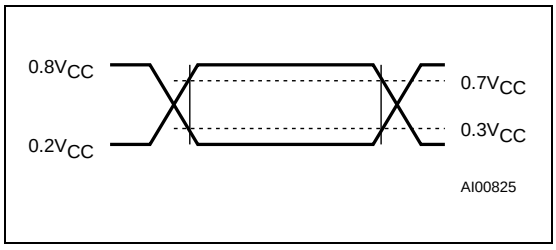
Symbol	Alt	Parameter	Min	Max	Unit
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	Input Rise Time		1	µs
t_{DL1DL1}	t_F	Input Fall Time		300	ns
t_{CHDX} (1)	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.7		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV} (2)	t_{AA}	Clock Low to Next Data Out Valid	0.3	3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W (3)	t_{WR}	Write Time		10	ms

Notes: 1. For a reSTART condition, or following a write cycle.
2. The minimum value delays the falling/rising edge of SDA away from SCL = 1 in order to avoid unwanted START and/or STOP conditions.
3. In the Multibyte Write mode only, if accessed bytes are on two consecutive 8 bytes rows (6 address MSB are not constant) the maximum programming time is doubled to 20ms.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Ref. Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 4. AC Testing Input Output Waveforms



DEVICE OPERATION (cont'd)

The 4 most significant bits of the device select code are the device type identifier, corresponding to the I^2C bus definition. For these memories the 4 bits are fixed as 1010b. The following 3 bits identify the specific memory on the bus. They are matched to the chip enable signals E2, E1, E0. Thus up to 8 x 2K memories can be connected on the same bus giving a memory capacity total of 16K bits. After a START condition any memory on the bus will identify the device code and compare the following 3 bits to its chip enable inputs E2, E1, E0.

The 8th bit sent is the read or write bit ($R\overline{W}$), this bit is set to '1' for read and '0' for write operations. If a match is found, the corresponding memory will acknowledge the identification on the SDA bus during the 9th bit time.

Figure 5. AC Waveforms

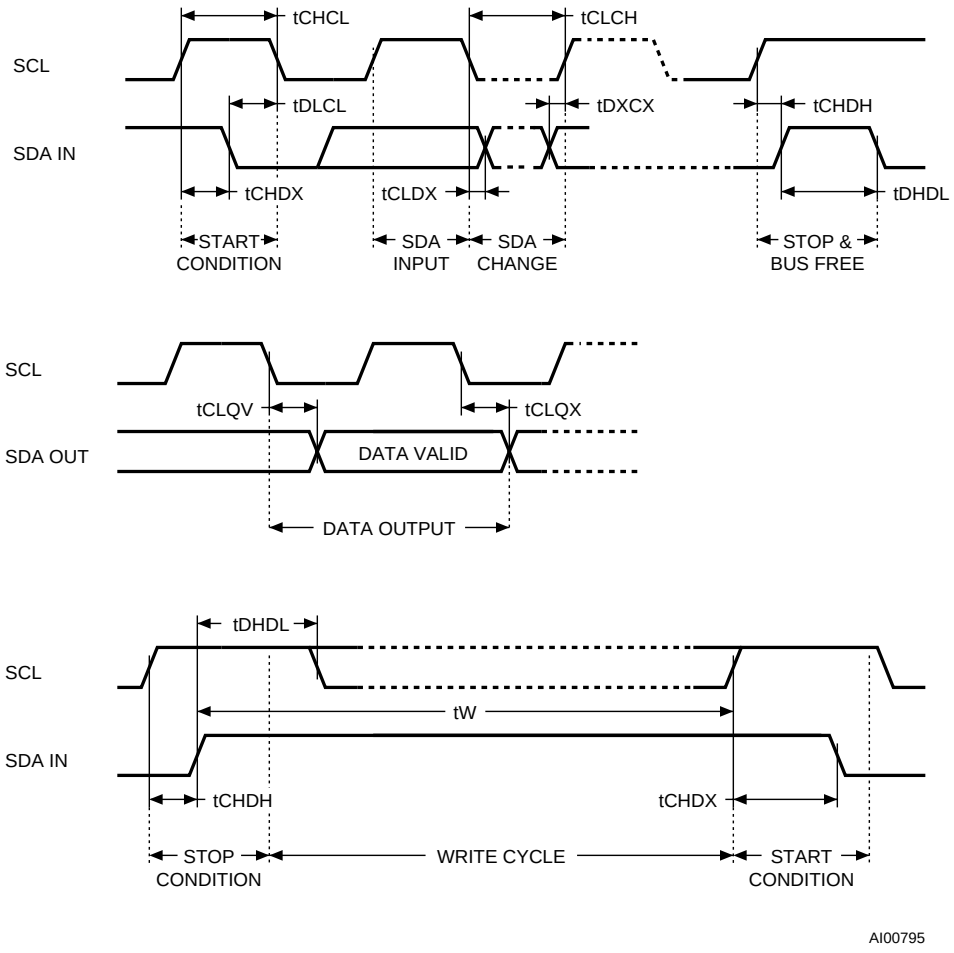
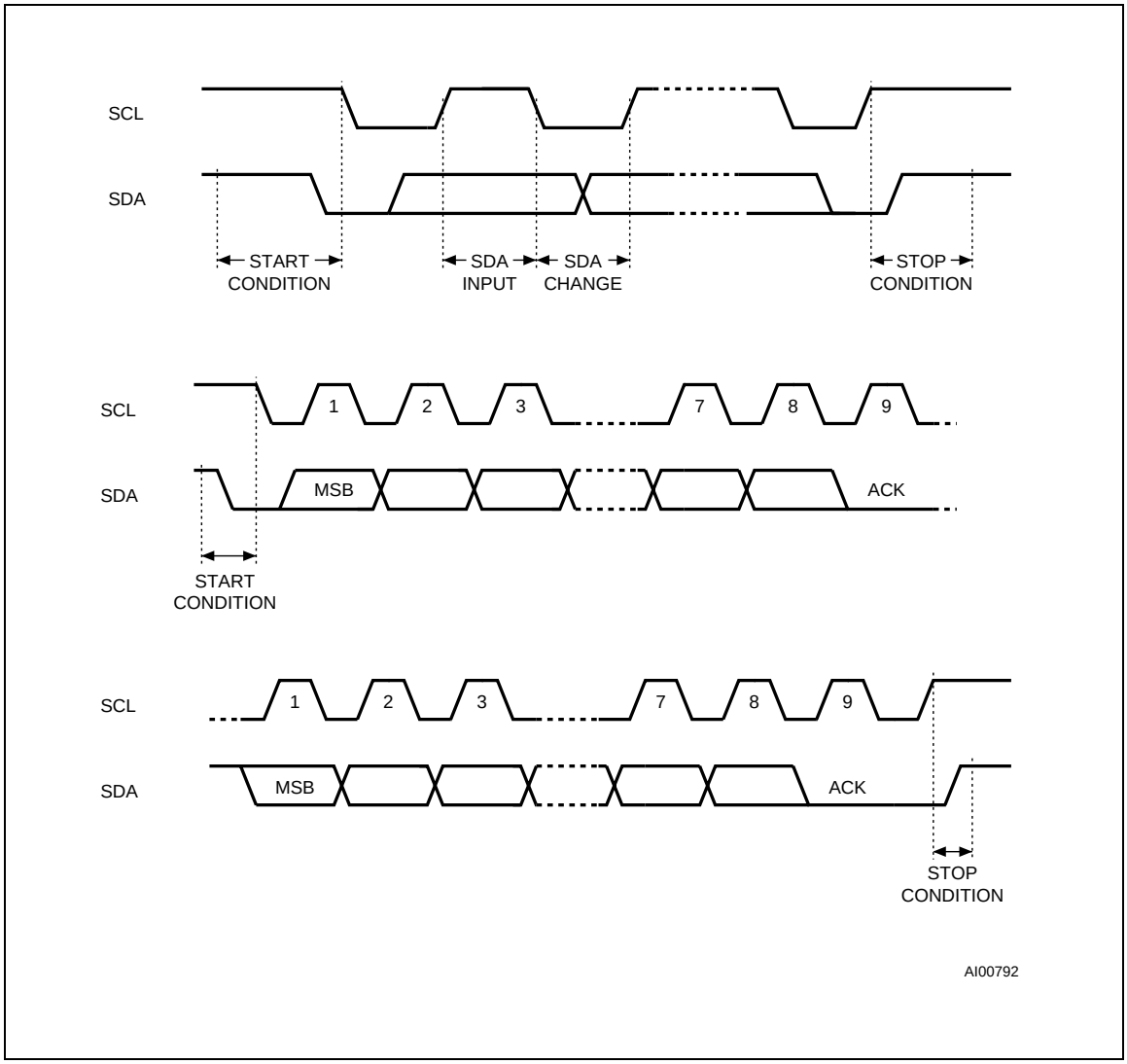


Figure 6. I²C Bus Protocol



Write Operations

The Multibyte Write mode (only available on the ST24/25C02 and ST24C02R versions) is selected when the MODE pin is at V_{IH} and the Page Write mode when MODE pin is at V_{IL}. The MODE pin may be driven dynamically with CMOS input levels.

Following a START condition the master sends a device select code with the $\overline{RW}$ bit reset to '0'. The memory acknowledges this and waits for a byte address. The byte address of 8 bits provides access to 256 bytes of the memory. After receipt of the byte address the device again responds with an acknowledge.

For the ST24/25W02 versions, any write command with $\overline{WC}$ = 1 will not modify the memory content.

Byte Write. In the Byte Write mode the master sends one data byte, which is acknowledged by the memory. The master then terminates the transfer by generating a STOP condition. The Write mode is independant of the state of the MODE pin which could be left floating if only this mode was to be used. However it is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL}, to minimize the stand-by current.

Multibyte Write. For the Multibyte Write mode, the MODE pin must be at V_{IH}. The Multibyte Write mode can be started from any address in the memory. The master sends from one up to 4 bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The duration of the write cycle is t_W = 10ms maximum except when bytes are accessed on 2 rows (that is have different values for the 6 most significant address bits A7-A2), the programming time is then doubled to a maximum of 20ms. Writing more than 4 bytes in the Multibyte Write mode may modify data bytes in an adjacent row (one row is 8 bytes long). However, the Multibyte Write can properly write up to 8 consecutive bytes only if the first address of these 8 bytes is the first address of the row, the 7 following bytes being written in the 7 following bytes of this same row.

Page Write. For the Page Write mode, the MODE pin must be at V_{IL}. The Page Write mode allows up to 8 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the 5 most significant memory address bits (A7-A3) are the same. The master sends from one up to 8 bytes of data, which are each acknowledged by the memory. After each byte is transfered, the internal byte address counter (3 least significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition. Care must be taken to avoid address counter 'roll-over' which could result in data being overwritten. Note that, for any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Figure 7. Write Cycle Polling using ACK

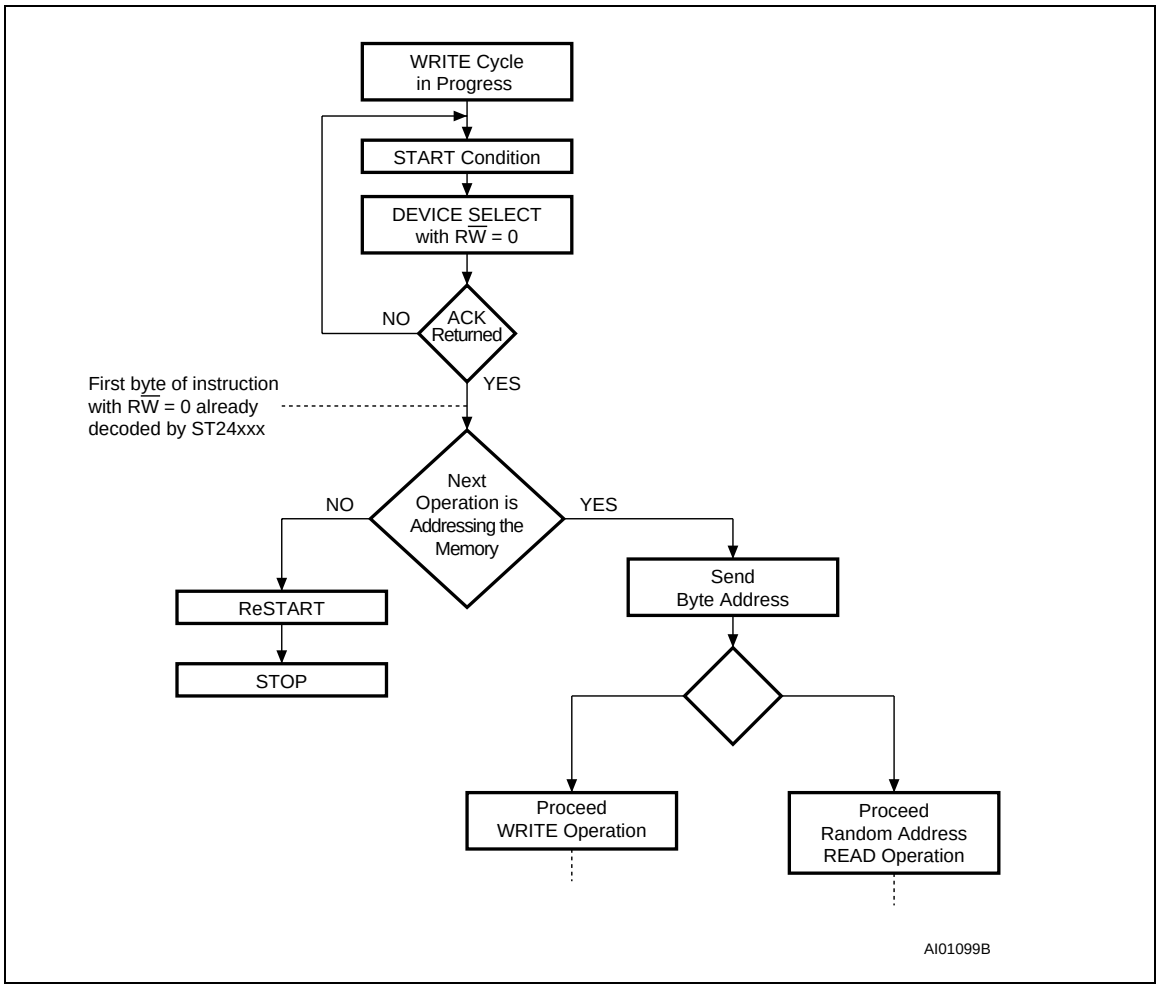
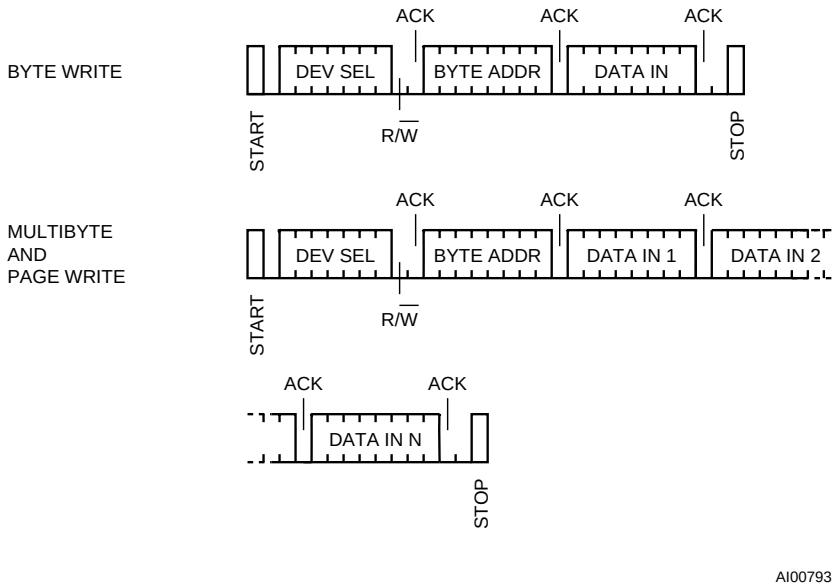


Figure 8. Write Modes Sequence (ST24/25C02 and ST24C02R)



Minimizing System Delays by Polling On ACK. During the internal write cycle, the memory disconnects itself from the bus in order to copy the data from the internal latches to the memory cells. The maximum value of the write time (t_W) is given in the AC Characteristics table, since the typical time is shorter, the time seen by the system may be reduced by an ACK polling sequence issued by the master. The sequence is as follows:

– Initial condition: a Write is in progress (see Figure 7).
– Step 1: the master issues a START condition followed by a device select byte (1st byte of the new instruction).
– Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it will respond with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction was already sent during Step 1).

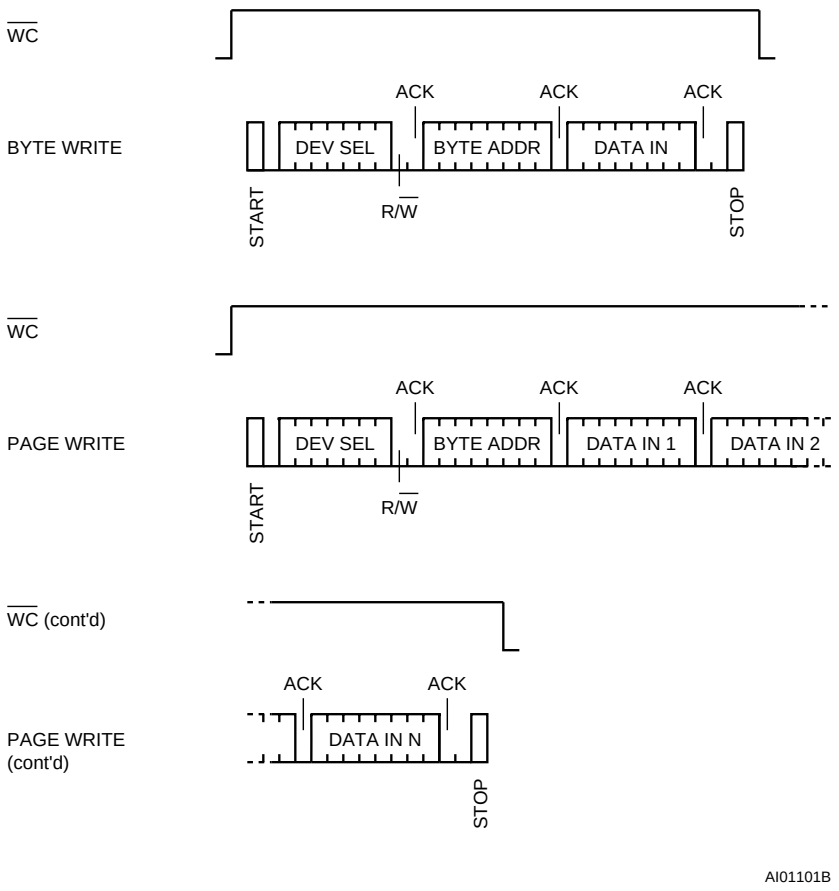
Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (or FFh).

Current Address Read. The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a memory address with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed by the internal byte address counter. This counter is then incremented. The master does NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

Random Address Read. A dummy write is performed to load the address into the address counter, see Figure 10. This is followed by another START condition from the master and the byte address is repeated with the $\overline{RW}$ bit set to '1'. The memory acknowledges this and outputs the byte addressed. The master have to NOT acknowledge the byte output, but terminates the transfer with a STOP condition.

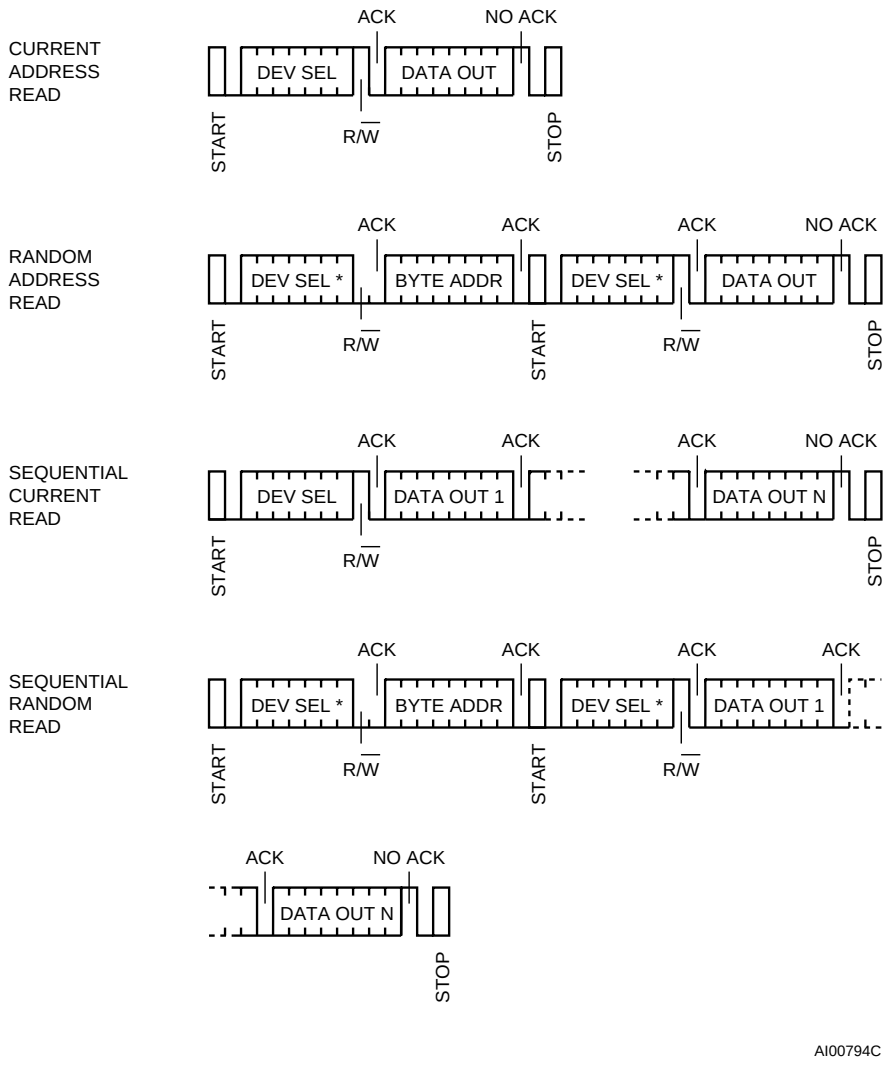
Figure 9. Write Modes Sequence with Write Control = 1 (ST24/25W02)



Sequential Read. This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master DOES acknowledge the data byte output and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must NOT acknowledge the last byte output, but MUST generate a STOP condition. The output data is from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After a count of the last memory address, the address counter will 'roll- over' and the memory will continue to output data.

Acknowledge in Read Mode. In all read modes the ST24/25x02 wait for an acknowledge during the 9th bit time. If the master does not pull the SDA line low during this time, the ST24/25x02 terminate the data transfer and switches to a standby state.

Figure 10. Read Modes Sequence



Note: * The 7 Most Significant bits of DEV SEL bytes of a Random Read (1st byte and 3rd byte) must be identical.

ORDERING INFORMATION SCHEME

Example: ST24C02 M 1 TR

Operating Voltage		Range
ST24C02	3V to 5.5V	Standard
ST24W02	3V to 5.5V	Hardware Write Control
ST25C02	2.5V to 5.5V	Standard
ST25W02	2.5V to 5.5V	Hardware Write Control
ST24C02R	1.8V to 5.5V	Standard

Package	
B	PSDIP8 0.25mm Frame
M	SO8 150mil Width

Temperature Range	
1	0 to 70 °C
5 *	–20 to 85 °C
6	–40 to 85 °C
3 *	–40 to 125 °C

Option	
TR	Tape & Reel Packing

Notes: 3 * Temperature range on special request only.
5 * Temperature range for ST24C02R only.

Parts are shipped with the memory content set at all "1's" (FFh).

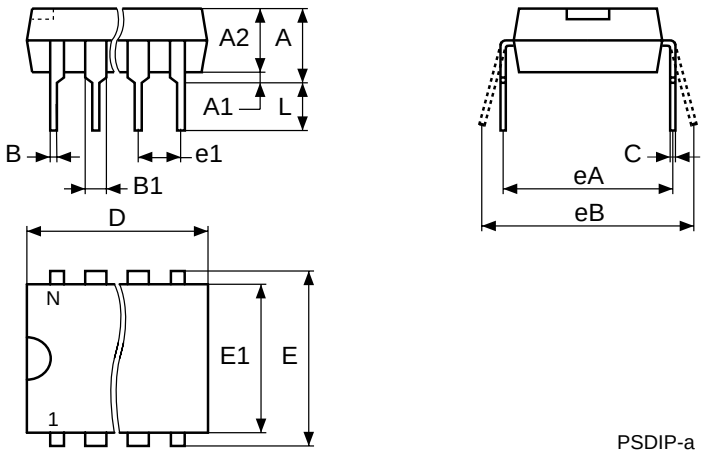
For a list of available options (Operating Voltage, Range, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

PSDIP8



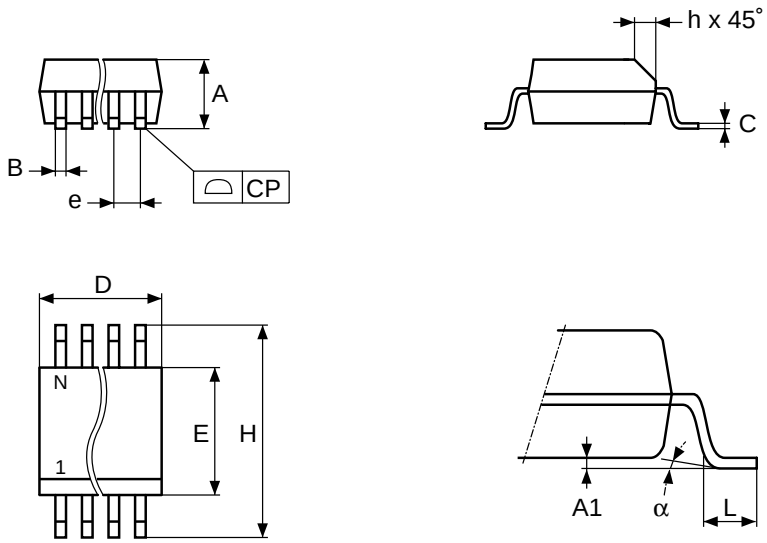
PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

SO8



SO-a

Drawing is not to scale