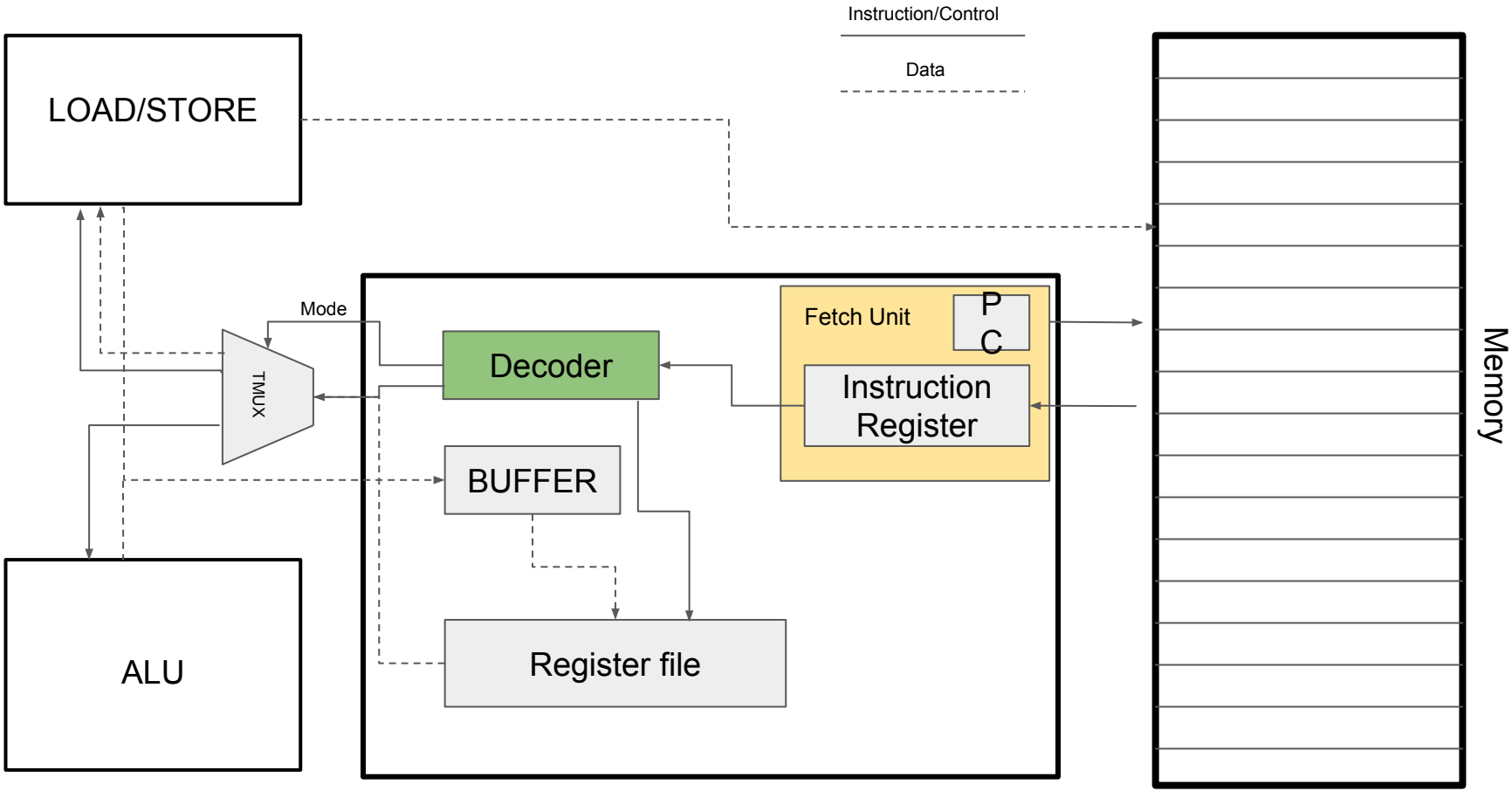
Instruction/Control
Data
LOAD/STORE
Mode
TMUX
Decoder
Fetch Unit
P
C
Instruction
Register
BUFFER
Register file
ALU
Memory

Architectural Features

- Simple non-pipelined Processor, capable of doing various Addition, Subtraction and Comparison instructions.
- Decoder creates new opcode for most instruction that are specific to each logic unit.
- Results from each execution will be stored in a buffer register, then later will be loaded in destination register during write back stage.

Experiments and Future Plans

- Currently, I have the simulator preloaded 3 instructions. Which loads 2 values on 2 different registers then adds them. I have tested this with all ALU operations, it seems it works fine.
- For the next step, I will work on branching, and finish off stage 3. After that I’m planning to write Insert or Bubble sort to use as benchmark.
- Most of work done is preparation for rest of stage 3 of this coursework.