

## DLD Quiz

Name: \_\_\_\_\_

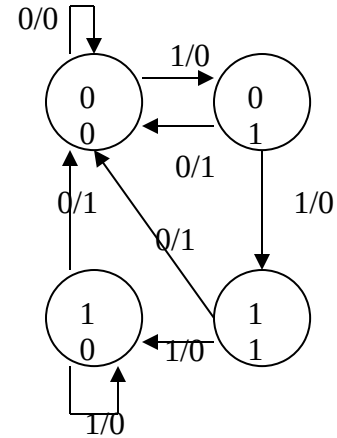
Roll No. \_\_\_\_\_

Time Allowed: **30 min**✓ **Do not spend too much time on a single question.****Section 1:****3+2 marks**

**Q1.** Starting from state 00 in the state diagram shown below, determine the state transitions and output sequence that will be generated when an input sequence of 0101101 is applied.

State Transitions:

00---00 ---01---00---01---11---00---01



Output Sequence: \_\_\_0010010\_\_\_\_\_

**Q2.** Can any flip flop(s) other than +ve/-ve edge triggered D-Flip-flop can be used in registers? Why? Why not? Give reasons. (Not more than 4 lines) **2 marks**

D-flipflops more feasible, one of reasons is  
 -- input volt (directly) = value stored

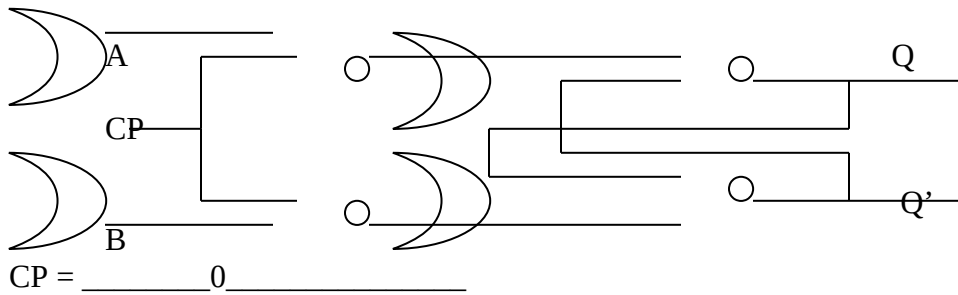
**Section 2:**

**Q1.** The state equation for L-M flip-flop is  $Q(t+1) = L'Q(t) + LM$ . Construct a state transition table (characteristic table) for the flip flop. **3 marks**

L	M	$Q(t+1)$
0	0	$Q(t)$
0	1	$Q(t)$
1	0	0
1	1	1

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**Q2.(a).** What should be the logical value of clock Pulse (CP) at the time of enabling the flip-flop whose diagram is shown below? **2+3+4 marks**

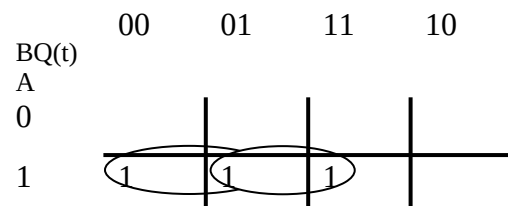


**(b)** Draw the characteristic table of the above flip flop.

CP	A	B	Q(t+1)
1	X	X	Q(t) No change
0	0	0	0 undefined as Q'=0 too
0	0	1	0 reset
0	1	0	1 set
0	1	1	Q(t) No change

**(c)** What is the characteristic equation of this flip flop?

A	B	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

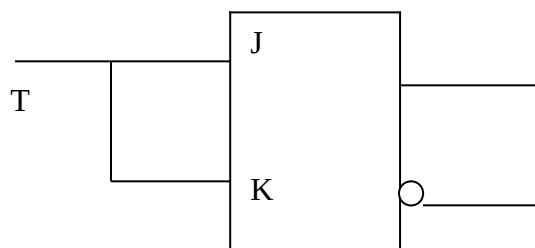


$$Q(t+1) = AB' + AQ(t)$$

**Q3.**

How can a J-K flip flop be converted into a T flip flop? A T-type FF changes its state at every clock pulse if its T-input is '1' and it remains in the present state as long as its T-input is '0'.

**3 marks**



J = K means  
 0 0 No change  
 1 1 Q'(t)

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as when

$T = 0$  No change

$T = 1$   $Q'(t)$