Roll # Solution 0111

National University of Computer and Emerging Sciences, Lahore Campus

Course:	Digital Logic Design	Course Code:	EE1005
Program:	BS(Computer Science/ Data Science/Robotics /BSR-2E)	Semester:	Spring 2023
Duration:	180 Minutes	Total Marks:	90
Paper Date:	31/5/2023	Weight	45%
Section:	ALL	Page(s):	10
Exam:	Final Exam	Roll No.	_____
		Section:	_____

Instruction/Notes:
- Attempt all the questions in the space provided to you in this answer booklet.
- Make sure to write down your roll # on EVERY sheet in the given space.
- Use of a calculator is not allowed.
- You can use a rough sheet but it will not be collected.

Marks				
CLO 1 (9)	CLO 2 (6)	CLO 3 (14)	CLO 4 (10)	CLO 5 (51)

Question 1: Short questions **(marks 5x3)**

1. $(2724)_8 + (3211)_4 = (\ 5006\ )_7$ CLO1

$(2\times8^3+7\times8^2+2\times8^1+4\times8^0) + (3\times4^3+2\times4^2+1\times4^1+1\times4^0)$

$= (1024+448+16+4) + (192+32+4+1)$

$= 1492 + 229$

$= (1721)_{10} = (5006)_7$

7	1721
7	245 – 6 ↑
7	35 – 0
	5 – 0

2. Represent the following decimal numbers into 6-bit binary and then subtract using 2's complement method.

(25) – (18) CLO1

25 in 6-bit 011001
18 in 6-bit 010010
2s complement of 18 101110

For (25)-(18), add 25 in the 2s complement of 18

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  011001
+ 101110
---------
 1000111
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The extra end carry, the 7th-bit is to be discarded. Rest is the answer.

Answer $(000111)_2 = (7)_{10}$

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3. Convert the following numbers

$(2A.9)_{16}$ to (52.44)$_8$ CLO1

$(2A.9)_{16} = (0010\ 1010 \cdot 1001)_2$

$0\ \ 5\ \ 2 \quad\ 4\ \ 4$

$= (52.44)_8$

4. Data stored in a register is "101011". Suppose T1 and T2 are two micro-operations carried out in sequence. After T1, the value changed to "010110" and after T2, value changed to"001011". Which micro-operation was performed on the register at T1 and T2 respectively? CLO2

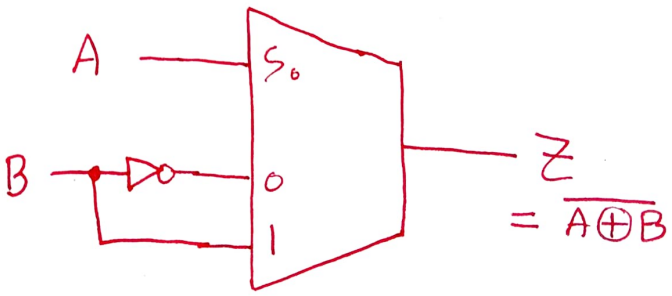
Data 101011

After T1 010110 Shift left operation

After T2 001011 Shift right operation after T1

5. Design XNOR gate using 2x1 MUX CLO2

A	B	XNOR = Z
0	0	1
0	1	0
1	0	0
1	1	1



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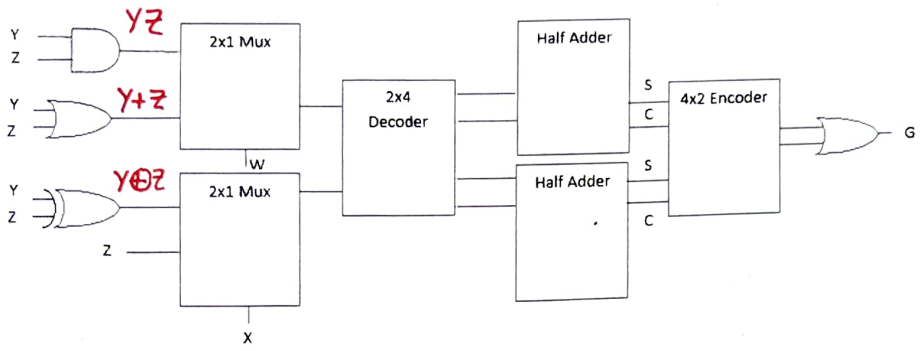
Question 2: Combinational Circuit (marks 8+6+10)

Part A CLO3

i. Given the circuit below, complete the truth table for the output G.



W	X	Y	Z	G
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1

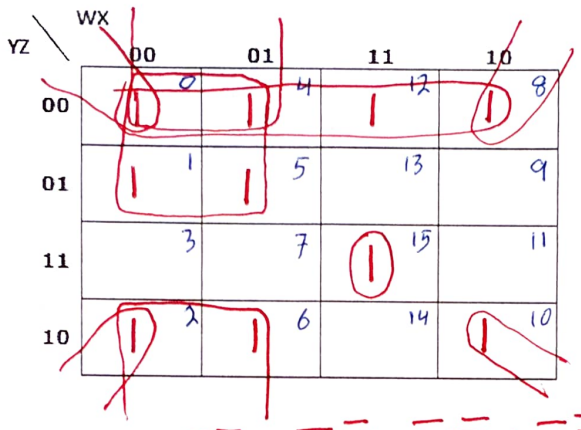
1	1	1	0	1
1	1	1	1	1

Part B

CLO3

Optimize the following Boolean function by means of a 4-variable map:

$$F(W,X,Y,Z) = \sum m(0,1,2,4,5,6,8,10,12,15)$$



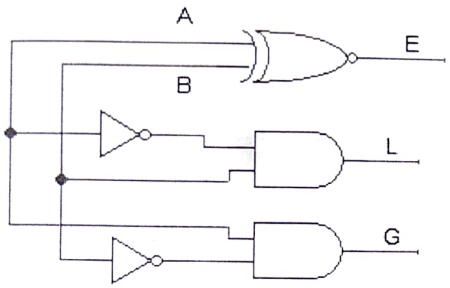
G (W, X, Y, Z) = $\bar{Y}\bar{Z} + \bar{W}\bar{Y} + \bar{W}\bar{Z} + \bar{X}\bar{Z} + WXYZ$

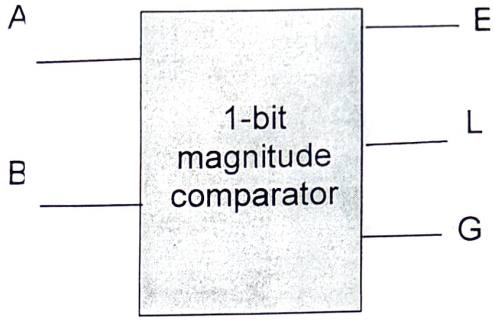
Part C

CLO4

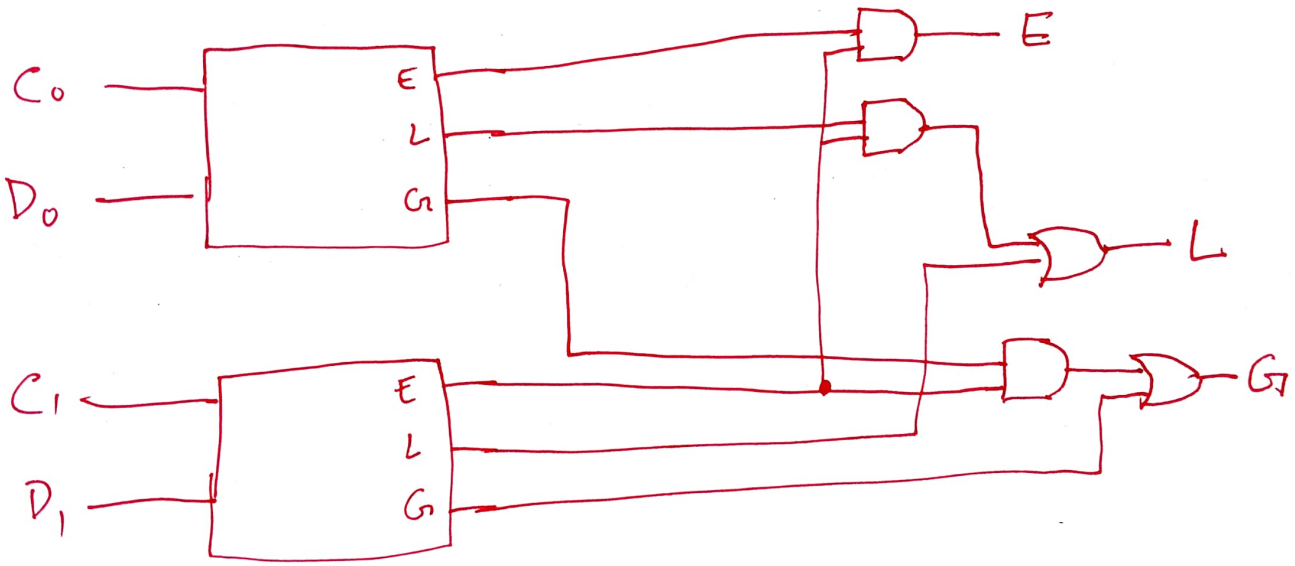
A magnitude comparator is a combinational circuit that compares two numbers of equal sizes and outputs E=1 if both numbers are equal; L=1, if the first number is less than the second number, and G=1 if the first number is greater than the second number. The truth table, circuit, and block diagram of the 1-bit magnitude comparator are shown below.

A	B	E	L	G
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0





Using the 1-bit magnitude comparator as a block and external gates, design the circuit of a two-bit magnitude comparator. A 2-bit magnitude comparator compares two numbers C and D of 2-bits each (C_1C_0 and D_1D_0) and there will be 3 outputs E=1, if C and D are equal, L=1, if C is less than D and G=1, if C is greater than D. Clearly label inputs/outputs to get credit.

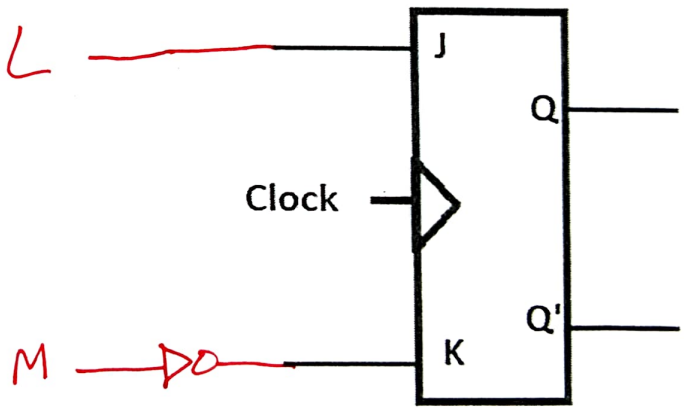


Question 3: Flip flops (marks 9+6)

Suppose you have the Flip flop **LM** with the following characteristic table. CLO5

L	M	Q
0	0	0
0	1	Q
1	0	Q'
1	1	1

Design this flip flop using JK-flip flop and additional gates



Give an excitation table for this flip flop

Present State Q	Next State Q	L	M
0	0	0	X
0	0	0	X
1	0	X	0
1	1	X	1

0 1 1 X

Question 4: Sequential Circuit Analysis (marks 12+4)

A sequential circuit is designed using two LM flip flops (described in the Q3) and an input X. The Input equations of the two LM flip flops (**A** & **B**) and the Output (Y) are given below: CLO5

$$L_A = X + AB' \qquad M_A = B' + A'X$$
$$L_B = A + A'B'X' \qquad M_B = (X \oplus A)'$$
$$Y = A' \oplus (B + X)$$

Your task is to analyze the given circuit. Use the characteristic table of LM flip flop (given in Q3) to **fill the state table then draw a state diagram** of the given sequential circuit.

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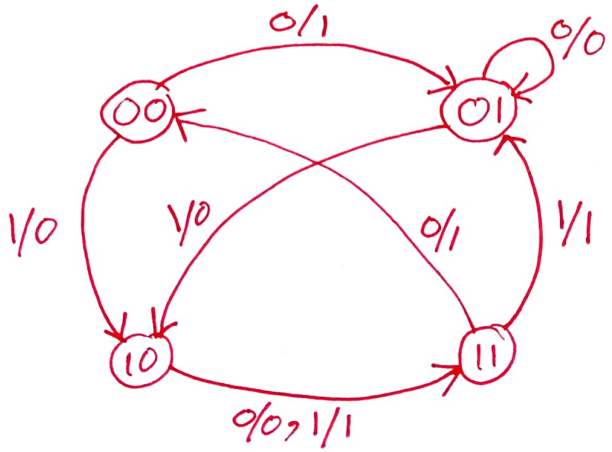
Present State		I/P	Next State		O/P	Flip-flop Inputs			
A	B	X	A^*	B^*	Y	L_A	M_A	L_D	M_B
0	0	0	0	1	1	0	1	1	1
0	0	1	1	0	0	1	1	0	0
0	1	0	0	1	0	0	0	0	1
0	1	1	1	0	0	1	1	0	0
1	0	0	1	1	0	1	1	1	0
1	0	1	1	1	1	1	1	1	1
1	1	0	0	0	1	0	0	1	0
1	1	1	0	1	1	1	0	1	1

State diagram:



Question 5: Registers (marks 20)

There is a three-plate stack in a canteen with a spring inside. The plate placed first stays at the top because of the spring. The two bottom places are empty. When a second plate is placed on the top, the previous plate moves to the middle place. When a third plate is placed on the top, the previous (second plate) goes to the middle place and the first plate goes to the bottom of the stack. There is only one place in the stack from where a plate can be placed (Inserted) in it or can be removed (deleted) from it and that is the top of the stack. This is essentially a LIFO (Last In First Out) system.

Using the concept of registers, design a digital system for this three-plate stack that can perform the following operations with the control signals Insert and Delete as follows: CLO5

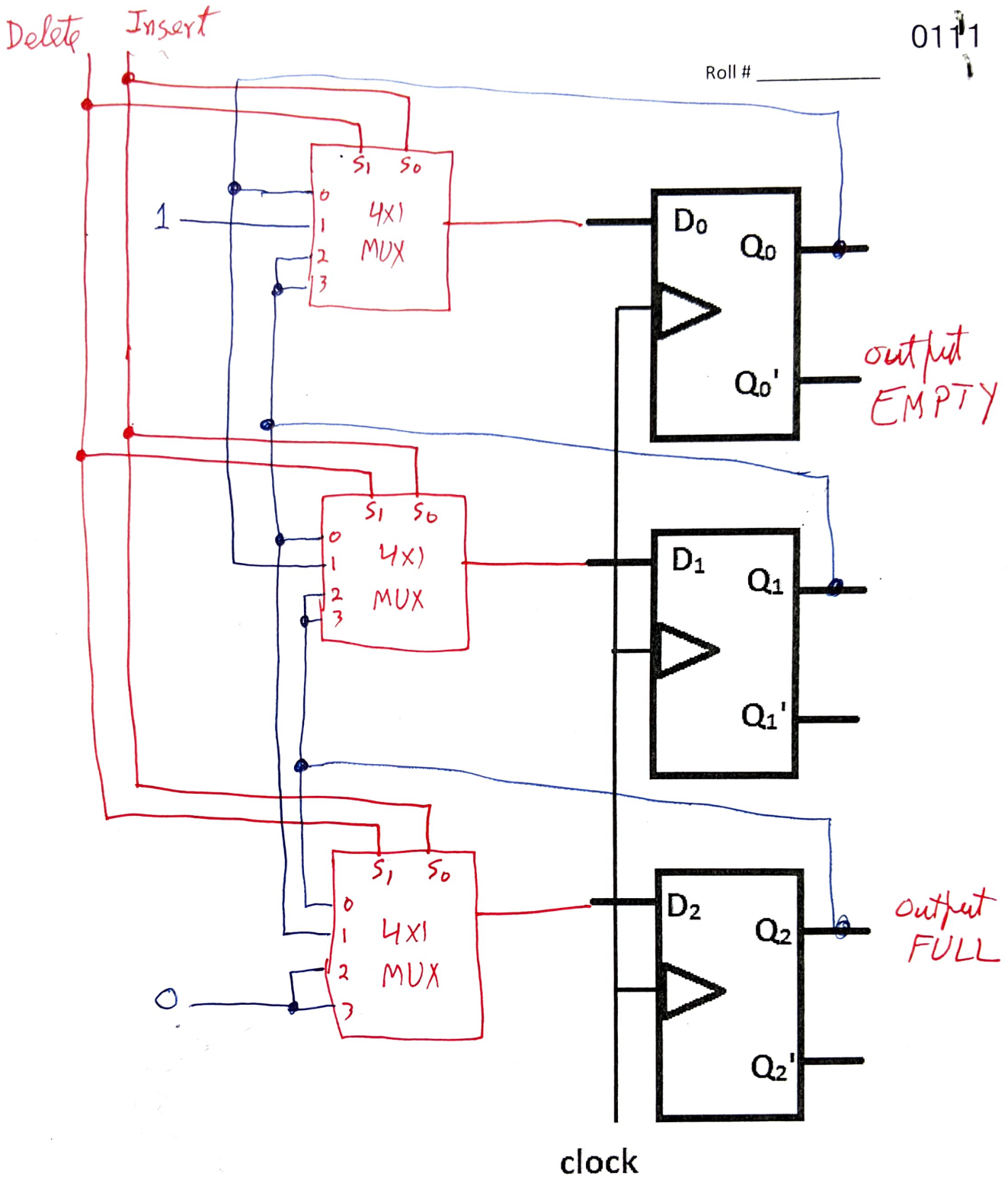
Control Signals		Function
Delete	Insert	
0	0	No change in the stack
0	1	Insert a plate into the stack
1	0	Remove a plate from the stack
1	1	Remove a plate from the stack

In addition, an output "Full" becomes 1 when the stack is full, i.e. all the three plates are in the stack. Another output "Empty" becomes 1 when the stack is empty, i.e. there is no plate in the stack. The outputs "Full" and "Empty" normally remain at logic 0.

Complete the circuit given below. You have 3 flip flops where D_0 is the top of the stack.

You may add any additional logic gates, functional blocks, as required.

Roll # _____


Delete
Insert
S1 S0
0
1
2
3
4X1
MUX
1
0
D0
Q0
Q0'
D1
Q1
Q1'
D2
Q2
Q2'
output
EMPTY
output
FULL
clock