Roll No. _____ Name: _____

National University of Computer and Emerging Sciences, Lahore Campus

Course: Digital Logic Design Course Code: EE227
Program: BS(Computer Science) Semester: Fall 2018 Duration: 1 Hour Total Marks: 30

Paper Date: 31st Dec 2018 Weight 45%
Section: ALL Page(s): 4
Exam: Final (objective) Roll No.
Name: Section:

Instruction/Notes: • *Attempt all the questions on this page in table given below. You can use extra sheets for your scratch work but* ***they will not be collected and marked****.*

• *Make sure you write your roll # on EVERY sheet of the booklet.*

• ***Use of calculator is not allowed.***

• ***This paper will be collected after 1 hour***

• Questions during exam are not allowed. Take reasonable assumptions where needed.

• Answers marked other this table will **NOT BE MARKED**

S.No	Answer	S.No	Answer
1		9	
2		10	
3		11	
4		12	
5		13	
6		14	
7		15	
8		16	
		17	
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1. In function implementation of n variables using MUX, _____ variables will go in selection lines.
2. $(18_{16} + (15)_8 =$ __(_____)$_2$
3. Convert $(198)_{10}$ to 8-bit binary. _____

4. Convert $(111001110010)_2$ to hexadecimal. _____

5. The BCD number for decimal 352 is _____

6. The sum of $(1101101)_2 + (10111)_2$ equals _____

7. In postulates of Boolean Algebra, distributive postulate is x+yz = _____ 8. How many flip-flops are required to construct a BCD counter? _____ 9. The SOP function F = ∑ A, B, C (0,2, 4,5,7), convert this to POS form _____ 10. Write dual of A+ (B.C)=_____

11. Any combinational circuit with *n* inputs and *m* outputs can be implemented with *n-to-*2^n line decoder and _____ OR gates

12. In binary number system the first digit (bit) from right to left is called as _____ 13. Which flip flop type has invalid/undefined output state? _____ 14. Odd parity of word can be conveniently tested by _____ gate 15. Dual and complement of the Boolean expression is same for:

(a)X + Y + Z (b) XY + Z’ (c) X'Y'Z' (d) None of above

16. When adding an even parity bit to the code 110010, the result is _____ 17. Write 2’s complement of $(10101)_2$ _____

18. Shift right register value is $(10101011)_2$ initially, what will the value after 4 clock cycles if serial out is connected to the serial in _____

19. The NOR gate output will be high if the two inputs are

a) 00

b) 01

c) 10

d) 11

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20. The following switching functions are to be implemented using a decoder: $f1 = \sum m(1, 2, 4, 8, 10, 14)$ $f2 = \sum m(2, 5, 9, 11)$ $f3 = \sum m(2, 4, 5, 6, 7)$

The minimum configuration of decoder will be

a) 2 to 4 line

b) 3 to 8 line

c) 4 to 16 line

d) 5 to 32 line

21. A universal logic gate is one which can be used to generate any logic function. Which of the following is a universal logic gate?

a) OR

b) AND

c) XOR

d) NAND

22. A full adder logic circuit will have

a) Two inputs and one output

b) Three inputs and three outputs

c) Two inputs and two outputs

d) Three inputs and two outputs

23. The gates required to build a half adder are

a) EX-OR gate and NOR gate

b) EX-OR gate and OR gate

c) EX-OR gate and AND gate

d) Four NAND gates

24. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a) Ex-NOR gate

b) OR gate

c) Ex-OR gate

d) NAND gate

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25. Behavior of sequential circuits are determined by state of their

a) clock
b) pulses
c) flip-flops
d) trigger

26. If one wants to design a binary counter, preferred type of flip-flop is a) D type
b) S-R type
c) Latch
d) J-K type

27. The term synchronous means

a) The output changes state only when any of the input is triggered b) The output changes state only when the clock input is triggered c) The output changes state only when the input is reversed d) None of the Mentioned

28. How many different states does a 3-bit asynchronous counter have? a) 2

b) 4

c) 8

d) 16

29. In an UP-counter, each flip-flop is triggered by

a) The output of the next flip-flop

b) The normal output of the preceding flip-flop

c) The clock pulse of the previous flip-flop

d) The inverted output of the preceding flip-flop

30. The flip-flop is only activated by

a) Positive edge trigger

b) Negative edge trigger

c) Either positive or Negative edge trigger

d) None of the Mentioned