National University of Computer and Emerging Sciences

Lahore Campus

Digital Logic Design (EE1005)

Final Exam

Date: May 20TH 2024

Total Time (Hrs): 3

Total Marks: 90

Total Questions: 6

Course Instructor(s)

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Roll No _____ Section _____ Student Signature _____

Instructions:

1. **CALCULATORS ARE NOT ALLOWED.**
2. **Answer all questions. Answer Q1, Q5(a) and Q6(a) on Answer Sheet and rest on the question paper.**

CLO# 1: Understand different number systems and their conversion

Q 1 Convert the following subtraction problem into an addition problem, $(11010)_2 - (10101)_2$ **[5]**

= 00101

11010 + 2's(10101)
1 1
11010
01011
(1)00101

CLO# 2: Recognize and use basic gates to implement logic circuits

Q 2 **[10]**

In a state-of-the-art factory, an advanced robotic arm equipped with four sophisticated sensors is deployed for automated item classification. These sensors can detect various intricate characteristics of the items passing through the assembly line. One sensor**(A)** detects whether the item possesses delicate components, indicating fragility. Second**(B)** measures the weight of the item, distinguishing between heavy and light objects. Third **(C)** separates the material composition of the item, identifying whether it is metallic or non-metallic. The last **(D)** one evaluates the item's intrinsic value, determining its economic significance. The robotic arm's task is to make intelligent decisions based on these inputs. It is programmed with a set of rules to sort the items effectively:

Complex Fragility Analysis (W): If an item is both fragile and heavy, the robotic arm must carefully place it in the "special handling" area to prevent damage during transportation.

Precise Valuable Item Identification (X): Items that are both metallic and valuable are of utmost importance. These items are sent to the "high-value storage" area for secure storage and processing, ensuring their safety and proper handling.

Material-specific Storage (Y): If an item is neither fragile nor heavy but is metallic, it should be directed to the "metallic storage" area.

Fallback to Standard Storage (Z): If an item does not meet any of the above conditions, it should be sent to the "standard storage" area. This area serves as the default location for items that do not require special handling or have specific material or fragility considerations.

$W = A \cdot B$ $\quad Y = A'B'C$

$X = C \cdot D$ $\quad Z = (AB + CD + A'B'C)'$

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i) Show truth table for the required robotic arm.

ii) Write the output(s) in canonical form

A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	1	1	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	0	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	0
1	1	1	0	1	0	0	0
1	1	1	1	1	1	0	0

$W = \sum_m (12, 13, 14, 15)$

$X = \sum_m (3, 7, 11, 15)$

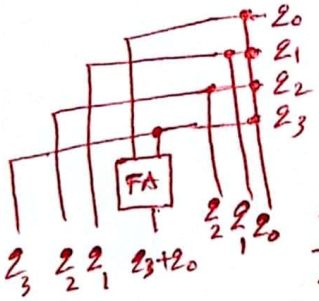
$Y = \sum_m (2, 3)$

$Z = \sum_m (0, 1, 4, 5, 6, 8, 9, 10)$

CLO# 3: Constructs optimized logic circuit design

Q 3 **[15]**

A 4x4 multiplier hardware is available to multiply two 4-bit numbers '**m**' and '**q**'. The client requires 9 times number '**q**' only. Simply cross the unnecessary logic unit in the diagram given below on the question paper.



$z_3\ z_2\ z_1\ z_0$

$1\ 0\ 0\ 1$

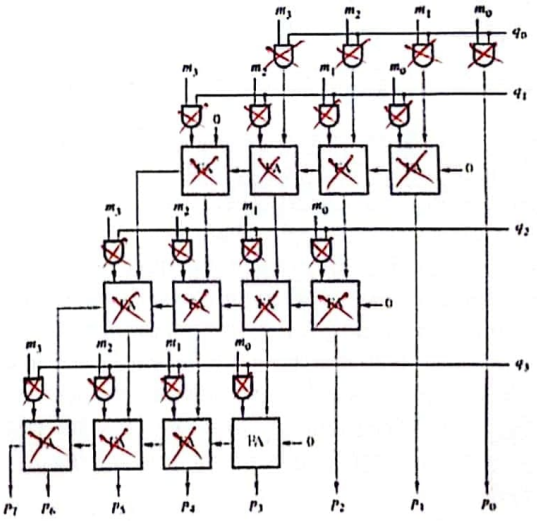
$z_3\ z_2\ z_1\ z_0$

$0\ 0\ 0\ 0\ X$

$0\ 0\ 0\ 0\ X\ X$

$z_3\ z_2\ z_1\ z_0\ X\ X\ X$

$z_3\ z_2\ z_1\ (z_3+z_0)\ z_2\ z_1\ z_0$



CLO# 4: Construct and utilize the basic functional blocks to design combinational circuits

Q 4 **[20]**

A 4-bit Arithmetic Logic Shift Unit along with (two 2x1 multiplexers) is shown in Figure below. This Unit has got two input data ports X and Y (4-bits each) and three select input bits that control the operation of this Unit as shown in the table on its right side.

Note that the input operands P, Q, R and T are all 4-bits (and therefore can have values between 0_{16} and F_{16}).

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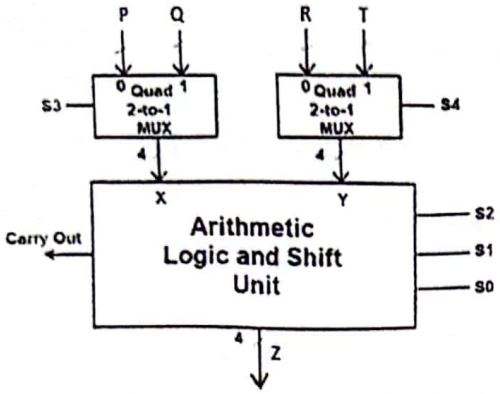


Select Inputs S2 S1 S0	Operation	Explanation (what appears at the output)
0 0 0	Z = X+1	Increment X
0 0 1	Z = X – Y	Subtract Y from X
0 1 0	Z = X + Y	Add Y to X
0 1 1	Z = X ∨ Y	Bitwise OR operation between X and Y.
1 0 0	Z = X ∧ Y	Bitwise AND operation between X and Y.
1 0 1	Z = X'	Complement Left input X
1 1 0	F = X ⊕ Y	Bitwise XOR operation between X and Y.
1 1 1	F = SHL Y	Shift Left the contents of input Y. (Carry Out may be affected).

S3 and S4 are the single bits select inputs of the multiplexers. If 0, left operand is selected else right operand is selected.

(a) Complete the following table. [15]

P	Q	R	T	S4	S3	S2	S1	S0	Z (in binary)	Carry Out	
5	3	2	C	1	0	0	1	0	0001	1	P+T = 5+C = 0101+1100
2	F	5	9	0	1	1	1	0	1010	—	Q⊕R = F+5 = 1111⊕0101
7	2	0	3	0	0	1	0	1	1000	—	P' = Not(0111) = 1000
D	3	7	2	1	0	1	0	0	0000	—	P∧T = 1101 ∧ 0010
5	2	D	F	0	1	0	1	1	1111	—	Q∨R = 0010 ∨ 1101 = 1111
F	E	D	B	1	0	0	1	0	1010	1	P+T = 1111+1011 = 1010 (1)
F	E	D	B	0	0	0	0	1	0010	1	P−R = 1111+2's(1101)
F	E	D	B	0	1	1	1	0	0011	—	Q⊕R = 1110⊕1101
F	E	D	B	1	1	1	1	1	0110	1	SHL T = SHL 1011 = 0110 (1)
F	E	D	B	1	0	0	0	0	0000	1	P+1 = 1111+1

(b) What will be the select inputs to perform the following operations? [5]

	S4	S3	S2	S1	S0
Z = T + 1	—	—	—	—	—
Z = Q⊕T	1	1	1	1	0

Not possible

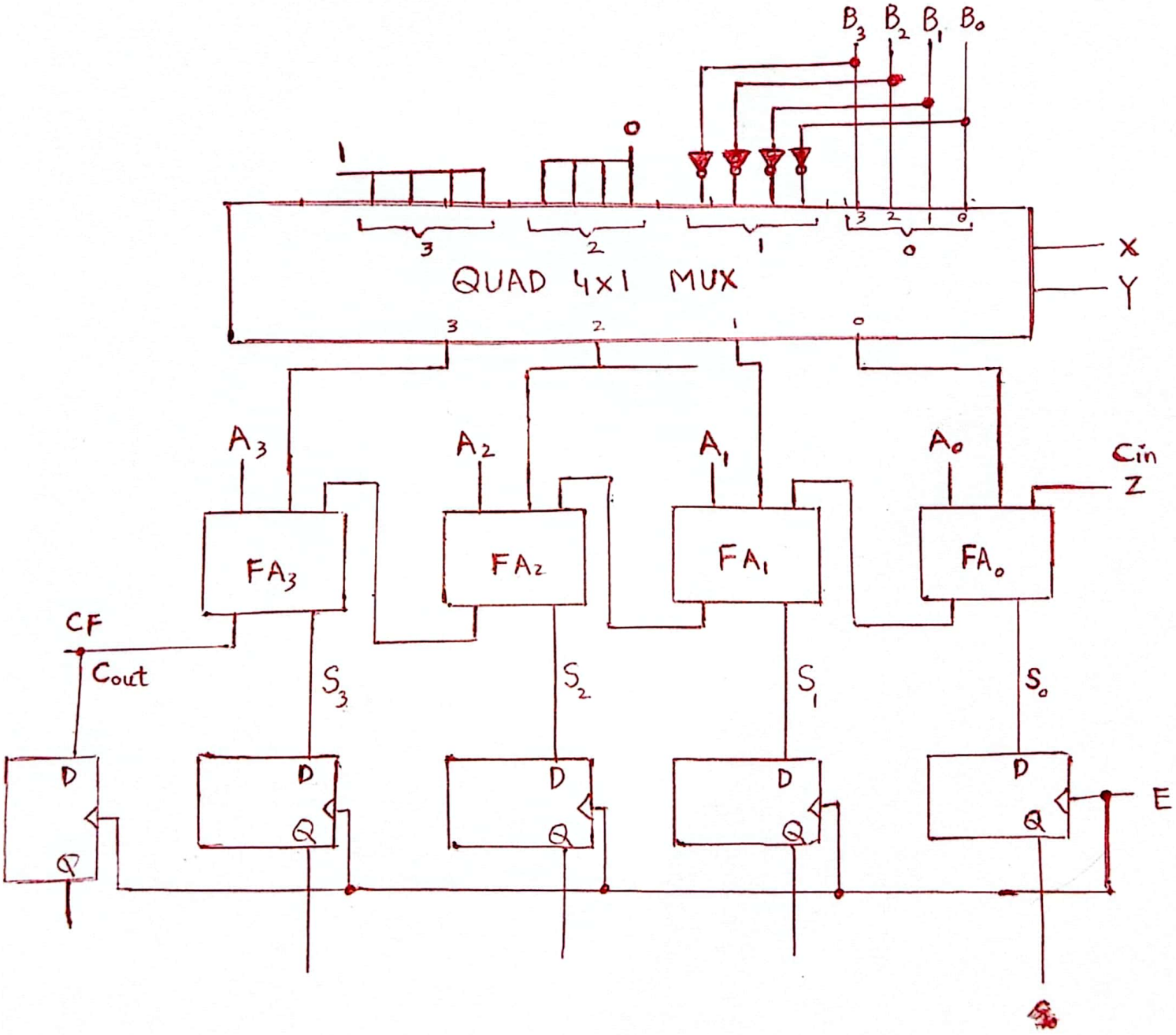
CLO# 5: Design and demonstrate synchronous/ asynchronous

Q 5 (a) [10]

Design and implement an Arithmetic Logic Unit (ALU) based on the provided truth table, which governs the operation of two 4-bit numbers (A and B) along with inputs X, Y, Z and E. Upon toggling switch Equals (E), ensure that the resultant computation is loaded in a 4-bit register and the Extra output should also be displayed as a Carry Flag (CF). You are provided with D Flip flops, Full Adders, one Quad 4x1 Multiplexer and Not Gates Only. Use optimum quantities of the above.

X	Y	Z	Output	Microoperation
0	0	0	D=A+B	Add
0	0	1	D=A+B+1	Add with carry
0	1	0	D=A+B'	Subtract with borrow
0	1	1	D=A+B'+1	Subtract
1	0	0	D=A	Transfer A
1	0	1	D=A+1	Increment A
1	1	0	D=A-1	Decrement A
1	1	1	D=A	Transfer A

Q# 5(a)


B3 B2 B1 B0
1
0
3
2
1
0
QUAD 4x1 MUX
X
Y
A3
A2
A1
A0
Cin
Z
FA3
FA2
FA1
FA0
CF
Cout
S3
S2
S1
S0
D
Q
E

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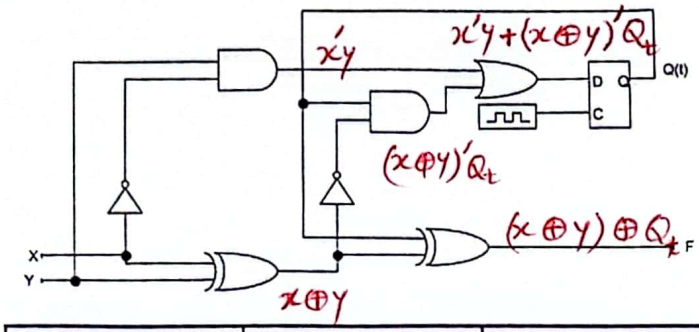
Q 5 (b) **[10]**



Analyze the given circuit and fill-in the state table.

$Q_{t+1} = x'y + (x \oplus y)' Q_t$

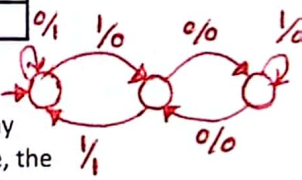
$F = (x \oplus y) \oplus Q_t$

X	Y	Q(t)	Q(t+1)	F
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Q 6 **[10+10]**

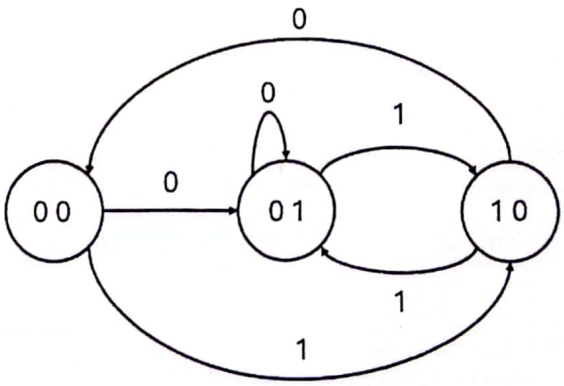
(a) Design a state diagram only that accepts binary input, one bit at a time. The output should be 1 for any sequence where the decimal equivalent of the binary numbers inputted so far is divisible by 3. Otherwise, the output should be 0. For instance, given the input sequence '10101110', the outputs should be '00001011', indicating that the sequences '10101', '1010111', and '10101110' convert to decimal numbers 21, 87, and 174, respectively, each of which is divisible by 3.

Q6(a)



(b) For the state diagram given fill the following utilizing JK Flip Flops (we don't care about un-used states)

A_t	B_t	x	A_{t+1}	B_{t+1}	J_A	K_A	J_B	K_B
0	0	0	0	1	0	X	1	X
0	0	1	1	0	1	X	0	X
0	1	0	0	1	0	X	X	0
0	1	1	1	0	1	X	X	1
1	0	0	0	0	X	1	0	X
1	0	1	0	1	X	1	1	X



Equations:

$J_A = x$ $\quad K_A = 1$

$J_B = (A_t \oplus x)'$ $\quad K_B = x$