National University of Computer and Emerging Sciences

Lahore Campus

Digital Logic Design (EE1005)

Sessional-II Exam

Total Time (Hrs): 1
Total Marks: 50
Total Questions: 3

Date: April 6TH 2024

Course Instructor(s)

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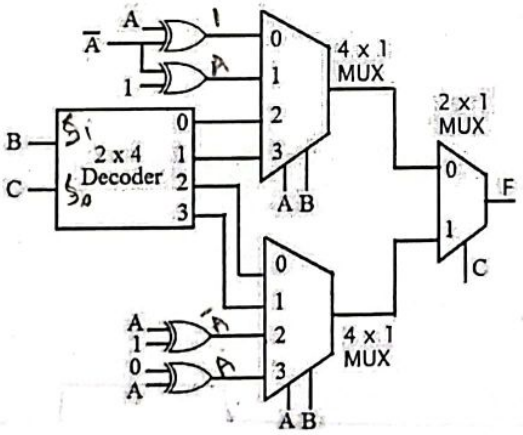
Instructions:

1. Solve questions 1 and 2 on the answer sheet and solve question 3 on the question paper and attach it with your answer sheet.
2. Show the required steps and label properly to get the full credit.
3. ***Solve the paper in the sequence provided in the question paper i.e Question 1 should be solved before question 2.***

CLO# 4: Construct and utilize the basic functional blocks to design combinational circuits.

Q 1: (a) For the logic diagram shown below, write down the output function F in Σ notation (Sum of Minterms form). Reduce the output function F in SOP. **[10+5]**



(b) Use a 4 x 1 Multiplexer (with minimum added logic) to implement the following 4-variable Boolean Function: $F(A, B, C, D) = \Sigma m(2, 3, 4, 6, 11, 12)$ **[10]**

CLO# 4: Construct and utilize the basic functional blocks to design combinational circuits.

Q 2: Use a single decoder and a minimum number of OR gates to implement the following two Boolean Functions. Don't forget to mention the size of the decoder.

[10]

$X(A, B, C) = (A+C').(B'+C)$

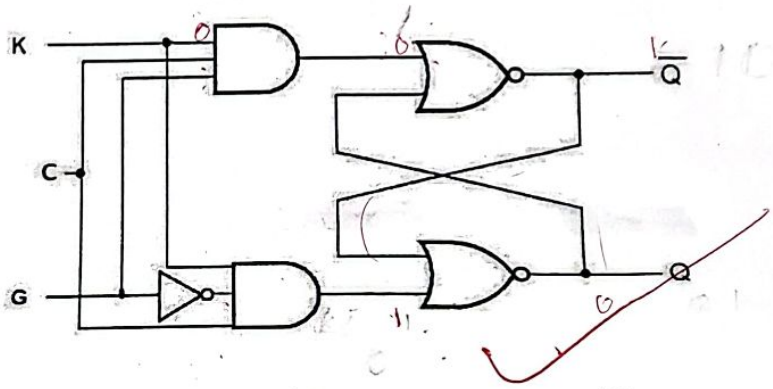
$Y(A, B, C) = A.B' + B.C$

CLO# 5: Design and demonstrate synchronous/ asynchronous digital circuits

Q 3: A new type of latch called KG latch has been introduced that is shown in the figure below: Solve this question here and attach this question paper with answer sheet.

(a) Fill-in the Next State Column of the function table of KG Latch. **[5]**

Latch Inputs		Next State
K	G	Q(t+1)
0	0	Q(t)
0	1	Q(t)
1	0	0
1	1	1



(b) *Derive the characteristic equation* Q(t+1) as a function of Q(t), K, and G. **[5]**

$Q(t+1) = KG + \bar{K}\bar{G}Q(t) + \bar{K}GQ(t)$

$Q(t+1) = KG + \bar{K}Q(t)$

(c) Show the timing behavior of KG latch in the space below: **[5]**