# National University of Computer and Emerging Sciences, Lahore Campus

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|---|---|---|---|
| Course: | Digital Logic Design | Course Code: | EE227 |
| Program: | BS(Computer Science) | Semester: | Fall 2018 |
| Duration: | 25 Minutes | Total Marks: | 10 |
| Quiz Date: | 12-12-18 | Weight: | |
| Section: | A | Page(s): | |
| Exam: | Quiz-5 | Roll Number | |

**Show your working otherwise no credit will be given.**

**Q1. Design a counter with the following binary sequence 0,1,3,2,4,5,7. Use SR flipflops. (10marks)**

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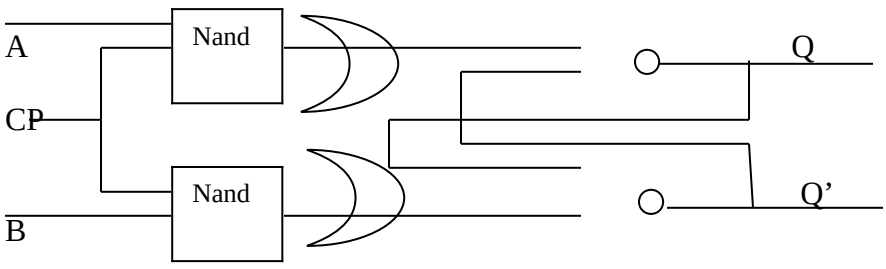
|---|---|---|---|---|
| | Course: | Digital Logic Design | Course Code: | EE227 |
| | Program: | BS(Computer Science) | Semester: | Fall 2018 |
| | Duration: | 25 Minutes | Total Marks: | 20 |
| | Quiz Date: | 29-11-18 | Weight: | |
| | Section: | A | Page(s): | |
| | Exam: | Quiz-4 | Roll Number | |

**Show your working otherwise no credit will be given.**

**Q1.** The state equation for T-R flip-flop is Q(t+1) = T'Q(t)+RT. Construct a characteristic table for the flip flop. **[10 marks]**

**Q2 (a).** What should be the logical value of clock Pulse (CP) at the time of enabling the flip-flop whose diagram is shown below? [**10 marks]**




CP = _____

**(b)** Fill the characteristic table of the above flip flop.

| CP | A | B | Q(t+1) |
|---|---|---|---|
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