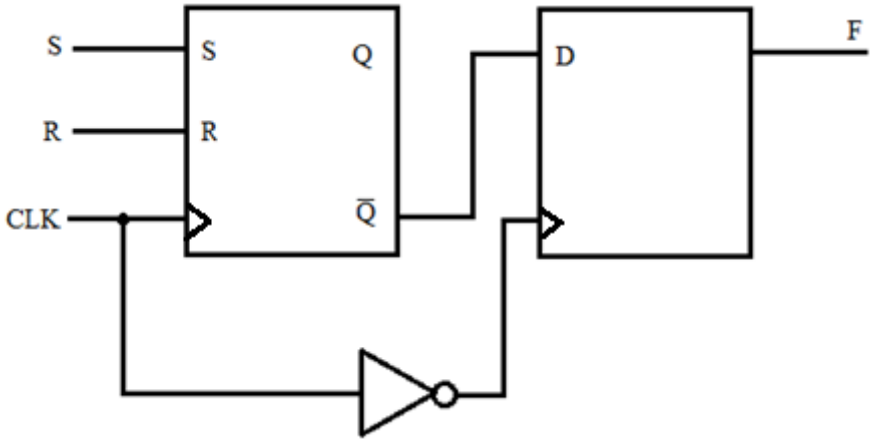
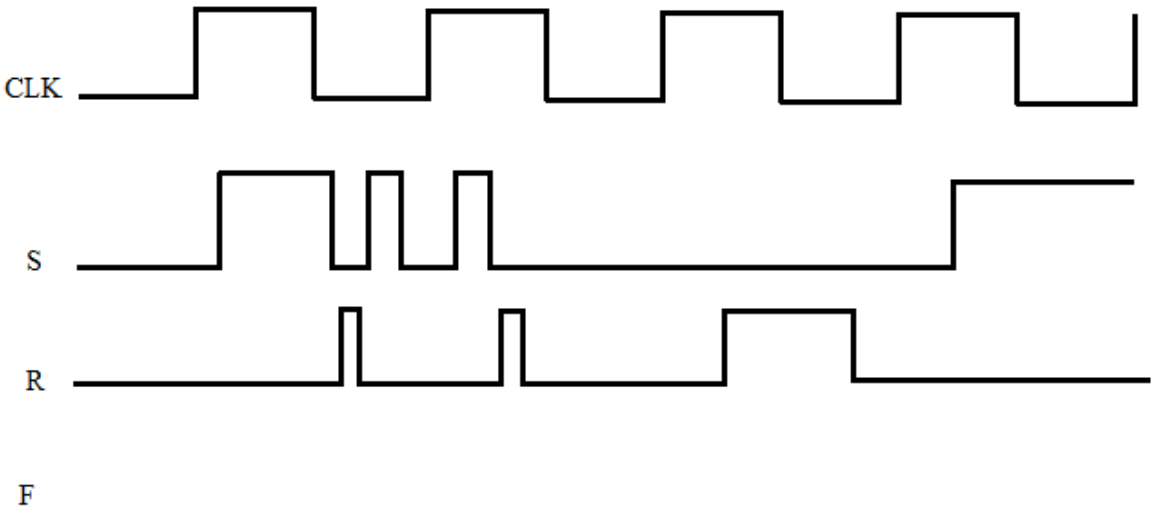
National University of Computer & Emerging Sciences, Lahore
Department of Electrical Engineering (Spring 2024)

EE1005 – Digital Logic Design
Assignment#3 (CLO-05)

Due Date: May 14, 2024

Question#1: Complete the timing diagram for the logic circuit given below: **Points: 20**
Note: Assume that the initial value of **F** is zero.





Characteristic tables for SR and D flip-flops:

C	S	R	Q(t+1)
0	X	X	**Q(t) No change**
1	0	0	**Q(t) No change**
1	0	1	**0**
1	1	0	**1**
1	1	1	**Invalid**

C	D	Q(t+1)
0	X	**Q(t) No change**
1	0	**0**
1	1	**1**

Question#2: **Points : 20**

For the synchronous sequential circuit shown in figure 1, do the following:

a) Determine expressions for the flip-flop inputs **J1, K1** and the output function **Z**.
b) Find state table.
c) Draw the state diagram.
d) State that whether the model is Mealy or Moore.

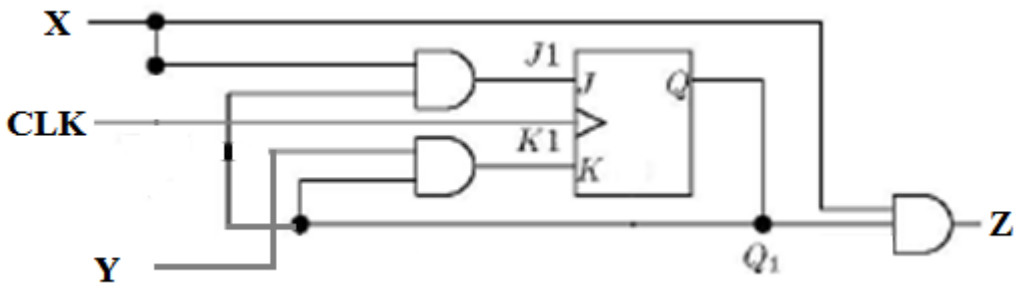


Figure 1

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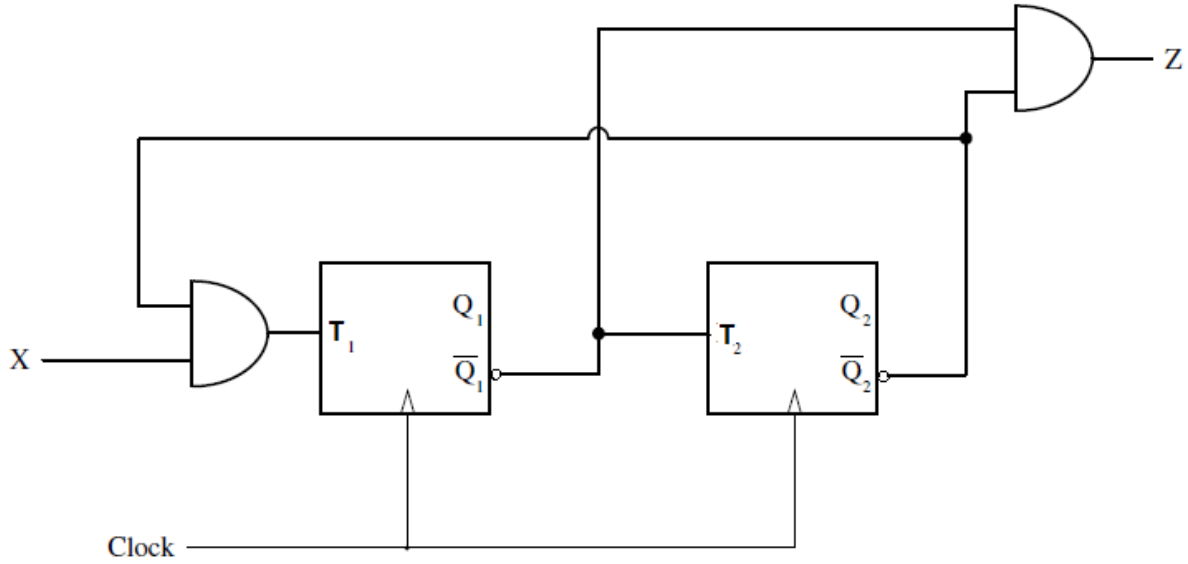
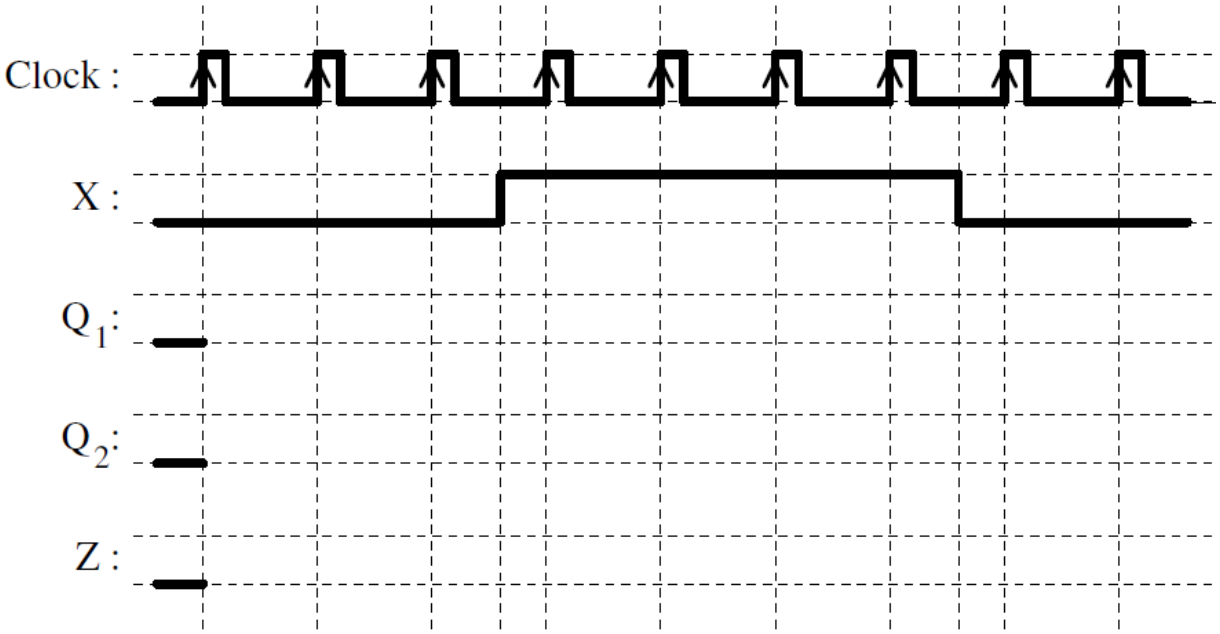
Question#3: **Points : 20**

Complete the timing diagram given below for the following synchronous sequential logic circuit.





Question#4: **Points: 30**

Design a synchronous binary arbitrary counter to produce the sequence 1, 4, 3, 5, 7, 6, 2, 1 and so on.

a) Find the state diagram and state table for the required circuit.
b) State that whether the model is Mealy or Moore.
c) Find an implementation of the circuit using positive edge triggered D flip flops and logic gates.
d) A counter is self-correcting if, after entering an unused state, it eventually returns to its proper count sequence. Is your designed counter shows self-correction behavior?

Question#5: **Points: 30**

A serial leading-1s detector is to be designed. A binary integer of arbitrary length is presented to the serial leading-1s detector, most significant bit first, on input $\boldsymbol{X}$. As long as the bits applied to $\boldsymbol{X}$ are $\mathbf{0}$, $\boldsymbol{Z} = \mathbf{0}$. When the first $\mathbf{1}$ is applied to $\boldsymbol{X}$, $\boldsymbol{Z} = \mathbf{1}$. For all bit values applied to $\boldsymbol{X}$ after the first $\mathbf{1}$ is applied, $\boldsymbol{Z} = \mathbf{0}$. To indicate that the sequence is complete and that the circuit is to be initialized to receive another sequence, input $\boldsymbol{Y}$ becomes $\mathbf{1}$. Otherwise, $\boldsymbol{Y}$ is $\mathbf{0}$.

a) Find the state diagram and state table for the required circuit.
b) State that whether the model is Mealy or Moore.
c) Find an implementation of the circuit using positive edge triggered D flip flops and logic gates.

Question#6: **Points: 30**

A Universal Serial Bus (USB) communication link requires a circuit that produces the sequence **00000001**. You are required to design a circuit that starts producing this sequence if the input $\boldsymbol{E} = \mathbf{1}$. If $\boldsymbol{E} = \mathbf{0}$, the output remains constant at $\mathbf{1}$.

Once the sequence starts, it does not see input **E** until the sequence is complete. When the sequence completes, it will see the input **E**.

a) Find the state diagram and state table for the required circuit.
b) State that whether the model is Mealy or Moore.
c) Find an implementation of the circuit using positive edge triggered D flip flops and logic gates.