National University of Computer and Emerging Sciences, Lahore Campus

Course Name:	Digital Logic Design	Course Code:	EE227
Program:	BCS & BDS	Semester:	Spring 2022
Duration:	30 Minutes	Total Marks:	20
Paper Date:	23-June, 2022	Weight	
Section:	ALL	Page(s):	3
Exam Type:	Final Part I Objective		

Name: M. ASAD TARIQ Roll No. 21L-5266 Section: BCS-2F

Instruction/Notes:
- *This part consists of 20 questions only.*
- *Attempt all questions on THIS PAPER.*
- *In MCQs, encircle the correct option, no cutting or overwriting is allowed!*
- *Once done, hand over this part to the invigilator.*
- *Make sure you have written your Roll No, Name and Section on Top.*
- ***Use of calculator is not allowed.***

20

(i) $(600)_{10} = (1130)_8$

512	1
64	6
8	3
600	

$(001\ 001\ 011\ 000)_2$
$(1\ 1\ 3\ 0)_8$

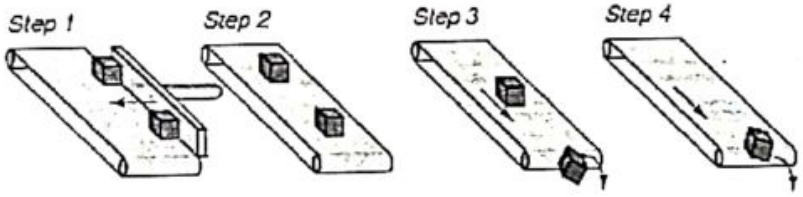
(ii) $(400)_8 + (9A)_{16} = (410)_{10}$

$4 \times 8^2 \quad 9 \times 16^1 + 10$
$256 \quad 154$

(iii) How many different numbers can a 5-bit binary word represent?

$2^5 = 32$.

(iv) A helpful analogy for a shift register is a *conveyor belt*. Examine this illustration showing a single conveyor belt at four different times, and determine which of the following shift register operations the sequence represents:



a) Parallel-in, serial-out
b) Parallel-in, parallel-out
c) Serial-in, serial-out
d) Serial-in, parallel-out

(v) What will be 8-bit binary representation of binary number 1110 having parity at most significant bit, following Even Parity?

10001110.

* Q.6. is MISSING from paper, so there are only 19 Question

(vii) Given the numbers $(1000100)_2$, $(1000003)_8$, $(1000002)_{10}$, $(1000001)_{16}$, which of the following is true?

A. They all have the same value
B. $(1000002)_{10}$ is the smallest
C. $(1000001)_{16}$ is the biggest
D. None of above
E. All of above

(viii) Which of the following describes the operation of a positive edge-triggered JK-type flip-flop?

A. If both inputs are HIGH, the output will flip.
B. The output will follow the input on 1 to 0 transition of clock.
C. When both inputs are LOW, an invalid state exists.
D. None of above

(ix) What are the contents of the circular shift left register (assume initially 1010 stored). Assume 3 clock pulses are used.

A. 0101 B. 1111 C. 0111 D. None of above

(x) Circuits that employs memory elements in addition to gates is called

A. Combinational circuit
B. Sequential circuit
C. Combinational sequence
D. Logic circuit

(xi) Dual and complement of the Boolean expression is same for:

A. X + Y + Z B. XY + Z' C. X'Y'Z' D. None of above

(xii) The main difference between latch and Flip flop (FF) is

A. FF stores more bits
B. Only 1 value of FF is changed in 1 clock cycle
C. Latch and FF are same
D. Both A & B
E. None of above

(xiii) The output of an XOR gate is zero (0) when _____ I) All the inputs are zero II) Any of the inputs is zero Any of the inputs is one IV) All the inputs are one

A. I only B. IV only C. I and IV D. II and III

(xiv) Parallel load transfer is done in:

A. 1 cycle
B. 2 cycles
C. 3 cycles
D. 4 cycles

(xv) Six bits are being used to save a number in signed 2s complement form. The range of this number will be from

$(-32)_{10}$ to $(31)_{10}$ $\quad -2^{6-1} \rightarrow 2^{6-1}-1$

(xvi) BCD to 7-Segment is a

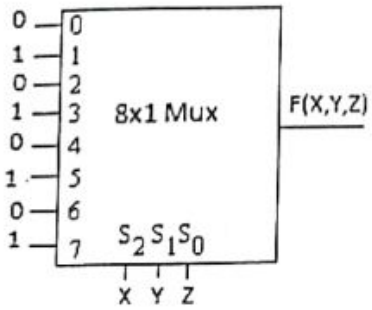
A. MUX B. Encoder C. Decoder D. All of these E. None

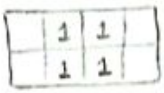
(xvii) If $F = \sum m(0, 1, 5, 6)$, then $F = \prod M(2,3,4,7)$ — assuming 3 input variables

(xviii) An 8-line to 1-line multiplexer is connected as shown, where output is F(X, Y, Z) and Z is the least significant input. Which of the following functions does F generate?

A. F(X,Y,Z) = Z'
C. F (X,Y,Z) = Z
E. None of above

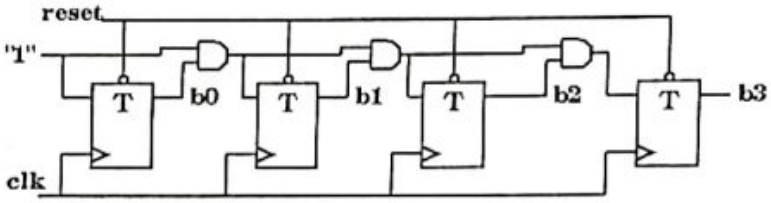
B. F(X,Y,Z) = Y
D. F(X,Y,Z) = Y+X





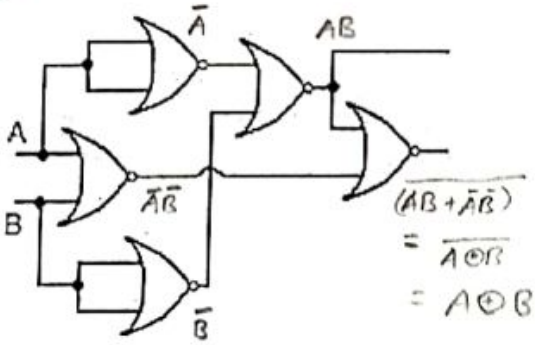
(xix) The sequential logic circuit shown below represents most closely the basic architecture of a:

A. Data-latch register
B. Ripple counter
C. Synchronous counter
D. Shift register
E. None



(xx) Identify the logic function performed by the circuit shown in the given figure:

A. 1-bit comparator
B. Full adder
C. Half adder
D. None of the above



(Carry)

National University of Computer and Emerging Sciences, Lahore Campus

Course Name:	Digital Logic Design	Course Code:	EE227
Program:	BCS & BDS	Semester:	Spring 2022
Duration:	150 Minutes	Total Marks:	80
Paper Date:	23-June-22	Weight	40%
Section:	ALL	Page(s):	9
Exam Type:	Final		

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Instruction/Notes:
1. *Attempt all the questions on **this** answer booklet. **You can do your scratch work on rough sheets but they will not be collected and marked.***
2. ***Properly label** all blocks and inputs/outputs to get credit.*
3. ***Provide only "one" final solution in the given space**. Otherwise, both solutions will be cancelled and no mark will be given. .*

Question # 1: (10) **[Marks: 10]**

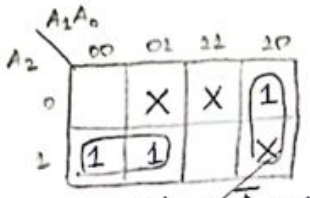
a) Design and implement a sequential circuit which counts the following sequence using D flip flops:

0, 2, 4, 5, 7, 0 and repeat

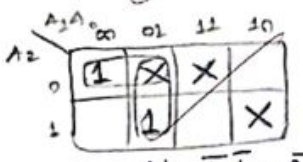
State Table and State Diagram

m	P.S. $A_2(t)$	P.S. $A_1(t)$	P.S. $A_0(t)$	N.S. A_2^+	N.S. A_1^+	N.S. A_0^+
0	0	0	0	0	1	0
1	0	0	1	X (0)	X (1)	X (0)
2	0	1	0	1	0	0
3	0	1	1	X (0)	X (0)	X (0)
4	1	0	0	1	0	1
5	1	0	1	1	1	1
6	1	1	0	X (1)	X (0)	X (0)
7	1	1	1	0	0	0

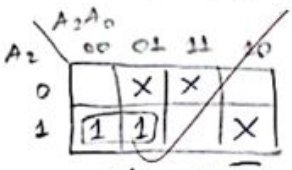
0 — 000
2 — 010
4 — 100
5 — 101
7 — 111



$A_2^+ = A_2\bar{A}_1 + A_1\bar{A}_0$



$A_1^+ = \bar{A}_2\bar{A}_1 + \bar{A}_1A_0$



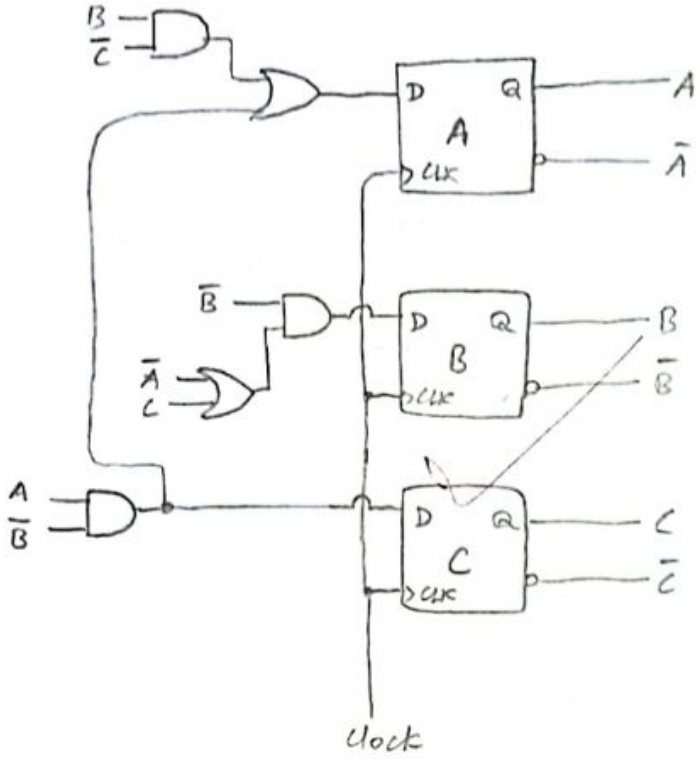
$A_0^+ = A_2\bar{A}_1$

Let $A = A_2$, $B = A_1$ & $C = A_0$ for easier reference:

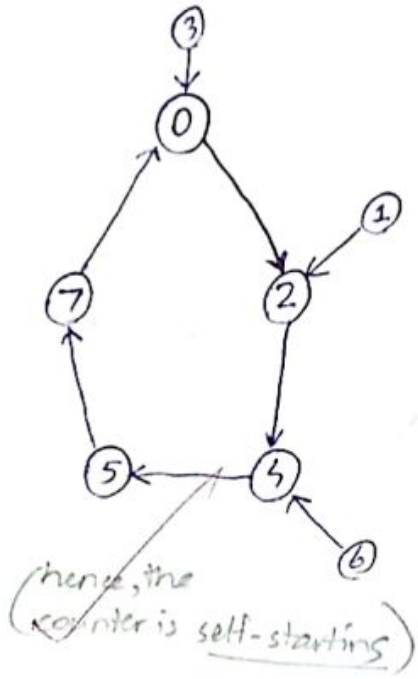
$A^+ = A\bar{B} + B\bar{C}$, $B^+ = \bar{A}B + \bar{B}C$, $C^+ = A\bar{B}$

$= \bar{B}(\bar{A} + C)$

Circuit Diagram:



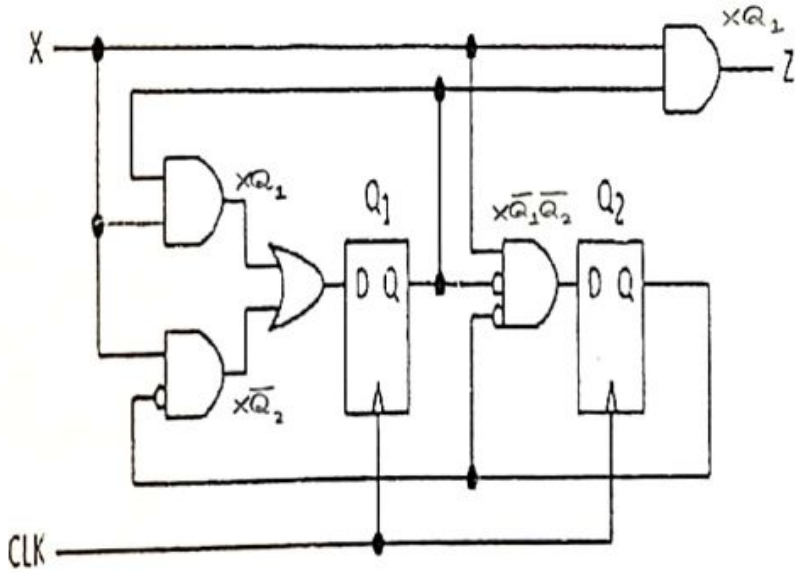
State Diagram:



Question # 2: 15 **[Marks: 15]**

Analyze the following circuit to derive the **equations, state table** and the **state diagram** of the sequential circuit shown below.

Note: Show complete solution of state table, equations, state diagrams to get full credit.



Equations

$Q_1(t+1) = D_1 = XQ_1 + X\bar{Q}_2$

$Q_2(t+1) = D_2 = X\bar{Q}_1\bar{Q}_2$

$Z = XQ_1$

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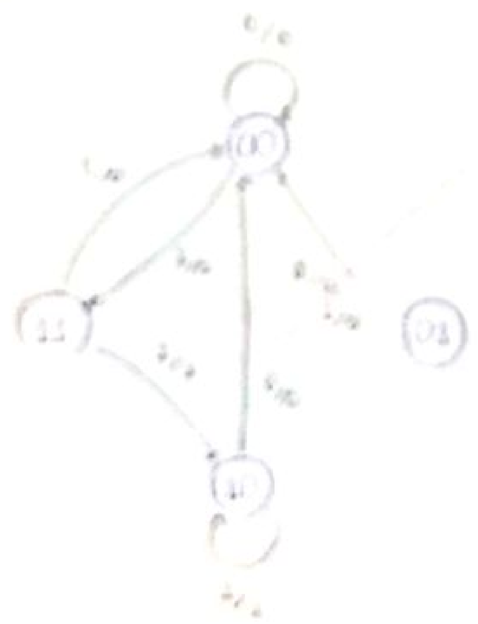
State Table and State Diagram

$Q_0(t)$	$Q_1(t)$	X	$Q_0(t+1)$	$Q_1(t+1)$	Z
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	0	0	0
1	1	1	1	0	1

State Diagram



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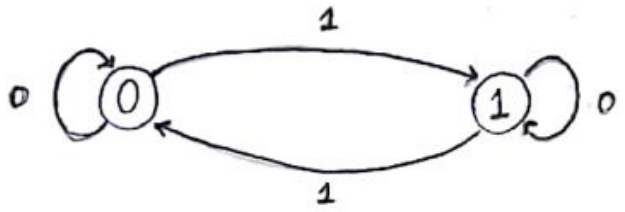
10 [15 Marks]

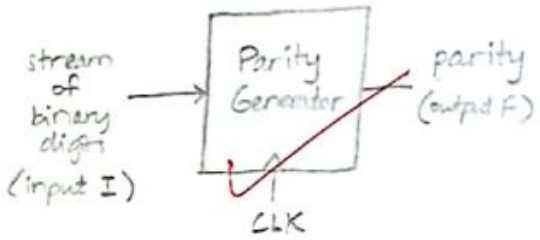
Question # 3:

A synchronous sequential circuit is to be designed for generating the parity of a continuous stream of binary digits. The output of the circuit produces a logic "1" if the number of 1's received at the input is even. The output is "0" otherwise. Implement the circuit using D flip-flops as memory elements.

State Diagram:



Level-0 Diagram



If the number of 1's received at the input is even, then the state of the circuit stays at 0 until a new 1 arrives. When another 1 arrives, it changes to 0.

Then it stays at 0 unless a 1 arrives again, in which case it changes to 1 again and so on.

Note: The current state of the D-flip/flop (which is 1 for even and 0 for odd number of 1's) will be given out as output F so we don't need to consider the external output F separately during the design:

State Table:

P.S. Q(t)	i/p I	N.S. Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Equation:

$$Q(t+1) = Q(t) \oplus I$$

(no need for K-map as obvious from table)

It is known that for D flip/flops:

$$D = Q(t+1)$$

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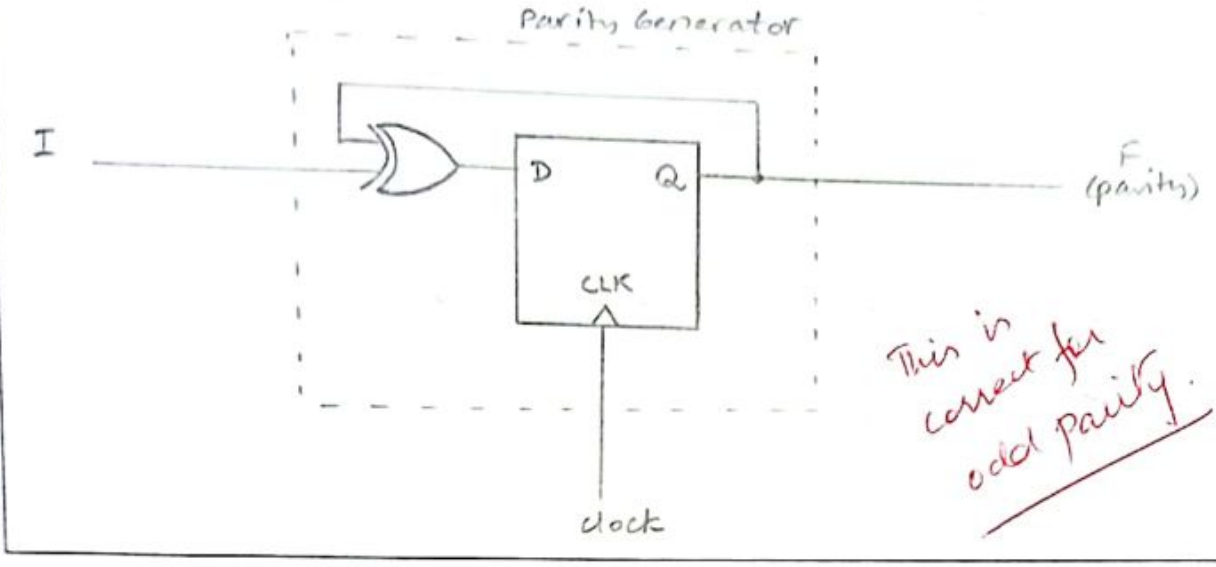
Circuit Diagram:



Question # 4: 20/ **[Marks: 20]**

Design and implement a sequential circuit that receives a continuous stream of BCD input digits and counts the frequency of digit 6 (binary 0110) received at its input. e.g., if the input BCD stream is 4326590662618, then the count is 4 (binary 0100) because there are four 6's in this stream. In the input stream, digit 6 can appear up to five times. (101)

Note: the BCD numbers are arriving serially; so, every BCD digit takes four clock cycles to arrive.

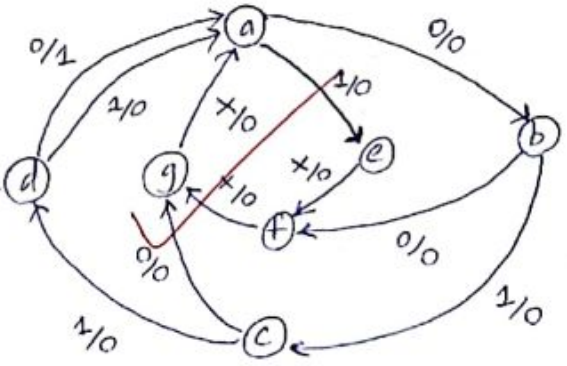
We can divide this circuit into two parts. One is a non-overlapping sequence recogniser which sends a signal to the second component if 0110 is found in the sequence (without overlap). The second component is a counter which increments upon receiving the signal.

For the seq. recogniser;

(the inner loop is there in case there is a mismatch so that the circuit waits for the next BCD to arrive)

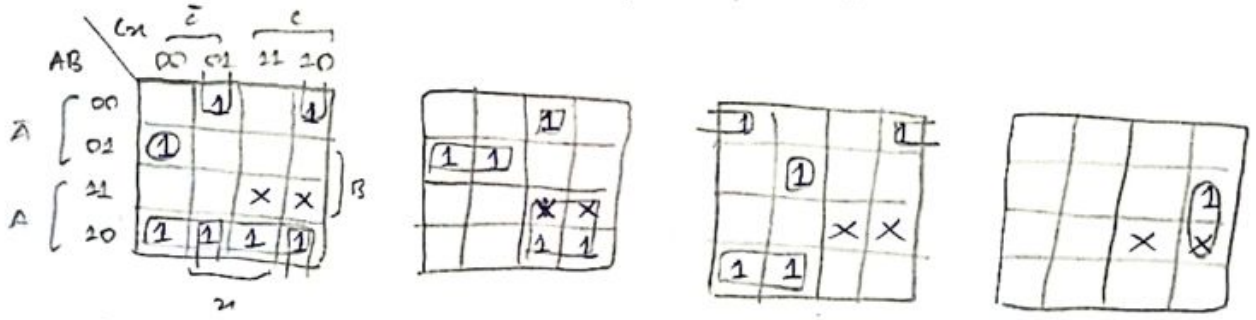
State Diagram

Let
a = 000
b = 001
c = 010
d = 011
e = 100
f = 101
g = 110
(remaining)



Let input be x, and output (signal to counter) be z.

P.S. A(t)	P.S. B(t)	P.S. C(t)	i/p x	N.S. A^+	N.S. B^+	N.S. C^+	o/p z
0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	0
0	0	1	0	1	0	1	0
0	0	1	1	0	1	0	0
0	1	0	0	1	1	0	0
0	1	0	1	0	1	1	0
0	1	1	0	0	0	0	1
0	1	1	1	0	0	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	0	0
1	1	1	0	x	x	x	0
1	1	1	1	x	x	x	0



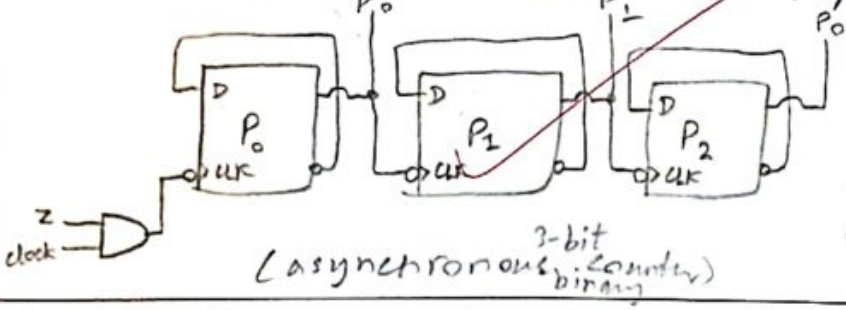
$A^+ = A\bar{B} + \bar{B}Cx + B\bar{C}\bar{x} + \bar{A}B\bar{C}\bar{x}$

$B^+ = AC + \bar{A}B\bar{C} + A\bar{B}Cx$

$C^+ = \bar{A}\bar{B}\bar{x} + AB\bar{C} + \bar{A}B\bar{C}x$

$Z = BC\bar{x}$

As for the counter, it is a 3-bit counter (because max count = 5 - 101 (3-bit)).
For instance, an implementation using D flip/flops could be:



(asynchronous 3-bit counter)

$P_2P_1P_0$ will be the frequency count

the counter will increment only when z will allow the clock pulse to reach it

(CONTINUED ON PAGE 9)

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Question # 5:

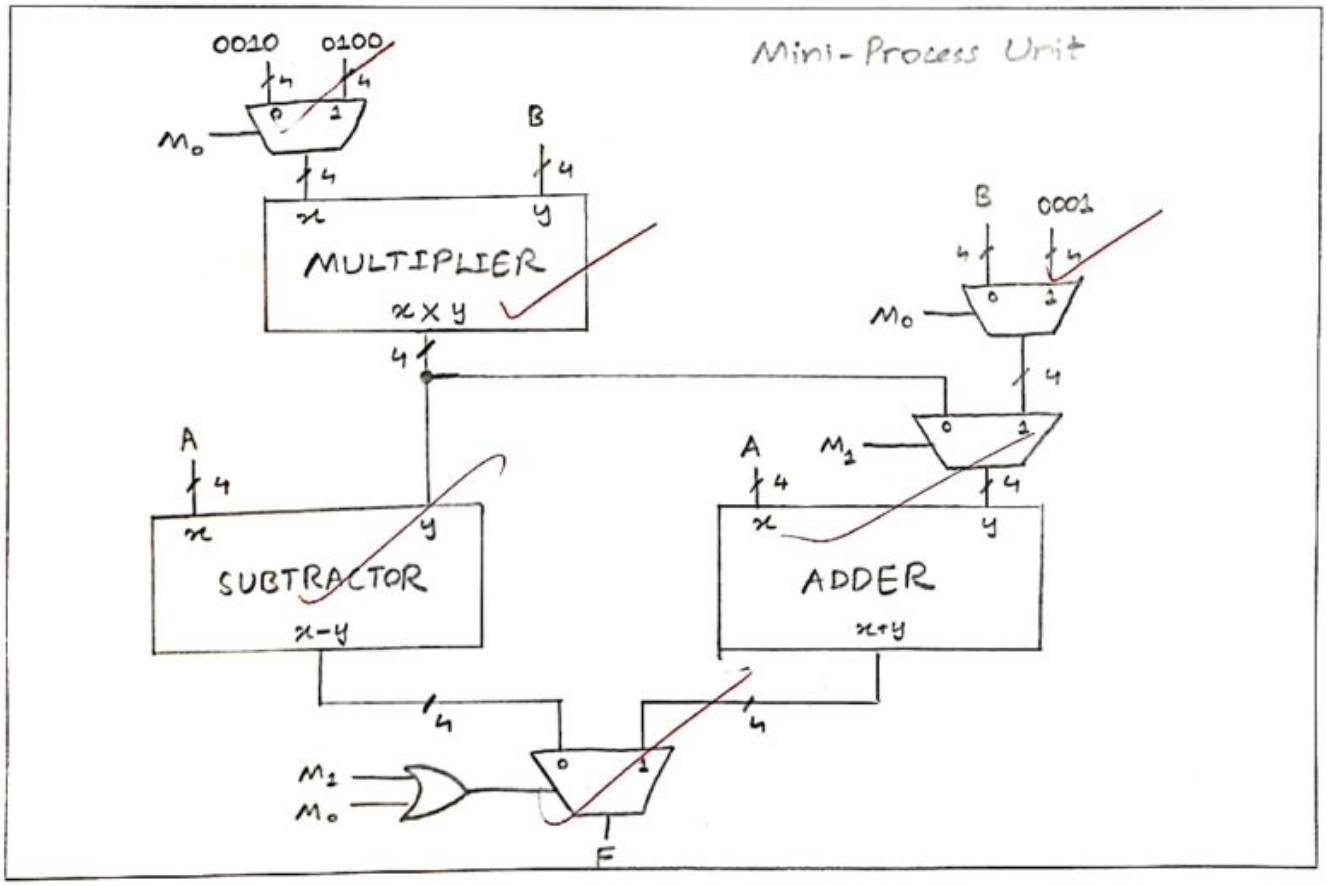
20 **[Marks: 20]**

Design a 4-bit mini-Process Unit that works according to the given functionality:

M_1	M_0	F(A,B) = Operation	Function Description
0	0	A – 2*B	Subtract 2 times B from A
0	1	A + 4*B	Add 4 times B to A
1	0	A + B	Add A and B
1	1	A + 1	Increment A

Where A and B are two 4-bit numbers. M inputs to your mini processor are control inputs. **Your task is to add required logic in the design given below in order to make mini-processor fully functional.**

Note: Assume that you already have Adder, Subtractor, Decoder(s), Encoder(s), MUX(s), DMUX(s) and Multiplier(s) blocks available. **Properly label all blocks and inputs/outputs to get full credit.**



Components used: 1 Adder, 1 Subtractor, 1 Multiplier,
↳ Quad 4-bit 2×1 MUX(s), 1 OR gate

Note: It is assumed that the results of addition/subtraction/multiplication do not overflow. If that is the case, then we can either show an overflow/carry/negative etc. flag, or we can use adders and subtractors that can deal with larger no. of bits.

or turn out to be invalid in any way

Question 4 continued:

So, the overall circuit implementation will be:

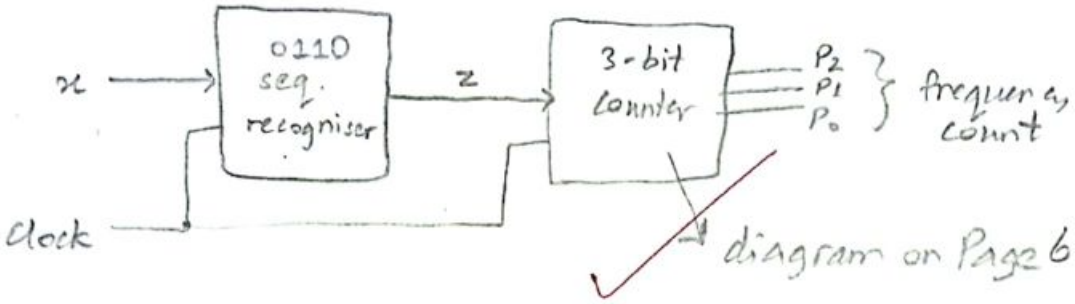


diagram on Page 6

Diagram of Seq. Recogniser: