EE227 - Digital Logic Design
Spring 2018

Credit Hours: 3 **Pre-Requisite:** None

Course Instructor: Omer Ali **Email:** ali.omer@nu.edu.pk
Folder: \\Xeon\fall2018\DLD (A) **Office Hours:** TBA

Objectives:
Upon completion of the course students will:
- Understand different Number systems & Boolean Algebra
- Design combinational and sequential circuits
- Understand the internal working of different components of a digital computer
- Design moderately complex sequential digital circuits using techniques studied in this course
- Be able to undertake Computer Architecture course in future

Important Instructions:
- According to the university policy:
  - You have to secure at least 50% marks to pass the course.
  - For 'A' grade the student must secure at least 80% marks in the course.
- Plagiarism is not tolerable in any of its form; minimum penalty would be an 'F' grade in the course without prior warning.
- You bear all responsibility for protecting your assignments. If anyone else submits your assignment, you will be considered equally responsible.

Text Book:
M. Morris Mano & Charles R. Kime, *Logic and Computer Design Fundamentals* (4th Edition Updated, Prentice Hall)

Reference Books:
- John F. Wakerly, *Digital Design: Principles and Practices* (3rd Edition, Pearson Education, 2001)
- Thomas L. Floyd, Digital Fundamentals (7th Edition, Prentice Hall, 2000)

Syllabus and Schedule:

Topics	Text	# of Lectures
DIGITAL SYSTEMS AND INFORMATION • Digital computers and Binary Numbers • Other base numbers (base-8, base-16 etc.) • Number base conversions	**Chapter 1**	**3**
COMBINATIONAL LOGIC CIRCUITS • Binary Logic and Introduction to Logic Gates • Timing Diagrams • Introduction to Boolean Algebra • Standard forms • Positive and Negative Logic • Boolean Functions and their implementation • Canonical and Standard Forms (Minterms, Maxterms, Conversions) • Minimization of Boolean functions using K-Map • Don't Care States • Universal gates and implementation of Boolean functions using universal gates	**Chapter 2**	**6**
COMBINATIONAL LOGIC DESIGN • Combinational Circuits • Analysis Procedure • Design Procedure	**Chapter 3**	**1**
Midterm I		
COMBINATIONAL LOGIC DESIGN (Continued) • Decoders • Encoders	**Chapter 3**	**4**

• Multiplexers • Demultiplexer		
ARITHMETIC FUNCTIONS AND HDLs • Binary Adders (Half Adder, Full Adders, Binary Ripple Carry Adder, Carry Look ahead Carry Adder) • Binary Subtractor • Binary Adder/Subtractor • Binary Multipliers • Code Conversion • Magnitude Comparator • Parity Generators/ Checkers • Design Applications • 1's and 2's Complements • Unsigned and Signed numbers and Arithmetic operations (Addition, subtraction, Multiplication and Division)	**Chapter 4**	**2**
SEQUENTIAL CIRCUITS • Introduction to Sequential Circuits • Introduction to Latches • Introduction to Flip Flops • Type of Flip Flops • Analysis of Sequential Circuits • Design Procedures • Introduction to develop state diagram and state table • State reduction excitation tables	**Chapter 5**	**5**
Midterm II		
REGISTERS AND REGISTER TRANSFERS • Registers • Counters • Synchronous/Asynchronous • Shift Registers • Serial Shift Registers • Loading Registers • Parallel Registers • Ripple Counters • Synchronous Binary Counters • Other Counters	**Chapter 7**	**4**
MEMORY BASICS • Read-Only Memories • Programmable Logic Array Devices • Random Access Memory • Static and Dynamic RAM • Array of RAM ICs • Memory construction using RAM Integrated Circuits	**Chapter 8**	**2**
A/D & D/A Converters (optional)	*	**1**
Final Exam		

* Material not in the text book will be provided to you in the class.

Evaluation Criteria:

Assignments + project	15%
Quizzes	15%
Midterm(2)	30%
Final	40%