National University of Computer & Emerging Sciences, Lahore
Department of Electrical Engineering (Spring 2024)

EE1005 – Digital Logic Design (BCS-2E, BCS-2F, BDS-2A)

Assignment#2

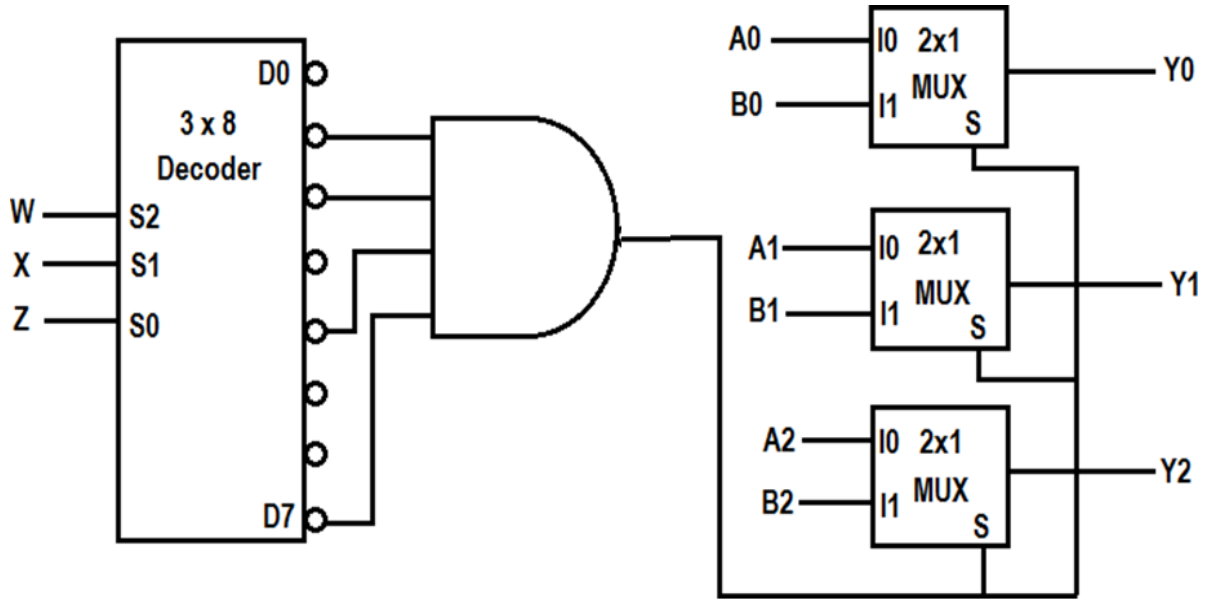
CLO-04

Due Date: April 4, 2024

Total Marks: 160

Question#1: **[Marks: 10]**

Find the truth table for the outputs Y0, Y1, and Y2.



Question#2: **[Marks: 20]**

Design a combinational circuit, using **2x1 multiplexers**, that accepts a 3-bit number as input and generates a 2-bit binary number as output that approximates the square root of the input number. For example, if square root is ≥ 2.5, give a result of 3. If the square root is < 2.5 and ≥ 1.5, give a result of 2.

Note: Use minimum additional logic along with 2x1 MUXs.

Question#3: **[Marks: 20]**

Design a combinational circuit that takes 3-bit pattern as input and outputs binary code of bit position of the first '**1**' in the pattern reading from MSB (2^{nd} position) to LSB (0^{th} position). An additional output variable **V** is required along with binary code to indicate that the binary code is valid or not i.e., if the input pattern is '000' then the output **V** should be '0' to indicate that the

binary code is not indicating the bit position of first '1' and we don't care about the binary code if V = 0.

Design the required circuit using dual 4x1 MUXs and minimum additional logic. Available resources along with **dual 4x1 MUXs** are **NOT gates, 2-input (AND, OR, NAND, NOR) gates**.

Question#4: **[Marks: 20]**

a) Design a 32x1 MUX with active low enable using dual 4x1 MUXs with active low enables and 2x1 MUX with low enable. Use minimum extra logic to design the required MUX.

b) Implement following Boolean functions using 16x1 MUX
   i. $F_1(A,B,C,D) = \sum m\ (1,2,5,6,11,12,15)$
   ii. $F_2(A,B,C,D,E) = \sum m\ (1,2,5,6,16,19,20,21,22,23,27,30,31)$

Question#5: **[Marks: 30]**

a) Design a 5x32 decoder using 3x8 and 2x4 decoders with active low enables and active high outputs. Use minimum extra logic to design the required decoder.

b) Add active low enable to 5x32 decoder designed in part (a).

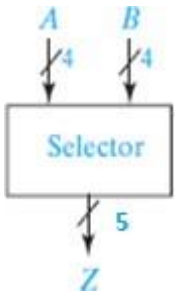
c) Implement following Boolean functions using 5x32 decoder. Use minimum extra logic. Available resources are NOT, AND, OR, NAND, NOR gates. Available input pins for each gate are 3, 6, 8 (except NOT gate).
   i. $F_1(A,B,C,D,E) = \sum m\ (0,\dots,25)$
   ii. $F_2(A,B,C,D,E) = \sum m\ (6,7,8,9,16,24,27,29)$
   iii. $F_2(A,B,C,D,E) = \sum m\ (1,2,6,7,8,20,24,26,28,30)$

Question#6: **[20 marks]**

Design an optimized combinational circuit to perform the arithmetic operation $(3\boldsymbol{x} + 6\,\mathbf{y} + 9)$. Here, $\boldsymbol{x}$ (2-bit) and $\boldsymbol{y}$ (3-bit) are two unsigned numbers. Available resources are **4-bit Adders**, **Full Adders (FA)**, **NOT gates**, **2-input (AND, OR, NAND, NOR) gates**. Show complete working.

Question#7:

The Selector Box below has two 4-bit, unsigned inputs, ***A*** and ***B***. Its output is ***Z*** = ***A***+*2* if ***A*** $\geq$ ***B*** and ***Z*** = ***B***+*2* if $A < B$. **[20 marks]**



Question#8:

Design a logic circuit that performs the following operations on **A** (3-bit number) and B (3-bit number) according to the status of selection bits S_1 and S_0: **[20 marks]**

S_1S_0	Operation	F (Output)
00	Incrementer	**A**+1
01	Tripler	3***A**
10	Multiplier	**A*B**
11	Square	$\mathbf{A}^2$