Roll no. _____ Name:_____

# National University of Computer and Emerging Sciences, Lahore Campus

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|---|---|---|---|---|
| Course: | Digital Logic Design | Course Code: | EE227 |
| Program: | BS(Computer Science) | Semester: | Fall 2018 |
| Duration: | 2 Hours | Total Marks: | 45 |
| Paper Date: | 31st Dec 2018 | Weight | 45% |
| Section: | ALL | Page(s): | 5 |
| Exam: | Final (Subjective) | Roll No. | |
| Name: | | Section: | |

**Instruction/Notes:**

- *Attempt all the questions on this answer booklet. You can use extra sheets for your scratch work but **they will not be collected and marked**.*
- *Make sure you write your roll # on EVERY sheet of the booklet.*
- ***Use of calculator is not allowed.***
- Questions during exam are not allowed. Take reasonable assumptions where needed.
- In your circuits, properly label all blocks and inputs/outputs to get credit.

**Question 1: [5+5 marks]** S_ring_Shifter is a shift register in which; the serial output is connected to the serial input if the serial output is 0, and the serial output is first complemented and then connected to the serial input if it is 1.

(i) Give FF (Flip Flop) level design of the above circuit. Do it for 4-bits.

(ii) List the sequence of states after every tick of 4 bit ring shifter starting from an initial state 0101 till the register get replaced by new values.

**$T_1$ = _____**

**$T_2$ = _____**

**$T_3$ = _____**

**$T_4$ = _____**

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**Question 2 [10 Marks]:** Design a circuit for **Division** that takes an 8-bit binary number X and a 4-bit binary number A, divides X by A and gives quotient and remainder as output. Assume that you already have Decoder(s), Encoder(s), MUX(s), DMUX(s), Adder-Subtractor(s), Multiplier(s), Registers and Counters blocks available. **Properly label all blocks and inputs/outputs to get credit.**

**Hint:** Division can be implemented using other arithmetic operations (addition, subtraction or multiplication)

**Note: Credit will be given on the basis of cost of the circuit.**

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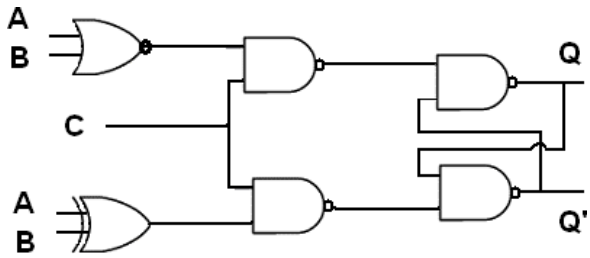
**Question 3 (a) [8 Marks]:** A-B Latch with control input C is shown below. Assume C=1, Fill in the characteristic table for A-B Latch:

**Characteristic Table:**

| Q(t) | A | B | Q(t+1) |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |




**Question 3 (b) [2 Marks]:** Characteristic table of X-Y Flip-Flop is given below. Fill in the excitation table of X-Y Flip-Flip.

**Characteristic Table:**

| X | Y | Q(t+1) |
|---|---|---|
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | Q(t)' |
| 1 | 1 | 1 |

**Excitation Table:**

| Q(t) | Q(t+1) | X | Y |
|---|---|---|---|
| 0 | 0 | | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

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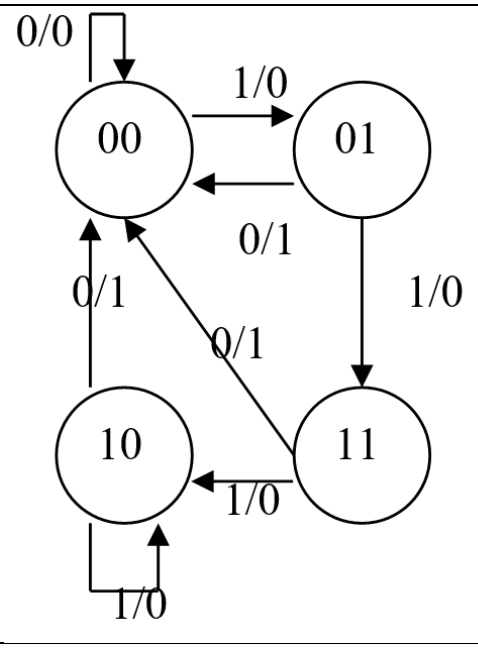
**Question 4. [5+5]** Starting from state 00 in the state diagram shown below, determine the state transitions and output sequence that will be generated when an input sequence of 0101101 is applied.
0/0

State transitions:

Output Sequence:_____




**Question 5[5].** How can a J-K flip flop be converted into a T flip flop? A T-type FF changes its state at every clock pulse if its T-input is '1' and it remains in the present state as long as its T-input is '0'.

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**ROUGH SHEET**