Digital Logic Design

(EE1005)

Date: February 28, 2024

Course Instructor(s)

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Sessional-I Exam

Total Time: 1 Hours

Total Marks: 50

Total Questions: 04

Semester: SP-2024

Campus: Lahore

Dept: Computer Science

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Roll No Section

Student Signature

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CLO#1: Understand different number systems and their conversion.

 $Q#1: (236.25)_7 + (102)_3 = (253.25)$

)7

[10 marks]

6+4= 10-7 = 3

6+9= 10-/= 3

/ 10

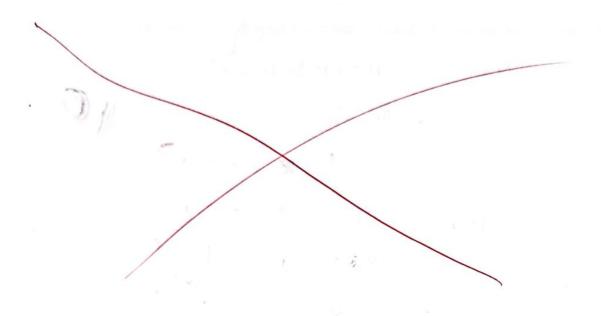
7/11/4 (14)7

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CLO#2: Recognize and use basic gates to implement logic circuits

O#2: Redraw the following logic diagram with the reduced number of gates. Available resources are 2-input (AND, OR, XOR) and NOT gate. $\begin{array}{c}
V = Y \\
V = Y$

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CLO#3: Constructs optimized logic circuit design.

Q#3: A Boolean function is given as follows:

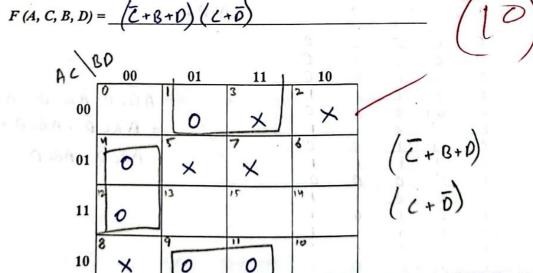
 $F(A, C, B, D) = \prod M(1, 4, 9, 11, 12)$

Don't care: $d(A, C, B, D) = \Sigma m(2, 3, 5, 7, 8)$

(Note: No marks will be given if K-map is not properly filled.)

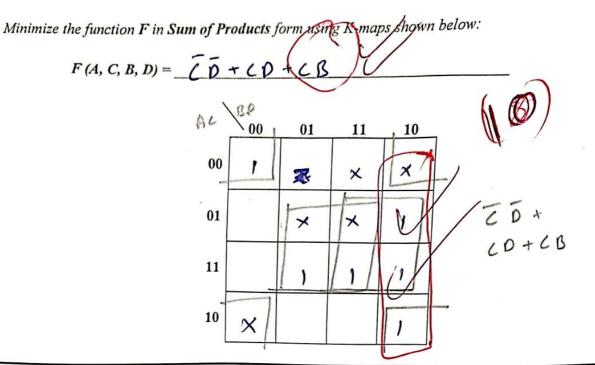
[10+10 marks]

Minimize the function F in Product of Sums form using K-maps-shown below:



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CLO#4: Construct and utilize the basic functional blocks to design combinational circuits

Q#4: A combinational circuit is required to be designed for coordinating a meeting among four parties (A, B, C, and D). The circuit should output 'F=1' if meeting can take place while ensuring that either party A or D must be present, and the meeting can only be scheduled if at least two parties express their willingness to attend. Otherwise, the meeting cannot take place i.e., 'F=0'. You don't need to draw the circuit. Only fill-in the truth table and write down the Boolean expression of function F in Sum of Minterms form (SOP). Do not optimize the expression.

[10 marks]
(Note: The presence and willingness of a party is represented by high logic level)

- 1	Inputs)	Output
A	В	С	D	F
0	0	0	0	0
0	0	0	1	0
0	O	1	0	0
0	0	1	1	1
0	101	0	0	0
0	1	0	1	
0		1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1)	0		1
1))	0	
1	1)	1	

