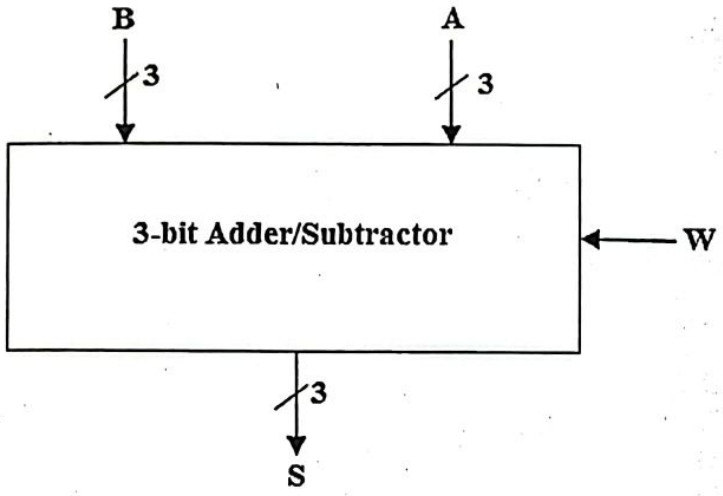
National University of Computer & Emerging Sciences, Lahore
Department of Electrical Engineering (Spring 2024)

EE1005 – Digital Logic Design (BCS-2E)
Quiz#3 (CLO-04)

Total Marks: 10 **Time Allowed: 10 minutes**

Roll #: [redacted]

Question: A **3-bit adder/subtractor** with selection bit **W** is given below. If **W = 0**, then two 3-bit numbers **A** and **B** are added. If **W = 1**, then the two numbers **A** and **B** are subtracted. **A** and **B** are signed numbers and negative numbers are represented in 2's complement form.



Determine the value of **S** and **OV** for the following input values. OV is the overflow flag that is '1' when overflow occurs.

Supposing A+B, A−B

Inputs			Outputs	
W	**A**	**B**	**S**	**OV**
0	010	001	011	0
0	100 (−4)	101 (−3)	001	1
1	011	111	100	1
1	110	111	111	1
0	101	001	100	0

$$\begin{array}{r} 010 \\ +001 \\ \hline 011 \end{array}$$

$$\begin{array}{r} 1100 \\ +1011 \\ \hline 10011 \\ \hline 0011 \end{array}$$

$$\begin{array}{r} 011 \\ -111 \\ \hline 0100 \end{array}$$

$$\begin{array}{r} 101 \\ -001 \\ \hline 100 \end{array}$$

$$\begin{array}{r} 110 \\ -111 \\ \hline 0111 \end{array}$$

$$\begin{array}{r} 011 \\ +001 \\ \hline 100 \end{array}$$

Date: April 23, 2024