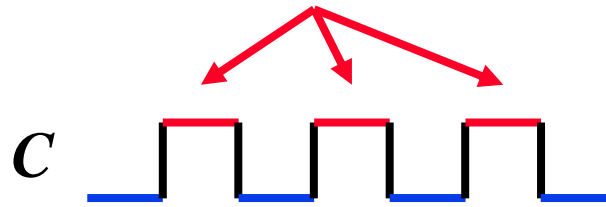# SEQUENTIAL LOGIC

FLIP FLOP
D- FLIP FLOP
JK- FLIP FLOP
T- FLIP FLOP

DIGITAL LOGIC DESIGN

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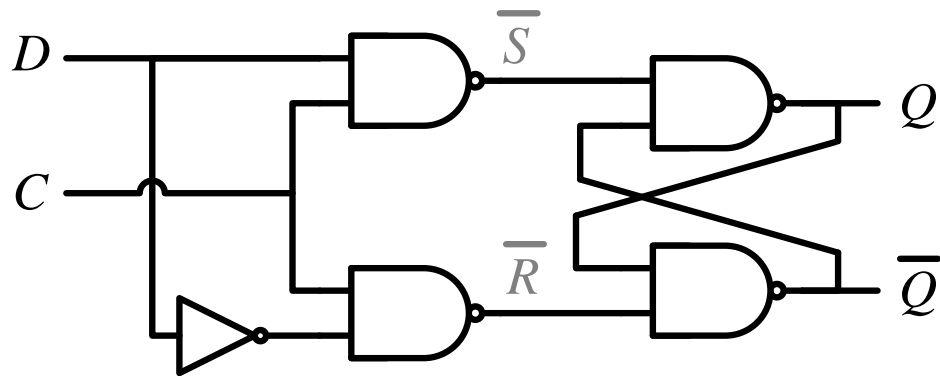# Flip-Flops

★ **Controlled latches are level-triggered**

C

★ **Flip-Flops are edge-triggered**

CLK   *Positive Edge*

CLK   *Negative Edge*

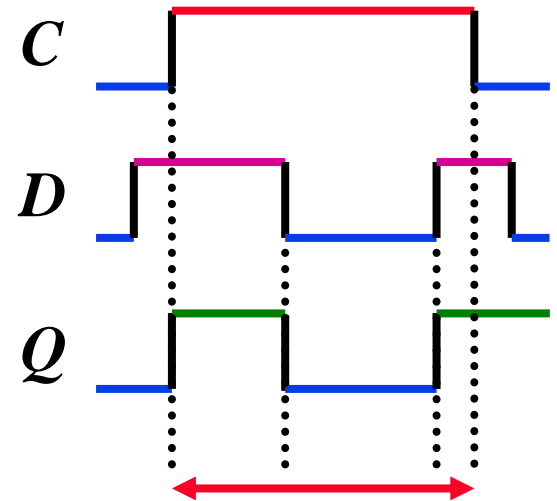# D Latch (D = Data)…..(Repeat)

★ *Flip flop are constructed by combining two D Latches with a clock signal*

Timing Diagram

C D	Q
0 x	Q_0
1 0	**0**
1 1	**1**

No change

Reset

Set

Output may change

Flip-Flops

★ **Master-Slave D Flip-Flop**

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Flip-Flops

★ **Master-Slave *D* Flip-Flop**

Looks like it is negative edge-triggered

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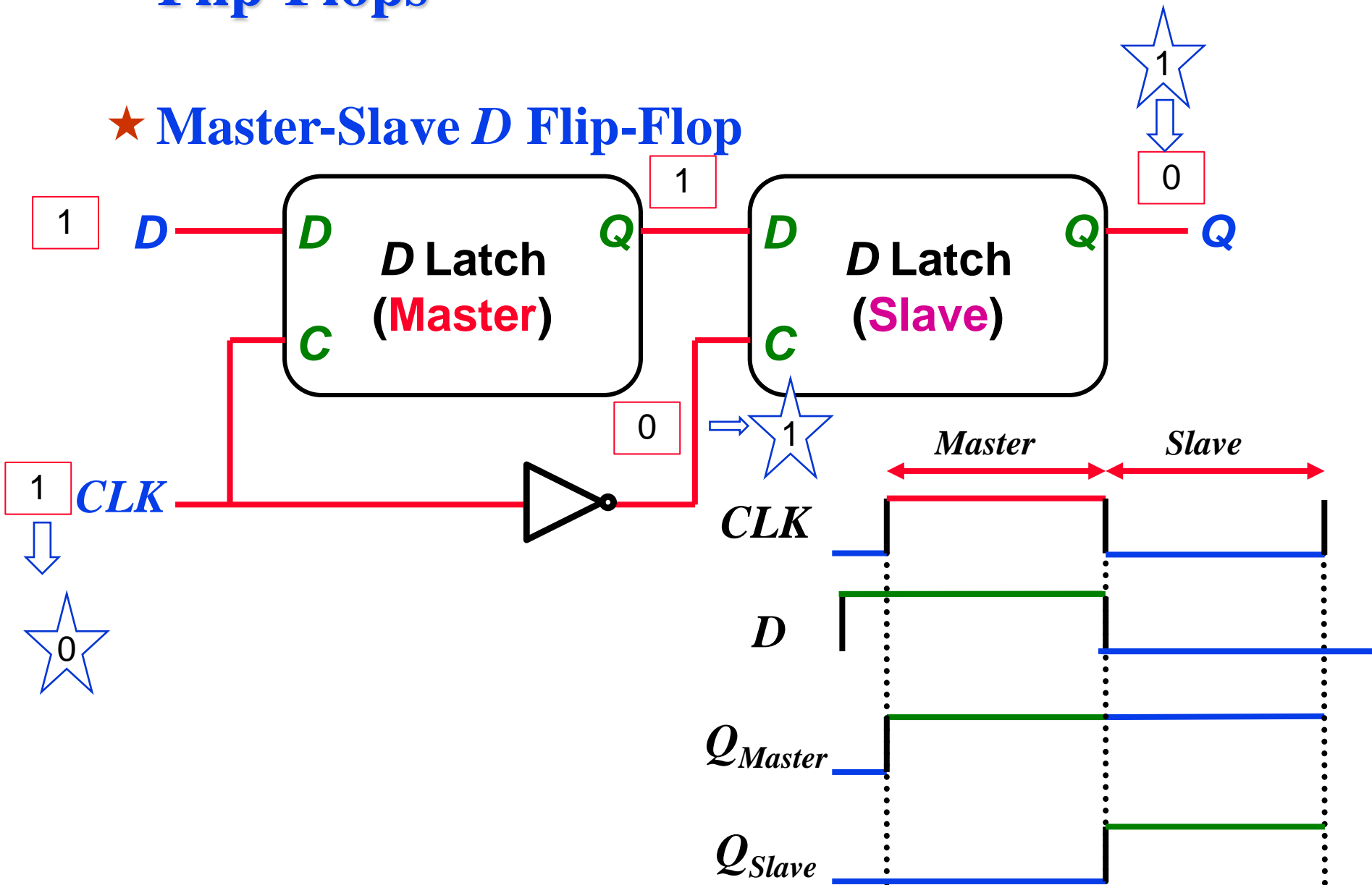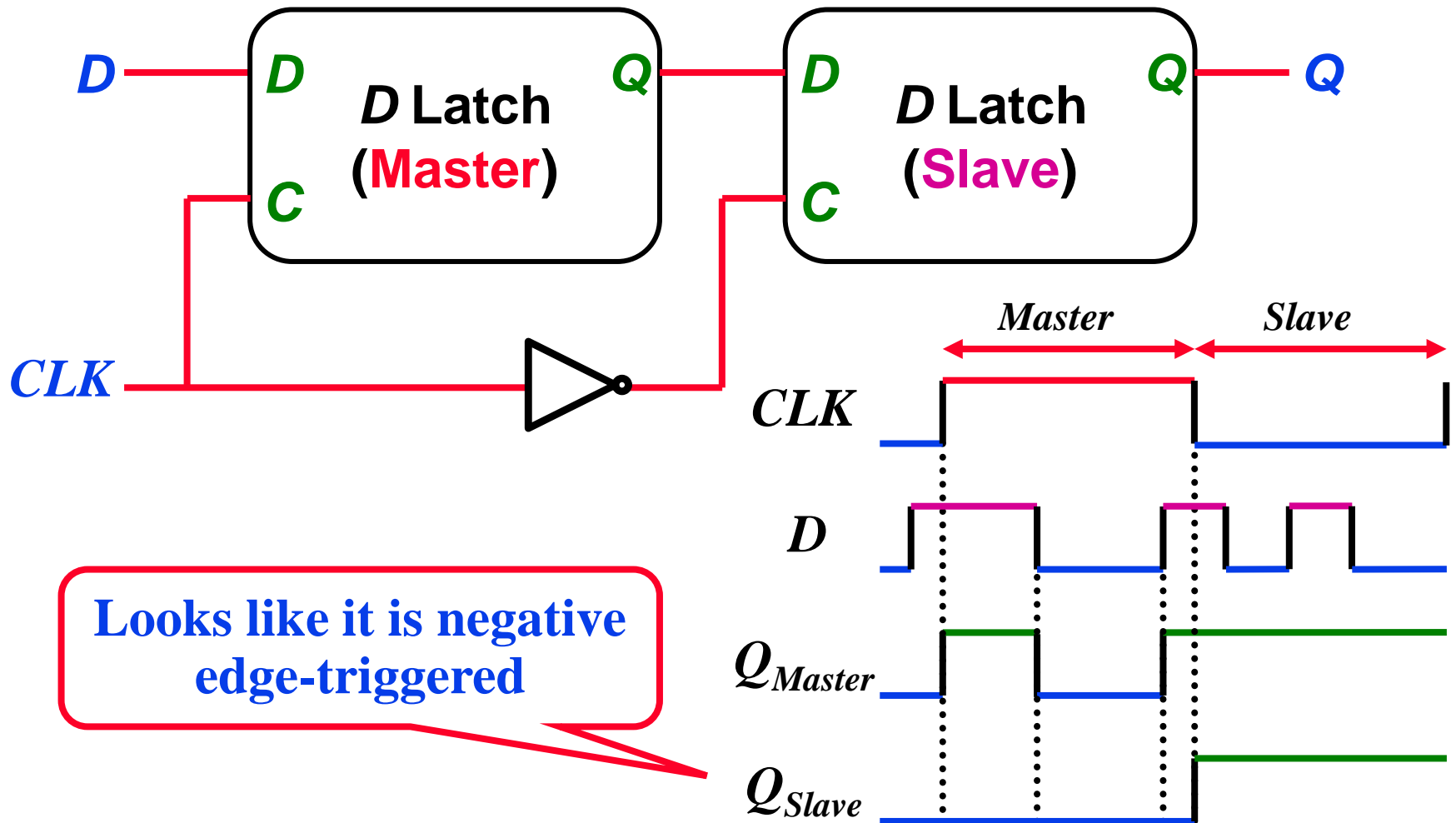
Flip-Flops
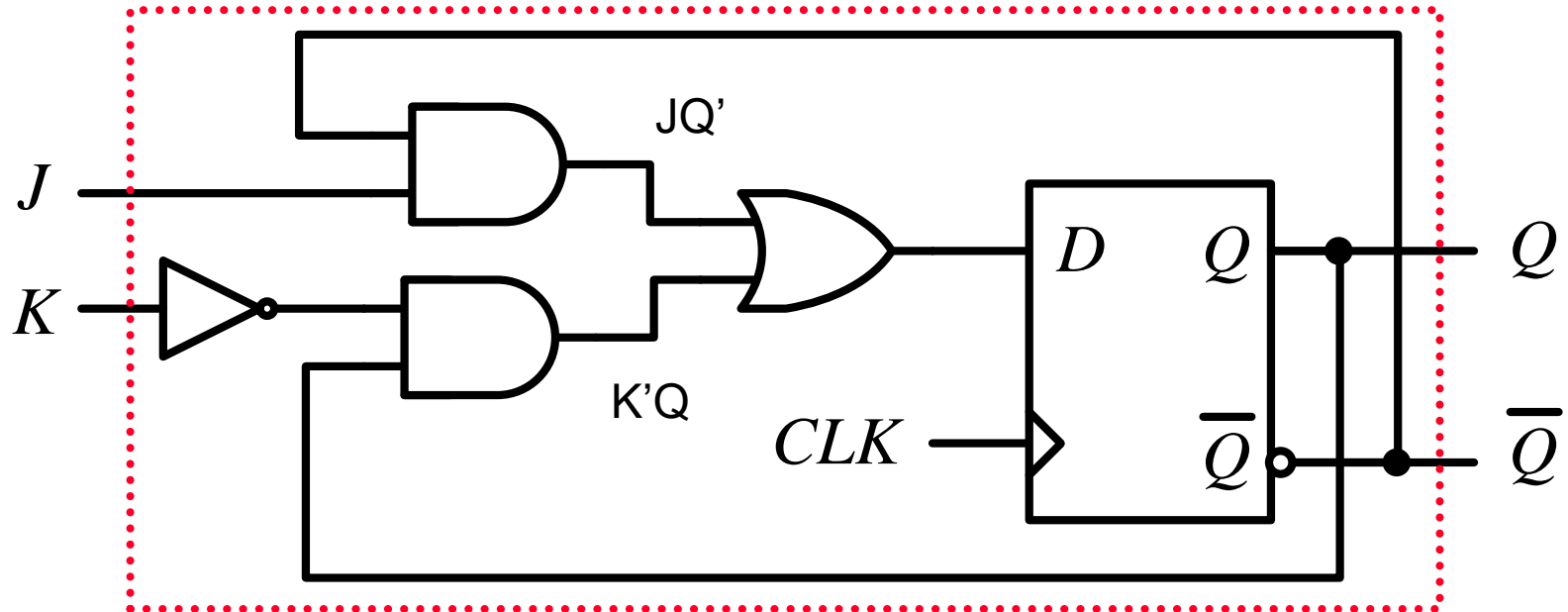
★ *JK* **Flip-Flop**

$$D = Q(t+1) = JQ' + K'Q$$

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

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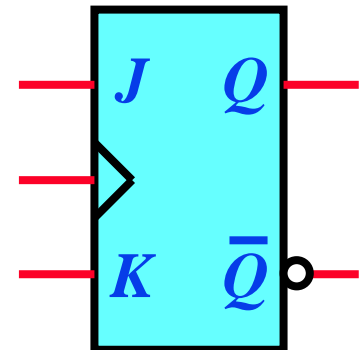
Flip-Flops

★ *T* **Flip-Flop**
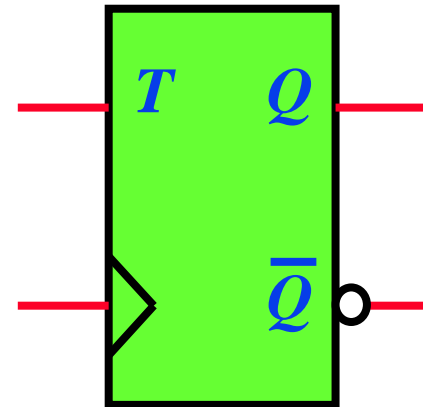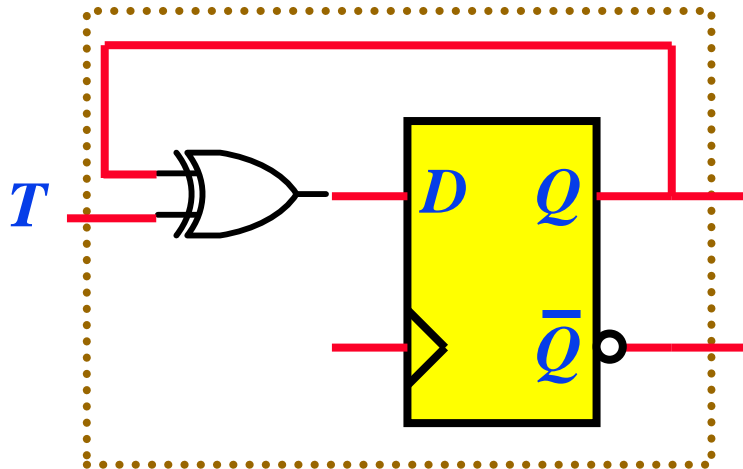
$$D = T \oplus Q$$

T	*Q(t+1)*
0	*Q(t)*
1	*Q'(t)*

Flip-Flop Characteristic Tables
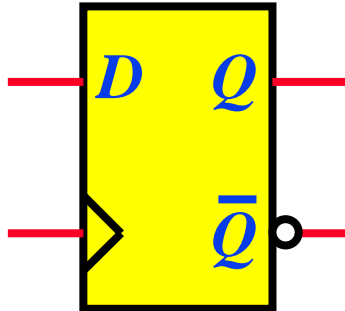
D	Q(t+1)
0	0
1	1

Reset

Set
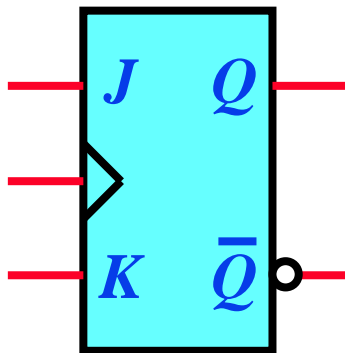
J	K	Q(t+1)
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

No change

Reset

Set

Toggle
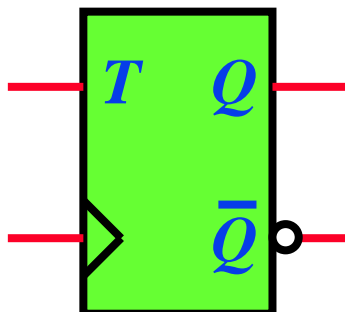
T	Q(t+1)
0	$Q(t)$
1	$Q'(t)$

No change

Toggle

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Flip-Flop Characteristic Equations
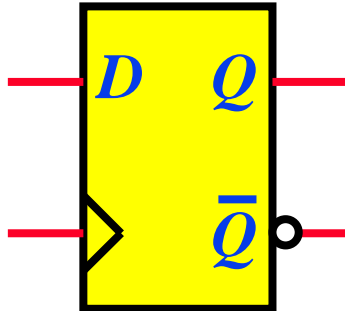
D	Q(t+1)
0	0
1	1

$$Q(t+1) = D$$
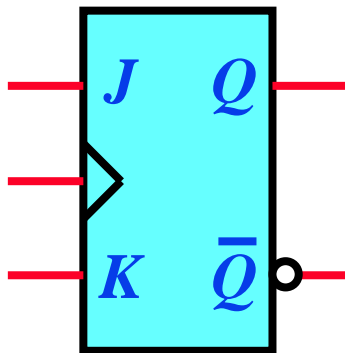
J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

$$Q(t+1) = JQ' + K'Q$$

T	Q(t+1)
0	Q(t)
1	Q'(t)

$$Q(t+1) = T \oplus Q$$

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