

## **EXERIMENT NO:11**

### **Title:-**

DESIGN AND IMPLEMENTATION OF MULTIPLEXER AND DEMULTIPLEXER

### **Objective:-**

To design and implement multiplexer and demultiplexer using verilog

### **Tool Required:-**

- SynaptiCAD Verilogger

### **THEORY:-**

#### **MULTIPLEX**

#### **ER:**

Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally

there are  $2^n$  input line and n selection lines whose bit combination determine which input is selected.

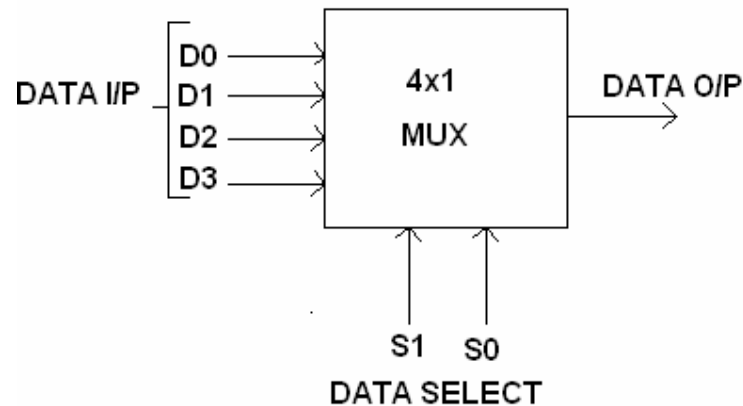
#### **DEMULTIPLEXER:**

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as

demultiplexer.

In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

### BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:

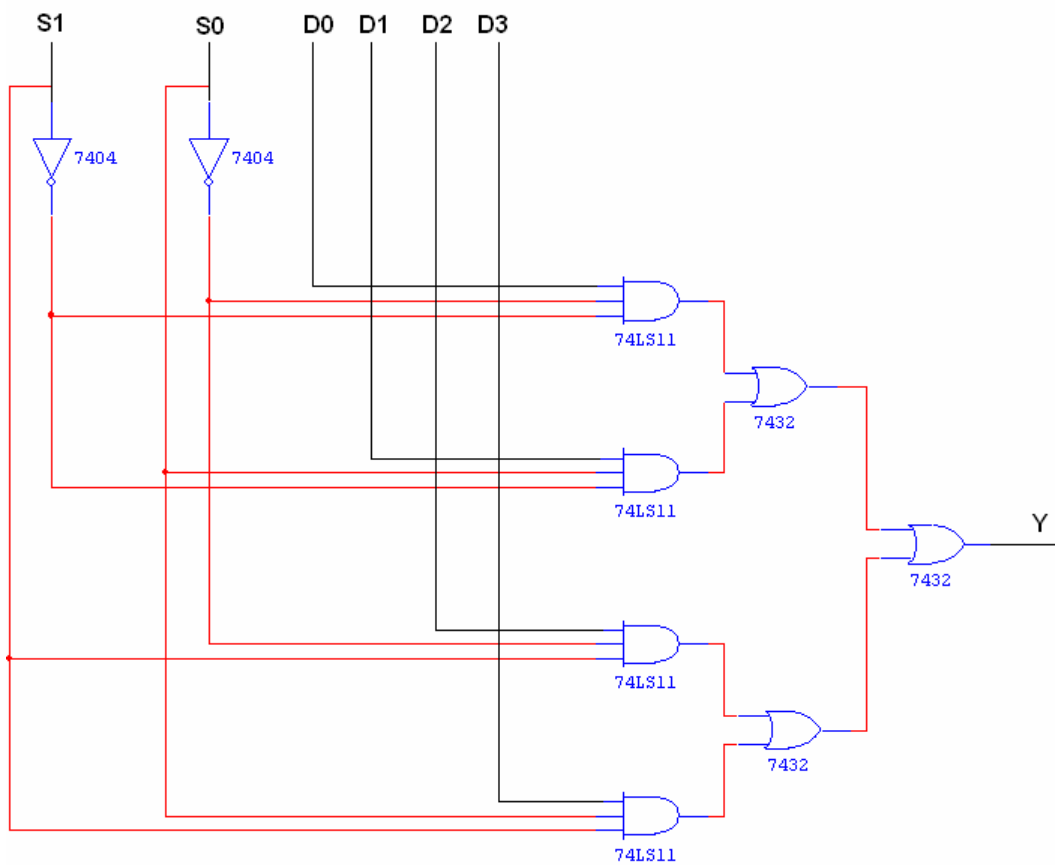


### FUNCTION TABLE:

S1	S0	INPUTS Y
0	0	$D0 \rightarrow D0 S1' S0'$
0	1	$D1 \rightarrow D1 S1' S0$
1	0	$D2 \rightarrow D2 S1 S0'$
1	1	$D3 \rightarrow D3 S1 S0$

$$Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0$$

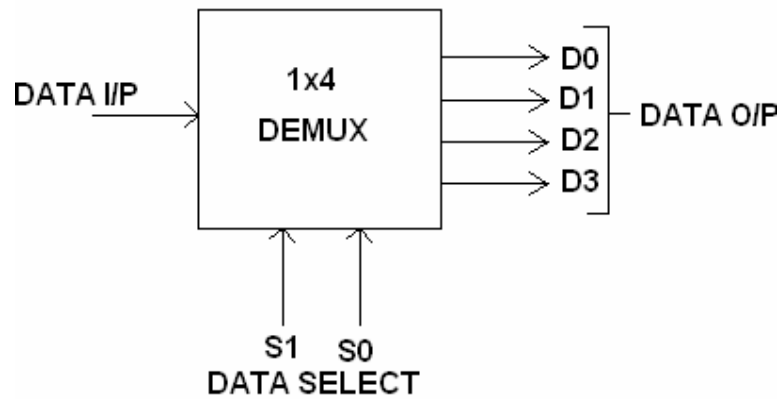
### CIRCUIT DIAGRAM FOR MULTIPLEXER:



### TRUTH TABLE:

S1	S0	Y = OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

### BLOCK DIAGRAM FOR 1:4 DEMULTIPLEXER:

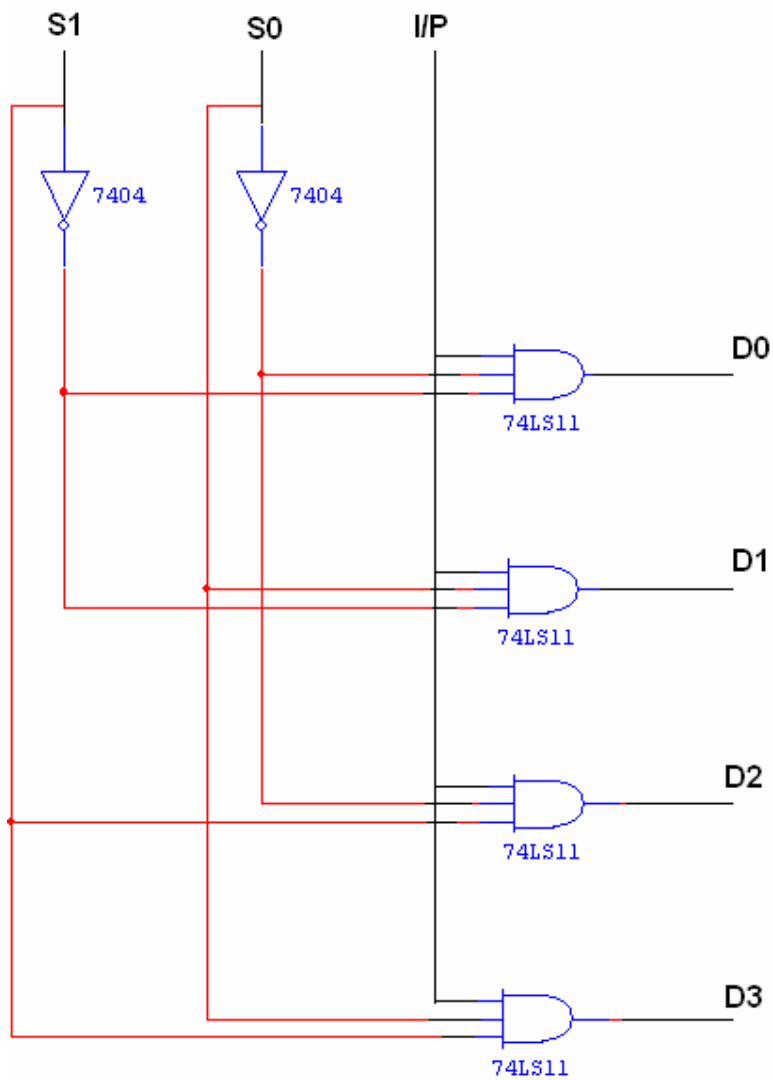


**FUNCTION TABLE:**

S1	S0	INPUT
0	0	$X \rightarrow D0 = X S1' S0'$
0	1	$X \rightarrow D1 = X S1' S0$
1	0	$X \rightarrow D2 = X S1 S0'$
1	1	$X \rightarrow D3 = X S1 S0$

$$Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0$$

**LOGIC DIAGRAM FOR DEMULTIPLEXER:**



**TRUTH TABLE:**

INPUT			OUTPUT			
S1	S0	I/P	D0	D1	D2	D3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0

<b>1</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>
<b>1</b>	<b>1</b>	<b>1</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>1</b>

### **TASKS:**

#### **Implement 1x4 DMUX in Verilog**

- 1.** Attach the screenshot of code and time diagram