



BINARY LOGIC AND LOGIC GATES

Digital logic design

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Binary Logic

■ Definition of Binary Logic

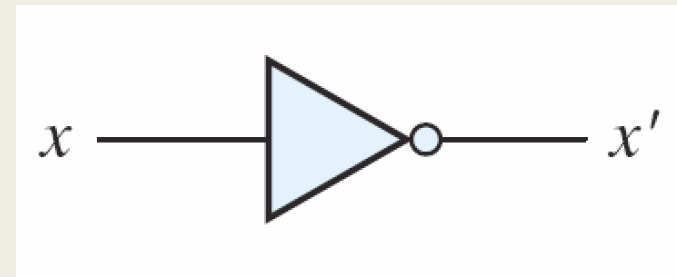
- *Binary logic consists of binary variables and a set of logical operations.*
- *The variables are designated by letters of the alphabet, such as A, B, C, x, y, z, etc, with each variable having two and only two distinct possible values: 1 and 0,*
- *Three basic logical operations: AND, OR, and NOT.*

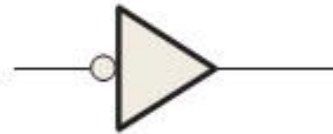
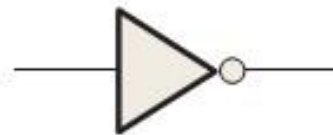
1. AND: This operation is represented by a dot or by the absence of an operator. For example, $x \cdot y = z$ or $xy = z$ is read “x AND y is equal to z,” The logical operation AND is interpreted to mean that $z = 1$ if only $x = 1$ and $y = 1$; otherwise $z = 0$. (Remember that x , y , and z are binary variables and can be equal either to 1 or 0, and nothing else.)
2. OR: This operation is represented by a plus sign. For example, $x + y = z$ is read “x OR y is equal to z,” meaning that $z = 1$ if $x = 1$ or $y = 1$ or if both $x = 1$ and $y = 1$. If both $x = 0$ and $y = 0$, then $z = 0$.
3. NOT: This operation is represented by a prime (sometimes by an overbar). For example, $x' = z$ (or $\bar{x} = z$) is read “not x is equal to z,” meaning that z is what x is not. In other words, if $x = 1$, then $z = 0$, but if $x = 0$, then $z = 1$, The NOT operation is also referred to as the complement operation, since it changes a 1 to 0 and a 0 to 1.

Not Function (NOT Gate)

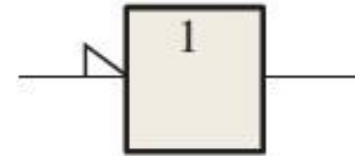
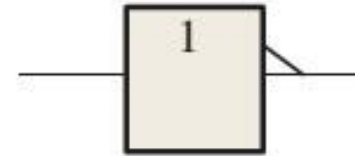
- Complement operation
 - Single input
 - Inverts value of input
 - Symbolized by prime x'
- Truth table
 - Input combinations on the left
 - Output of function on the right
- Graphic symbol
 - NOT gate
 - Little circle indicates inversion

input	output
x	Not x
0	1
1	0

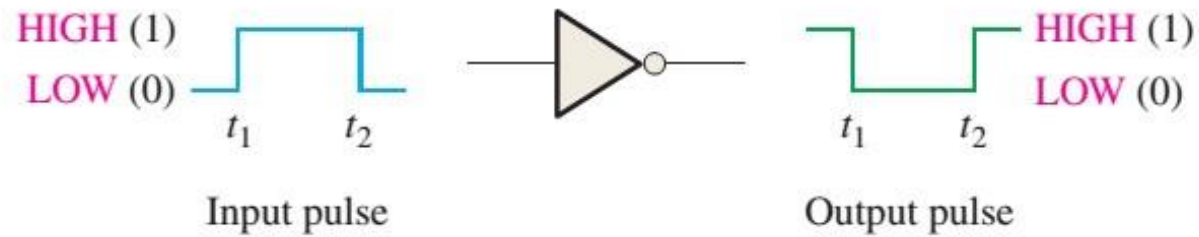




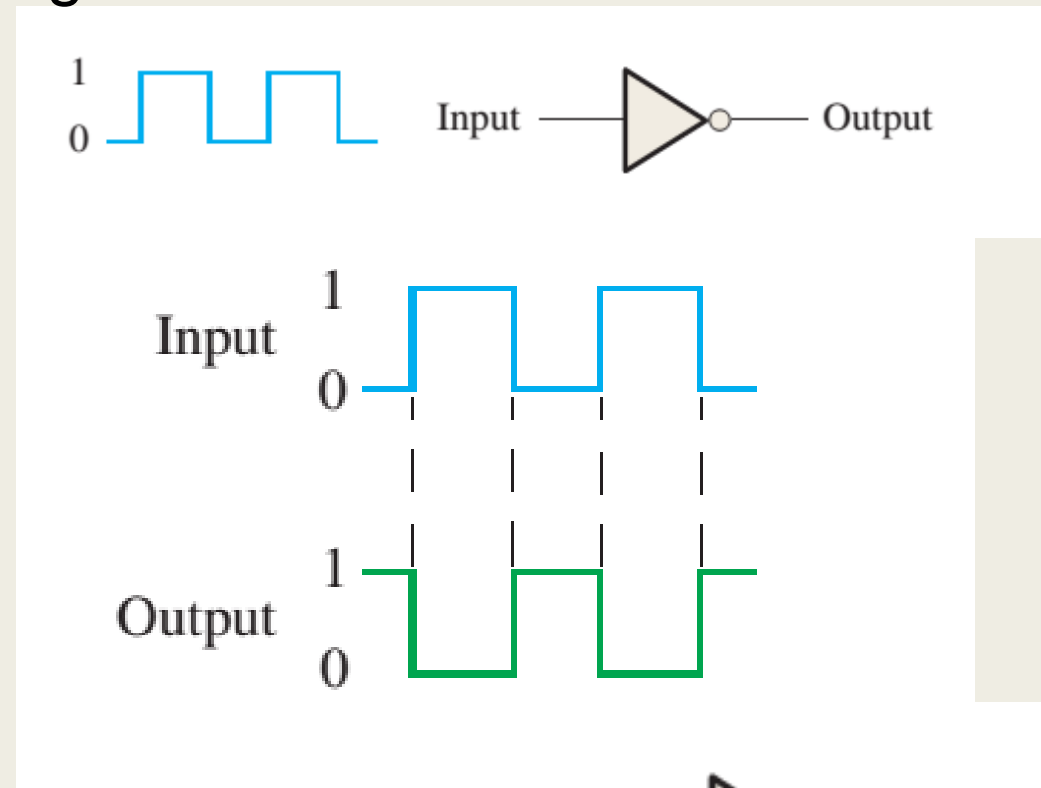
(a) Distinctive shape symbols
with negation indicators



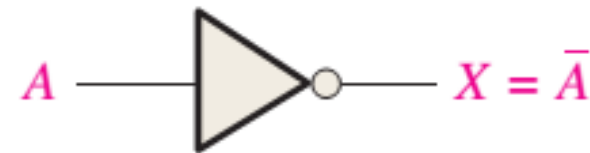
(b) Rectangular outline symbols
with polarity indicators



Timing Diagram



Logical Expression



AND Gate

- Operation to check if two conditions are satisfied

- Two inputs
- Output = 1 if and only if both inputs are 1
- Symbolized by dot or absence of operator

$x \cdot y$ or xy

- Truth table

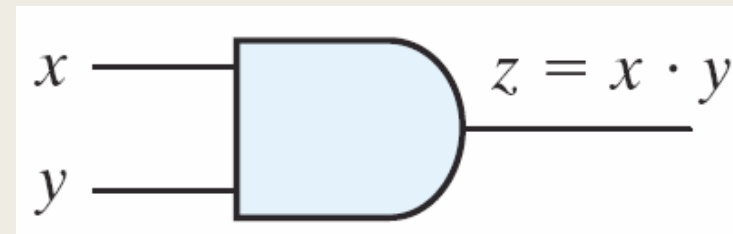
- Needs to consider $2^2 = 4$ input combinations

- Graphic symbol

- AND gate

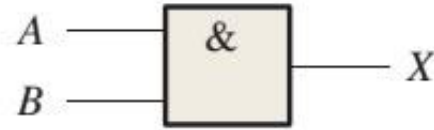
inputs output

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1



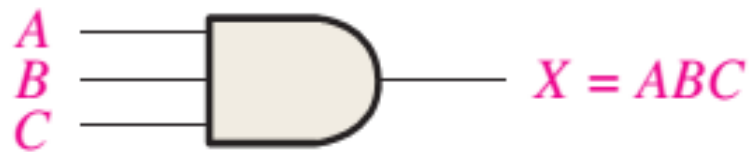
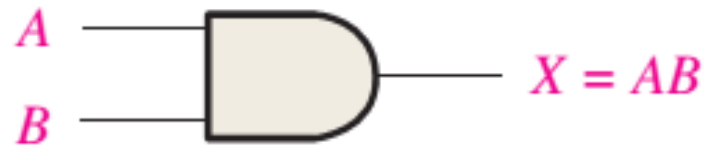


(a) Distinctive shape

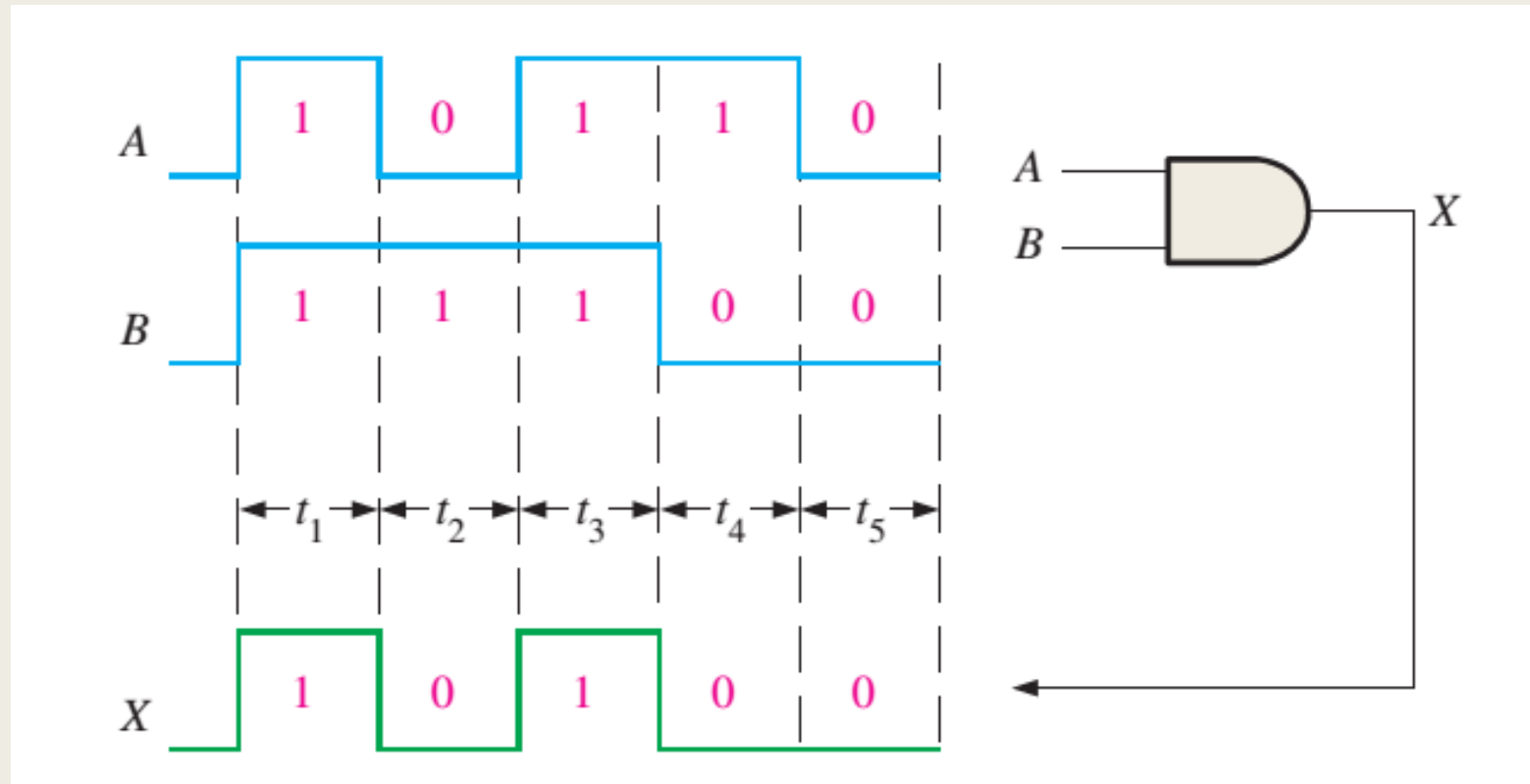


(b) Rectangular outline with the AND (&) qualifying symbol

Logical Expression



Timing Diagram of an AND gate



Application of an AND gate

Seat belt alarm system

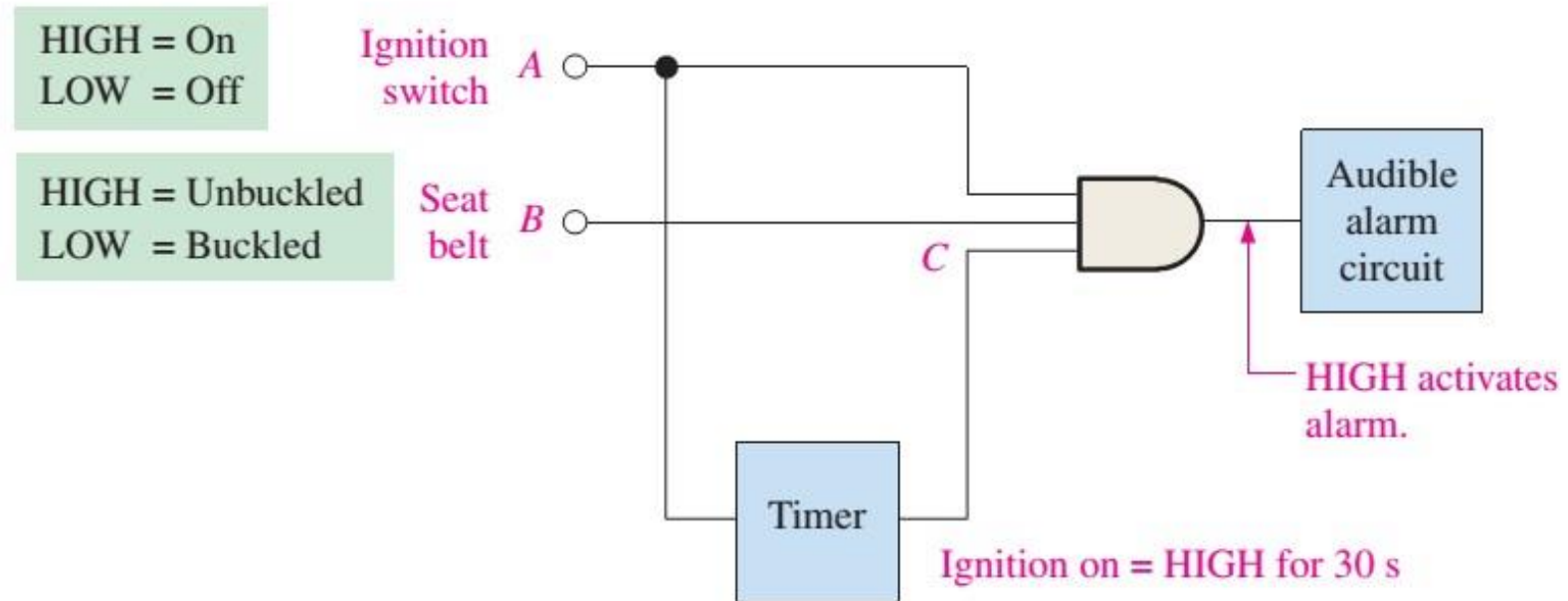


FIGURE 3-17 A simple seat belt alarm circuit using an AND gate.

OR Gate

- Operation to check if at least one condition is

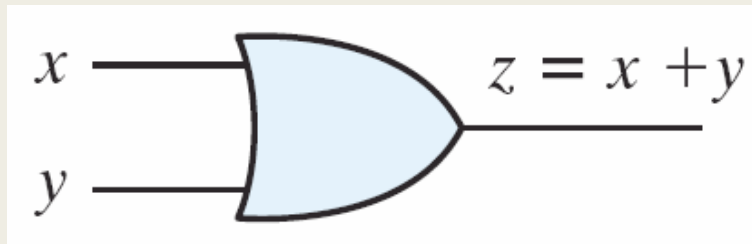
■ met

- *Two inputs*
- *Output = 1 if any one or both inputs are 1*
- *Symbolized by “plus” sign: $x + y$*

- Truth table

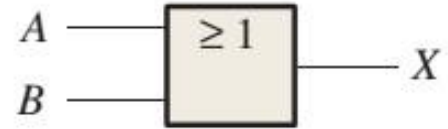
- *Graphic symbol*
- *OR gate*

x	y	z
0	0	0
0	1	1
1	0	1
1	1	1





(a) Distinctive shape

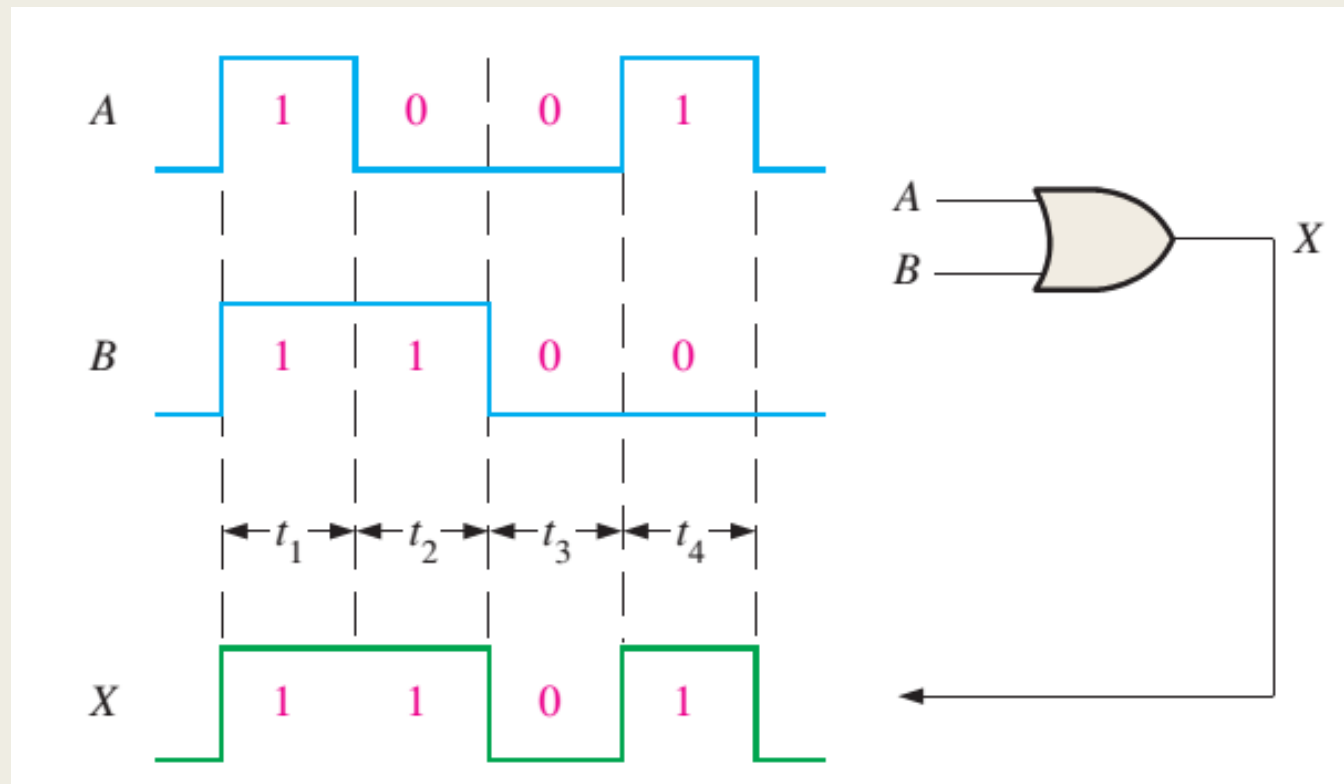


(b) Rectangular outline with the OR (≥ 1) qualifying symbol

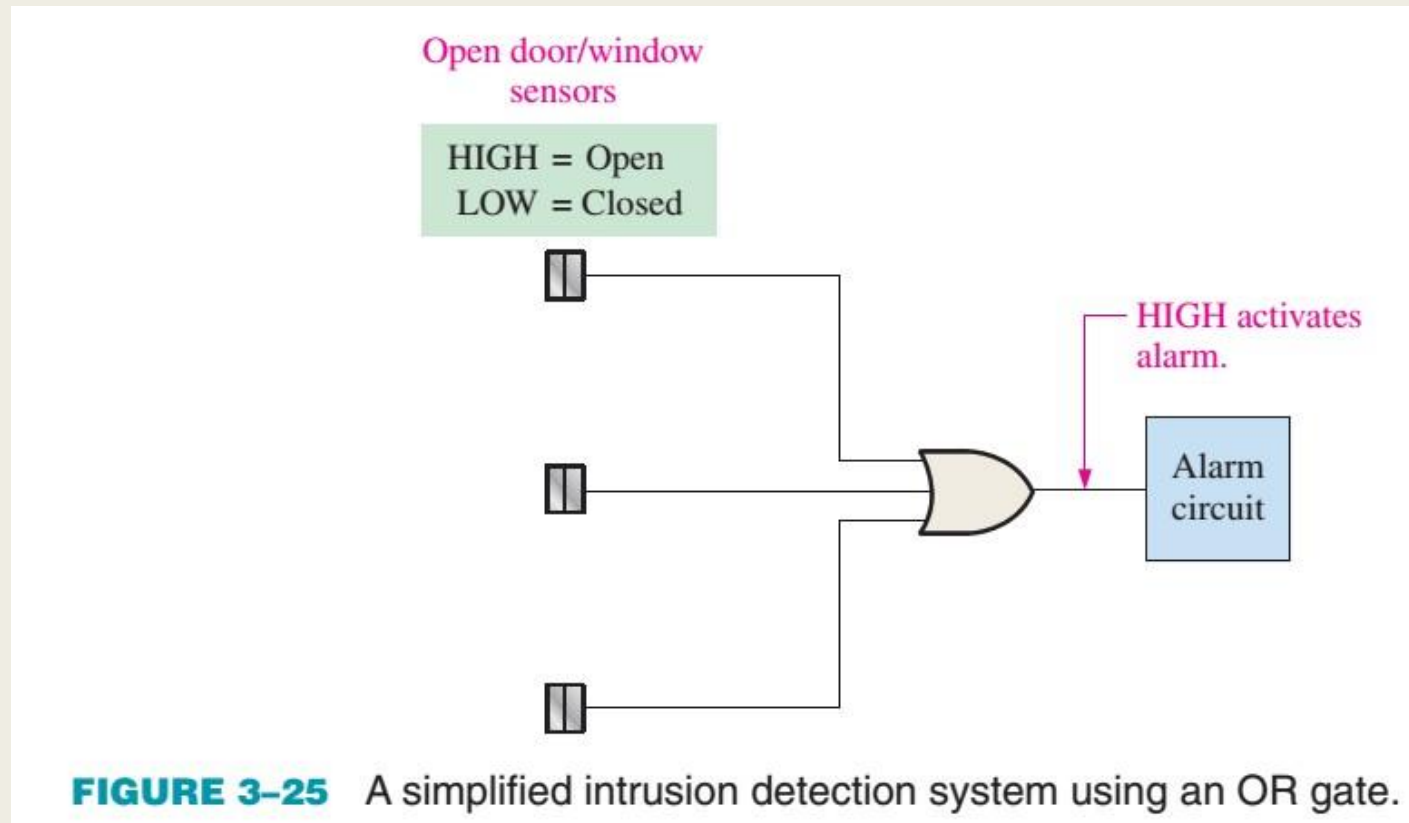
Logical Expression



Timing Diagram of an OR gate



Application of an OR gate Security system



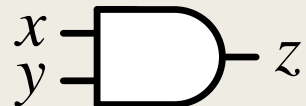
Binary Logic

■ Truth Tables, Boolean Expressions, and Logic Gates

AND

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

$$z = x \cdot y = xy$$



OR

x	y	z
0	0	0
0	1	1
1	0	1
1	1	1

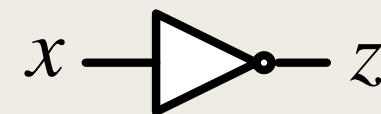
$$z = x + y$$



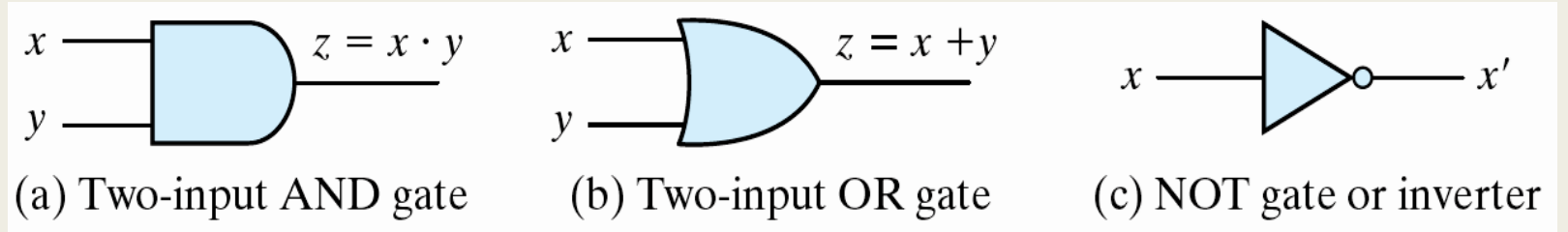
NOT

x	z
0	1
1	0

$$z = \overline{x} = x'$$



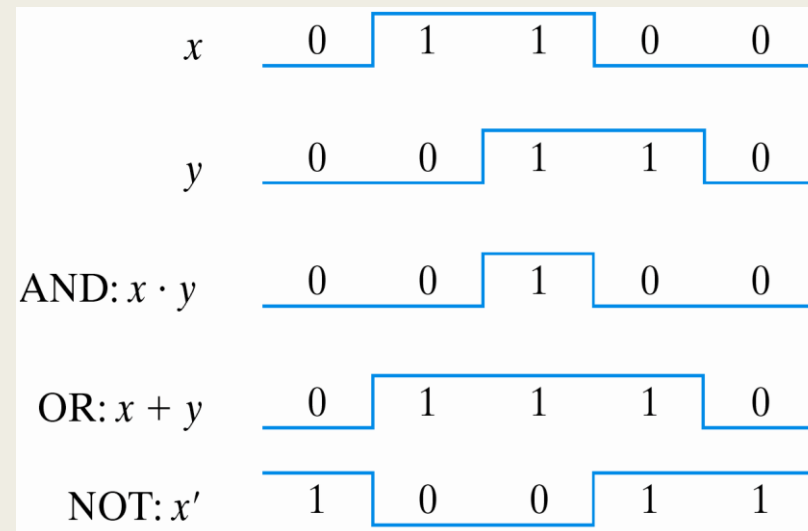
Binary Logic



■ Logic gates

- *Graphic Symbols and Input-Output Signals for Logic gates:*

Fig. 1.4 Symbols for digital logic circuits



Iqra chaudhary Fig. 1.5 Input-Output signals for gates

Binary Logic

- Logic gates

- *Graphic Symbols and Input-Output Signals for Logic gates:*

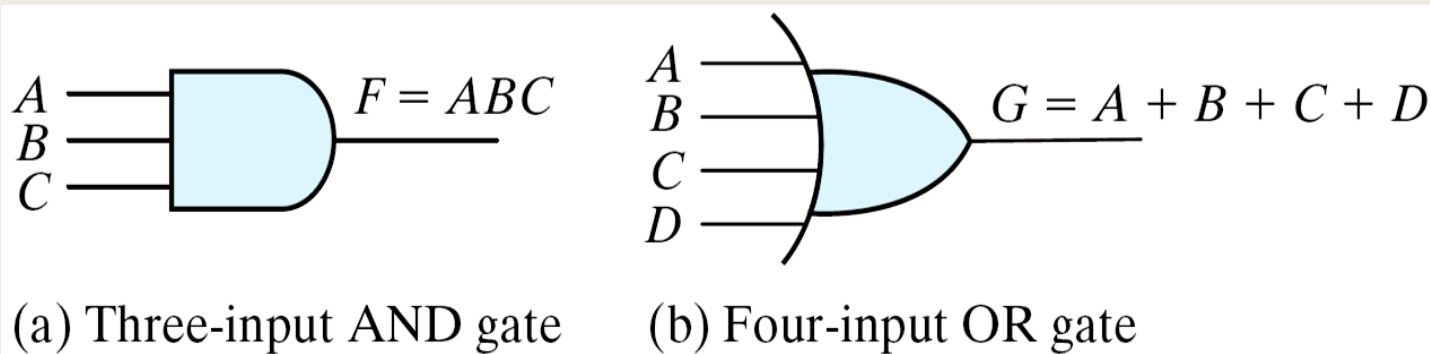


Fig. 1.6 Gates with multiple inputs

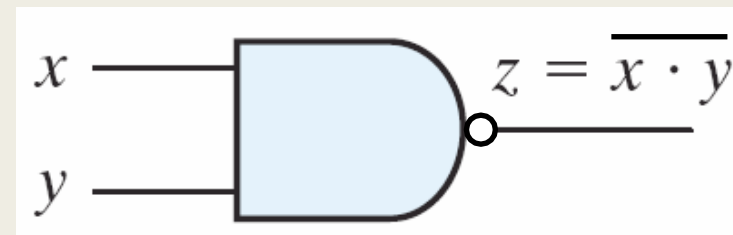
Some more about Logic Gates

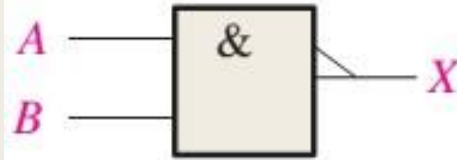
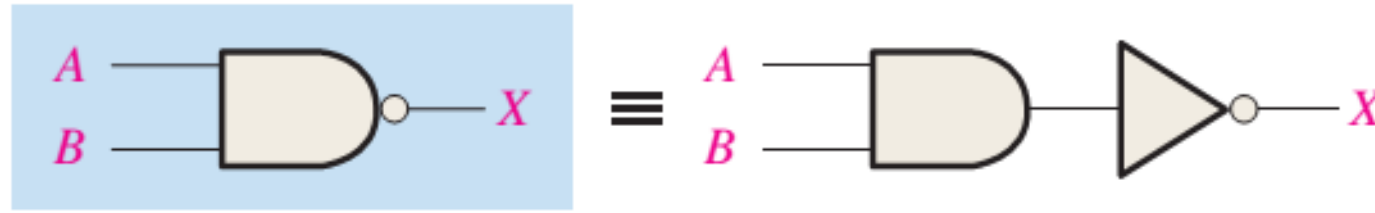
- Basic Gates
 - AND
 - OR
 - Not
- Extended Gates
 - NAND
 - NOR
 - XOR
 - XNOR

NAND Gate

- Operation to check if two conditions are met (for two input)
 - Output = 0 if and only if both inputs are 1
 - Symbolized by dot or absence of operator with a bar over them
 - $\overline{x \cdot y}$ or \overline{xy}
- Truth table
 - Needs to consider $2^2 = 4$ input combinations
- Graphic symbol
 - NAND gate

Inputs		Output
x	y	z
0	0	1
0	1	1
1	0	1
1	1	0

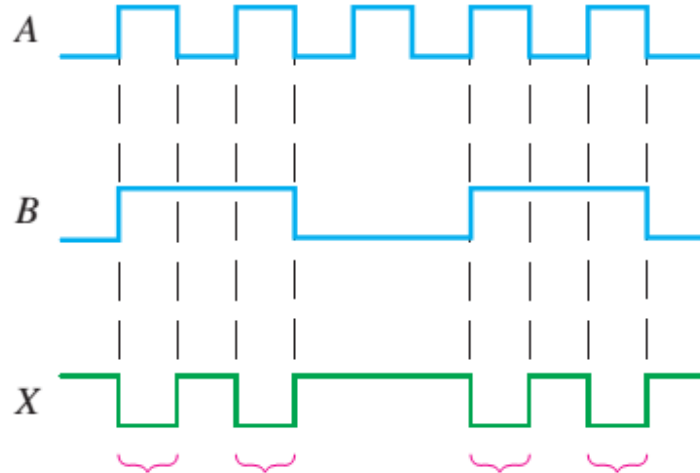




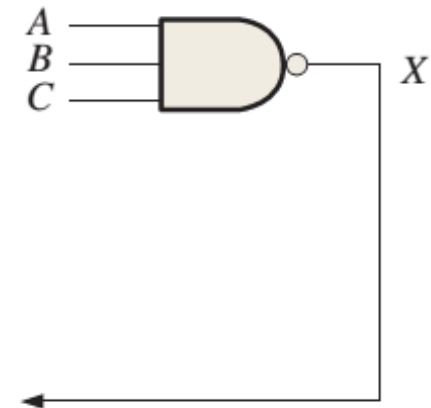
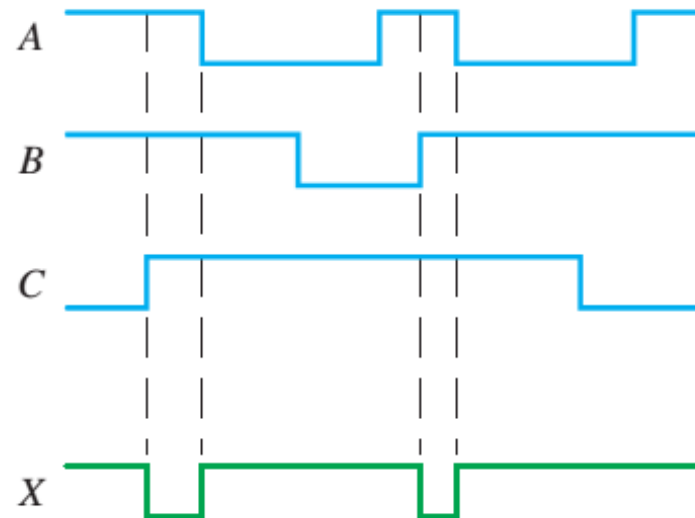
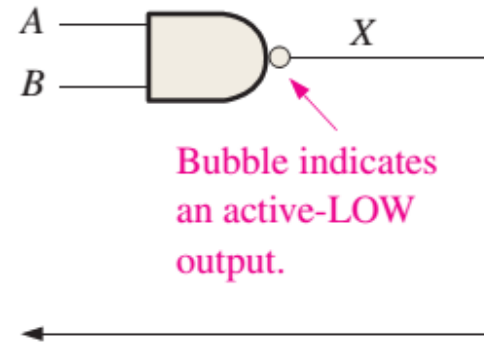
(b) Rectangular outline, 2-input NAND gate with polarity indicator

Logical Expression

$$X = \overline{AB}$$



A and B are both HIGH during these four time intervals; therefore, X is LOW.



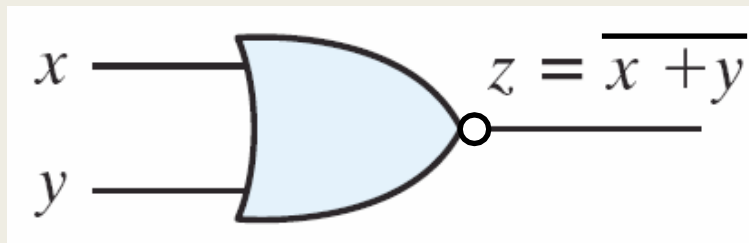
NOR Gate

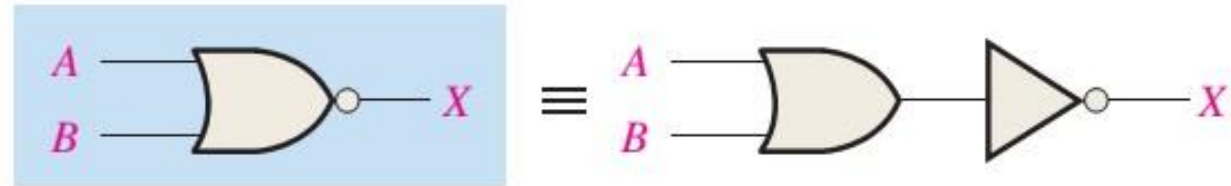
- Operation to check if two conditions are not met (for two input)
 - Output = 1 if and only if both inputs are 0
 - Symbolized by + operator with a bar over them

$$\overline{x+y}$$

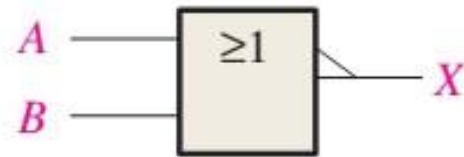
- Truth table
- Graphic symbol
 - NAND gate

Inputs		Output
x	y	z
0	0	1
0	1	0
1	0	0
1	1	0





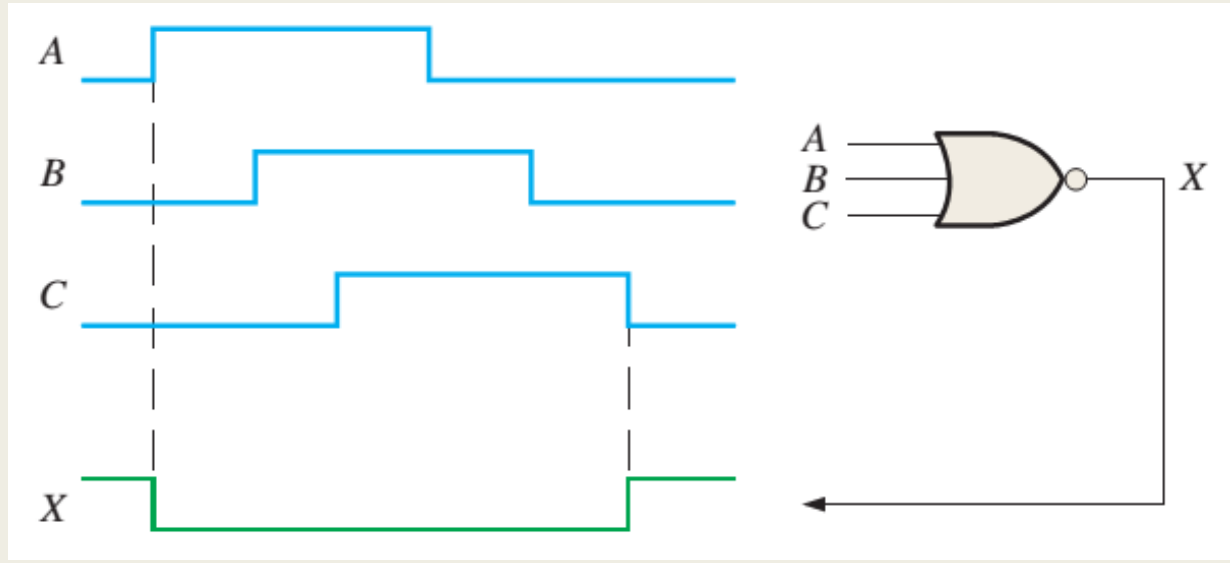
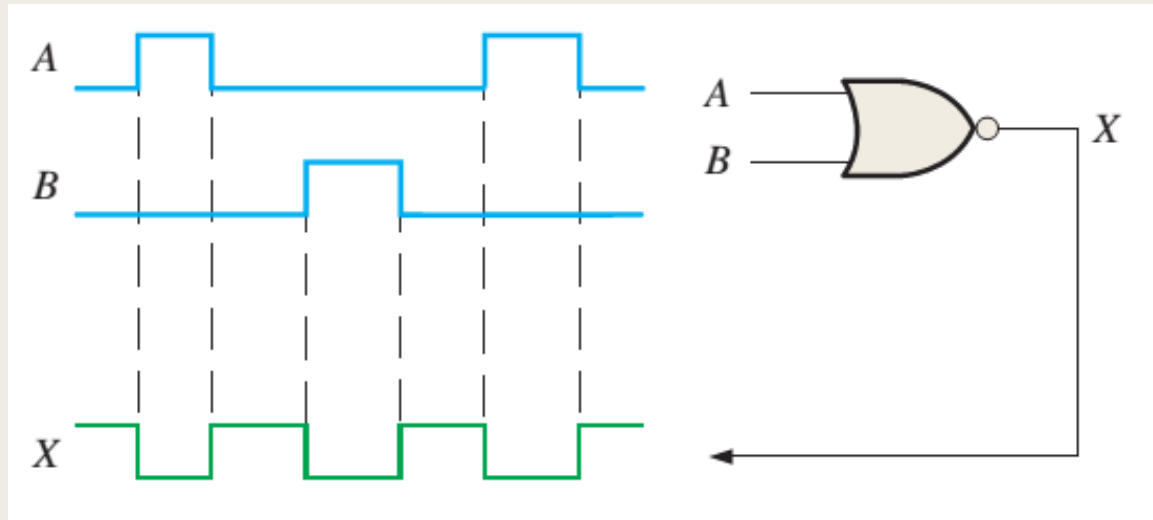
(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent



(b) Rectangular outline, 2-input NOR gate with polarity indicator

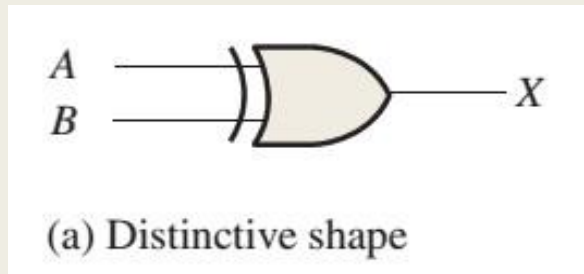
Logical Expression

$$X = \overline{A + B}$$

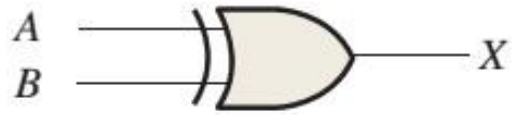


XOR Gate

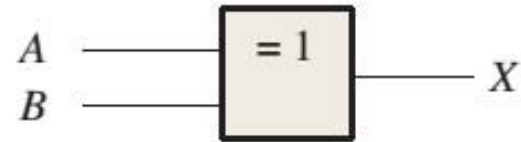
- Operation to check if two conditions are not met (for two input)
 - Output = 1 if one of the inputs is 1
 - Symbolized by \oplus operator $x \oplus y$
- Truth table
- Graphic symbol
 - XOR gate



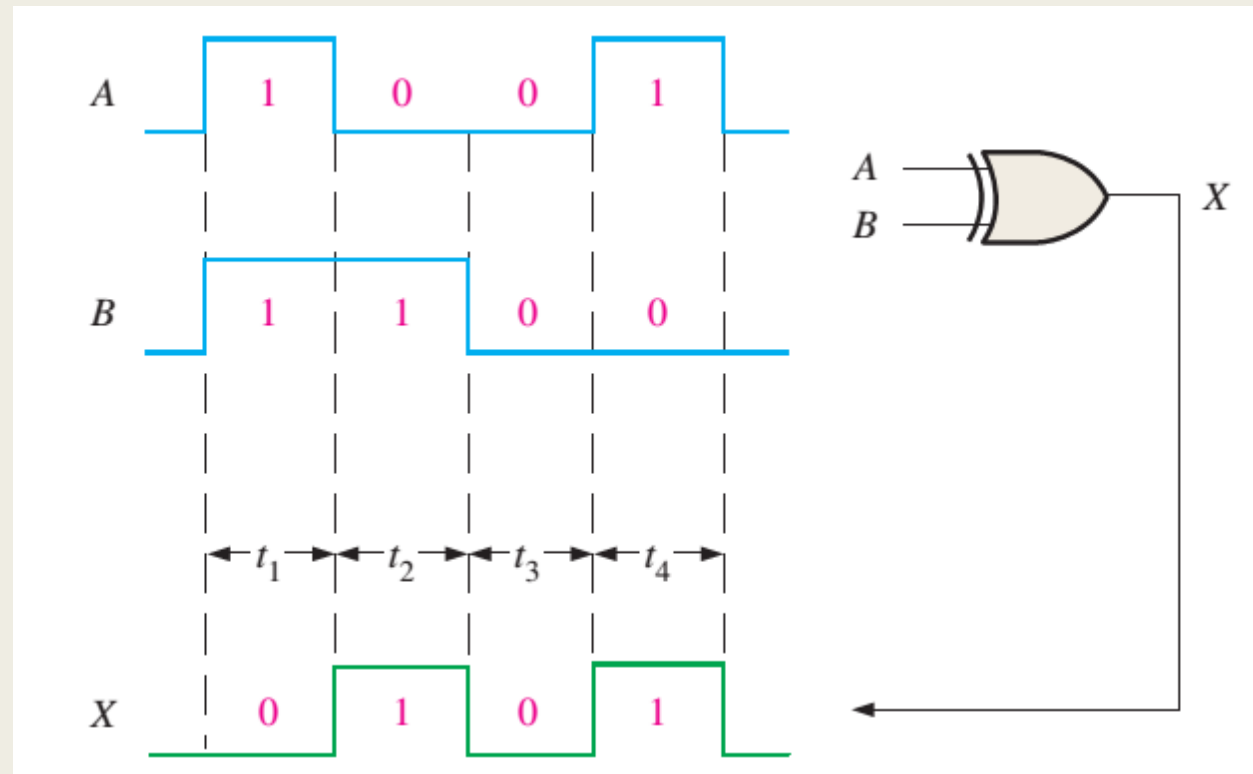
Inputs		Output
x	y	z
0	0	0
0	1	1
1	0	1
1	1	0



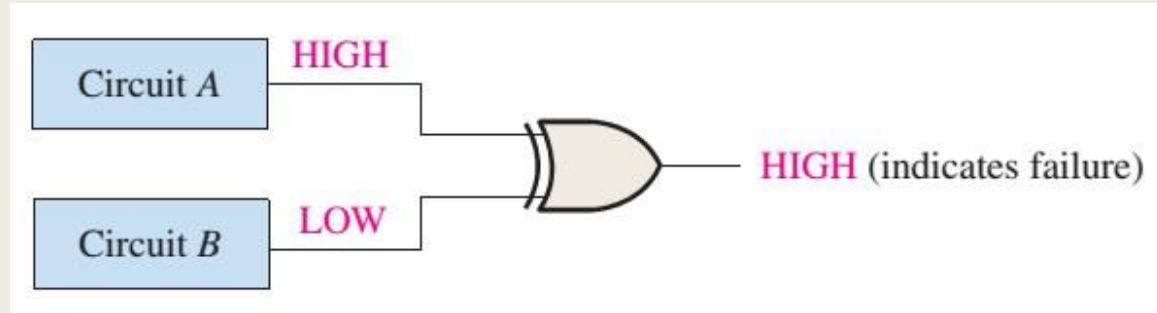
(a) Distinctive shape



(b) Rectangular outline



Two identical
circuits
connected in
parallel

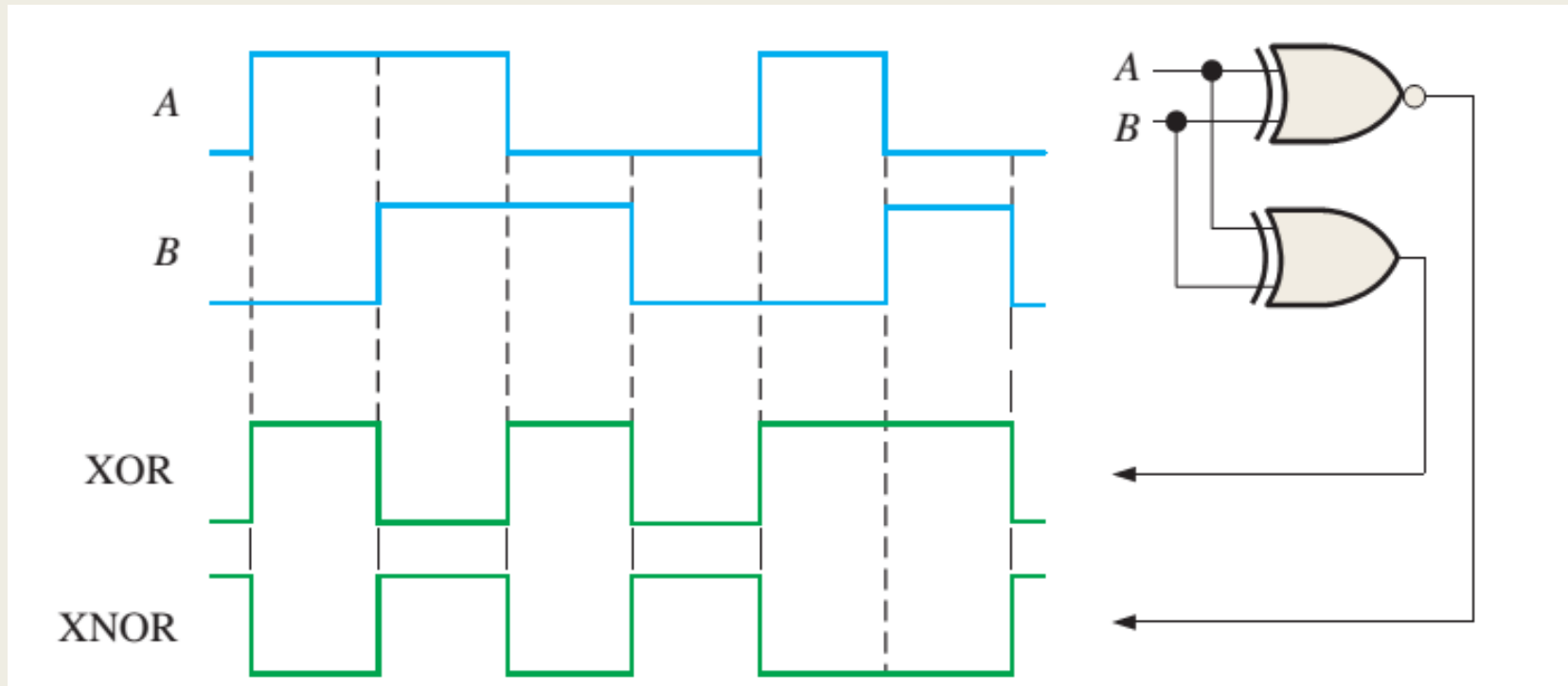


An XOR gate used to add two bits.

Input Bits		Output (Sum)
<i>A</i>	<i>B</i>	Σ
0	0	0
0	1	1
1	0	1
1	1	0 (without the 1 carry bit)

The diagram shows an XOR gate with two inputs, A and B, and one output, Σ. The output Σ is 0 when both inputs are 1, which is noted as 'without the 1 carry bit'.

XOR and XNOR



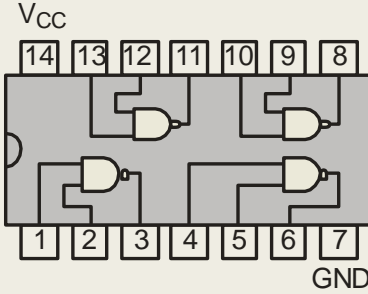
Multiple-input XOR

- Extension of exclusive-OR not straightforward
 - What is the definition for 3 variables?
- Turns into “odd” function
 - Function is 1 when there is
 - an odd number of 1's

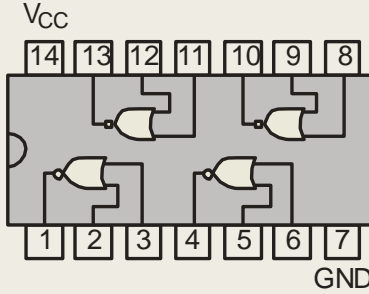
x	y	z	$x \oplus y \oplus z$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Fixed function Logic

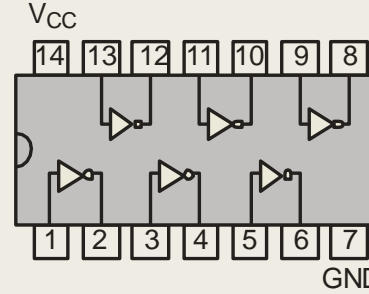
Some common gate configurations of 74 series are shown



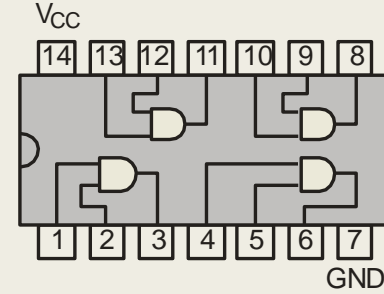
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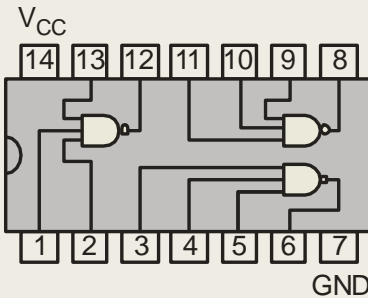
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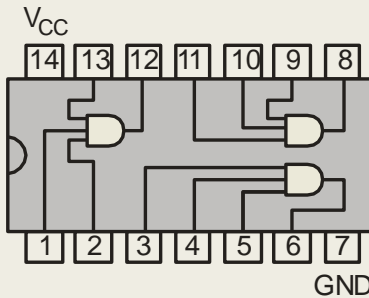
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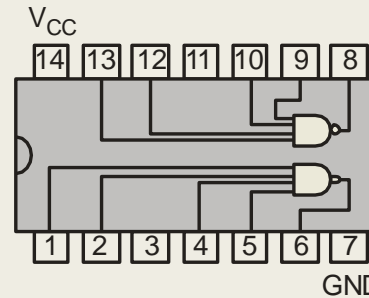
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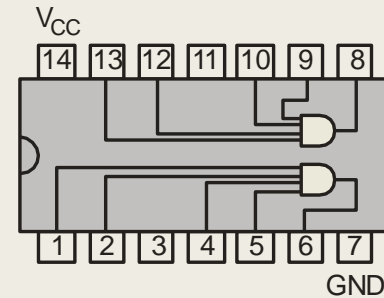
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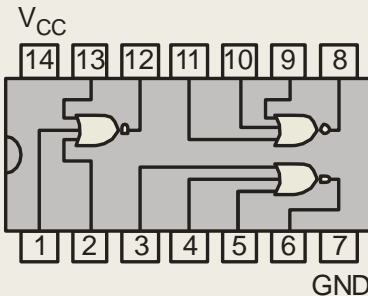
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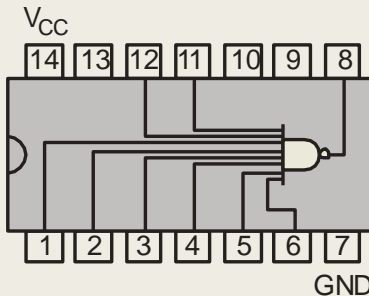
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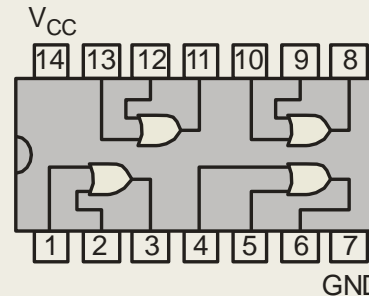
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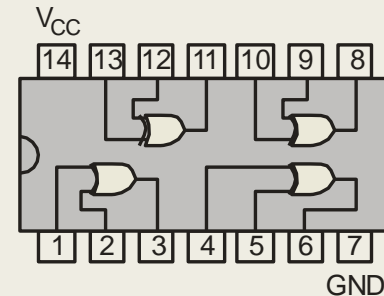
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'30



'32



'86

Thank You