



COMBINATIONAL LOGIC

**MULTIPLEXER
DEMULTIPLEXERS**

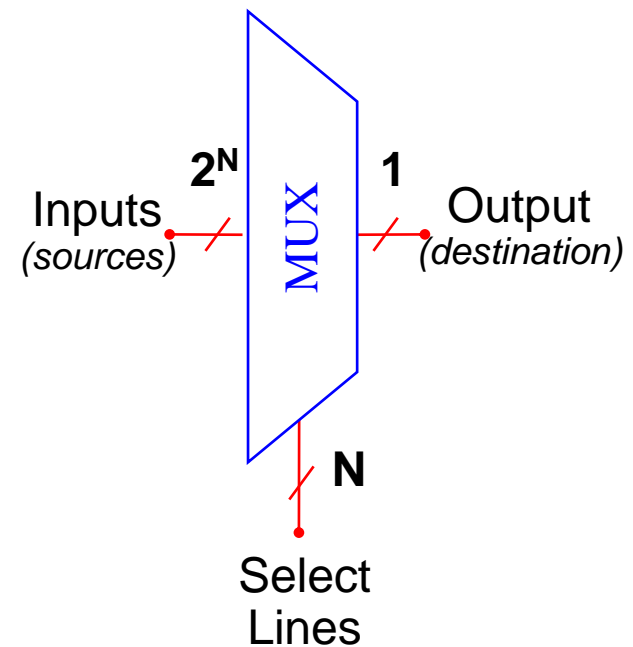
DIGITAL LOGIC DESIGN

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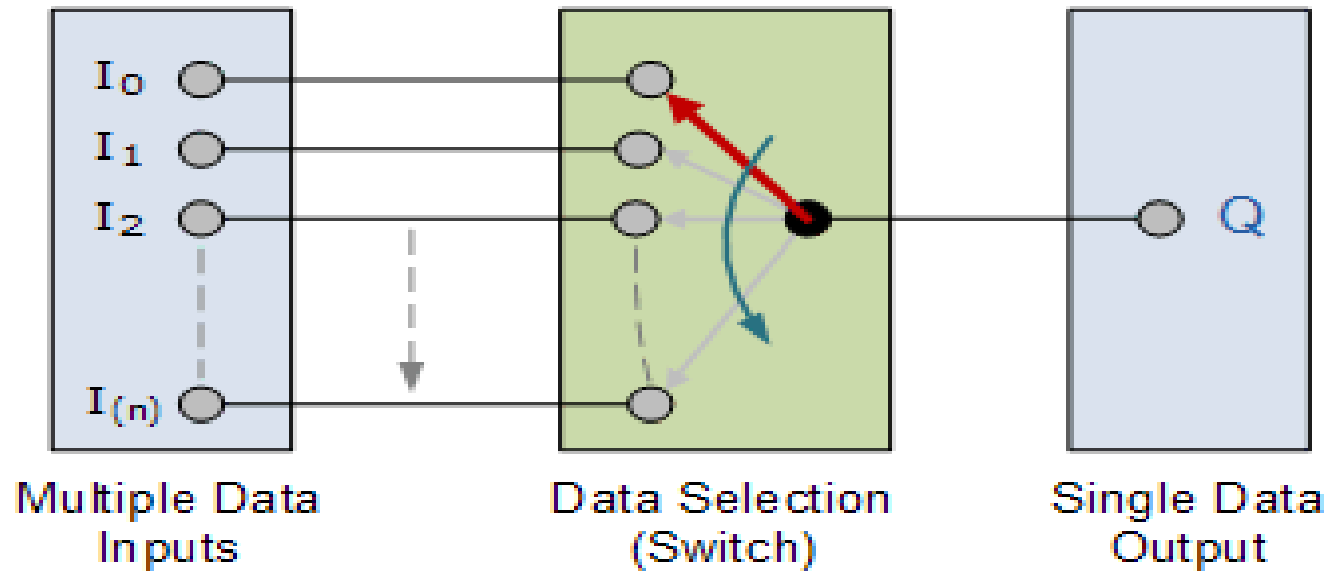
Multiplexer

- ★ Multiplexer is a combinational circuit that has 2^n input lines, n selection lines and a single output line. The select lines determine which input is connected to the output.
- ★ Multiplexer also known as a data selector.
- ★ Mux acts as an electronic switch. It allows for conditional transfer of data.
- ★ MUX Types
 - 2-to-1 (1 select line)
 - 4-to-1 (2 select lines)
 - 8-to-1 (3 select lines)
 - 16-to-1 (4 select lines)

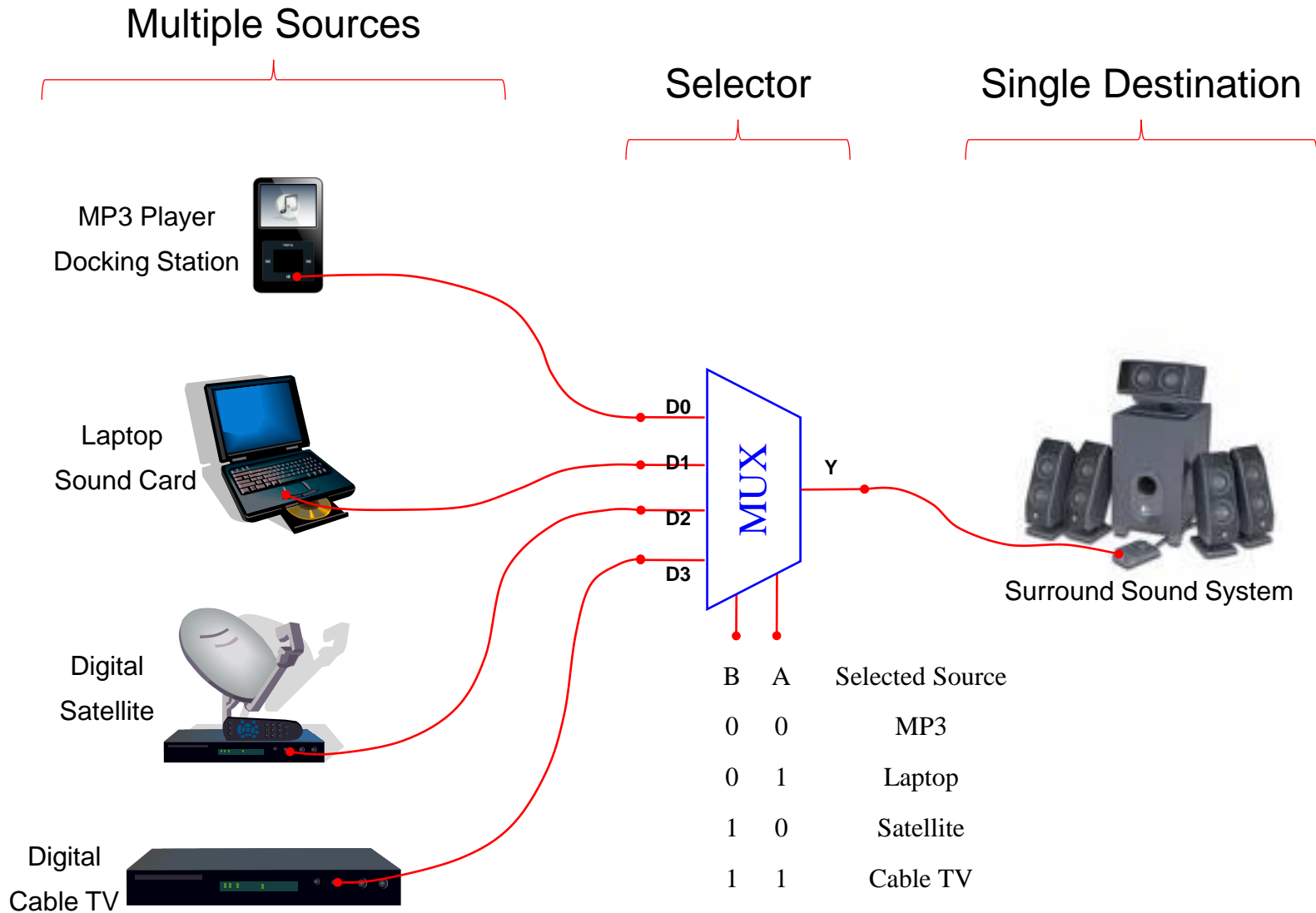
Multiplexer
Block Diagram



Multiplexers

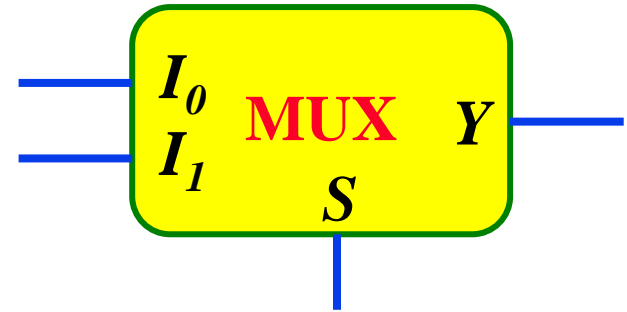


Typical Application of a MUX

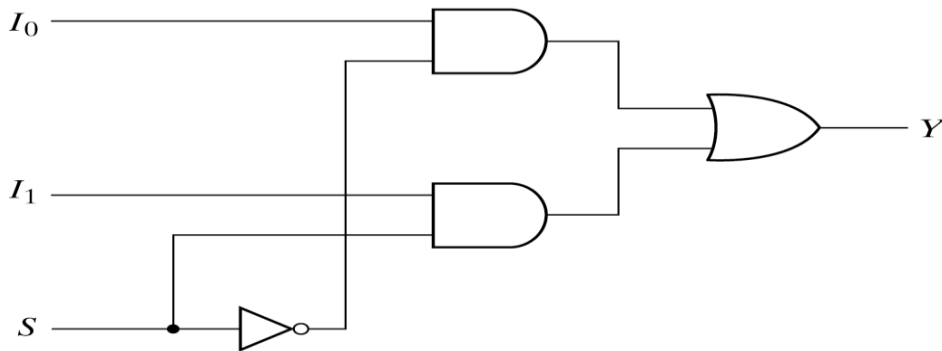


Multiplexers : 2-to-1 lines mux

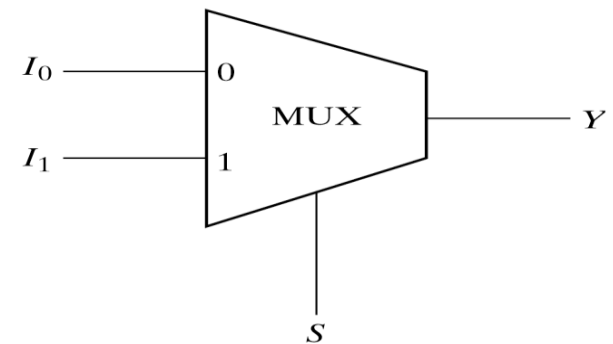
S_0	Y
0	I_0
1	I_1



$$Y = I_0 \bar{S}_0 + I_1 S_0$$



(a) Logic diagram

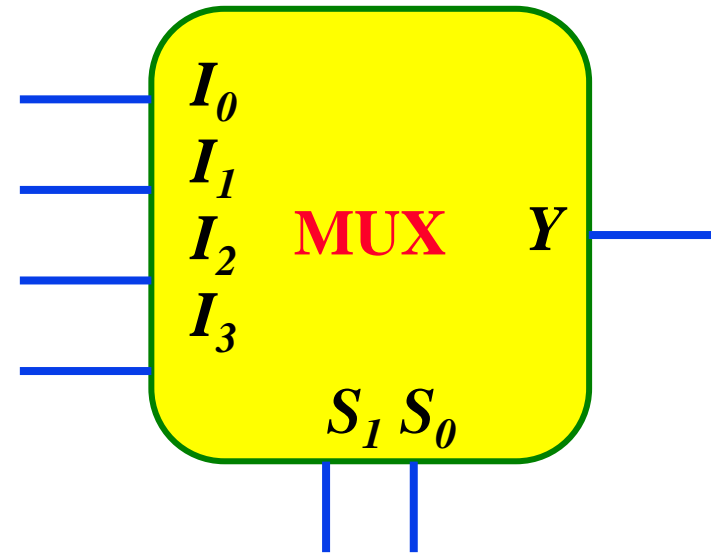


(b) Block diagram

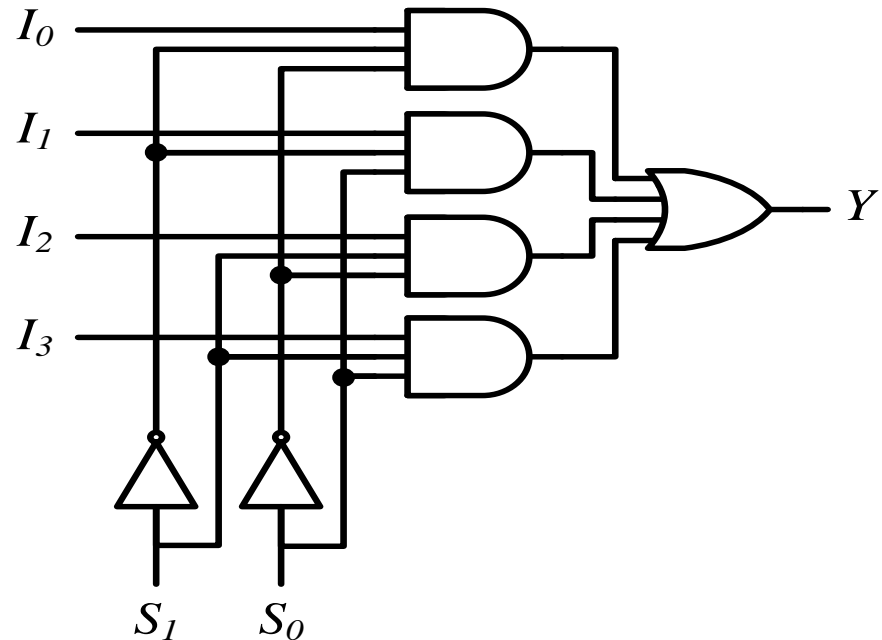
Fig. 4-24 2-to-1-Line Multiplexer

Multiplexers: 4 to 1 line mux

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



$$Y = I_0 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_1 S_0 + I_2 S_1 \bar{S}_0 + I_3 S_1 S_0$$



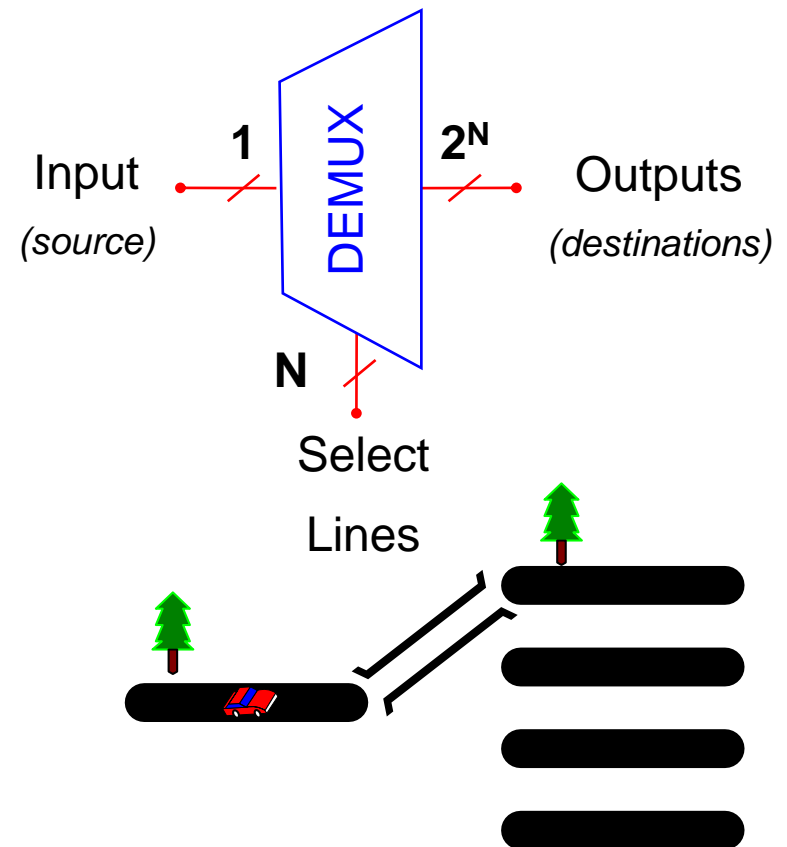
What is a Demultiplexer (DEMUX)?

★ Demux is a combinational circuit that has a single input lines, n selection lines and 2^n output line. The select lines determine which output the input is connected to.

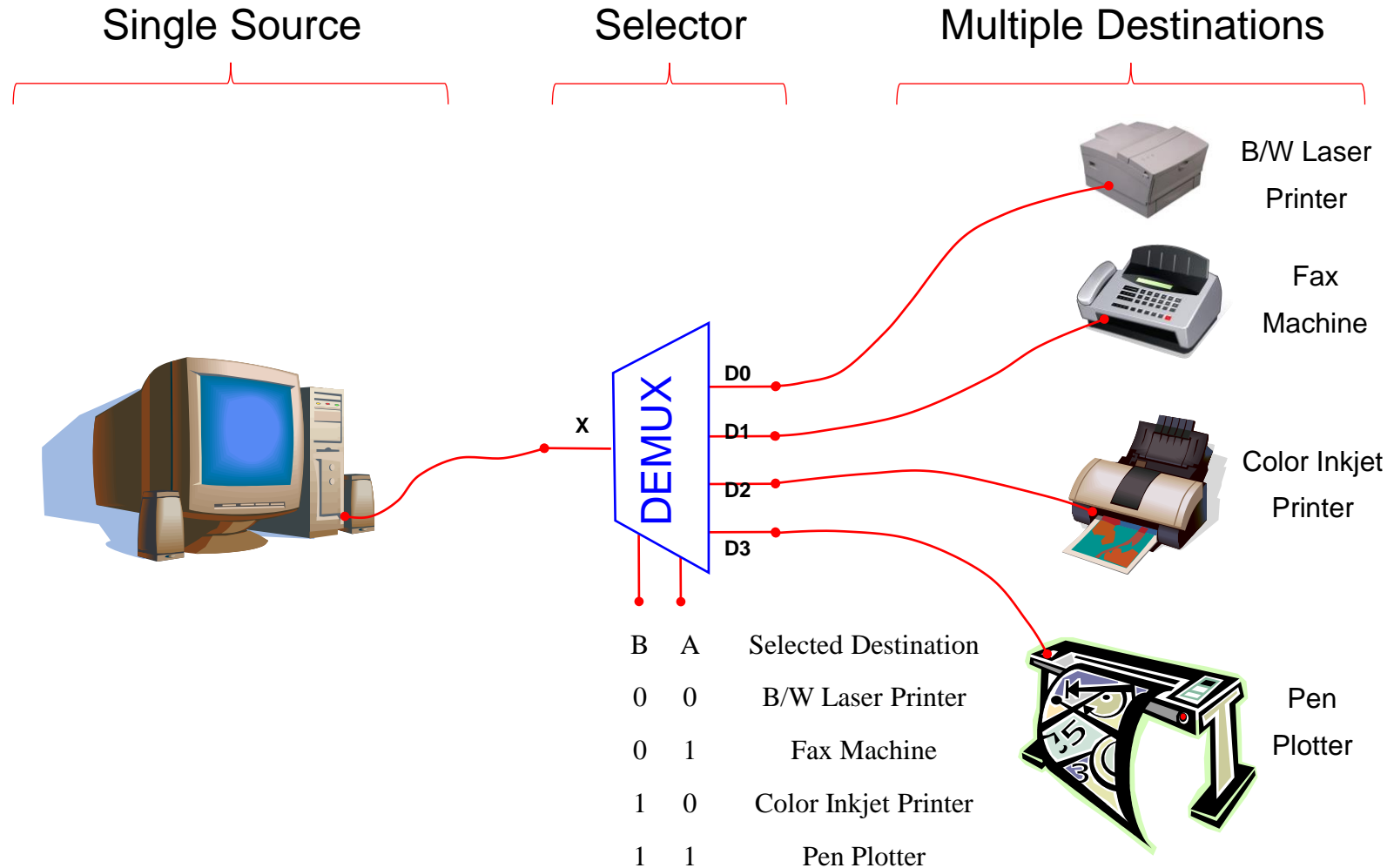
★ DEMUX Types

- 1-to-2 (1 select line)
- 1-to-4 (2 select lines)
- 1-to-8 (3 select lines)
- 1-to-16 (4 select lines)

Demultiplexer
Block Diagram

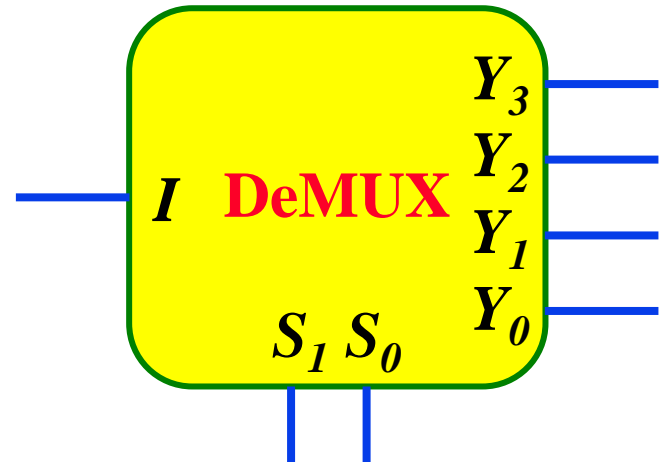


Typical Application of a DEMUX



DeMultiplexers (1 to 4 lines demux)

S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

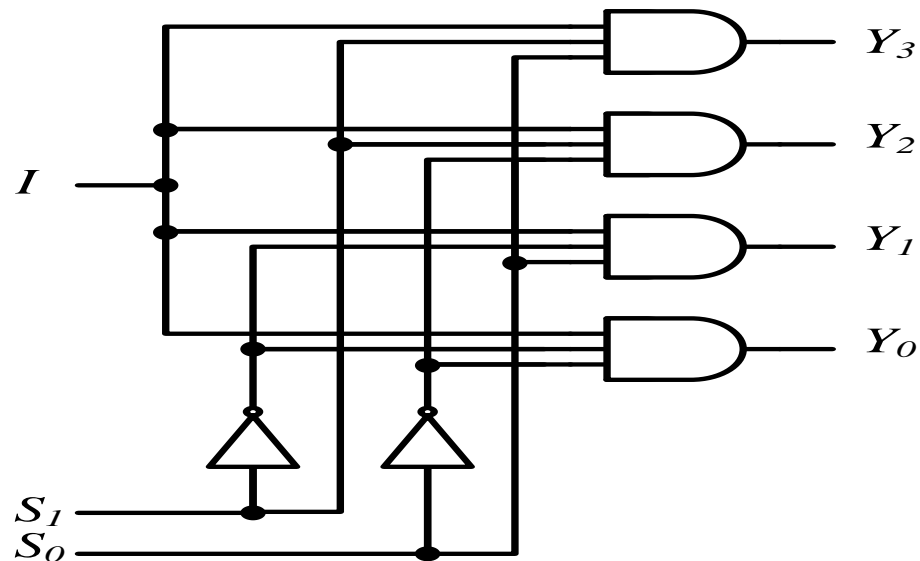


$$Y_0 = \text{I} \bar{S}_1 \bar{S}_0$$

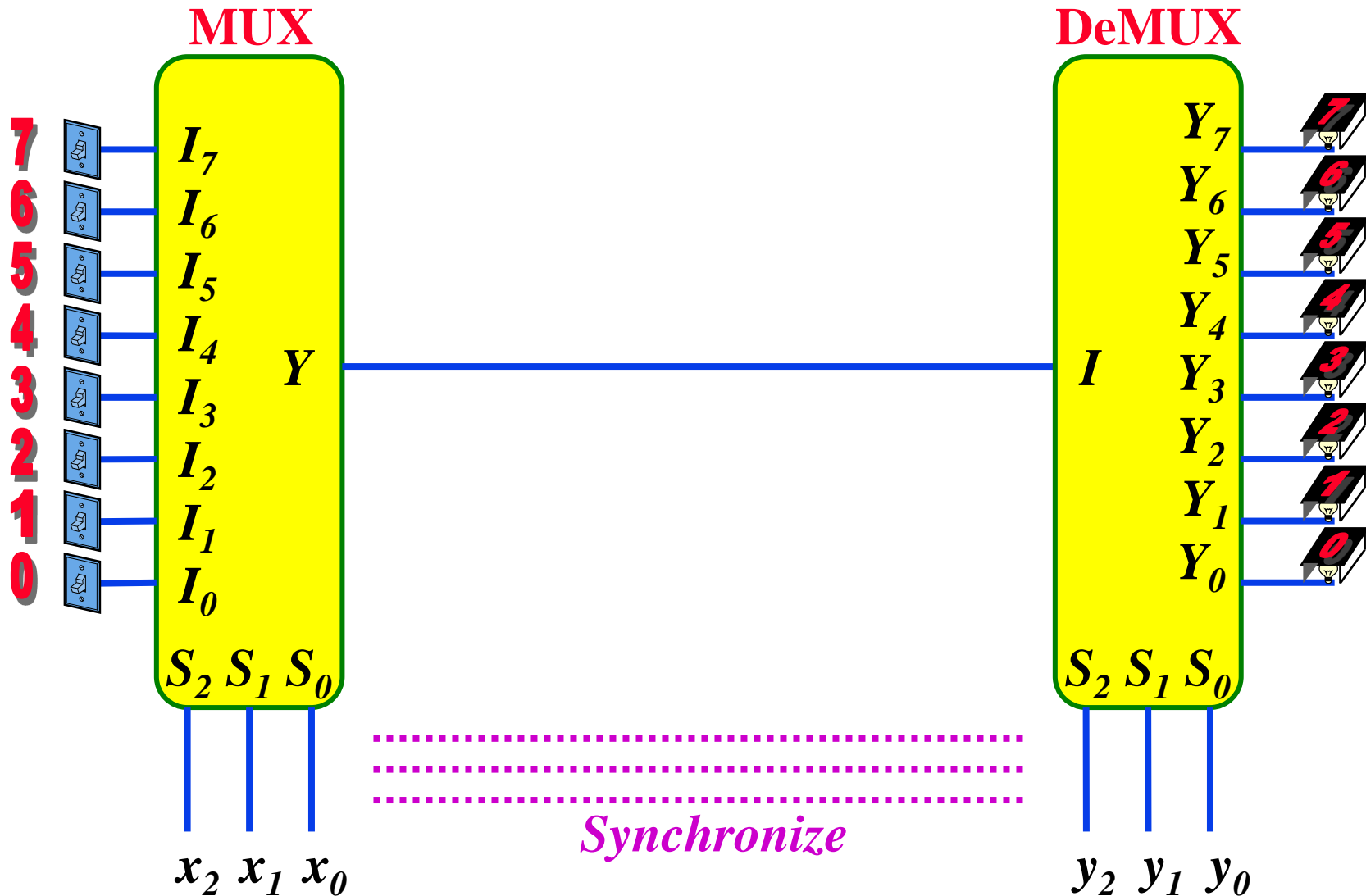
$$Y_1 = \text{I} \bar{S}_1 S_0$$

$$Y_2 = \text{I} S_1 \bar{S}_0$$

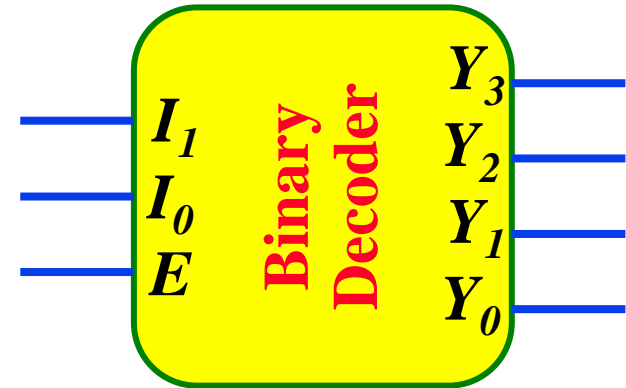
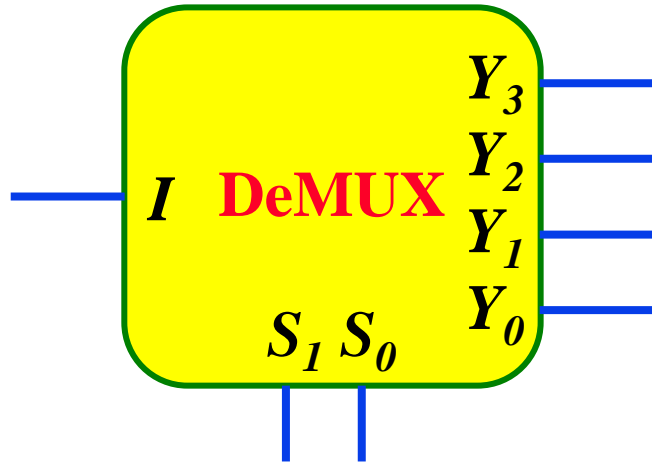
$$Y_3 = \text{I} S_1 S_0$$



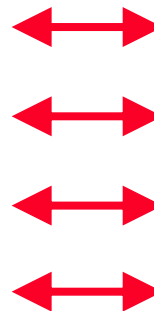
Multiplexer / DeMultiplexer Pairs



DeMultiplexers / Decoders



S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

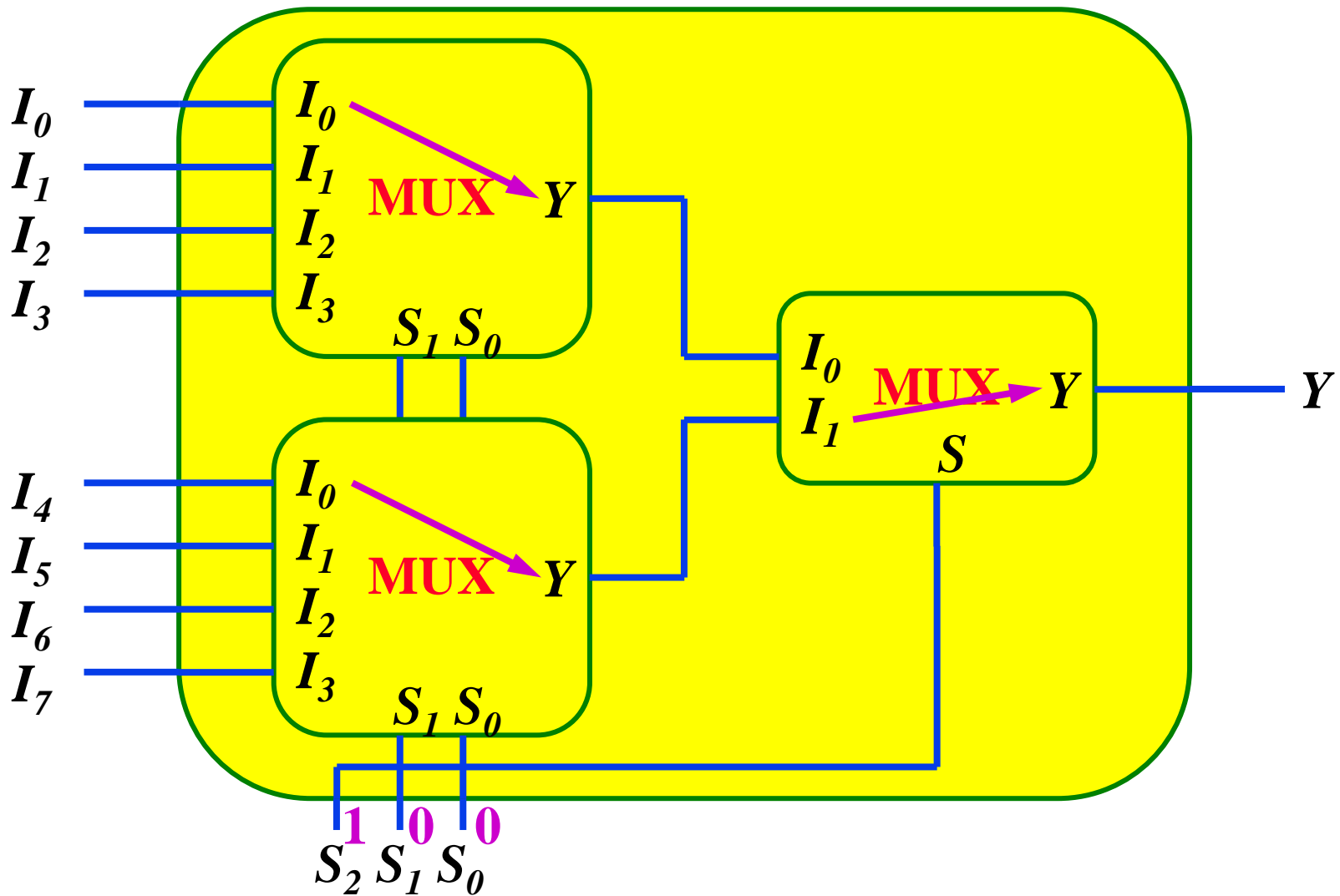


E	I_1	I_0	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0



Multiplexer Expansion

★ 8-to-1 MUX using Dual 4-to-1 MUX and single 2-to-1 MUX



Motivation

★ Design a single bit ALU

ALU = Arithmetic Logic Unit
(Add, Sub, And, Or)

M input signal (m=0 for addition and m=1 for Subtraction)

