Experiment
#7

Title:-

Simplifying Boolean expression and its implementation using logic gates and Verilog

Objective:-

- **Boolean laws**

Parts required:-

- IC Type 7404 Quadruple 2-input NOT gates
- IC Type 7432 Quadruple 2-input OR gates
- IC Type 7411 triple 3-input and gates

Equipment required:-

- Trainer/ proto board
- Wire cutter
- Patch Cord
- Voltmeter
- SynaptiCAD Verilogger

Theory:-

This lab is about simplification of Boolean expression by utilizing Boolean laws.

Boolean laws and rules:

1	**Commutative Law** (a) $A + B = B + A$ (b) $A\,B = B\,A$	**7**	(a) $0 + A = A$ (b) $0\,A = 0$
2	**Associate Law** (a) $(A + B) + C = A + (B + C)$ (b) $(A\,B)\,C = A\,(B\,C)$	**8**	(a) $1 + A = 1$ (b) $1\,A = A$
3	**Distributive Law** (a) $A\,(B + C) = A\,B + A\,C$ (b) $A + (B\,C) = (A + B)\,(A + C)$	**9**	(a) $A + \overline{A}\,B = A + B$ (b) $A\,(\overline{A} + B) = A\,B$

4	**Identity Law** (a) $A + A = A$ (b) $A\,A = A$	**10**	**De Morgan's Theorem** (a) $\overline{(A + B)} = \overline{A}\ \overline{B}$ (b) $\overline{(A\,B)} = \overline{A} + \overline{B}$
5	(a) $AB + A\overline{B} = A$ (b) $(A+B)(A+\overline{B}) = A$	**11**	**(a)** $\overline{A} + A = 1$ **(b)** $\overline{A}\ A = 0$
6	**Redundance Law** (a) $A + A\,B = A$ (b) $A\,(A + B) = A$		

Boolean expression

$F = A.B.C + \bar{A} + A.\bar{B}.C$

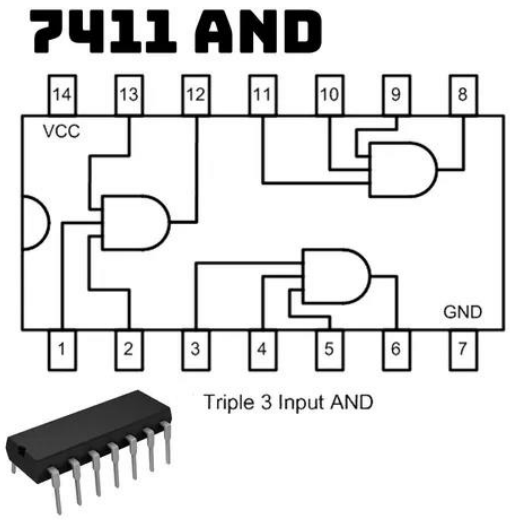
$F = A.C(B + \bar{B}) + \bar{A}$

$F = A.C(1) + \bar{A}$ (After applying law no. 11(a))

$F = A.C + \bar{A}$

$F = \bar{A} + C$ (After applying law no. 9(a))

IC 7411 3-input AND gates



TASK: Draw the truth tables and circuit diagrams for both the original and simplified version of the Boolean expression. Also attach the screenshots of timing diagram and the code.