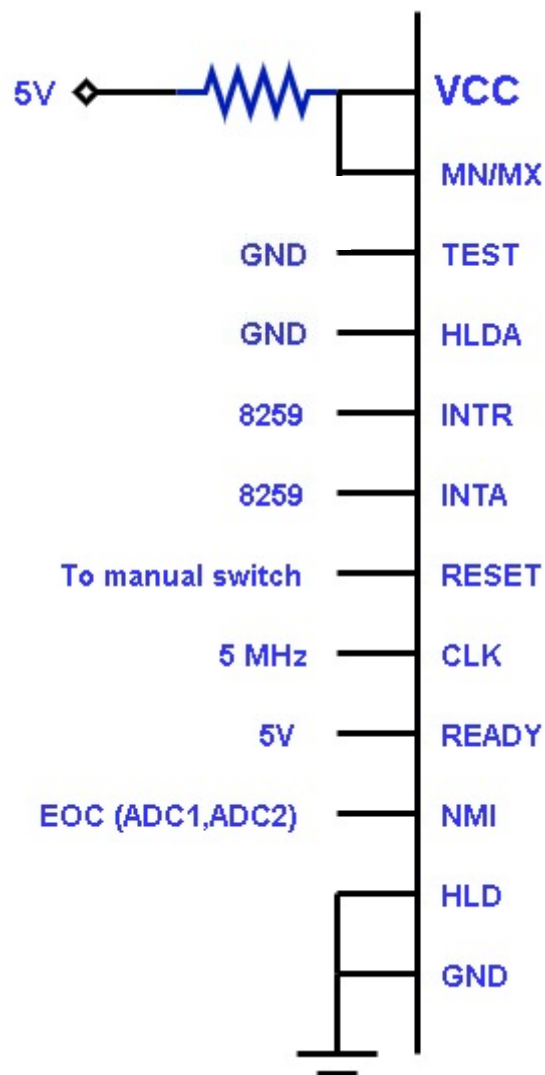
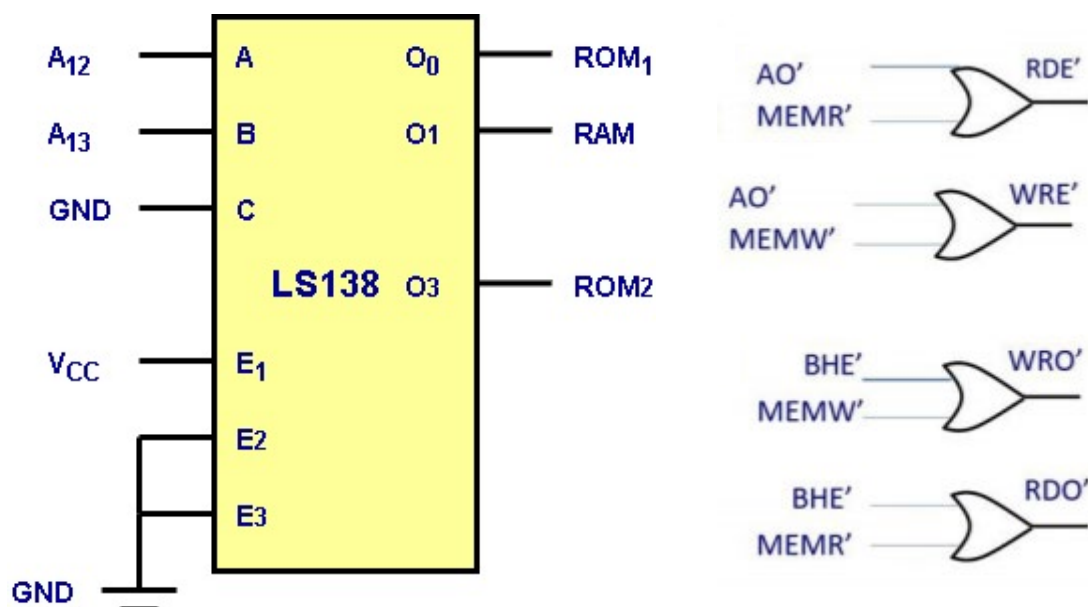


Inputs To 8086



8284 supplies clock signal to 8086

INTR and INTA signals are generated using 8259 and is supplied as input to 8086

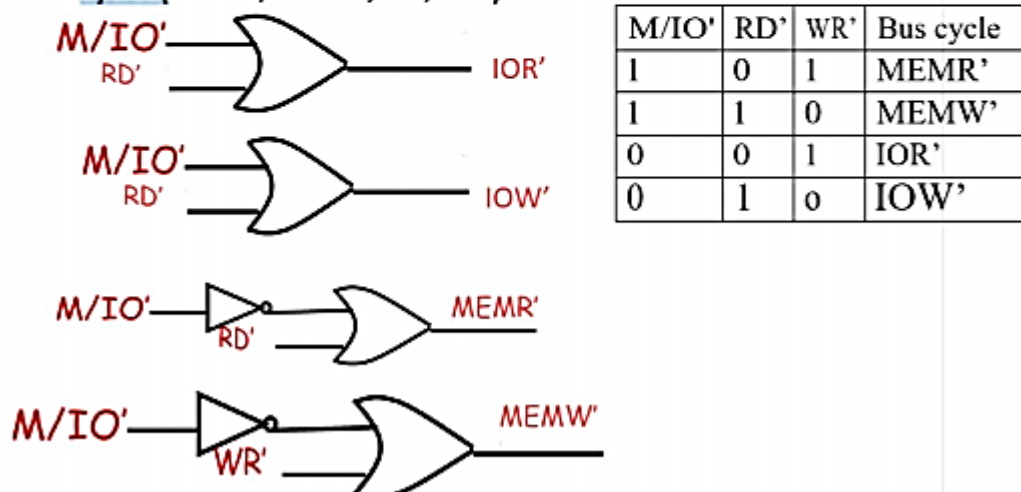


MEMORY DECODER

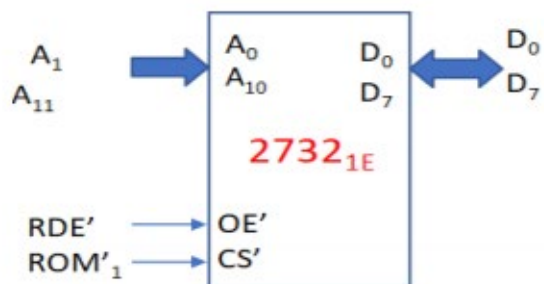
LS138: A 3:8 decoder as part of the decoding logic for memory interfacing.

On the right, the read and write signals for even and odd addresses are generated.

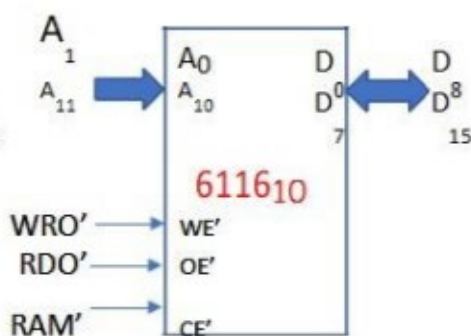
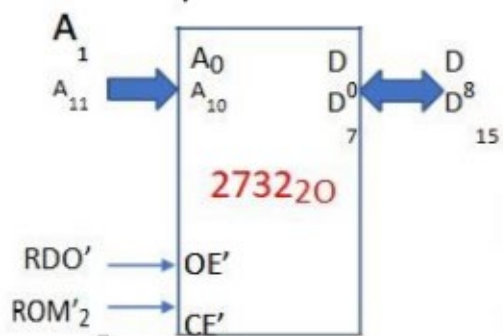
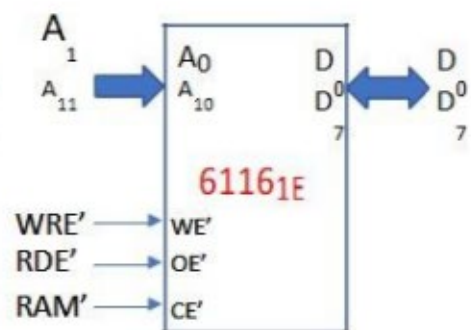
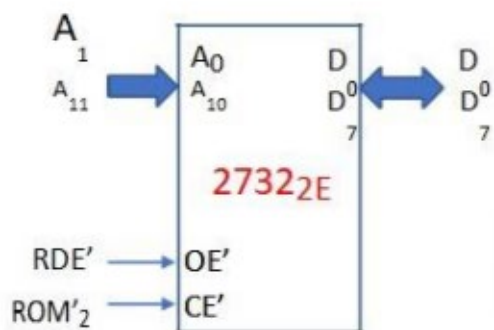
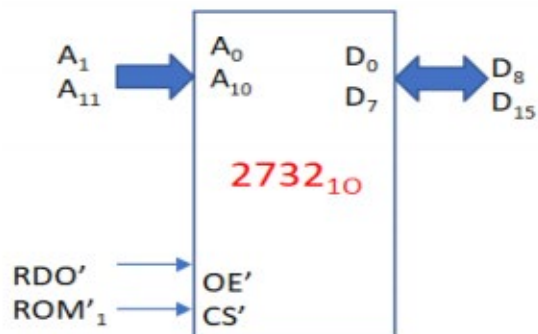
List of various input combinations which form the 4 bus cycles (MEMR, MEMW, IOR, IOW)



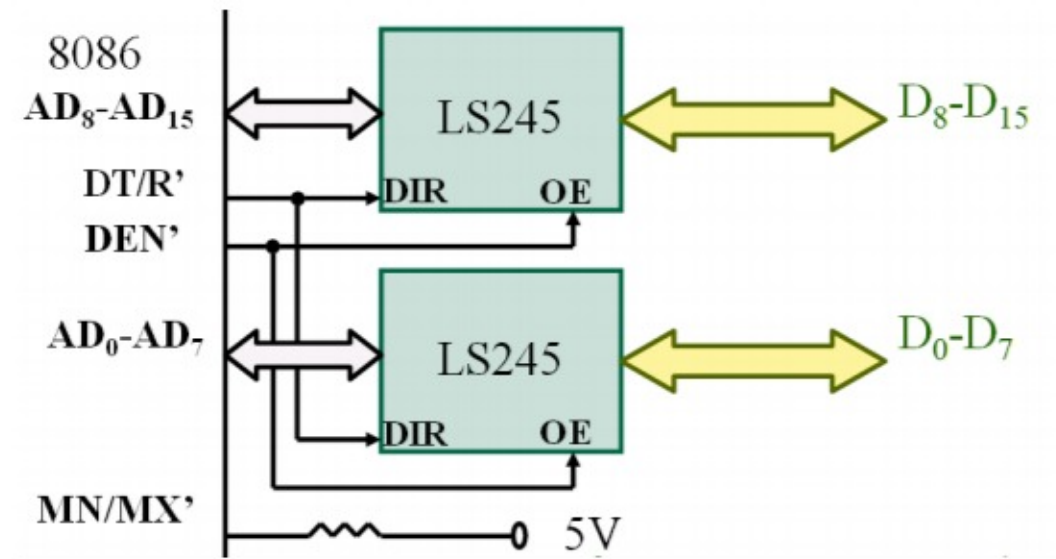
MEMORY INTERFACING



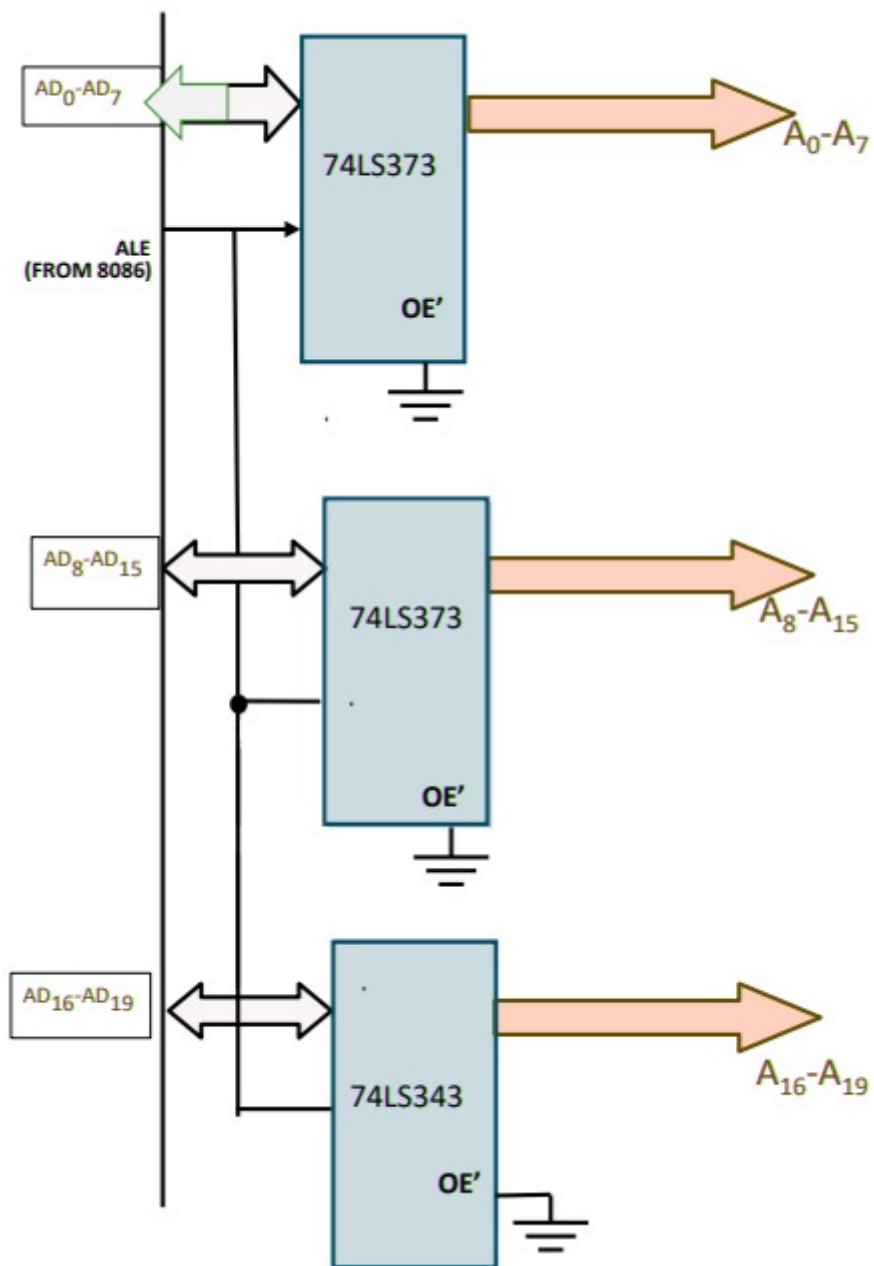
Here RDE' and RDO' signals are generated using OR gate as shown above while ROM and RAM signals are from decoder IC.

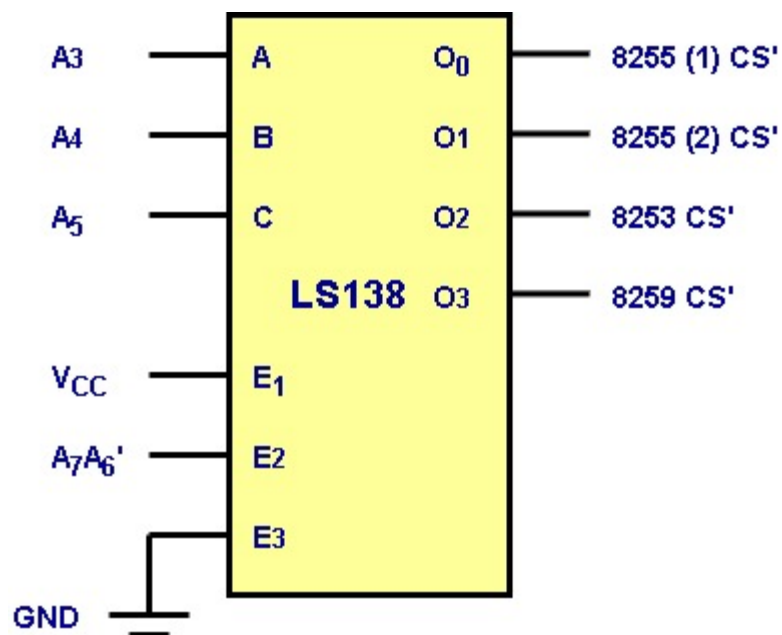


SYSTEM BUS OF 8086



Here DT/R' and DEN' signals are obtained from the microprocessor 8086.

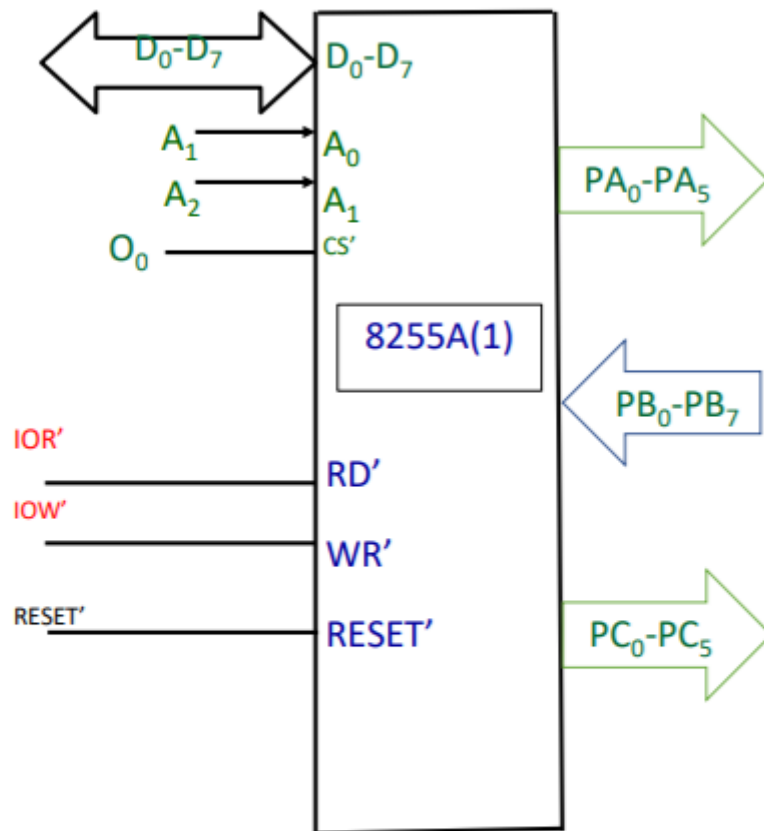




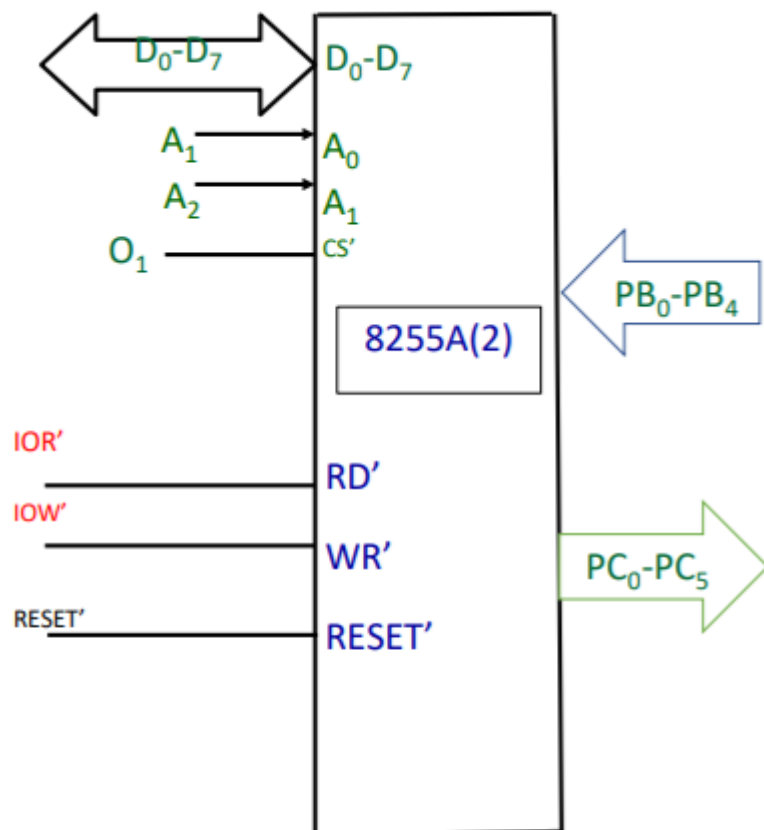
74LS138 is a high speed 1:8

Decoder/Demultiplexer.

Its output O₀, O₁, O₂ and O₃ goes to the CS' input of 8255A(1), 8255A(2), 8253A and 8259 respectively.

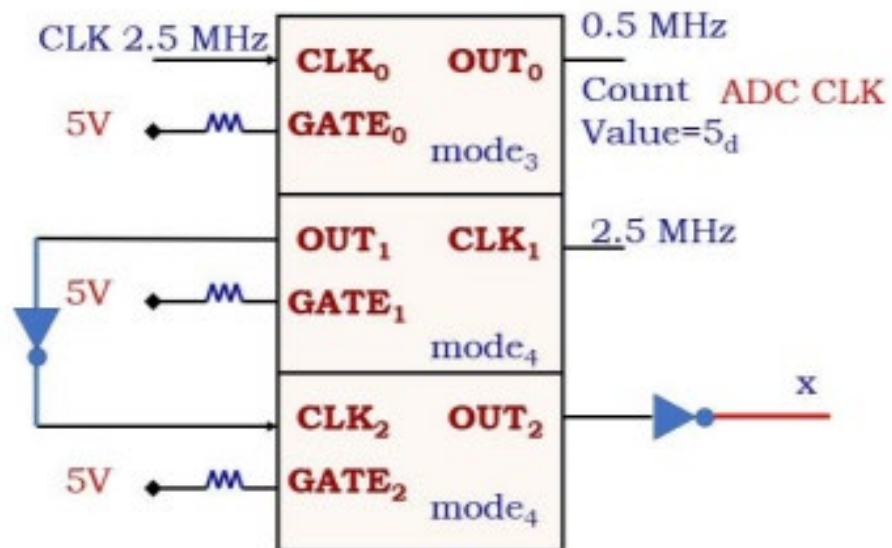
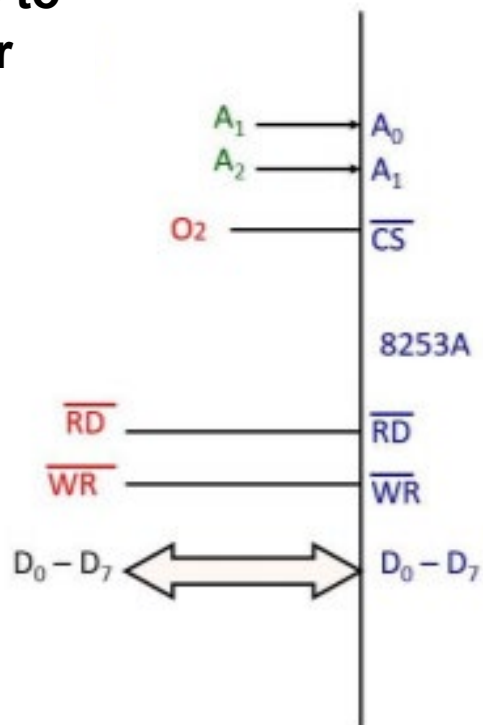


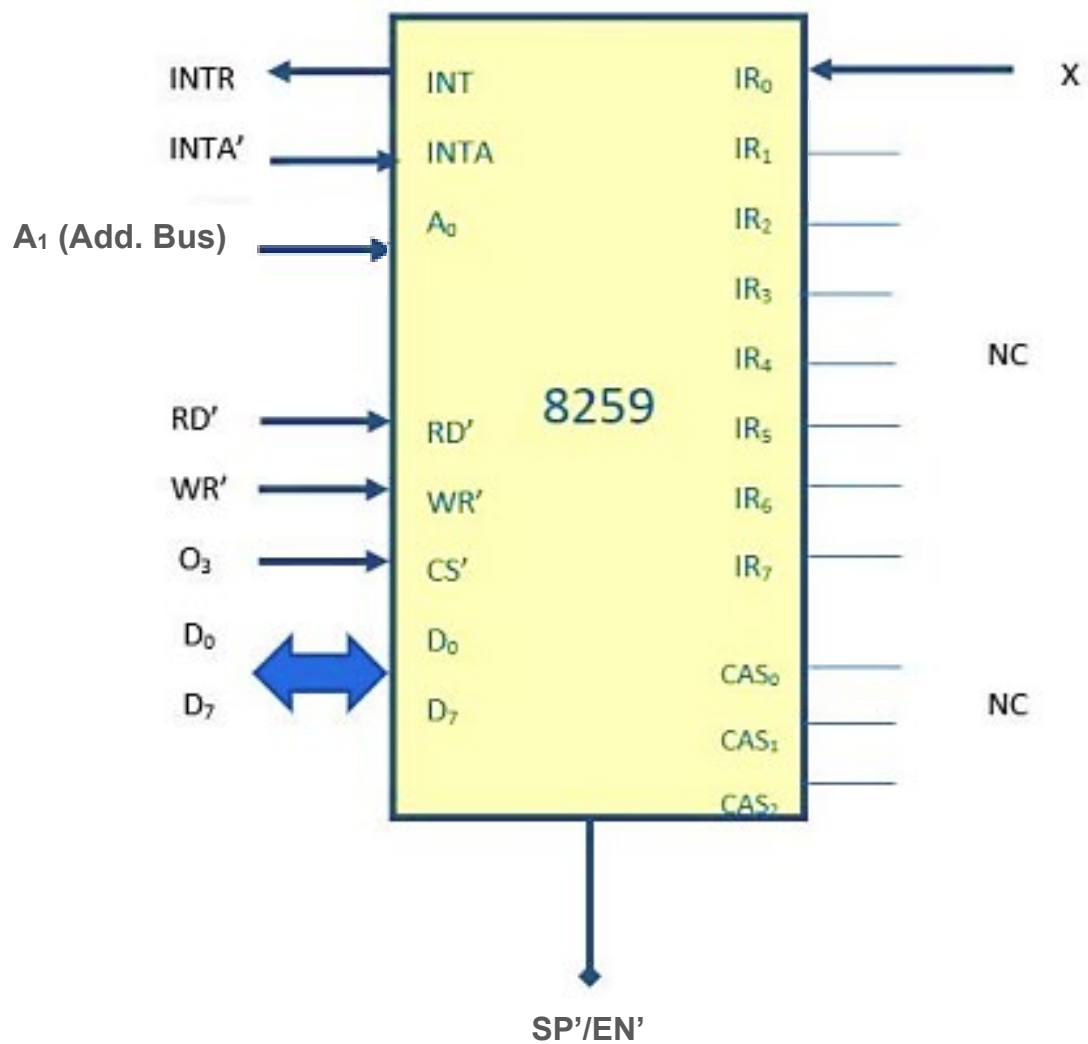
Port C is used for ADC interfacing, BSR

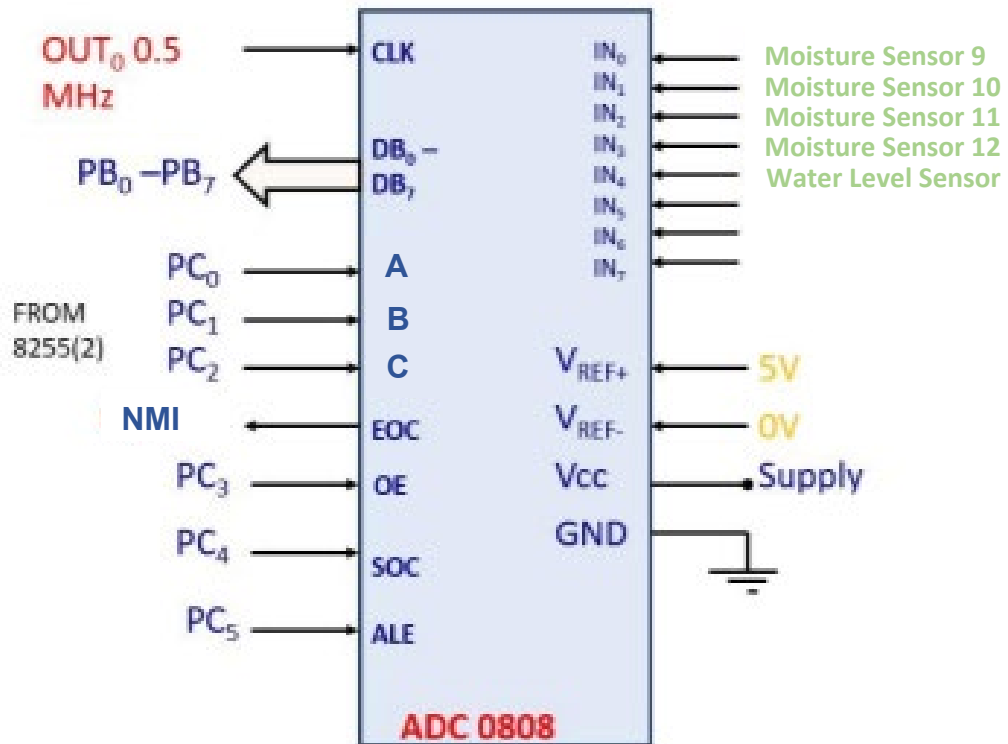
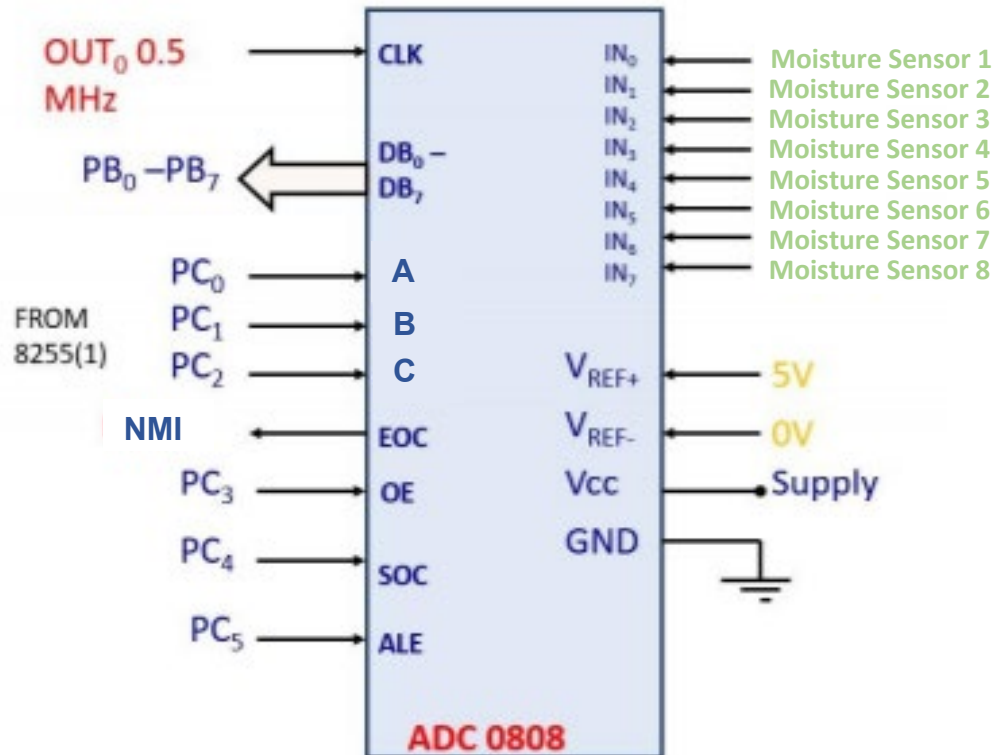


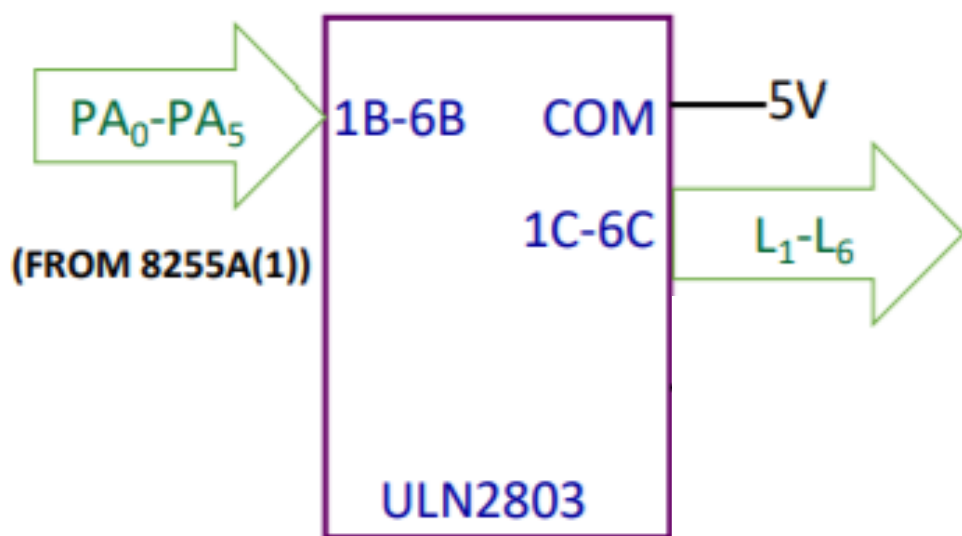
Port C is used for ADC interfacing, BSR

8253A Interface to the processor

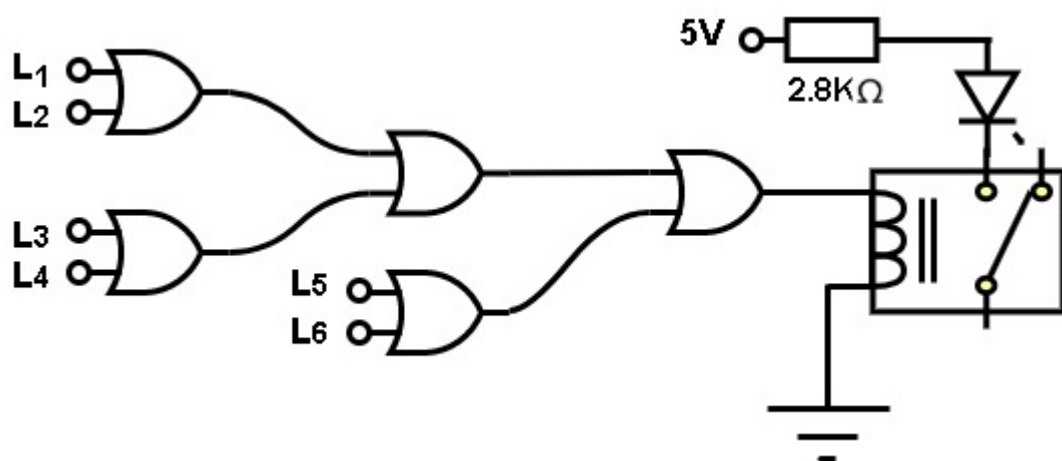








ULN2803 is a Darlington transistor array. It is used as Relay Driver.



L₁, L₂, L₃, L₄, L₅, L₆ from ULN2803

L₁, L₂, L₃, L₄, L₅, L₆
from ULN2803

