Digital electronics and pulse Technique.

Assaignment - 02

ID: 2113030122 1

Question - 01: NAND Gate implementation using AND & NOT Gate

Logic ~~ckt~~ circuit:

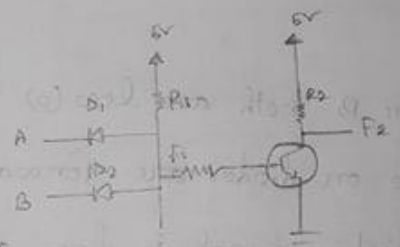

fig: NAND Gate logic circuit.

voltage table:

A	B	D_1	D_2	f_1	f_2
0V	0V	FB	FB	OFF	ON
0V	5V	FB	RB	OFF	ON
5V	0V	RB	FB	OFF	ON
5V	5V	RB	RB	ON	OFF

fig: voltage table for NAND Gate

Description:

=> When A or B both are low (0) then the Respective diode or diodes are forward biased. Then the transistor input is low and transistor is off.

So, current doesn't conduct.

Hence the output (f_2) is high.

=> When A and B both are high the diodes D_1, D_2 are in reversed biased. And we get

high in transistor gate and the transistor become on and current conducts. Hence the output (f2) is low. Now from the voltage table we get a truth table of NAND Gate Here A & B are our input and f2 is our output.

Truth table:

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

fig: Truth table for NAND Gate.

Question + 02: NOR Gate implementation using OR and NOT Gate.

Logic circuit:

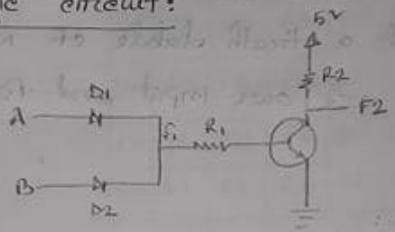

fig: Logic circuit for NOR Gate.

voltage table:

A	B	D_1	D_2	f_1	f_2
0V	0V	RB	RB	OFF	ON
0V	5V	RB	FB	ON	OFF
5V	0V	FB	RB	ON	OFF
5V	5V	FB	FB	ON	OFF

fig: voltage table for NOR Gate.

Description:

=> when A and B both are low then there no current is flowed by f_2.

Hence the transistor input is low and it become off and the output f_2 become high.

=> when either A or B or both A and B are high then the diode or diodes are forward biased respectively. Then the transistor get high input and it become on and current conducts. Hence the output F_2 is low

Truth table:

A	B	f_2
0	0	1
0	1	0
1	0	0
1	1	0

fig: Truth table for NOR Gate.