Operation Of VGA Display

Workshop

Lab 04

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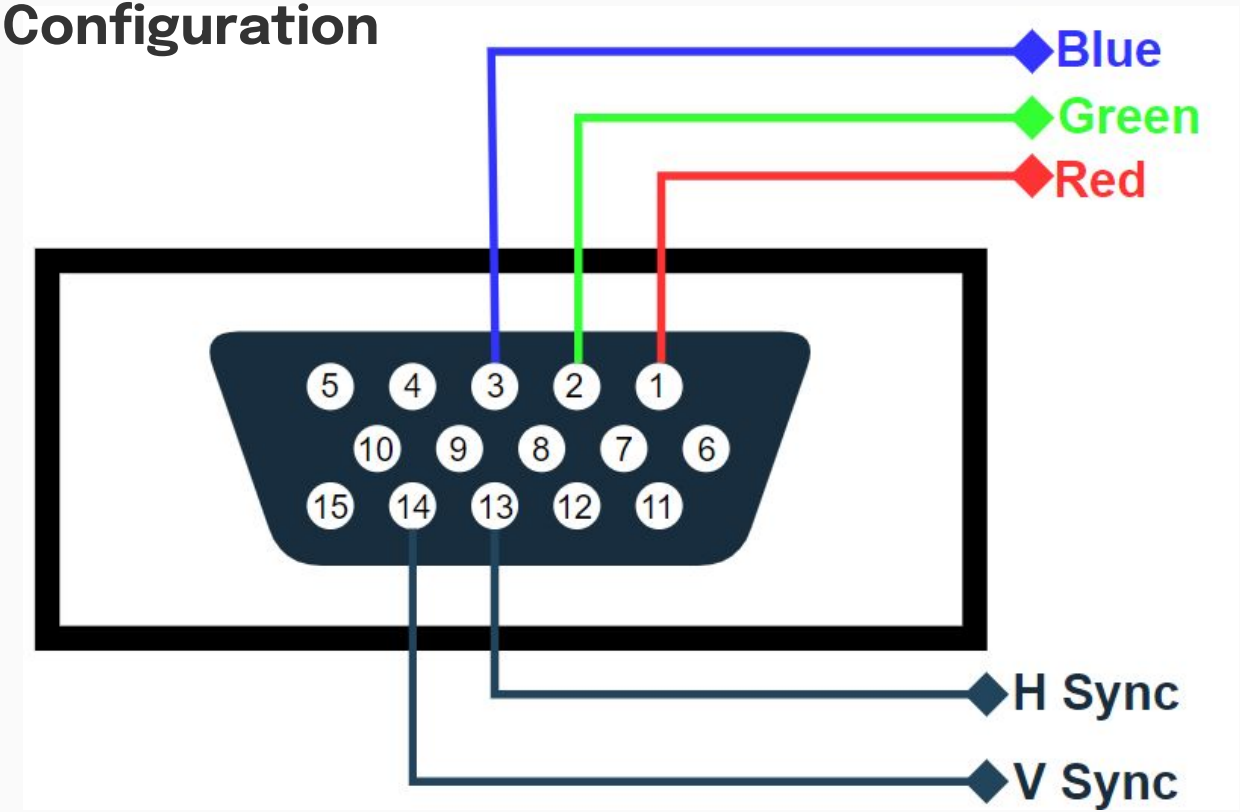
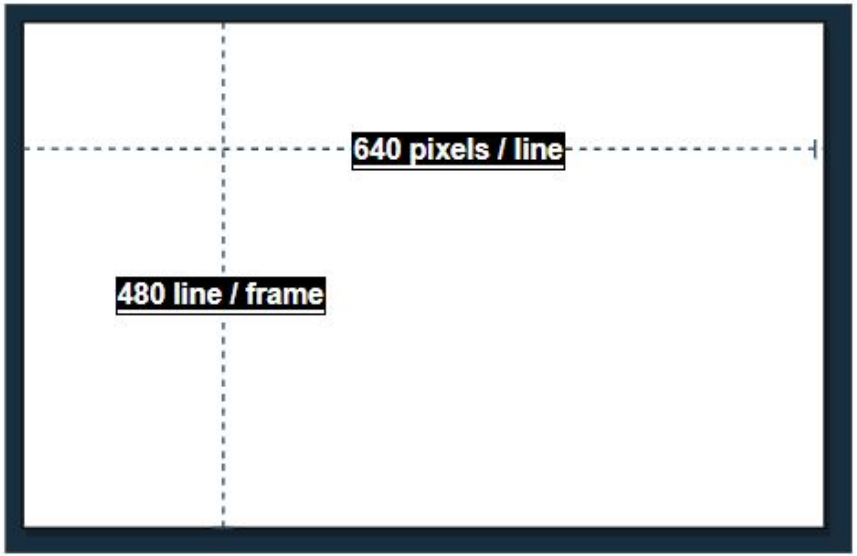
VGA Pin Configuration

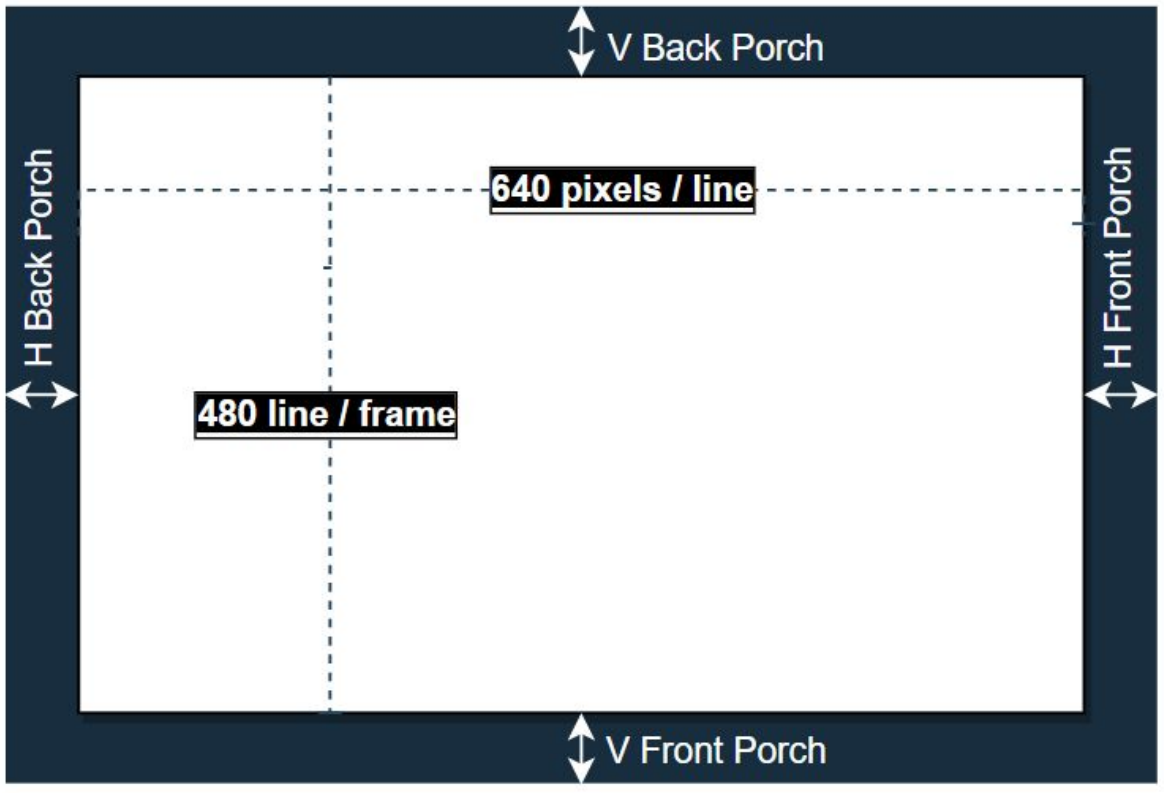


VGA Basics

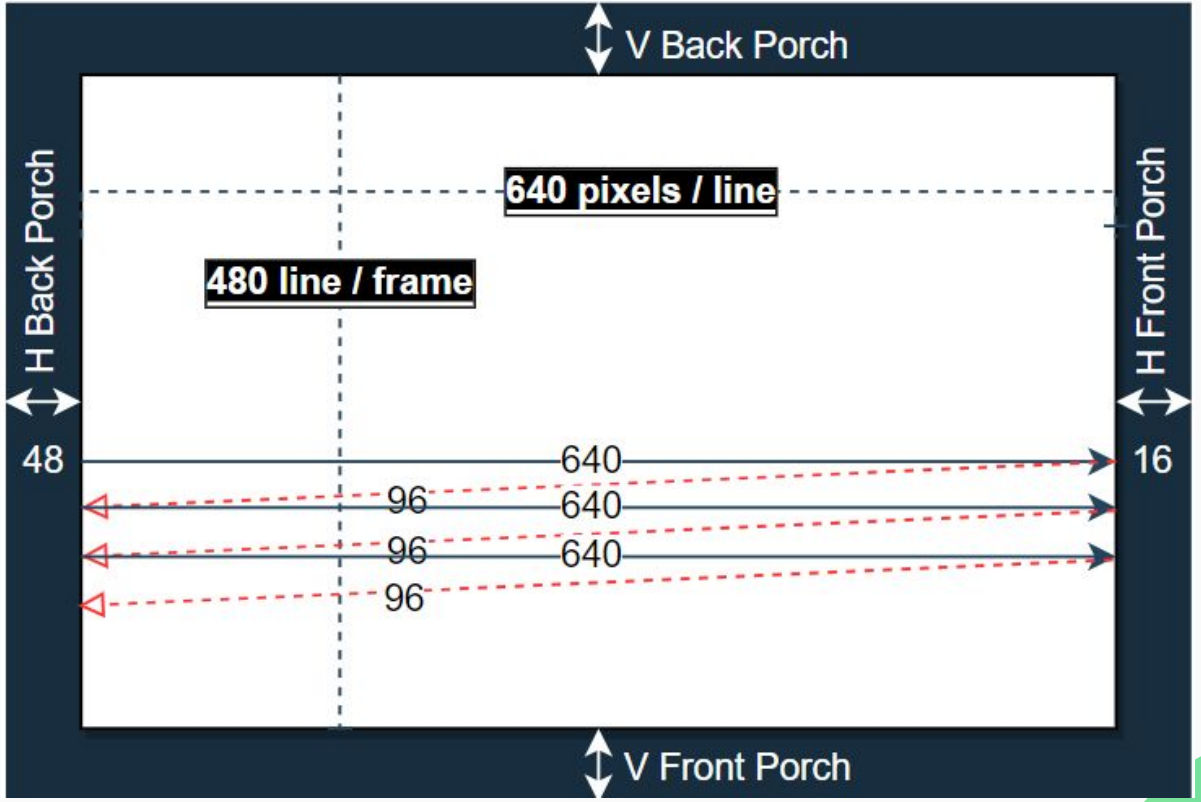
In this example, we are considering a screen resolution of 640x480. All further information will be based on this resolution. First, let's understand what 640x480 means: 640 represents the visible pixels per line, and 480 denotes the number of lines, as shown in the diagram below:



VGA Basics


V Back Porch
H Back Porch
640 pixels / line
H Front Porch
480 line / frame
V Front Porch

VGA Basics

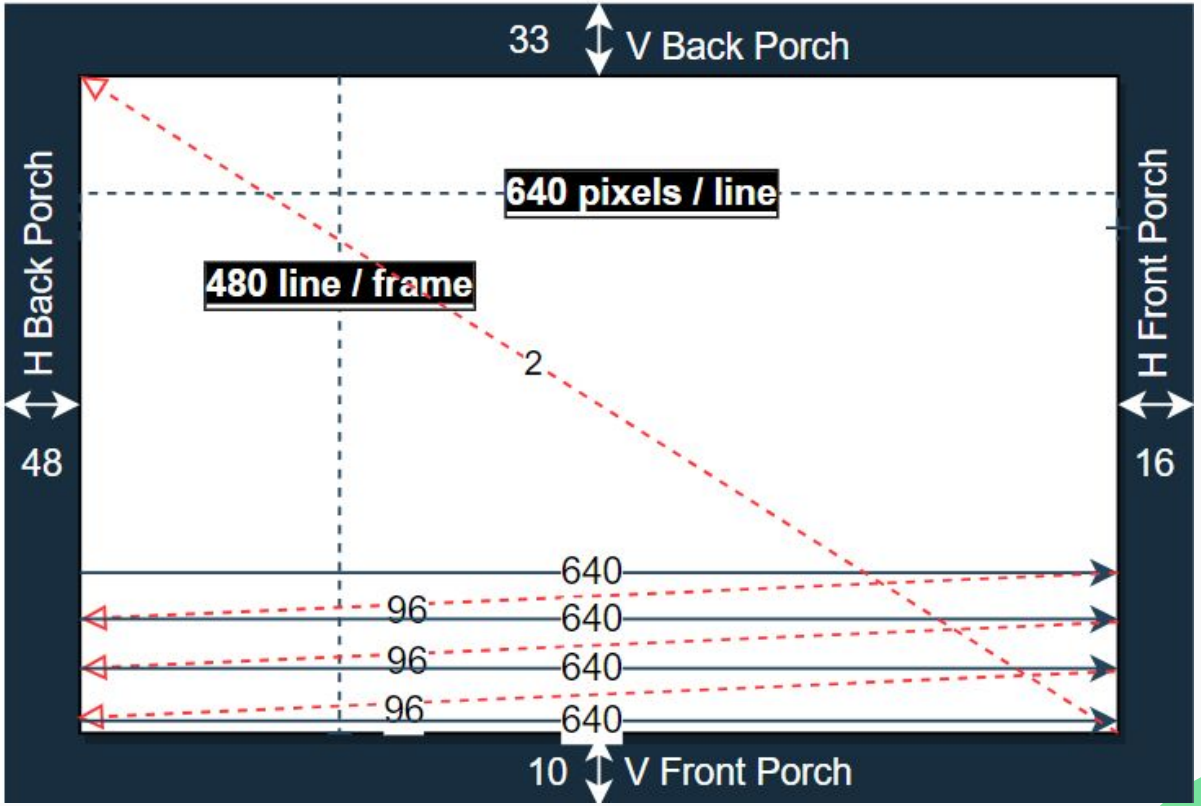

V Back Porch
H Back Porch
640 pixels / line
480 line / frame
H Front Porch
48
640
16
96
640
96
640
96
V Front Porch

VGA Basics

In the previous diagram, we initially calculate the total number of cycles required to complete the pixels for one line. The HSync signal returns to the beginning of the next line, necessitating a horizontal back porch of 48 cycles. With 640 horizontal pixels, 16 cycles are allocated for the horizontal front porch, and an additional 96 cycles are required to return to the start of the next line.

The calculation is as follows:
48 (horizontal back porch) + 640 (horizontal pixels) + 16 (horizontal front porch) + 96 (return to the next line) = 800, which equals one horizontal cycle (1H cycle).

VGA Basics


33
V Back Porch
H Back Porch
48
640 pixels / line
480 line / frame
2
H Front Porch
16
640
96
640
96
640
96
640
10
V Front Porch

VGA Basics

In the previous diagram, we initially calculate the total number of cycles required to complete the 480 lines per frame. The VSync signal returns to the beginning of the frame, necessitating a vertical back porch of 33 cycles. With 480 vertical line, 10 cycles are allocated for the vertical front porch, and an additional 2cycles are required to return to the start of the frame.

The calculation is as follows:
33 (vertical back porch) + 480 (vertical lines) + 10 (vertical front porch) + 2 (return to the beginning of the frame) = 525.

VGA Basics

VGA Horizontal Timing Analysis

In the diagram below, we observe that the first 96 clocks are allocated for returning to the start of the next line. Throughout this entire period, the HSync signal remains at 1. Following this, there's a horizontal back porch of 48 cycles where the HSync signal switches to 0. This marks the start of the visible display for 640 clock cycles, during which we can modify the values of red, green, and blue. Afterward, the horizontal front porch begins for 16 clocks, during which time both HSync and RGB return to low again.

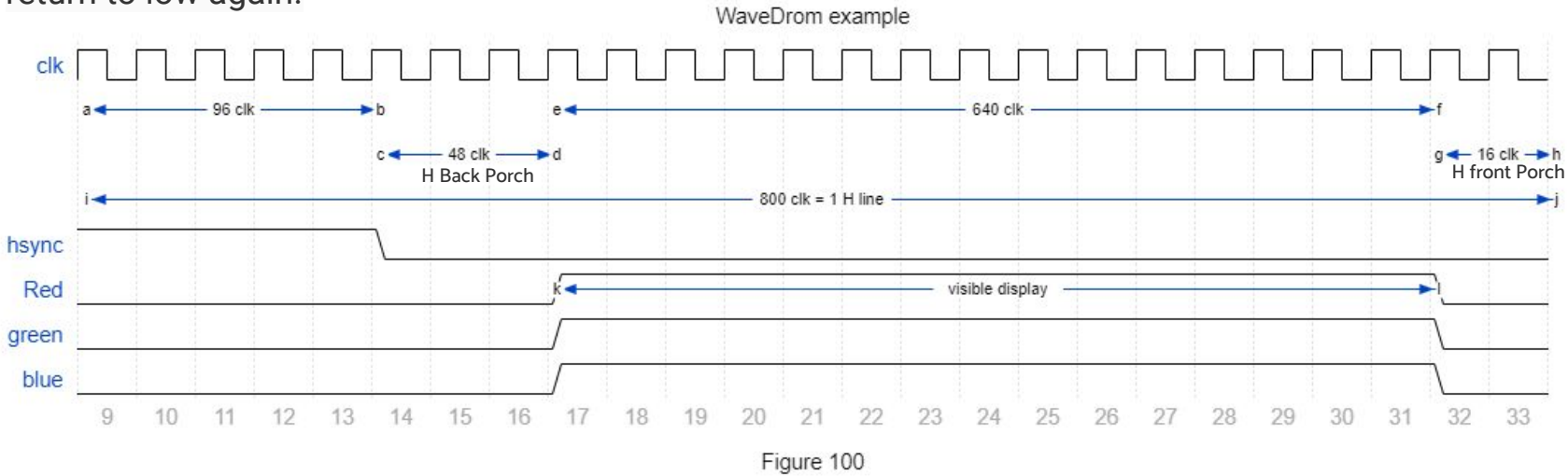


Figure 100

VGA Basics

VGA Vertical Timing Analysis

In the diagram below, we observe that the first 2 hsync are allocated for returning to the start of the frame. Throughout this entire period, the VSync signal remains at 1. Following this, there's a vertical back porch of 33 hsync where the VSync signal switches to 0. This marks the start of the visible display for 480 hsync cycles, during which we can modify the values of red, green, and blue. Afterward, the vertical front porch begins for 10 hsync, during which time both VSync and RGB return to low again.

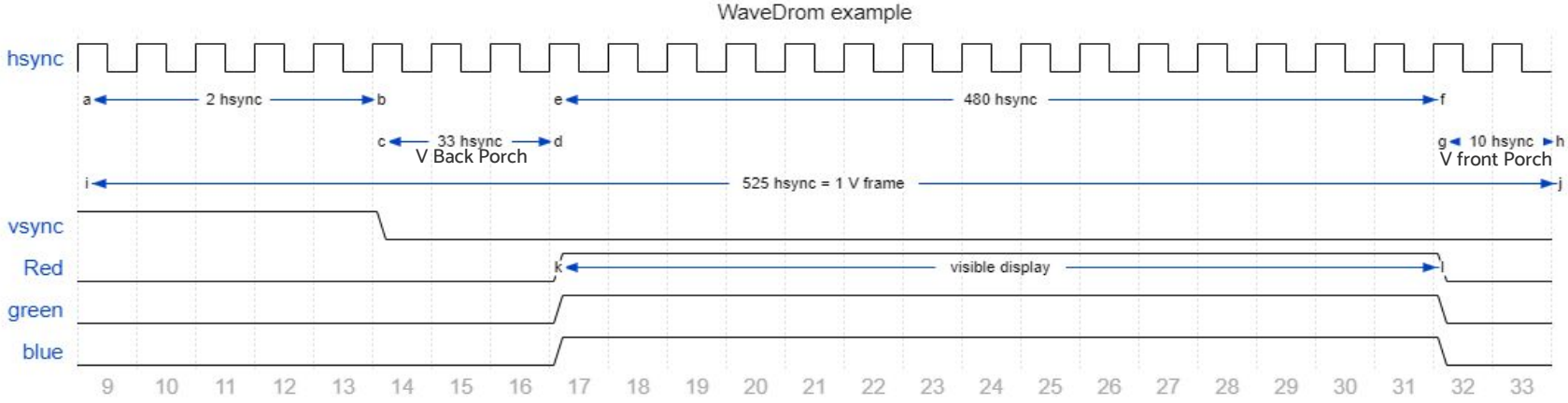


Figure 100

VGA Basics

Task

The task is to display a basic output on the screen. The screen will be divided into three sections vertically. With 480 pixels along the y-axis, dividing it by 3 gives 160 pixels per section. The display will showcase red from 1 to 160, green from 161 to 320, and blue from 321 to 480, just as illustrated in the diagram below. Clk frequency should be **25Mhz.** For tang nano 9k default clock is 27MHz so we need to convert it to 25Mhz clk frequency by adding PLL and clk divider IP from gowin.

Source Code Reference Github Abdul Muheet Ghani

Testimonial

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Sponsored By:

Edmund from Symbiotic EDA. for sponsoring FPGA.

Thanks:

Lushay Lab (They've provided crucial resources and guidance throughout the project), Also thanks to Slidesgo.

Future Work

This is version 1.0 of our course. We will continue this training and very soon release further versions. For any questions or to stay connected with us.

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