RISC-V SoC and Firmware Development

Lab: 02

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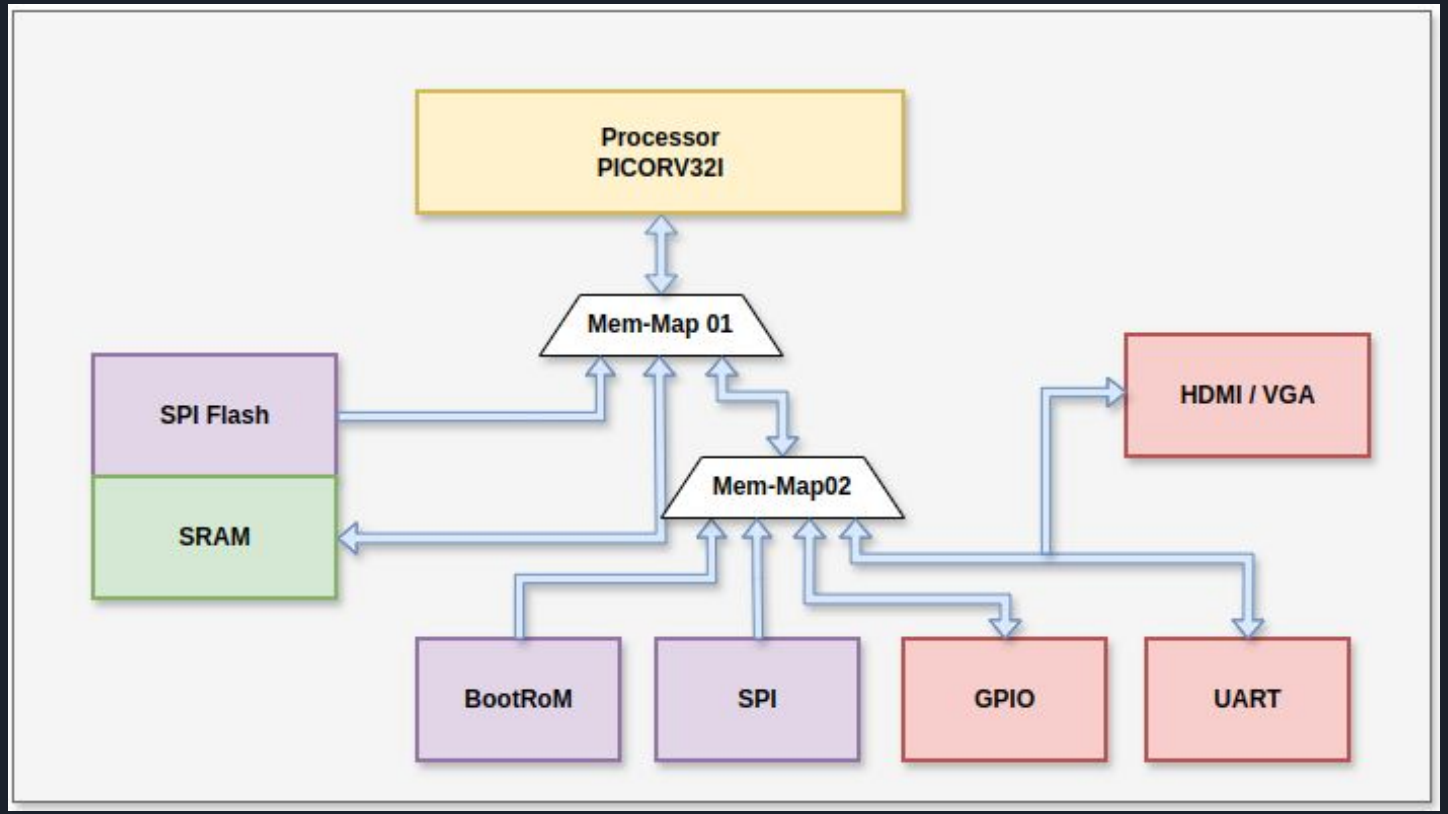
Picotiny SoC Overview.

- **A System on Chip (SoC)** is an integrated circuit that combines all the essential components of a computer or electronic system onto a single chip. SoCs typically include a processor (such as a CPU or microcontroller), memory, input/output (I/O) ports, and various other components, and interfaces for peripheral devices, all connected by a system bus. The main advantage of an SoC is that it consolidates multiple functions into one compact design, resulting in increased efficiency, reduced power consumption, and lower production costs compared to using multiple separate chips.
- SoCs are commonly used in mobile devices, IoT devices, and embedded systems, where space and power efficiency are essential.

Picotiny SoC Overview.

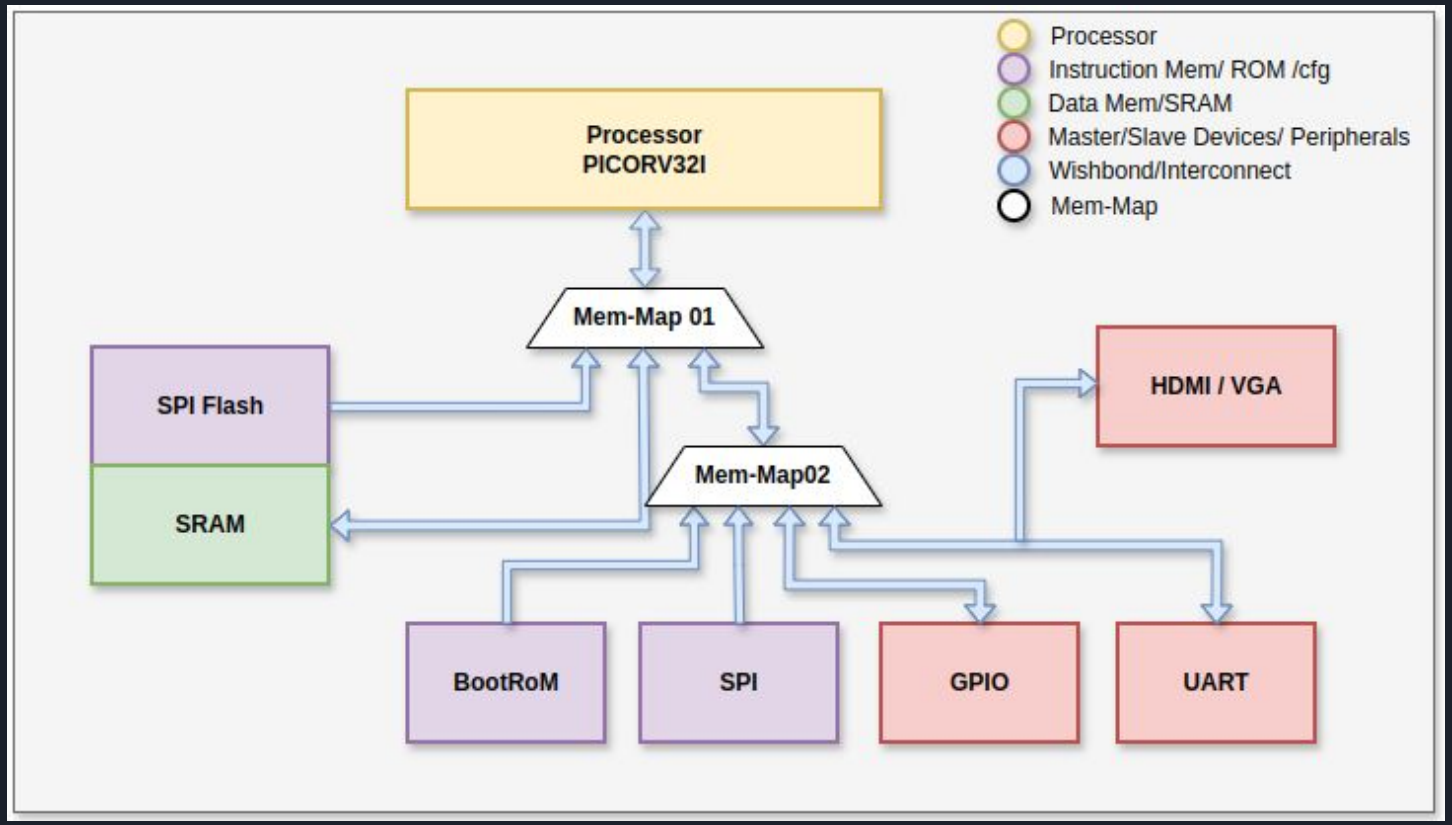


Picotiny SoC Overview.

Peripherals:

- Peripherals are external devices that are connected to a central processing unit (CPU) to perform various tasks such as taking input from external devices or sending output to external devices.
- The primary goal is to interact CPU with external devices such as keyboard,mouse,screen,sensors e.t.c through peripherals.

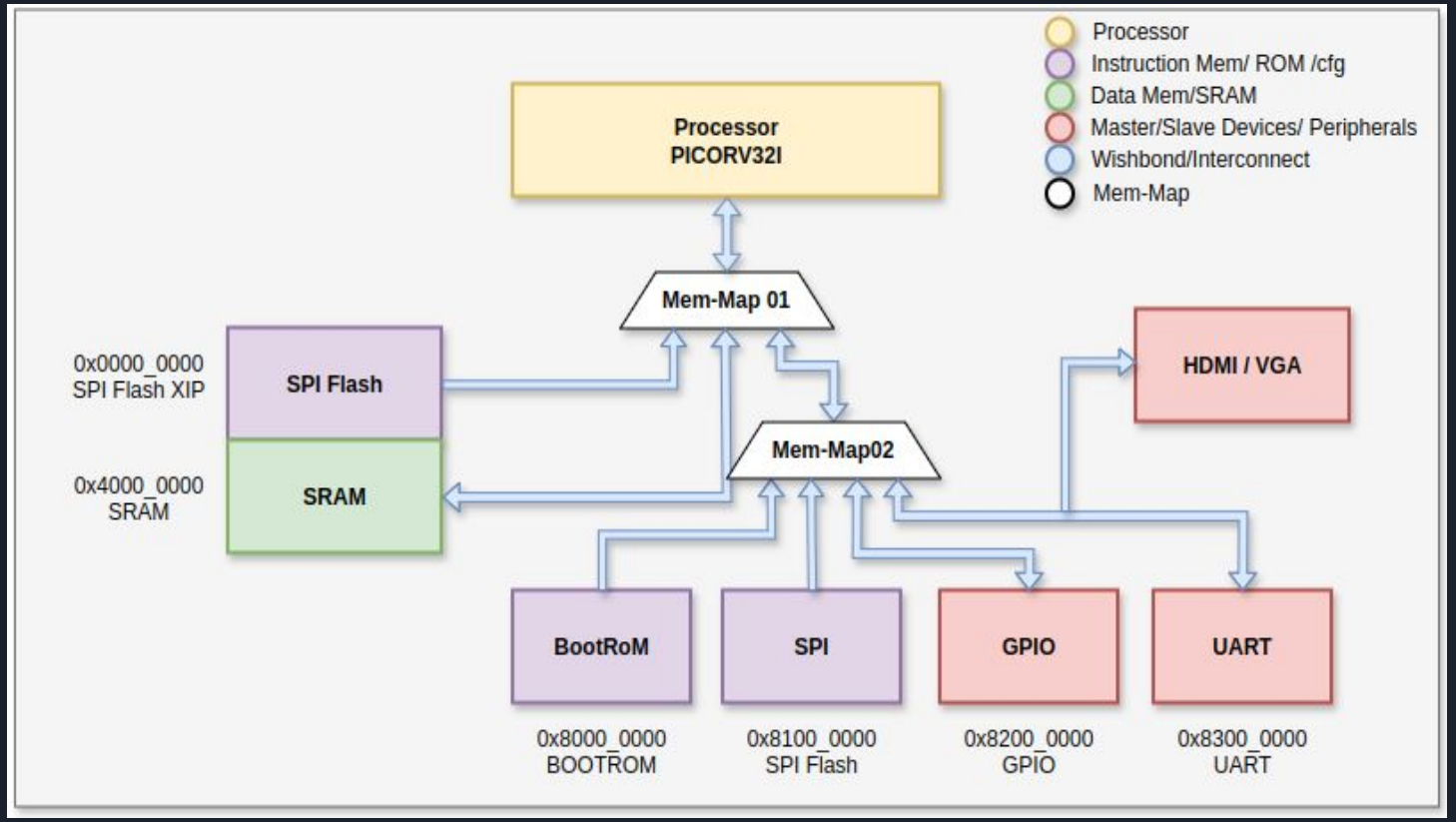
Picotiny SoC Overview.



Memory-Map.

- **A memory map** in computing defines how a system's memory and hardware resources are organized and accessed. It provides a structured layout, mapping specific memory addresses to particular functions, peripherals, or types of data. This mapping allows the processor and software to interact with various parts of the system, such as RAM, ROM, and input/output (I/O) devices, by reading from or writing to specific memory addresses.

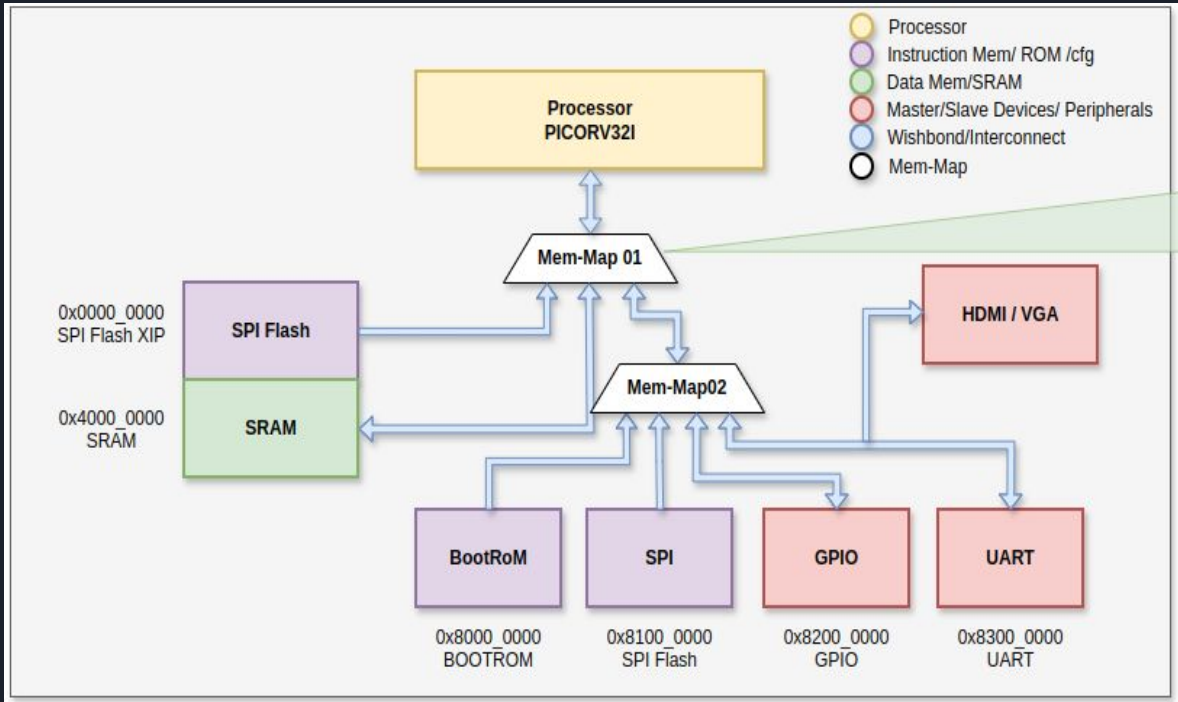
Memory-Map.


Processor
Instruction Mem/ ROM /cfg
Data Mem/SRAM
Master/Slave Devices/ Peripherals
Wishbond/Interconnect
Mem-Map
Processor
PICORV32I
Mem-Map 01
Mem-Map02
0x0000_0000
SPI Flash XIP
SPI Flash
0x4000_0000
SRAM
SRAM
HDMI / VGA
BootRoM
SPI
GPIO
UART
0x8000_0000
BOOTROM
0x8100_0000
SPI Flash
0x8200_0000
GPIO
0x8300_0000
UART

Memory-Map.

Memory-Map 01		
01	0x0000_0000	SPI Flash XIP
02	0x4000_0000	SRAM
03	0x8000_0000	Peripherals
Memory-Map 02		
01	0x8000_0000	BOOTROM
02	0x8100_0000	SPI Flash
03	0x8200_0000	GPIO
04	0x8300_0000	UART

Memory-Map.



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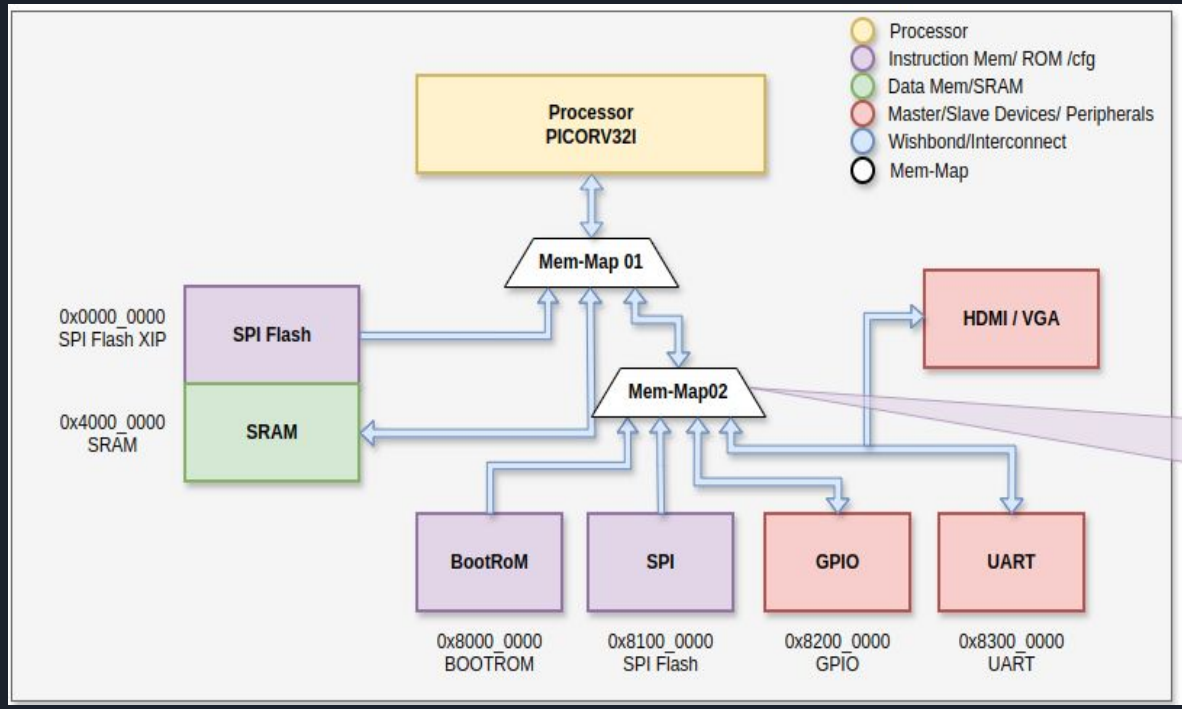

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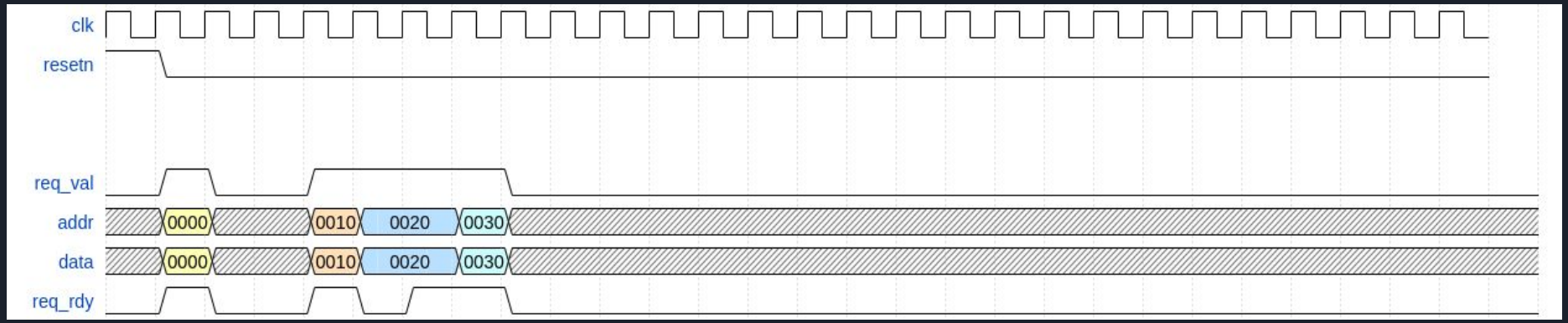
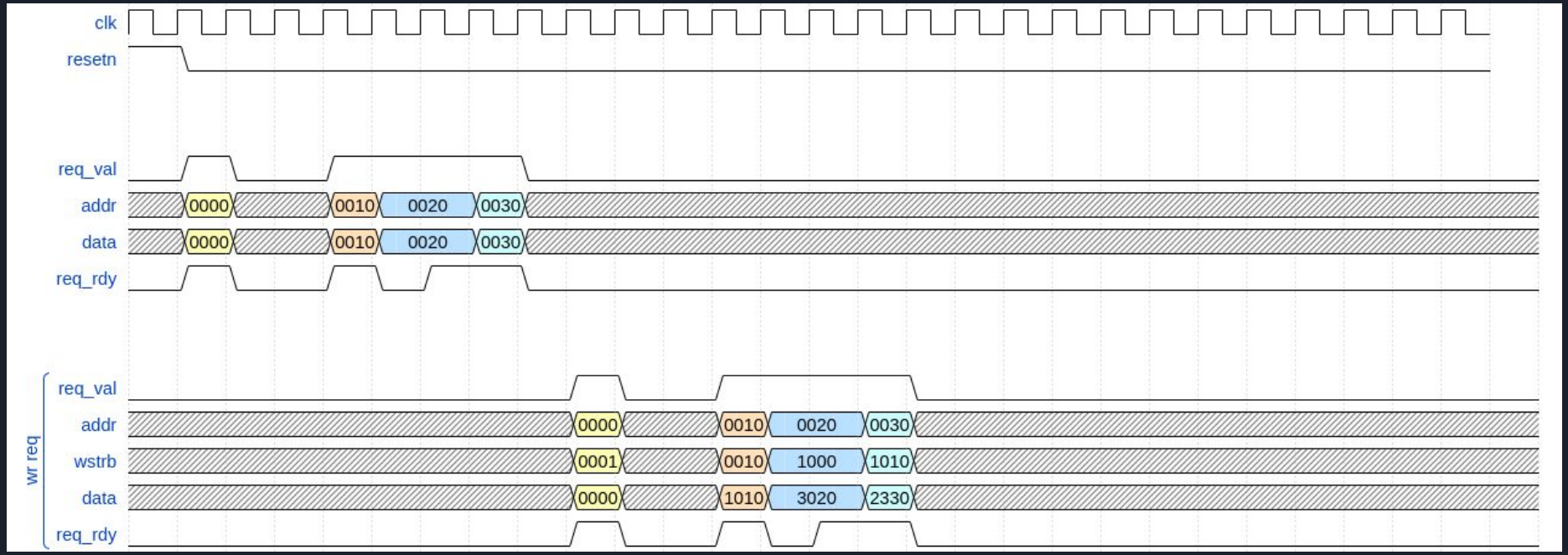
Wishbone Bus Protocol.

- The Wishbone Bus Protocol is an open-source, simple, and flexible system-on-chip (SoC) interconnect standard. Developed to provide a method for connecting various intellectual property (IP) cores within an SoC, Wishbone facilitates communication between different components, such as processors, memory controllers, and I/O interfaces.

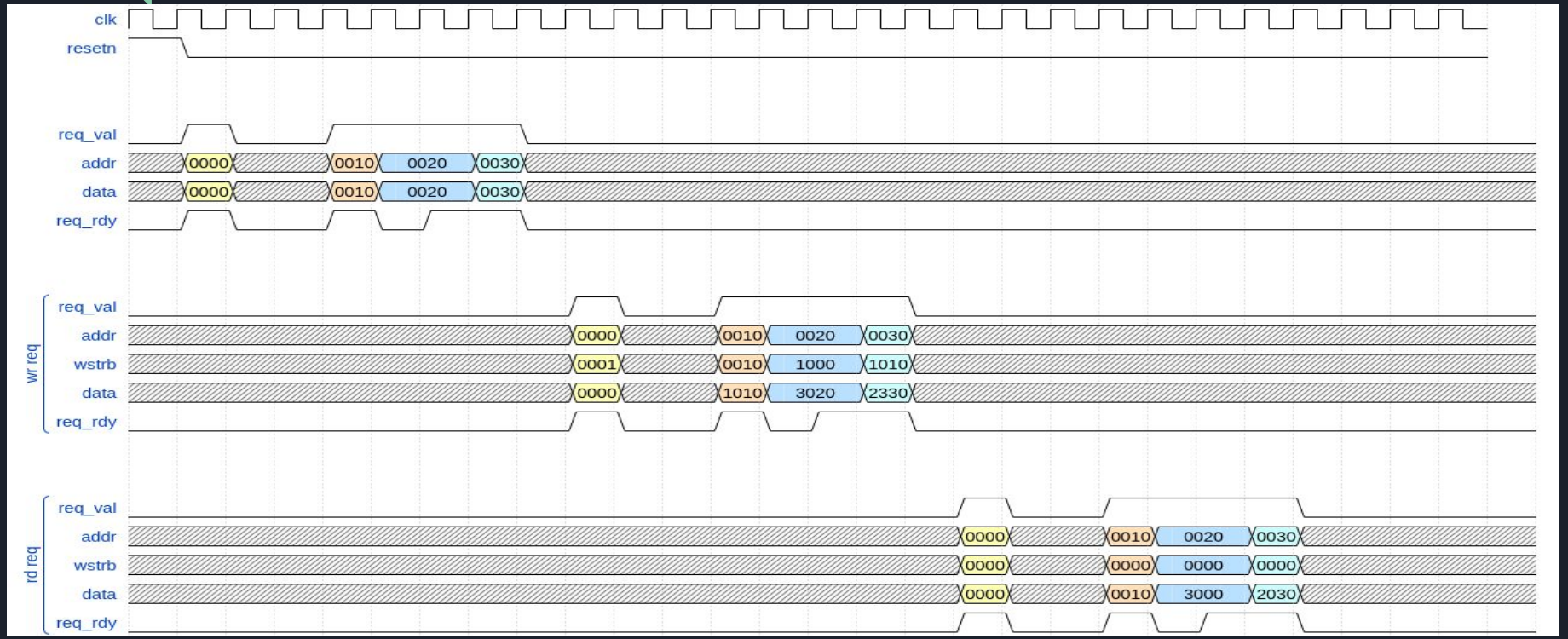
Wishbone Bus Protocol.



Wishbone Bus Protocol.



Wishbone Bus Protocol.



TESTIMONIAL

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