RISC-V SoC and Firmware Development

Lab: 03

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- BootFlow, Clk, PLL, Reset.

SoC Peripherals.

- Compact, lightweight System on Chip (SoC) based on RISC-V architecture Integrates a RISC-V core with essential peripherals

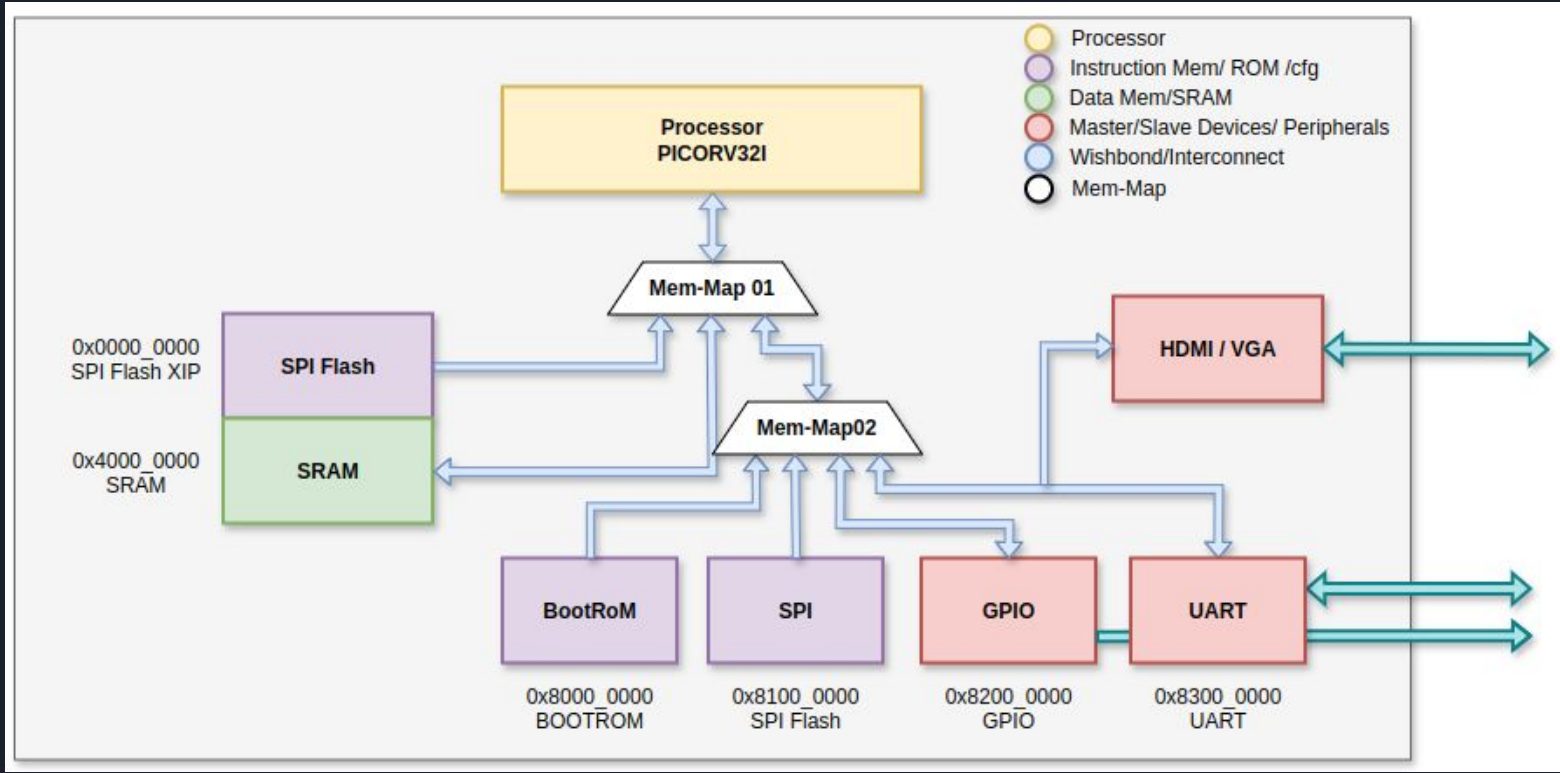
PERIPHERALS

- UART (Universal Asynchronous Receiver-Transmitter) GPIO (General Purpose Input/Output)
- Boot RAM,flash SPI,GPIOs

Role in project

- Serves as the central processing unit for managing game logic
- Handles interactions between the FPGA and external interfaces.
- HDMI for display the game
- UART for keyboard input for game

SoC Peripherals.



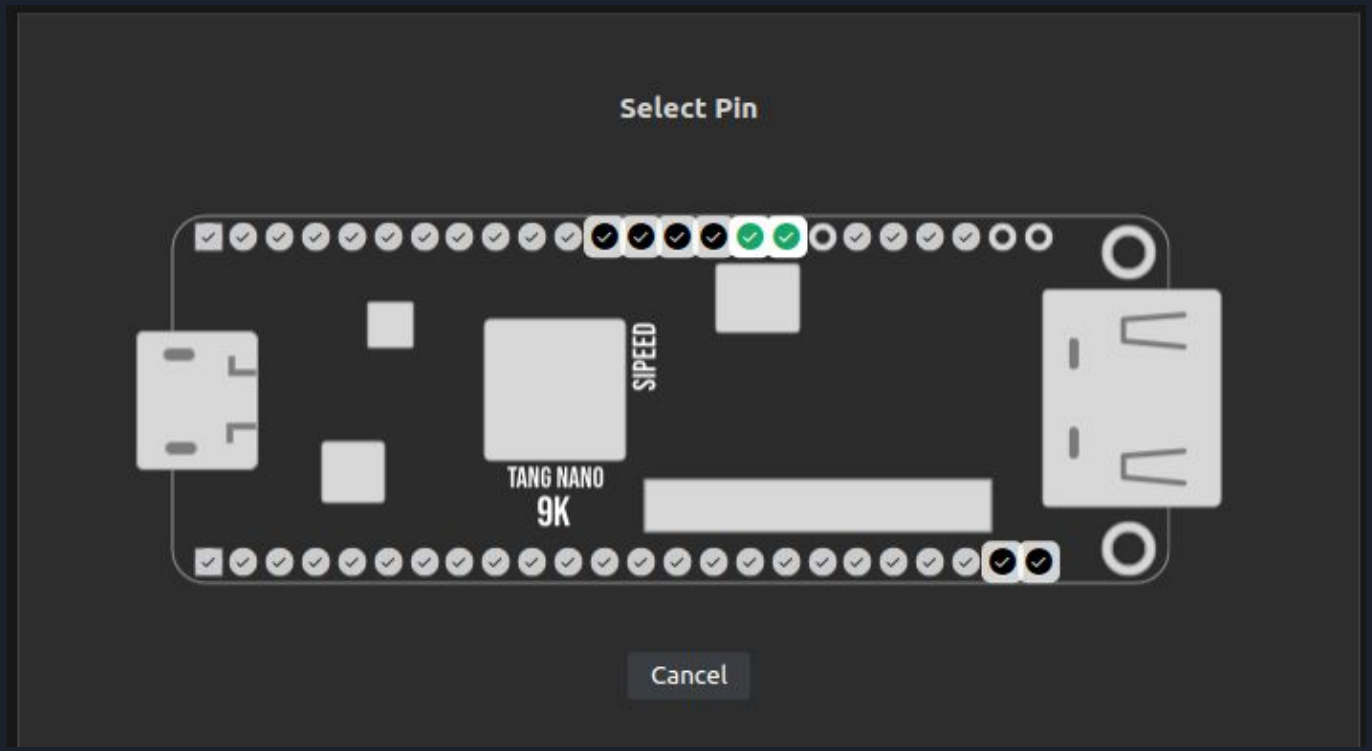
SoC Peripherals.

Constraints

+ Add From Template + Add Constraint

PORT NAME	LOCATION	PORT OPTIONS
tmds_d_p[0]	71,70	8ma Drive
tmds_d_p[1]	73,72	8ma Drive
tmds_d_p[2]	75,74	8ma Drive
tmds_clk_p	69,68	8ma Drive
ser_tx	17	8ma Drive, Pull Up, LVCMOS33
flash_csb	60	8ma Drive, Pull Up, LVCMOS33
flash_clk	59	8ma Drive, Pull Up, LVCMOS33
gpio[6]	3	8ma Drive, Pull Up
gpio[5]	16	8ma Drive, Pull Up
gpio[4]	15	8ma Drive, Pull Up
gpio[3]	14	8ma Drive, Pull Up
gpio[2]	13	8ma Drive, Pull Up
gpio[1]	11	8ma Drive, Pull Up
gpio[0]	10	8ma Drive, Pull Up
flash_miso	62	8ma Drive, Pull Up, LVCMOS33
flash_mosi	61	8ma Drive, Pull Up, LVCMOS33
ser_rx	18	Pull Up, LVCMOS33
resetn	4	Pull Up
clk	52	Pull Up, LVCMOS33

SoC Peripherals.



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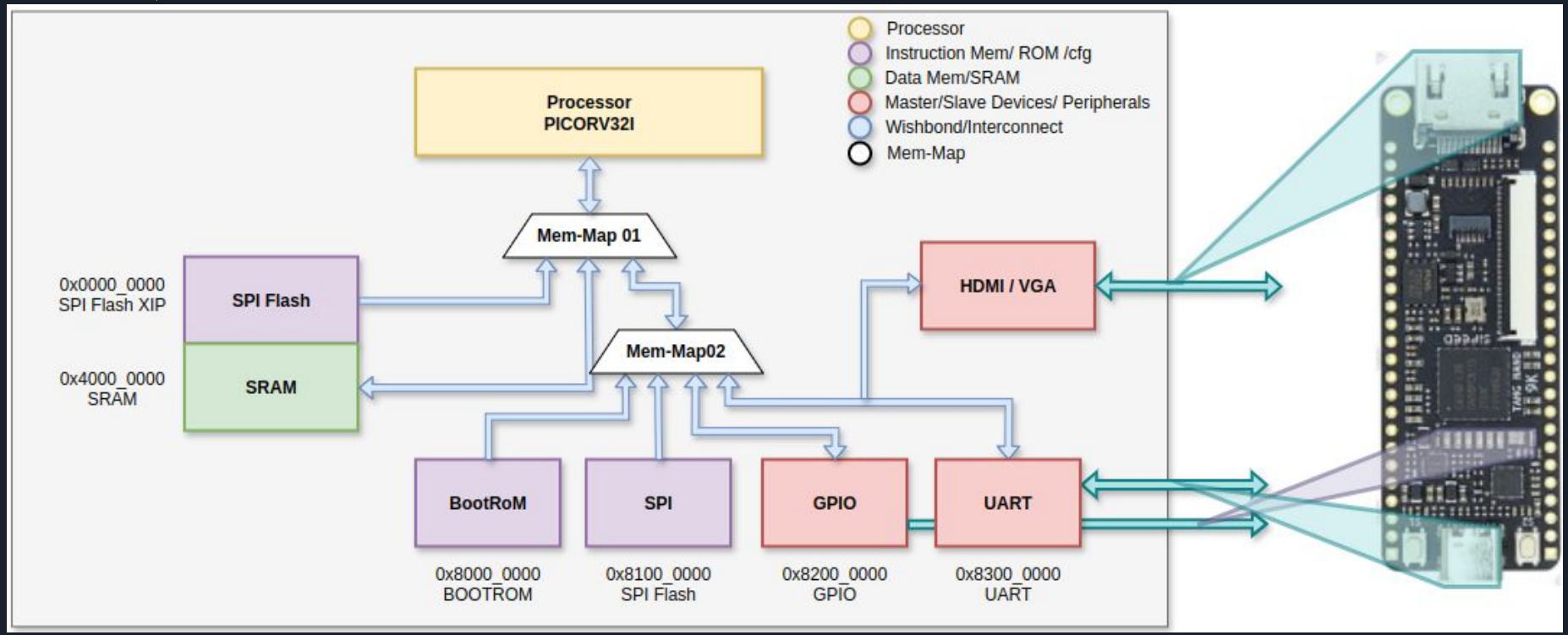
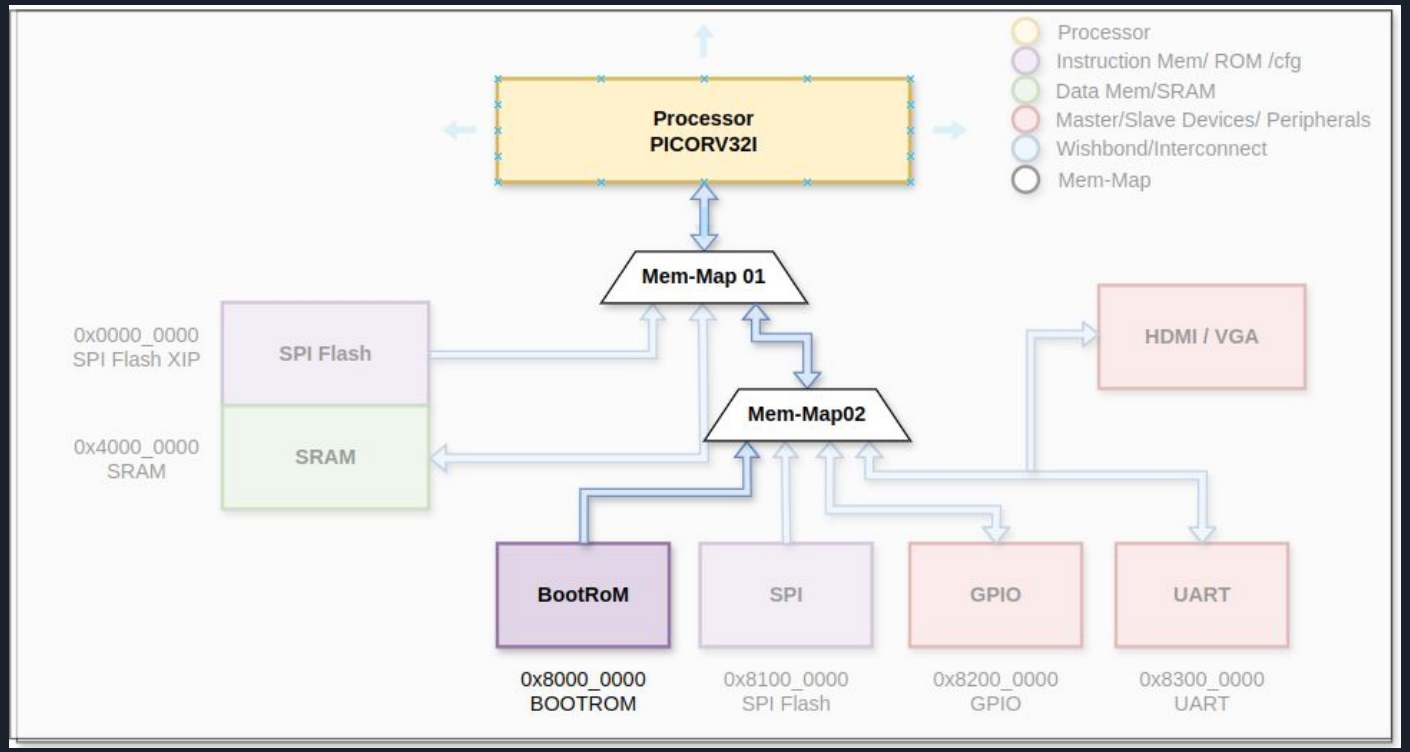


BootFlow, Clk, PLL, Reset.



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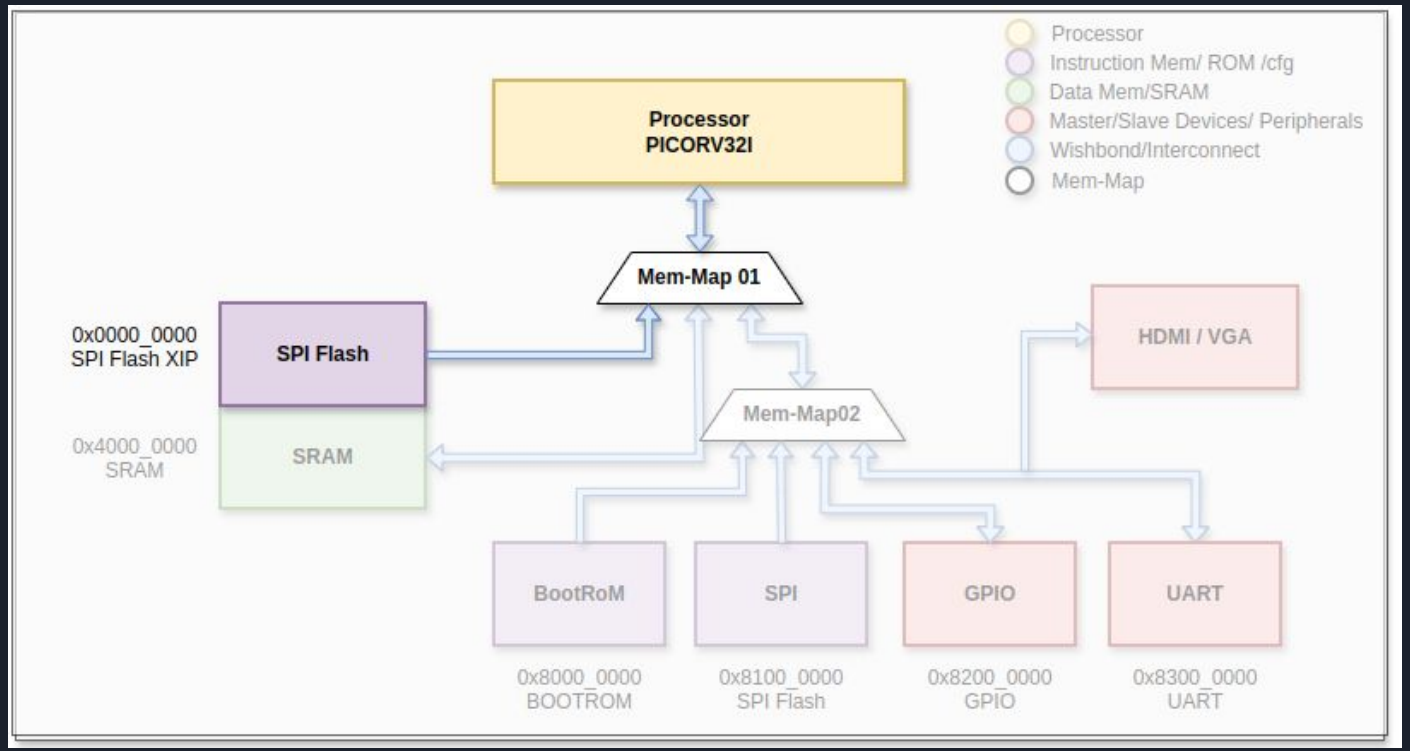

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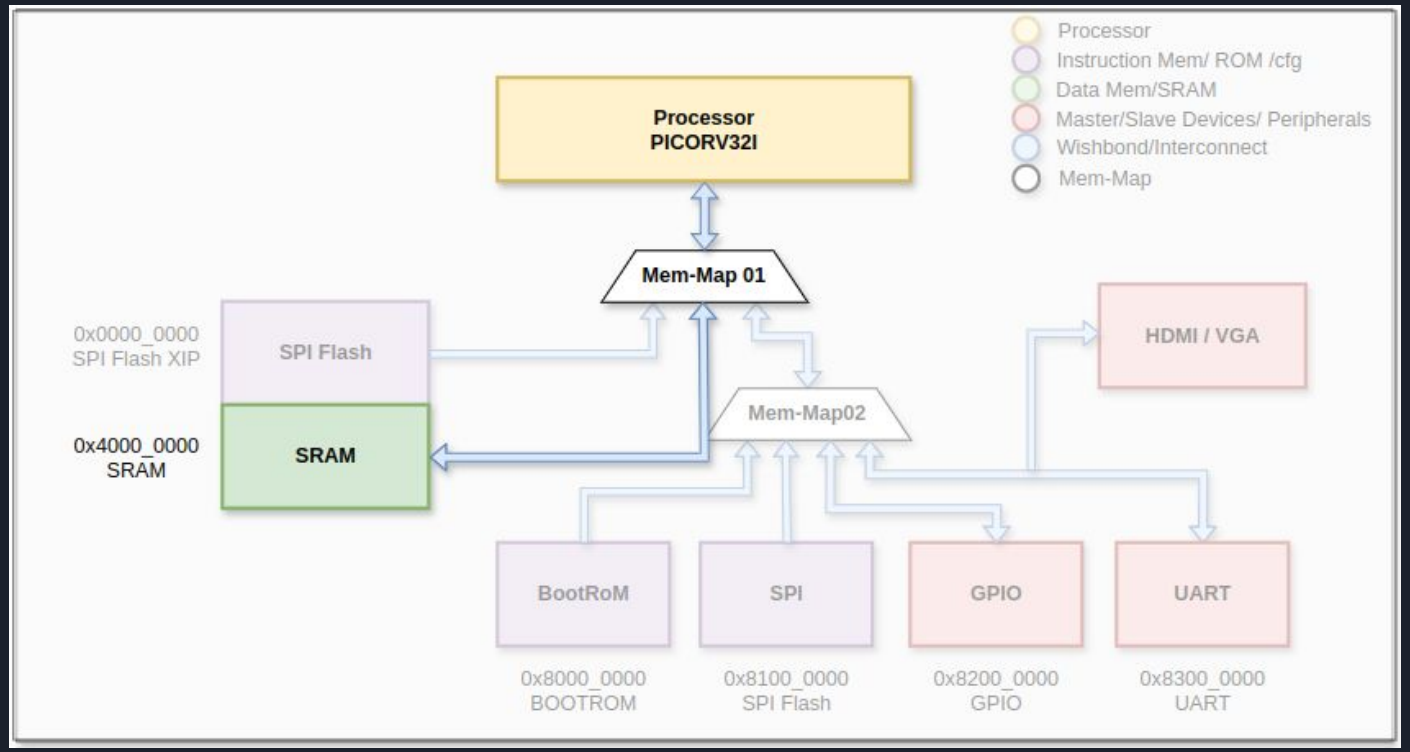

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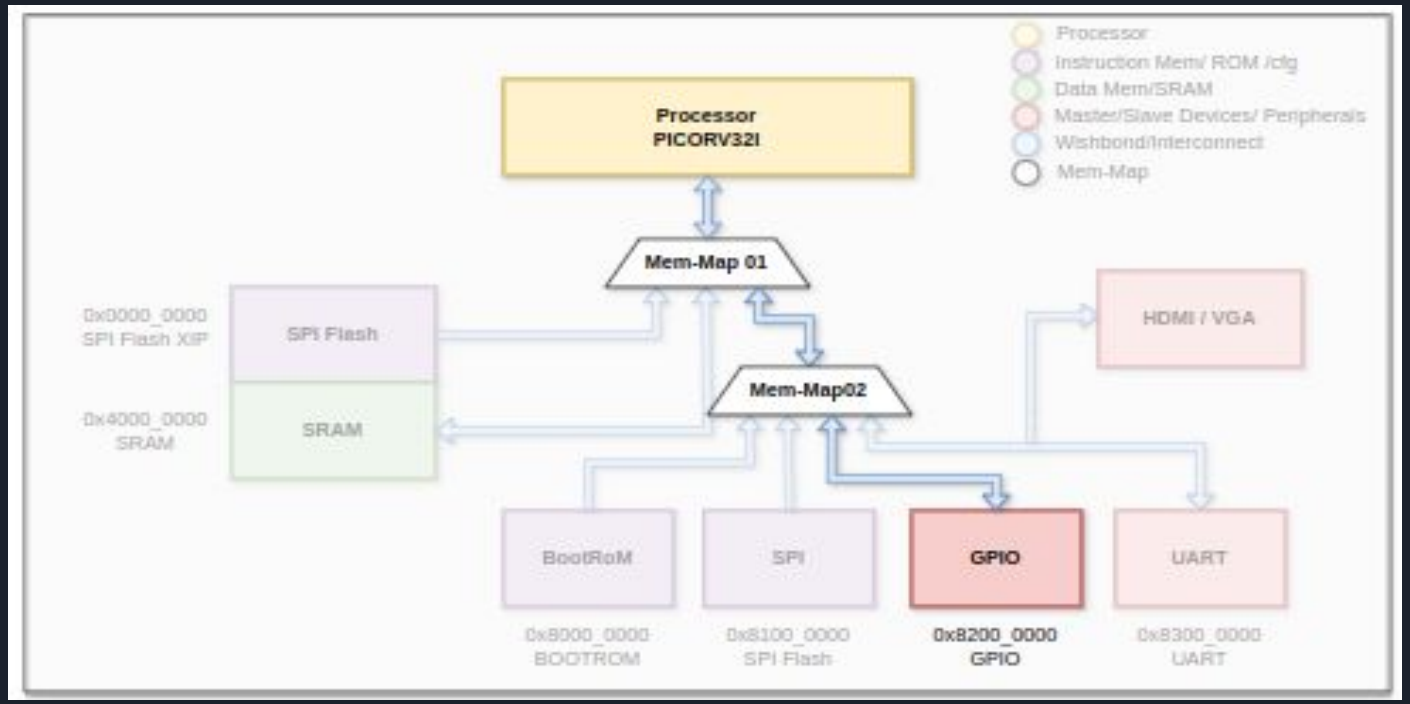

TESTIMONIAL

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Sponsored By: Edmund from Symbiotic EDA. for sponsoring FPGA.

Thanks: Lushay Lab (They've provided crucial resources and guidance throughout the project)