RISC-V SoC and Firmware Development

Lab: 01

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- Introduction Of FPGA
- Installation Of Lushay Lab
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Introduction to FPGA

Setup Guide

Step 01: OSS-CAD-Suite

- OSS-CAD-Suite is a project managed by the yosys
- enabling users to visually set up and execute the operating system toolchain.

OSS-CAD-Suite Installation Link:

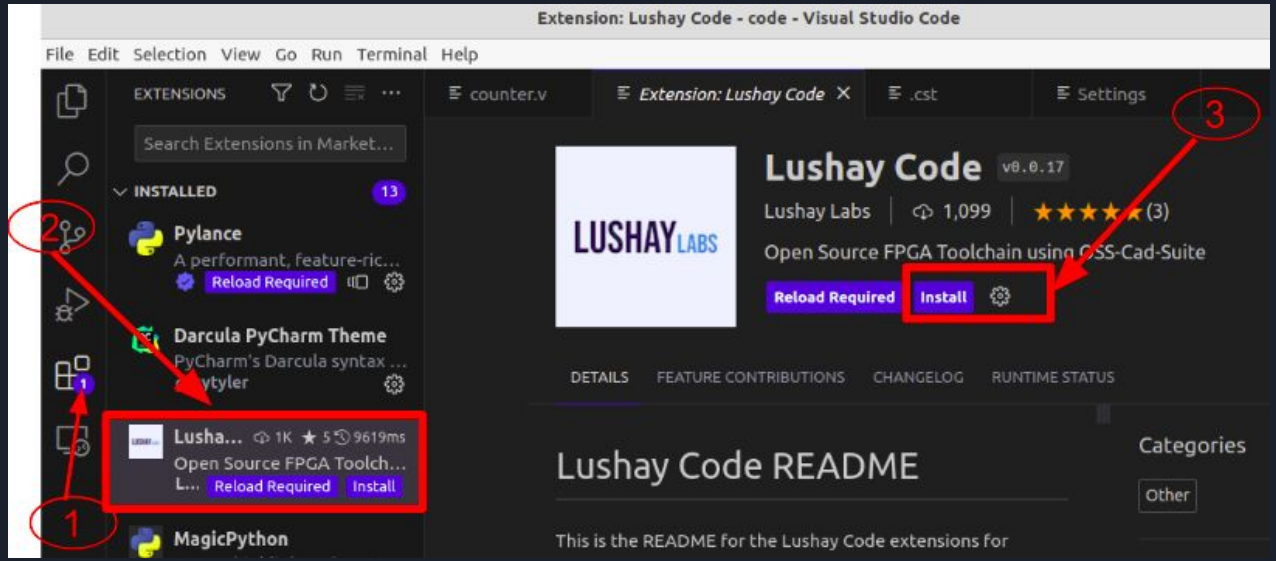
https://github.com/YosysHQ/oss-cad-suite-build/releases/download/2023-04-06/oss-cad-suite-linux-x64-20230406.tgz

- You can use the above link for OSS-CAD-Suite installation.
- *OSS-CAD-Suite Installation Link:*
- **https://github.com/YosysHQ/oss-cad-suite-build/releases/download/2023-04-06/oss-cad-suite-linux-x64-20230406.tgz**

Setup Guide

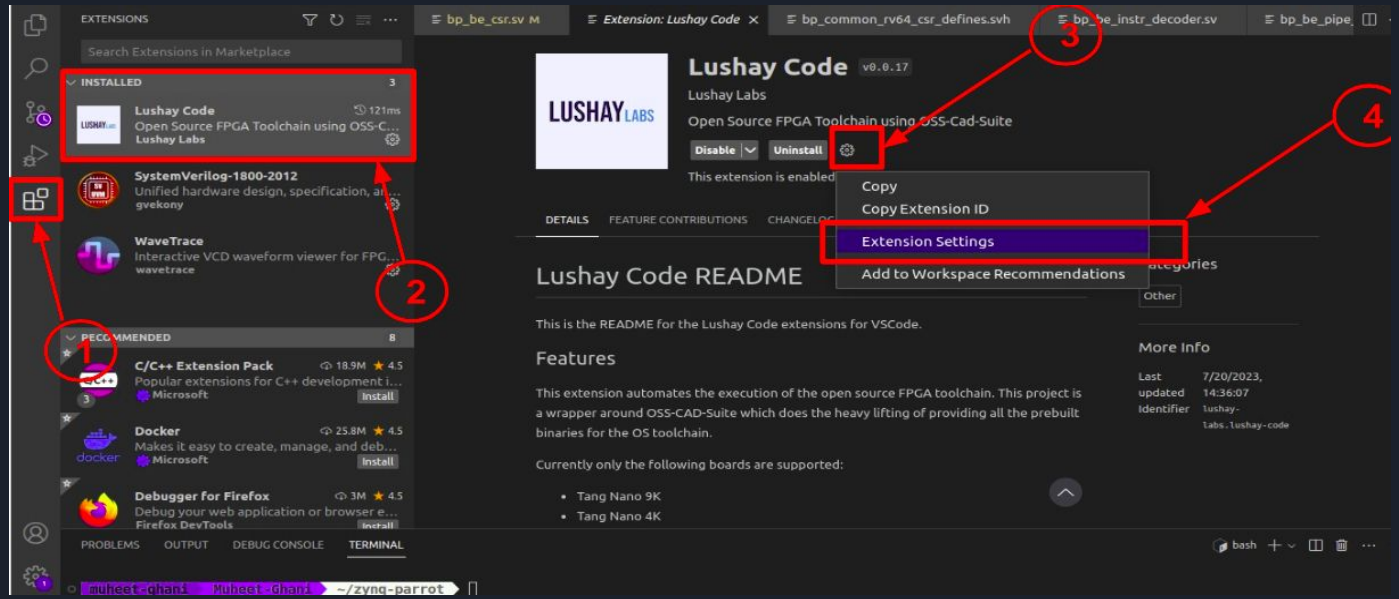
Step 02: Lushay Lab Extension Installation In VS Code

- Second step is to open up the VSCode and go to the Extensions tab and install the Lushay code.

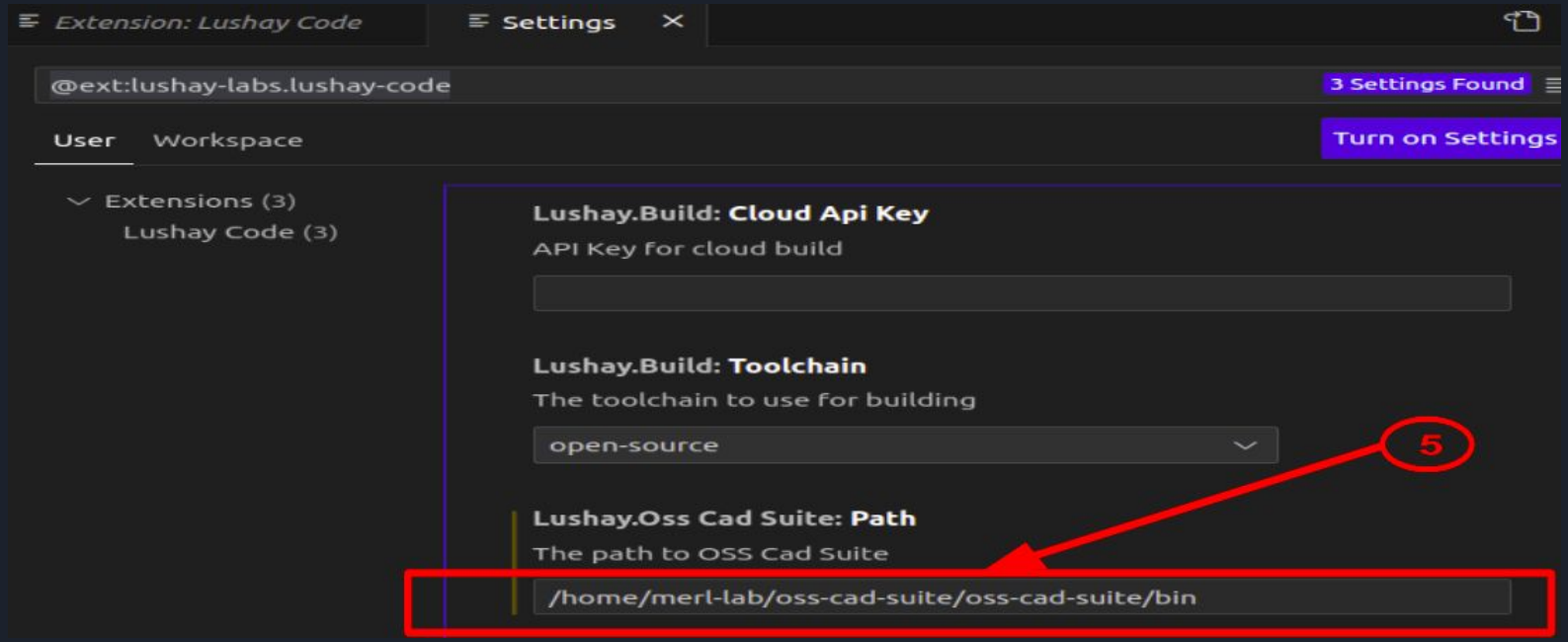


Setup Guide

Choose the recently extracted OSS-CAD-Suite folder specifically, the folder named ”oss-cad-suite” containing the ”bin” subfolder.



Setup Guide


Extension: Lushay Code
Settings
@ext:lushay-labs.lushay-code
3 Settings Found
User
Workspace
Turn on Settings
Extensions (3)
Lushay Code (3)
Lushay.Build: Cloud Api Key
API Key for cloud build
Lushay.Build: Toolchain
The toolchain to use for building
open-source
5
Lushay.Oss Cad Suite: Path
The path to OSS Cad Suite
/home/merl-lab/oss-cad-suite/oss-cad-suite/bin

Simulation Guide.

Step 01: Write Verilog Code

Make the folder i.e Counter and create verilog file i.e counter.v. and copy the below just for the reference.

```
module top
    (
        input clk,
        output [5:0] led
    );
    localparam WAIT_TIME = 13500000;
    reg [5:0] ledCounter = 0;
    reg [23:0] clockCounter = 0;

    always @(posedge clk) begin
        clockCounter <= clockCounter + 1;
        if (clockCounter == WAIT_TIME) begin
            clockCounter <= 0;
            ledCounter <= ledCounter + 1;
        End
    end
    assign led = ~ledCounter;
endmodule
```

Simulation Guide.

Step 02: Write Verilog Testbrnch

Create the Test bench for counter code

```
`timescale 1ns/1ns
module test;

reg clk = 0;
initial begin
    while(1)
    begin
        clk = ~clk;
        #10;
    end
end

initial begin
    $dumpvars(0,test);
    $dumpfile("dump.vcd");

    #1000;
    $finish();
end

top u_led_counter
(
    .clk(clk),
    .led()
);
endmodule
```

Simulation Guide.

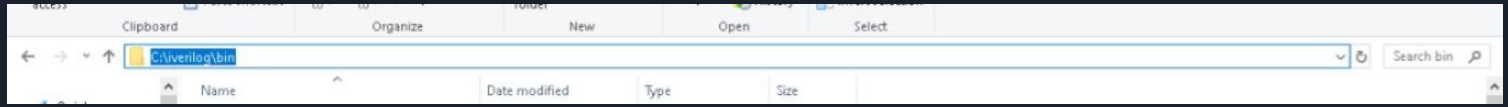
Step 03: Install Icarus Verilog

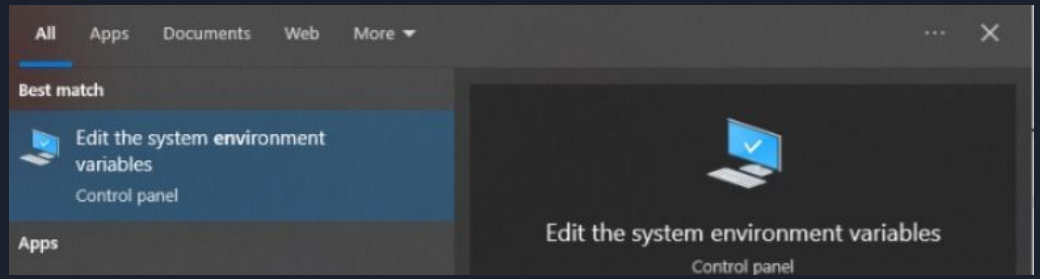
- Install Icarus verilog from.
  - https://bleyer.org/icarus/ (Latest Stable release).

Simulation Guide.

Step 04: Setup Environment Variable.

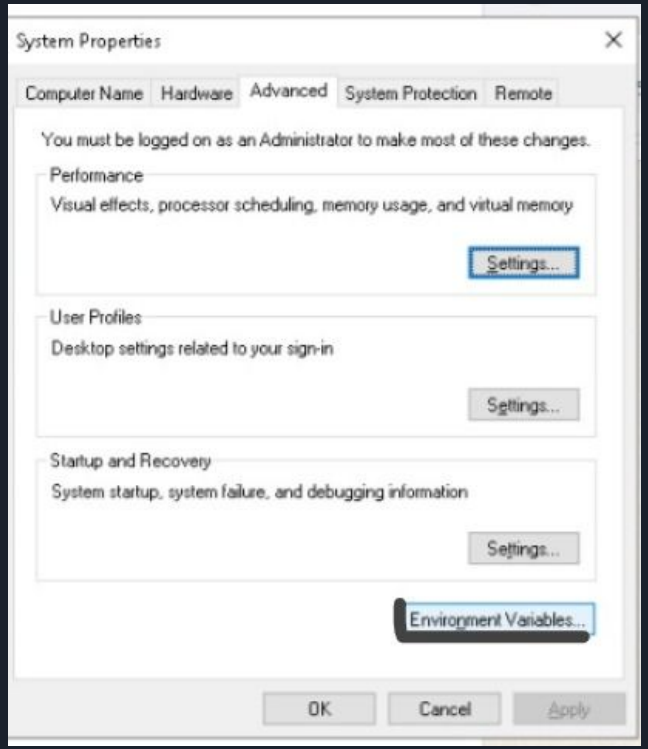
- After Installing Icarus Verilog.
  In Local Disk (C:), bin. Copy the path of bin folder.



- Open the Edit the system environment variable in control panel.
  - 

Simulation Guide.

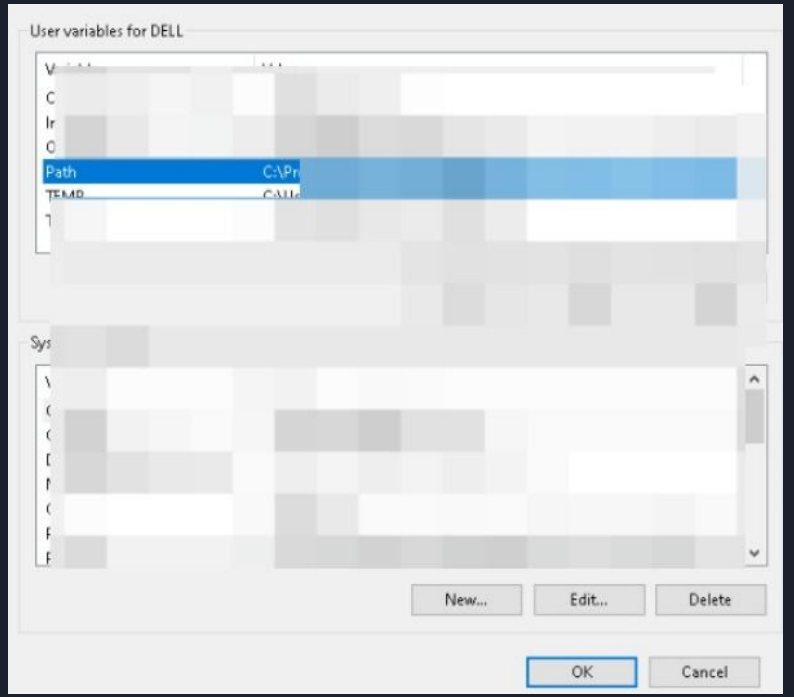
Step 04: Setup Environment Variable.



Simulation Guide.

Step 04: Setup Environment Variable.

Double click on Path variable



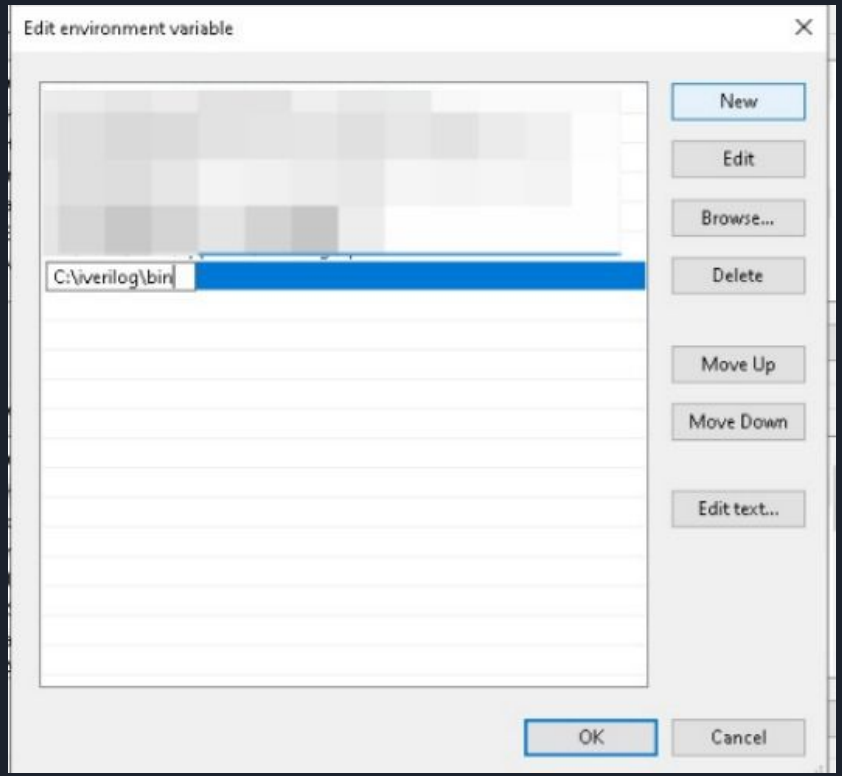
Simulation Guide.

Step 04: Setup Environment Variable.

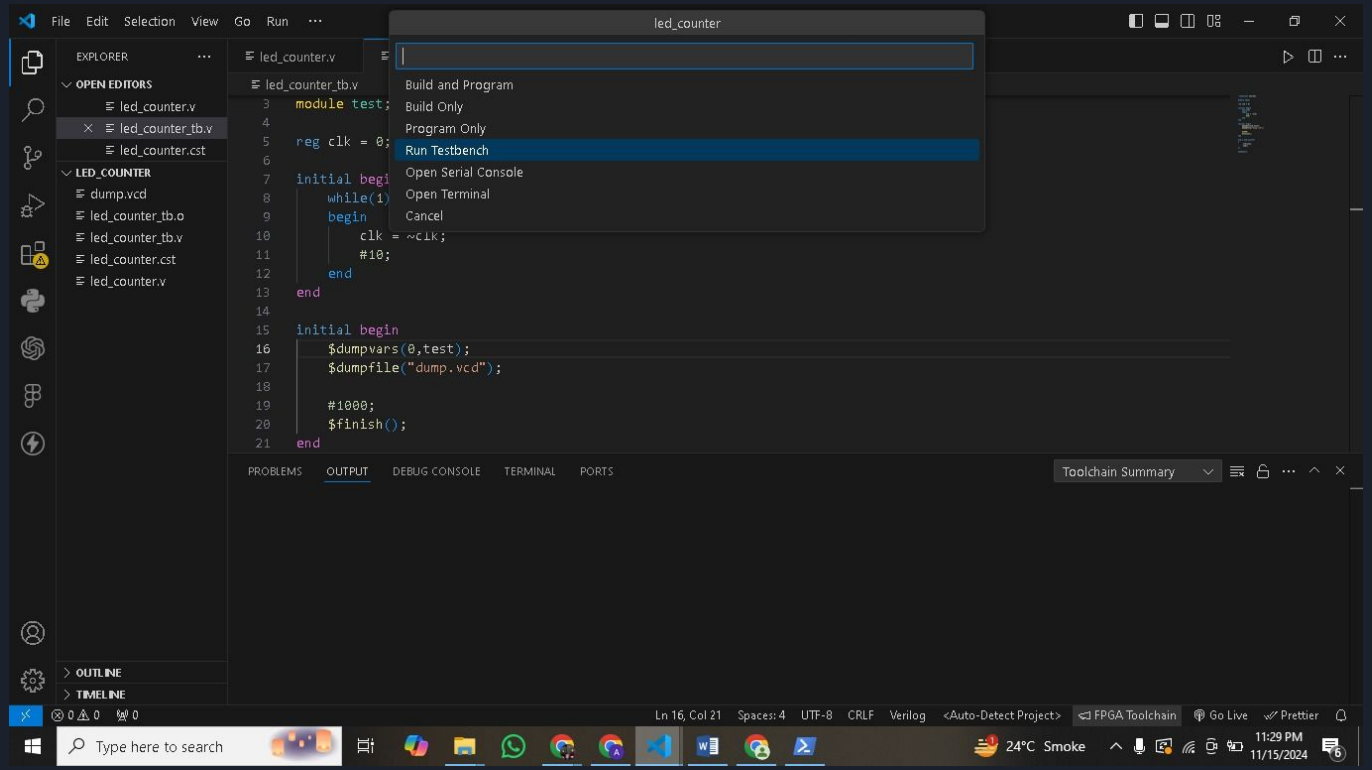
Double click on Path variable

Now Open Power shell n type

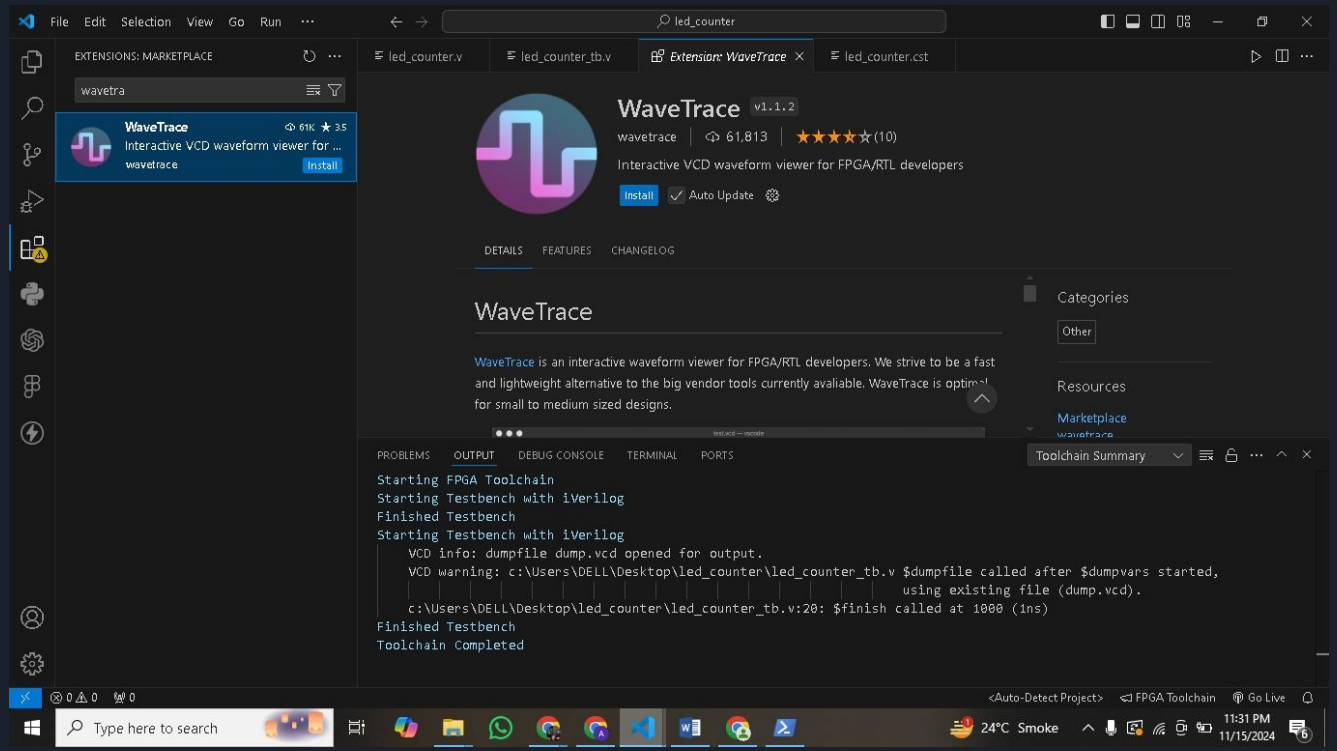
Iverilog -o output_file input file



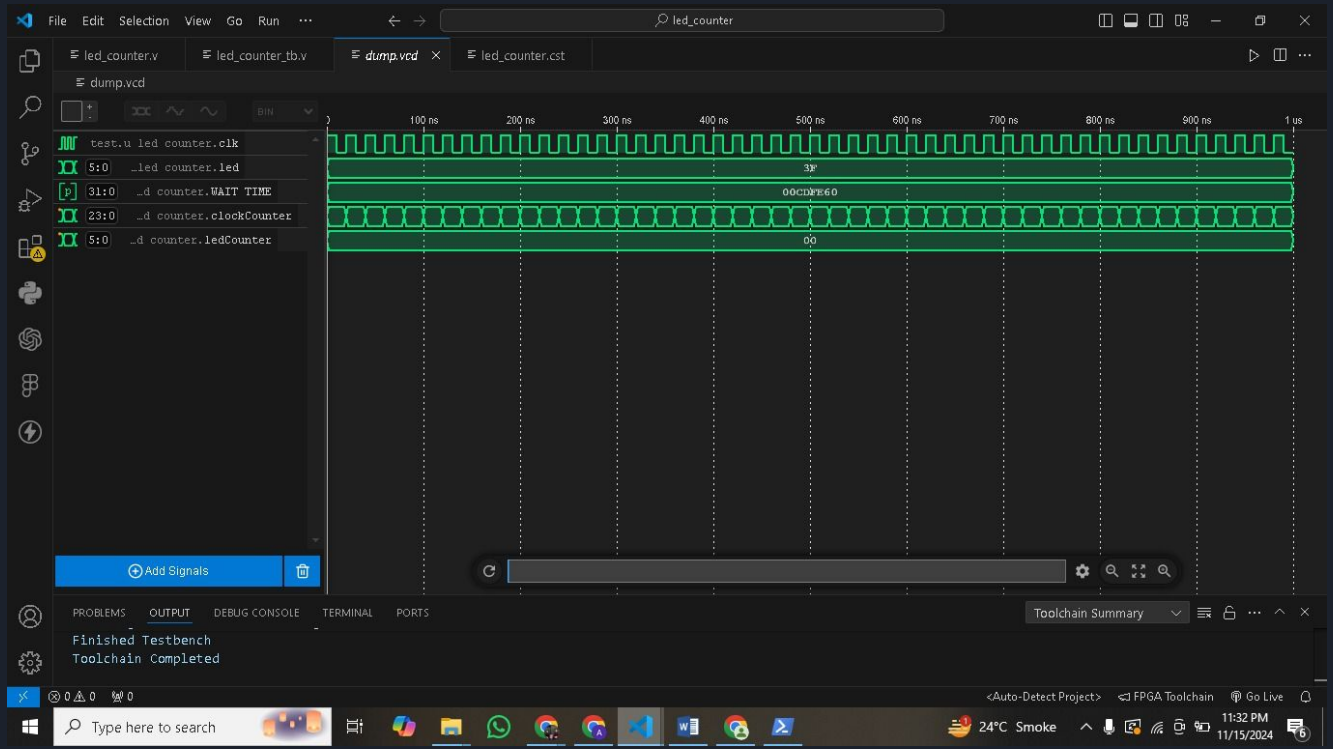
Simulation Guide.



Simulation Guide.



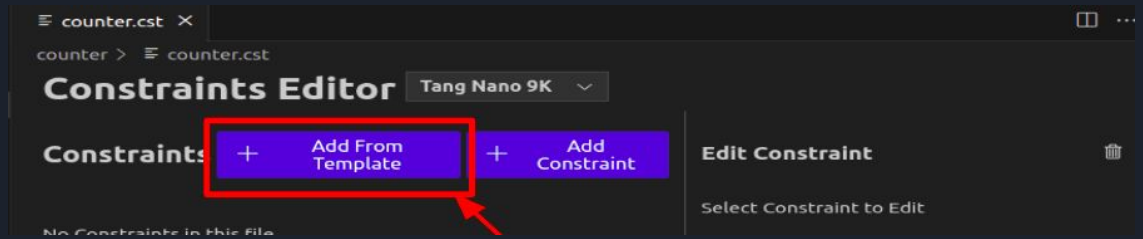
Simulation Guide.



FPGA Porting.

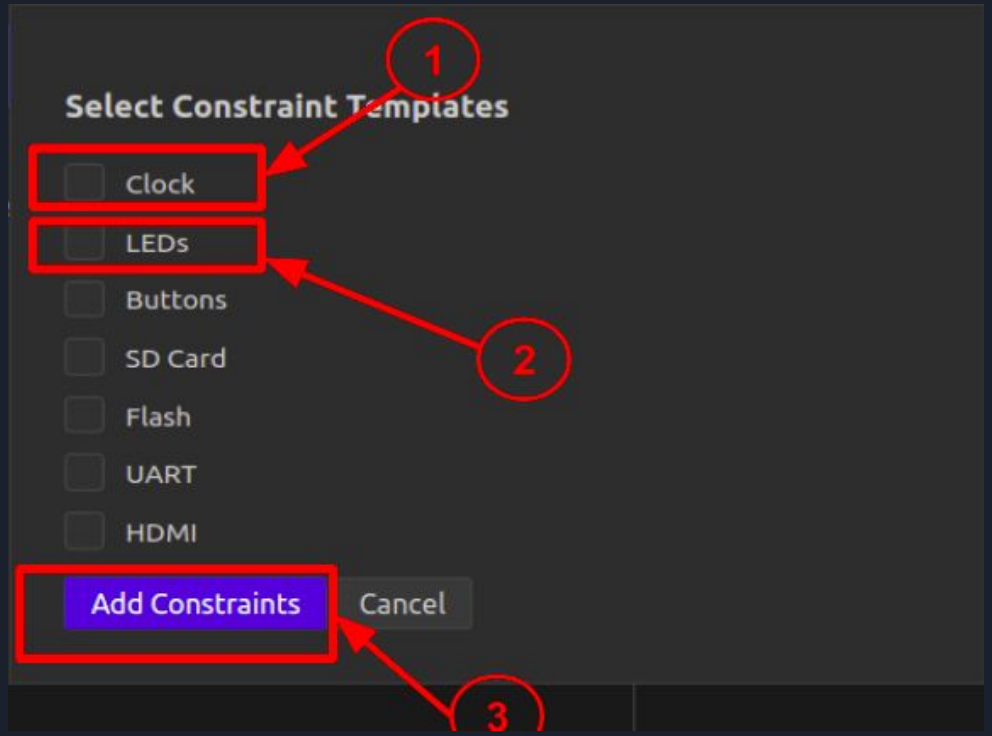
Step 02: Create .cst file

When .cst is created on VS Code. this type of interface will be open for constraints. Now click on “Add From Template”.



FPGA Porting

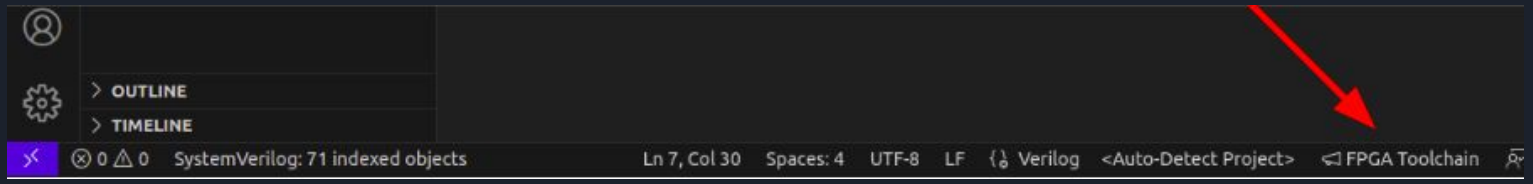
Next you have to select clk, and led and then click “add constraint”.



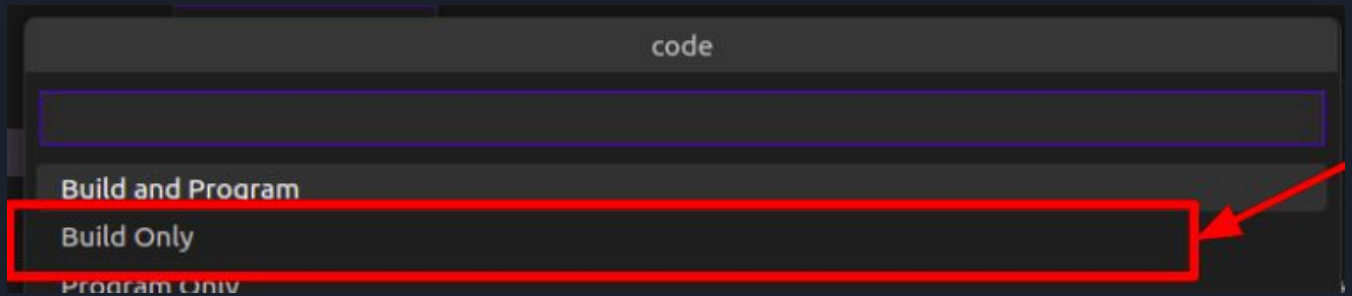
FPGA Porting.

Step 03: Synthesis And PNR

Now click on the bottom right hand side called “fpga toolchain”



Now click on “build only” which starts synthesis and pnr



FPGA Porting.

Step 04: Program FPGA

Now After completing the “build only” step successfully bitstream have generated with .fs extension file now it’s time to program onto the FPAG. Now again click on the bottom right side “FPGA toolchain” button and hit the “program only” option just below the “build only” option.

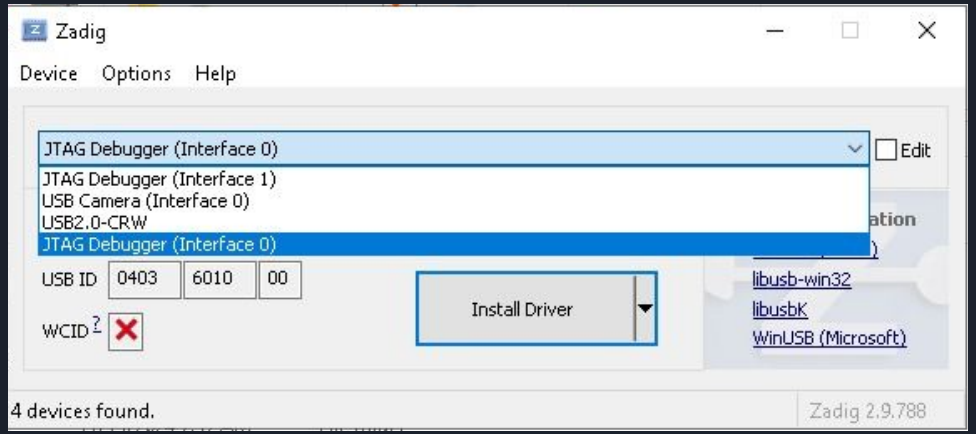
If it show’s the error message of the “FTDI port not found” then run this command on terminal.

```
curl -sSL
https://raw.githubusercontent.com/lushaylabs/openfpgaloader-ubuntufix/main/setup.sh | sh
```

FPGA Porting.

Step 04: Program FPGA For Windows

- Download zadig from
  https://zadig.akeo.ie/
- After Installing zadig. Open **Options** from menu bar and click **List All Devices.**
  Connect FPGA from PC,
- **Now Select JTAG Debugger (Interface 0).**



Exercise.

Now Add button on the counter logic and make the counter which depend on the button.

TESTIMONIAL

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Under The Supervision Of:

Dr.Ali Ahmed (Team Lead MERL).

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