Sequential Circuit

6.1 Sequential Circuits

- It consists of a combinational circuit to which memory elements are connected to form a feedback path.
- The memory elements are devices capable of storing binary information within them.
- The binary information stored in the memory elements at any given time defines the state of the sequential circuit.
- The sequential circuit receives binary information from external inputs.
- These inputs, together with the present state of the memory elements, determine the binary value at the output terminals.

6.1 Sequential Circuits

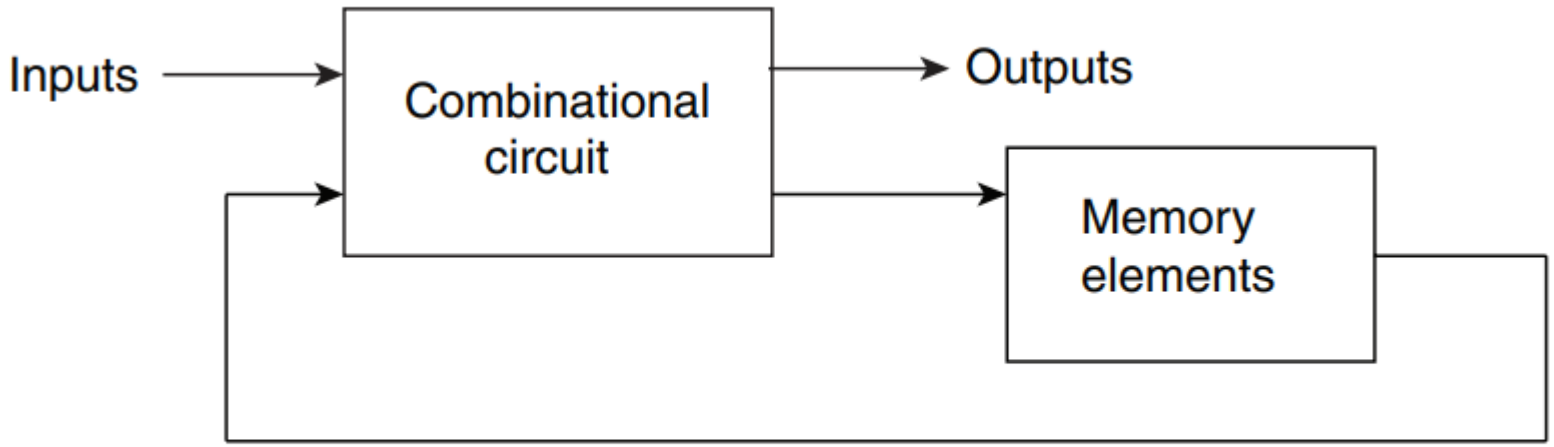


Figure 6.1 Block diagram of a sequential circuit

Types of Sequential Circuit

Their classification depends on the timing of their signals.

1. Synchronous Circuits
2. Asynchronous Circuits

Synchronous and Asynchronous

- A **synchronous sequential circuit** is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time.
- The behavior of an **asynchronous sequential circuit** depends upon the order in which its input signals change and can be affected at any instant of time. The memory elements commonly used in asynchronous sequential circuits are time-delay devices. The memory capability of a time-delay device is due to the fact that it takes a finite time for the signal to propagate through the device.

6.2 Flip Flops

A flip-flop circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit) until directed by an input signal to switch states. The major differences among various types of flip-flops are in the number of inputs they possess and the manner in which the inputs affect the binary state.

6.2.1 Basic Flip-Flop Circuit

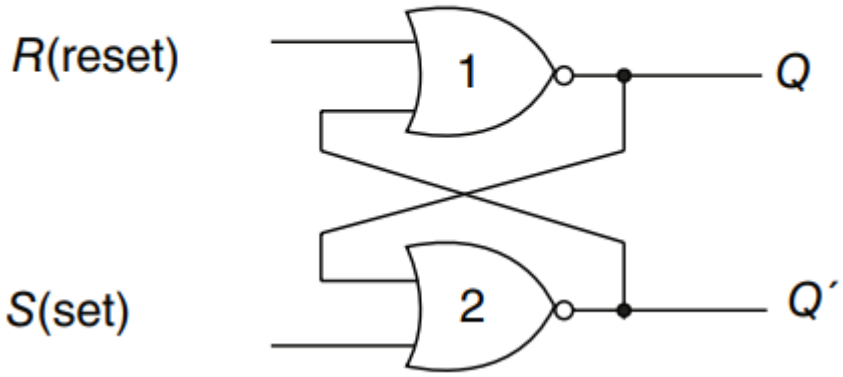
6.2.2 Clocked RS Flip-Flop

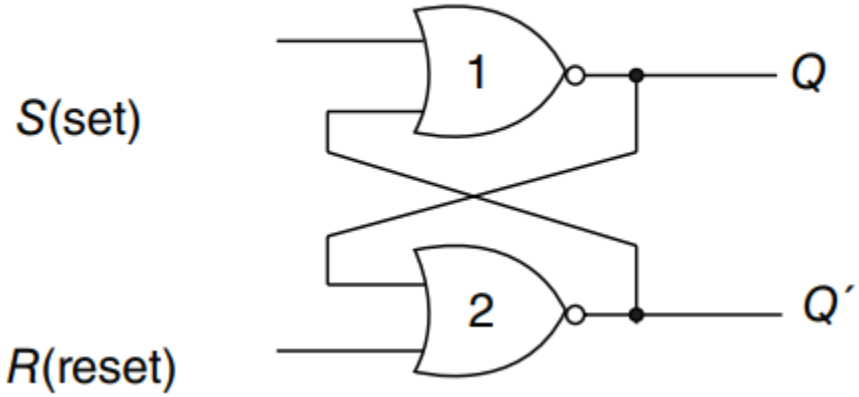
6.2.3 D Flip-Flop

6.2.4 JK Flip-Flop

6.2.1 Basic Flip-Flop Circuit

- A flip-flop circuit can be constructed from two NAND gates or two NOR gates. These constructions are shown in the logic diagrams.



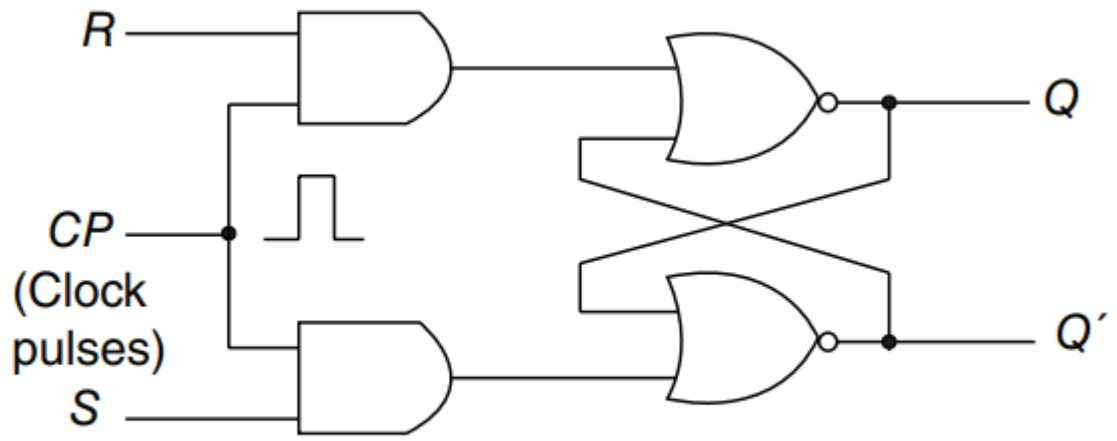


S-R Flip Flop

- Each circuit forms a basic flip-flop upon which other more complicated types can be built.
- The cross-coupled connection from the output of one gate to the input of the other gate constitutes a feedback path.
- Each flip-flop has two outputs, Q and Q’, and two inputs, set and reset.
- This type of flipflop is sometimes called a direct-coupled RS flip-flop or SR latch.
- The R and S are the first letters of the two input names.

6.2.2 Clocked RS Flip-Flop

The basic flip-flop as it stands is an asynchronous sequential circuit. By adding gates to the inputs of the basic circuit, the flip-flop can be made to respond to input levels during the occurrence of a clock pulse. The clocked RS flip-flop consists of a basic NOR flip-flop and two AND gates.



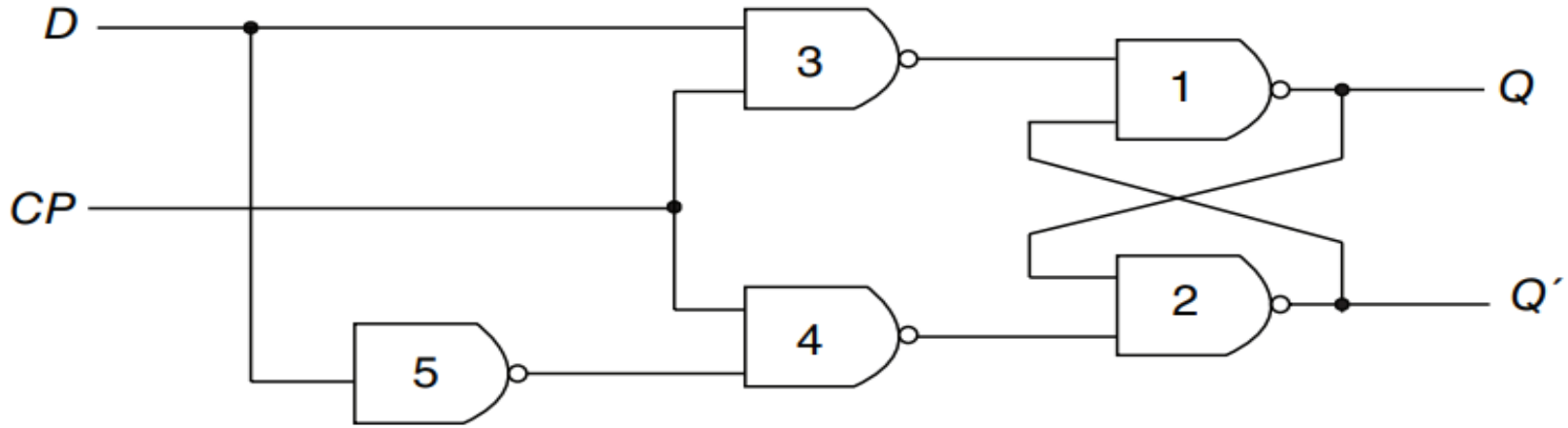
(a) Logic diagram

Q	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

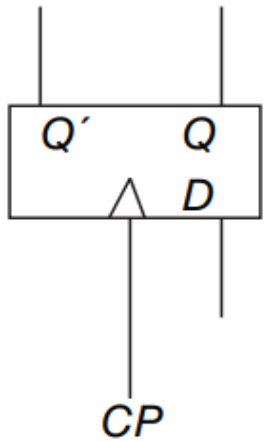
(c) Characteristic table

6.2.3 D Flip-Flop

- The D flip-flop is a modification of the clocked RS flip-flop.
- NAND gates 1 and 2 form a basic flip-flop and gates 3 and 4 modify it into a clocked RS flip-flop.
- The D input goes directly to the S input, and its complement, through gate 5, is applied to the R input.
- As long as the clock pulse input is at 0, gates 3 and 4 have a 1 in their outputs, regardless of the value of the other inputs.



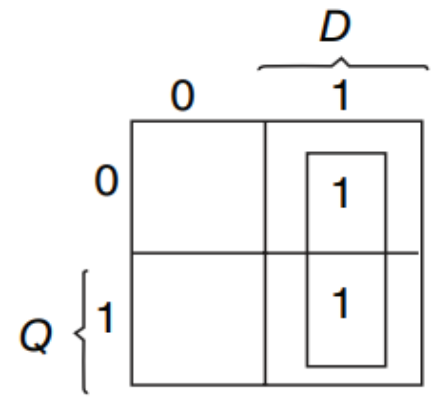
(a) Logic diagram with NAND gates



(b) Graphic symbol

Q	D	Q(t + 1)
0	0	0
0	1	1
1	0	0
1	1	1

(c) Characteristic table



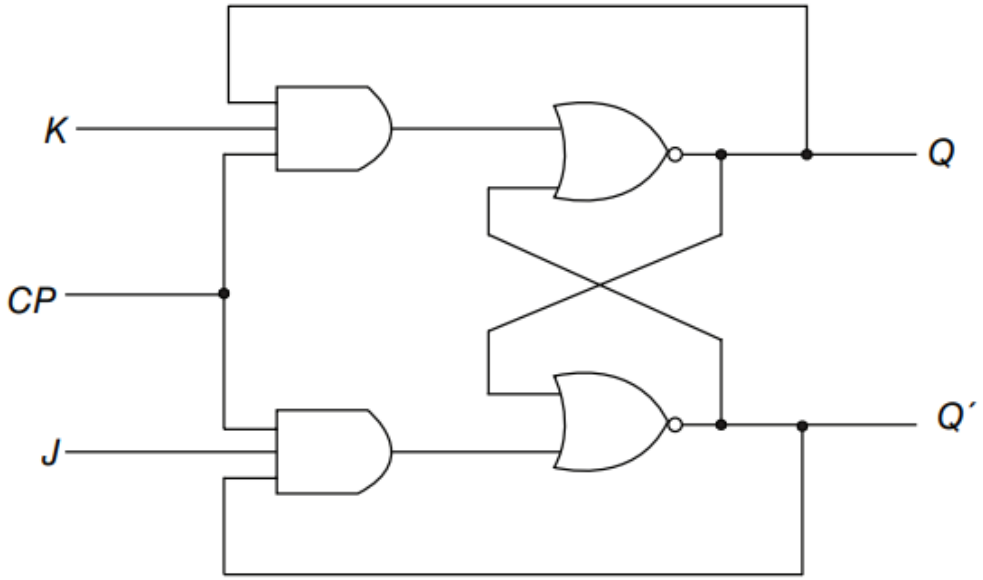
$Q(t + 1) = D$

(d) Characteristic equation

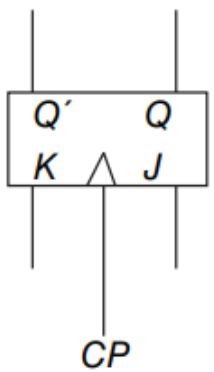
Figure 6.5 Clocked *D* flip-flop

6.2.4 JK Flip Flop

- A JK flip-flop is a refinement of the RS flip-flop in that the indeterminate state of the RS type is defined in the JK type.
- Inputs J and K behave like inputs S and R to set and clear the flip-flop (note that in a JK flip-flop, the letter J is for set and the letter K is for clear).
- When inputs are applied to both J and K simultaneously, the flip-flop switches to its complement state, that is, if Q = 1, it switches to Q = 0, and vice versa.



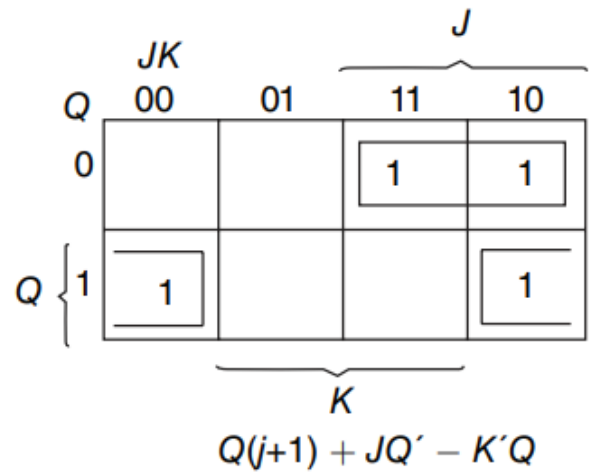
(a) Logic diagram



(b) Graphic symbol

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(c) Characteristic table



$Q(j+1) + JQ' - K'Q$

(d) Characteristic equation

Figure 6.6 Clocked *JK* flip–flop

6.3 Triggering of Flip Flops

- The state of a flip-flop is switched by a momentary change in the input signal.
- This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop.
- Asynchronous flip-flops require an input trigger defined by a change of signal level.
- This level must be returned to its initial value (0 in the NOR and 1 in the NAND flip-flop) before a second trigger is applied.
- Clocked flip-flops are triggered by pulses. A pulse starts from an initial value of 0, goes momentarily to 1, and after a short time, returns to its initial 0 value.

6.3 Triggering of Flip Flops

- A sequential circuit has a feedback path between the combinational circuit and the memory elements.
- This path can produce instability if the outputs of memory elements (flip-flops) are changing while the outputs of the combinational circuit that go to flip-flop inputs are being sampled by the clock pulse.
- This timing problem can be prevented if the outputs of flip-flops do not start changing until the pulse input has returned to 0.

Clock Pulse Transition

- A clock pulse may be either positive or negative. A positive clock source remains at 0 during the interval between pulses and goes to 1 during the occurrence o a pulse. The pulse goes through two signal transitions; from 0 to 1 and the return from 1 to 0. The positive transition is defined as the positive edge and the negative transition as the negative edge. This definition applies also to negative pulses.

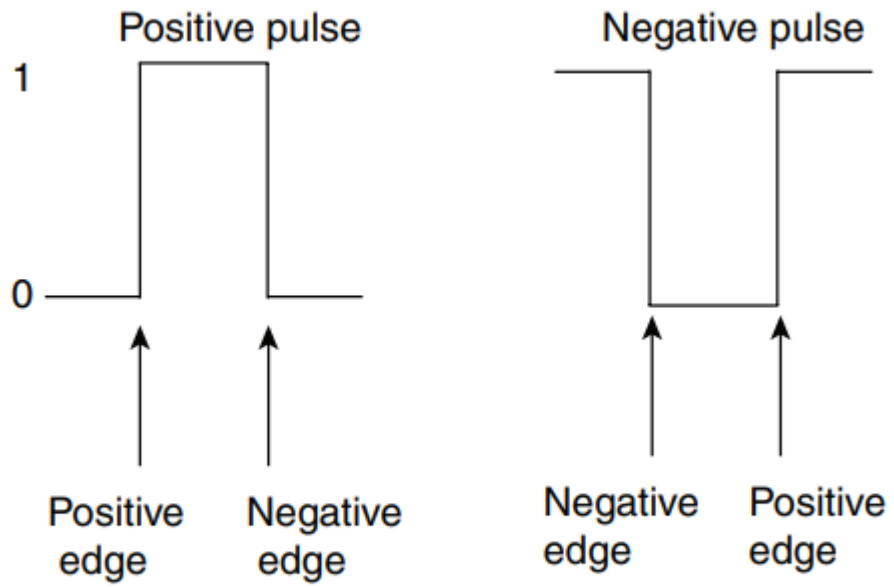


Figure 6.8 Definition of clock pulse transition