XOR and XNOR

- XOR
- XNOR
- Parity Bit Generator and Checker
  - Even and Odd Parity
- Implement Logic using MSI Blocks
  - Decoder, Encoder, Multiplexer, ROMs, PLAs etc.
  - Adder, Subtractor, Shifter, Comparator.

XOR

- The Exclusive OR (or XOR) relationship $F=A \oplus B$ $F=A \oplus B$ is defined by the truth tables shown in Fig. 1 and the equivalent two-variable logic expressions SOP form $F=A \cdot B' + A' \cdot B$ and
- POS form $F=(A+B) \cdot (A'+B')$.

A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

A	B	C	F'
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

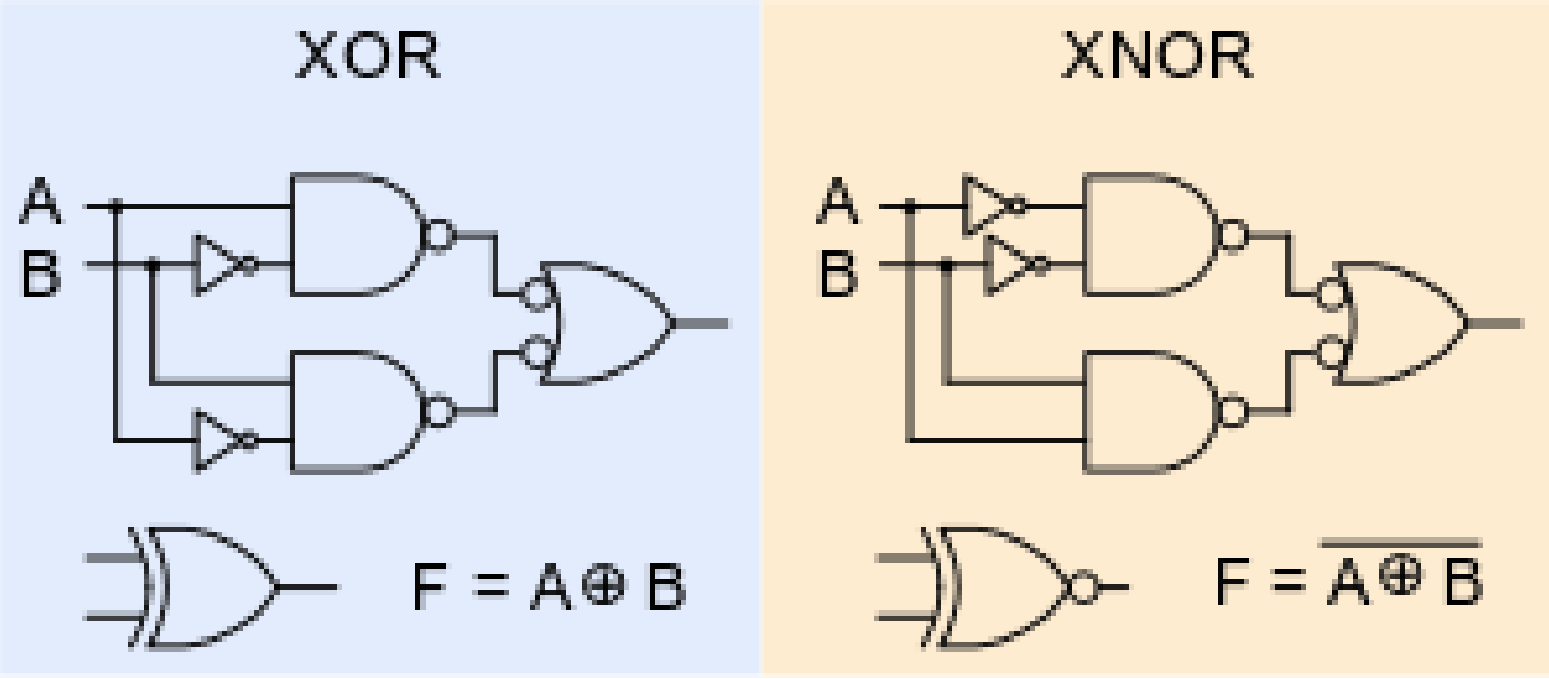
XNOR

- The Exclusive NOR (or XNOR) relationship F=(A⊕B)'shown in the truth tables has the equivalent two-variable logic expressions:
- SOP form F =A'·B'+A·B and
- POS form F =(A'+B)·(A+B')

A	B	F
0	0	1
0	1	0
1	0	0
1	1	1

A	B	C	F'
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

- The XOR output is asserted whenever an odd number of inputs are asserted, and the XNOR is asserted whenever an even number of inputs are asserted
  the XOR is an odd detector, and the XNOR an even detector



What is Parity Bit?

- The parity generating technique is one of the most widely used error detection techniques for the data transmission. In digital systems, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s (of data bits) to 1s and 1s to 0s.
- Hence, a Parity Bit is added to the word containing data in order to make number of 1s either even or odd. The message containing the data bits along with parity bit is transmitted from transmitter to the receiver.

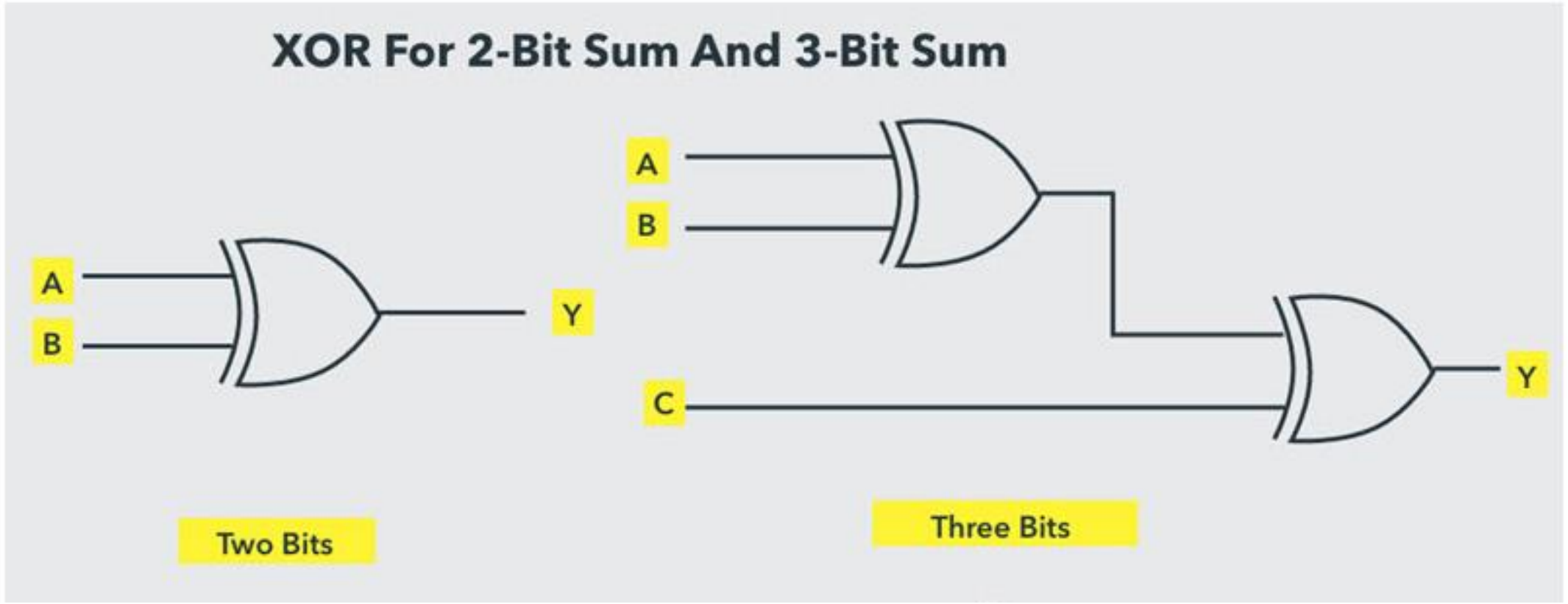
Parity Generator and Checker

- A Parity Generator is a combinational logic circuit that generates the parity bit in the transmitter.
- On the other hand, a circuit that checks the parity in the receiver is called Parity Checker.
- A combined circuit or device of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data.

Even Parity and Odd Parity

- The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s an even number, whereas in odd parity, the added parity bit will make the total number of 1s an odd number.
- The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and sum of even number of 1s is always 0. Such error detecting and correction can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of inputs).
- To produce two bits sum, one Ex-OR gate is sufficient whereas for adding three bits, two Ex-OR gates are required.

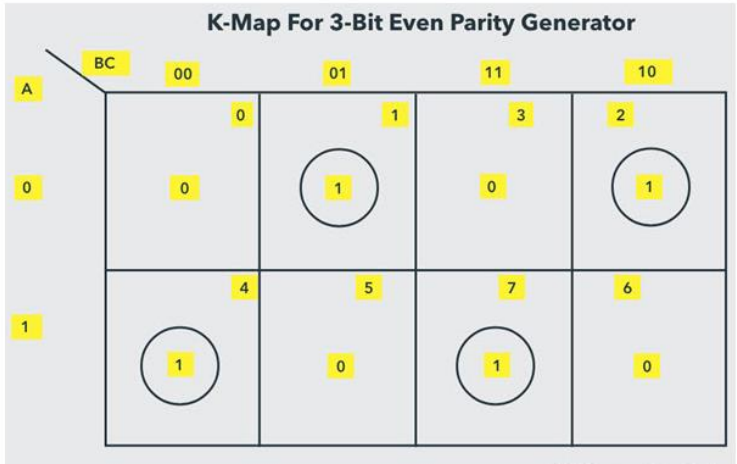
2- and 3-bits sum using XOR



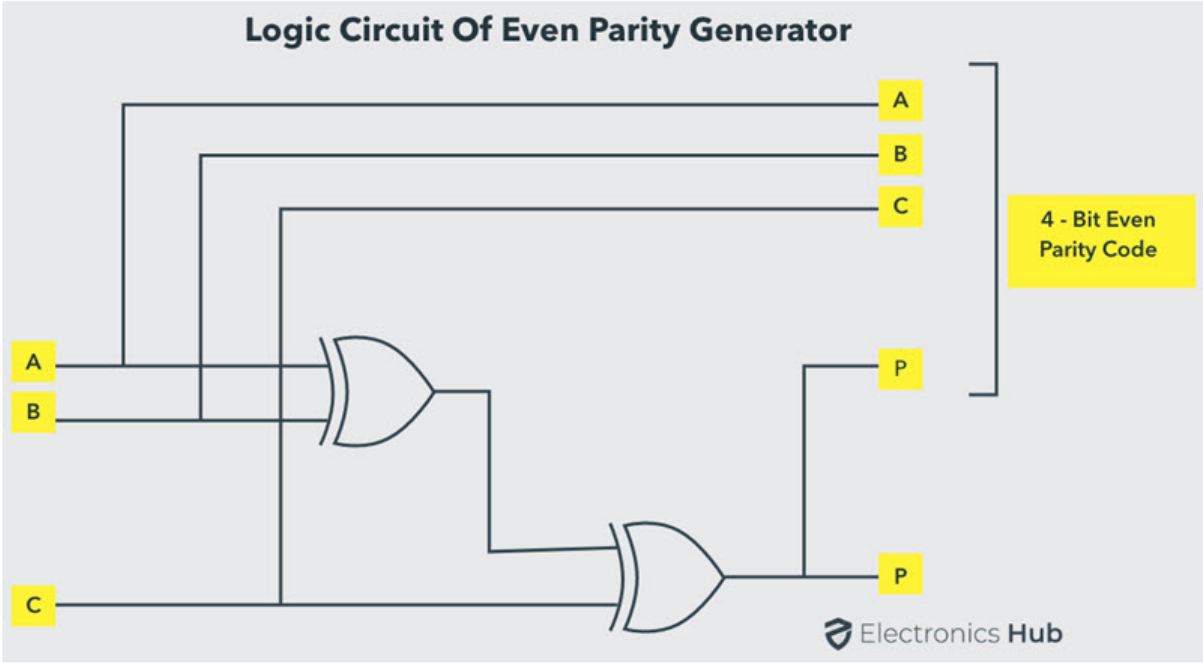
Even Parity Generator

- Let us assume that a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuit and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



Circuit Diagram of Even Parity Generating

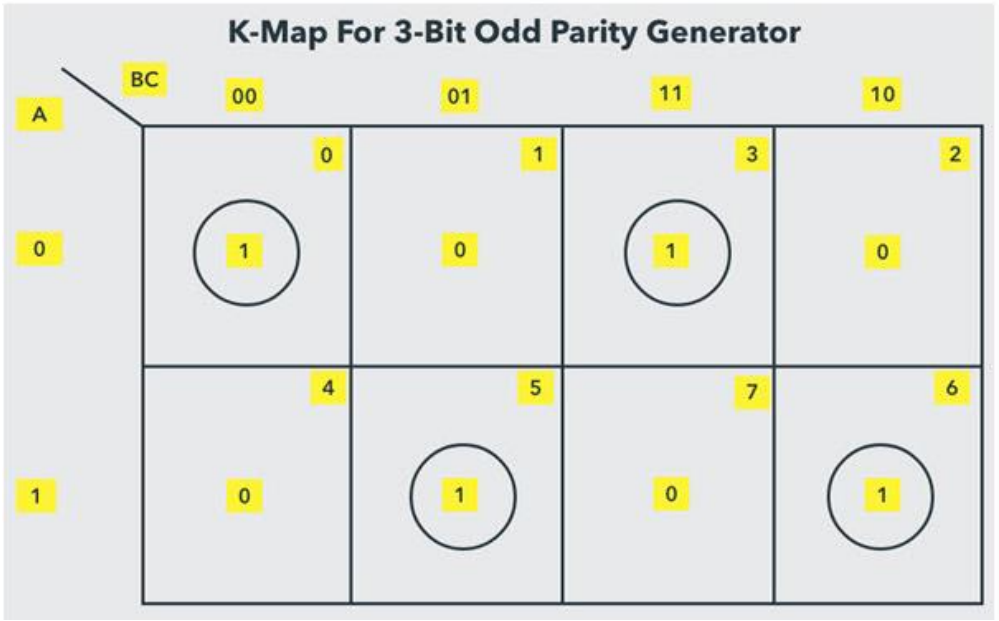


Odd Parity Generator

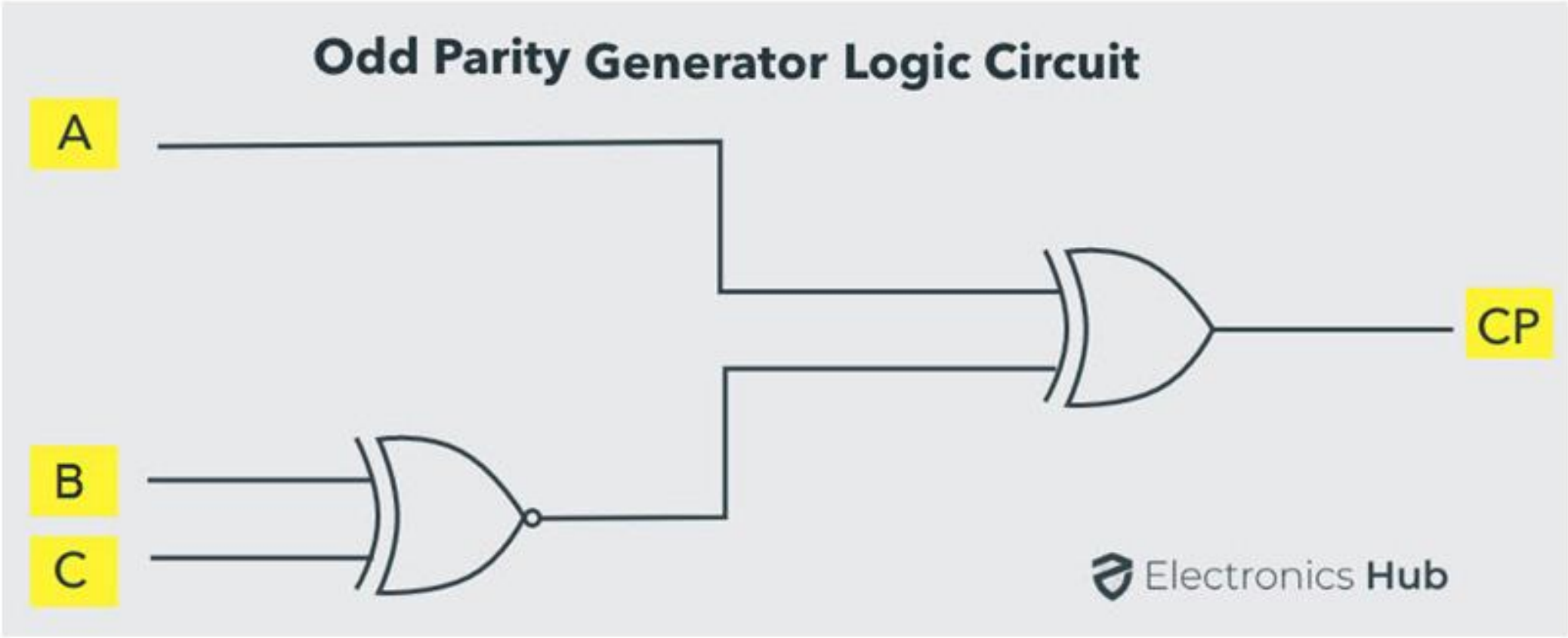
- Let us consider that the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit.
- In the given truth table below, 1 is placed in the parity bit in order to make the total number of bits odd when the total number of 1s in the truth table is even.

3-Bit Odd Parity Generator

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



Circuit Diagram Odd Parity Generator



Implementing Logic using MSI Blocks

- Implementation of Boolean functions using MSI blocks will be covered.
- Medium Scale Integration (MSI) devices have a complexity of approximately 10 to 200 gates in a single package.
- They usually perform specific elementary digital functions such as decoders, adders and registers

Combinational MSI Blocks

Various blocks available for implementing logic are :

- Decoders
- Encoders
- Multiplexers
- ROMs
- PLAs (Programmable Logic Arrays)

Arithmetic MSI Units

Various blocks available for implementing arithmetic logic are:

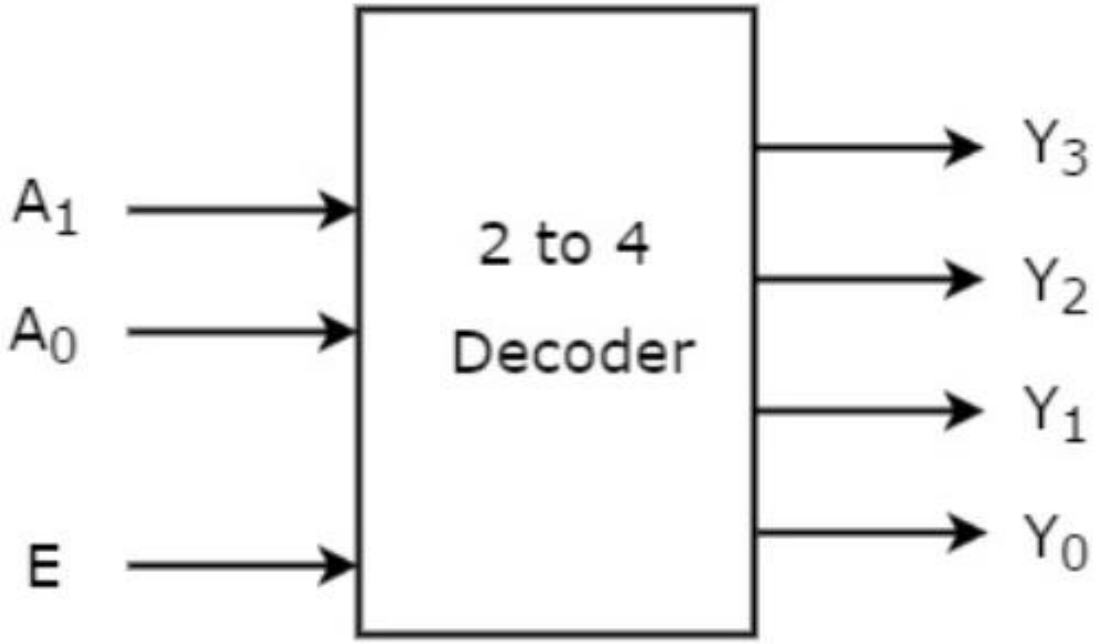
- Adders
- Subtracters
- Shifters
- Comparator

Decoder

- Discrete quantities of information are represented in digital computers with binary codes.
- A binary code of n bits is capable of representing up to 2^n distinct elements of the coded information.
- A decoder is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2^n unique outputs.
- If the n-bits coded information has unused bit combinations, the decoder may have less than 2^n outputs.

2 to 4 Decoder with Enable

- Let 2 to 4 Decoder has two inputs A_1 & A_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The block diagram of 2 to 4 decoder is shown in the following figure.



Truth Table of 2-4 Decoder with Enable

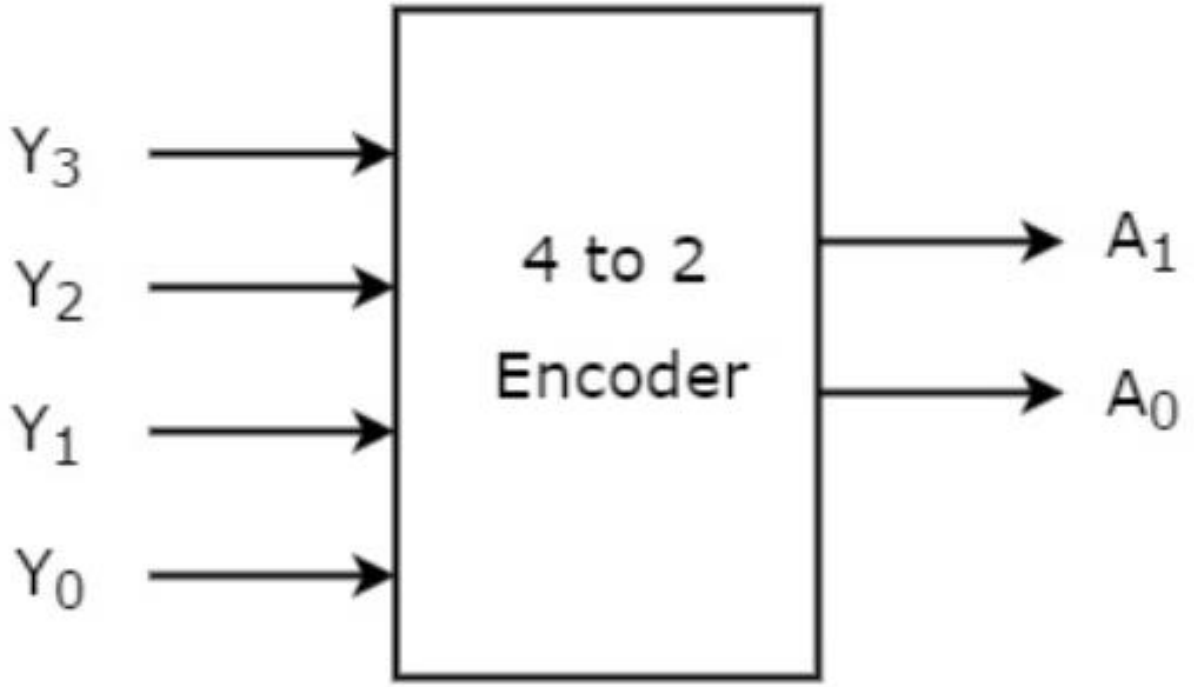
Enable	Inputs		Outputs			
E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Encoder

- An Encoder is a combinational circuit that performs the reverse operation of Decoder.
- It has maximum of 2^n input lines and ‘n’ output lines.
- It will produce a binary code equivalent to the input, which is active High.
- Therefore, the encoder encodes 2^n input lines with ‘n’ bits. It is optional to represent the enable signal in encoders

4 to 2 Encoder

- Let 4 to 2 Encoder has four inputs Y_3, Y_2, Y_1 & Y_0 and two outputs A_1 & A_0. The block diagram of 4 to 2 Encoder is shown in the following figure.



Truth Table of 4-2 Encoder

Inputs				Outputs	
Y_3	Y_2	Y_1	Y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Programable Logic Devices

- Programable Logic Devices PLDs are the integrated circuits.
- They contain an array of AND gates and another array of OR gate.
- There are 3 kinds of PLDs based on the type array, which programmable feature.

1. Programmable Read Only Memory
2. Programmable Array Logic
3. Programmable Logic Array

- The process of entering the information into these devices is known as programming.

Read-Only Memory (ROM)

- A read-only memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package.
- The connections between the outputs of the decoder and the inputs of the OR gates can be specified for each particular configuration by “programming” the ROM.
- The ROM is very often used to implement a complex combinational circuit in one IC package and thus eliminate all interconnecting wires.
- A ROM is essentially a memory (or storage) device in which a fixed set of binary information is stored.
- The binary information must first be specified by the user and is then embedded in the unit to form the required interconnection pattern.

ROM

- It consists of *n* input lines and *m* output lines.
- Each bit combination of the input variables is called an *address.* Each bit combination that comes out of the output lines is called a *word.*
- The number of bits per word is equal to the number of output lines *m.* An address is essentially a binary number that denotes one of the minterms of *n* variables. The number of distinct addresses possible with *n* input variables is 2*n.* An output word can be selected by a unique address, and since there are 2*n* distinct addresses in a ROM, there are 2*n* distinct words which are said to be stored in the unit.

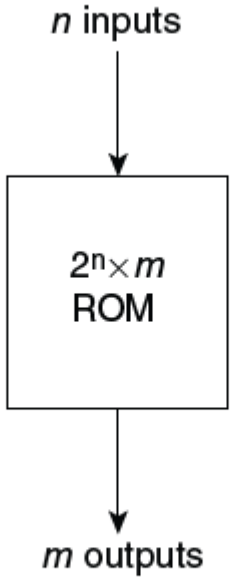


Figure 5-21 ROM block diagram

Logic Diagram of ROM

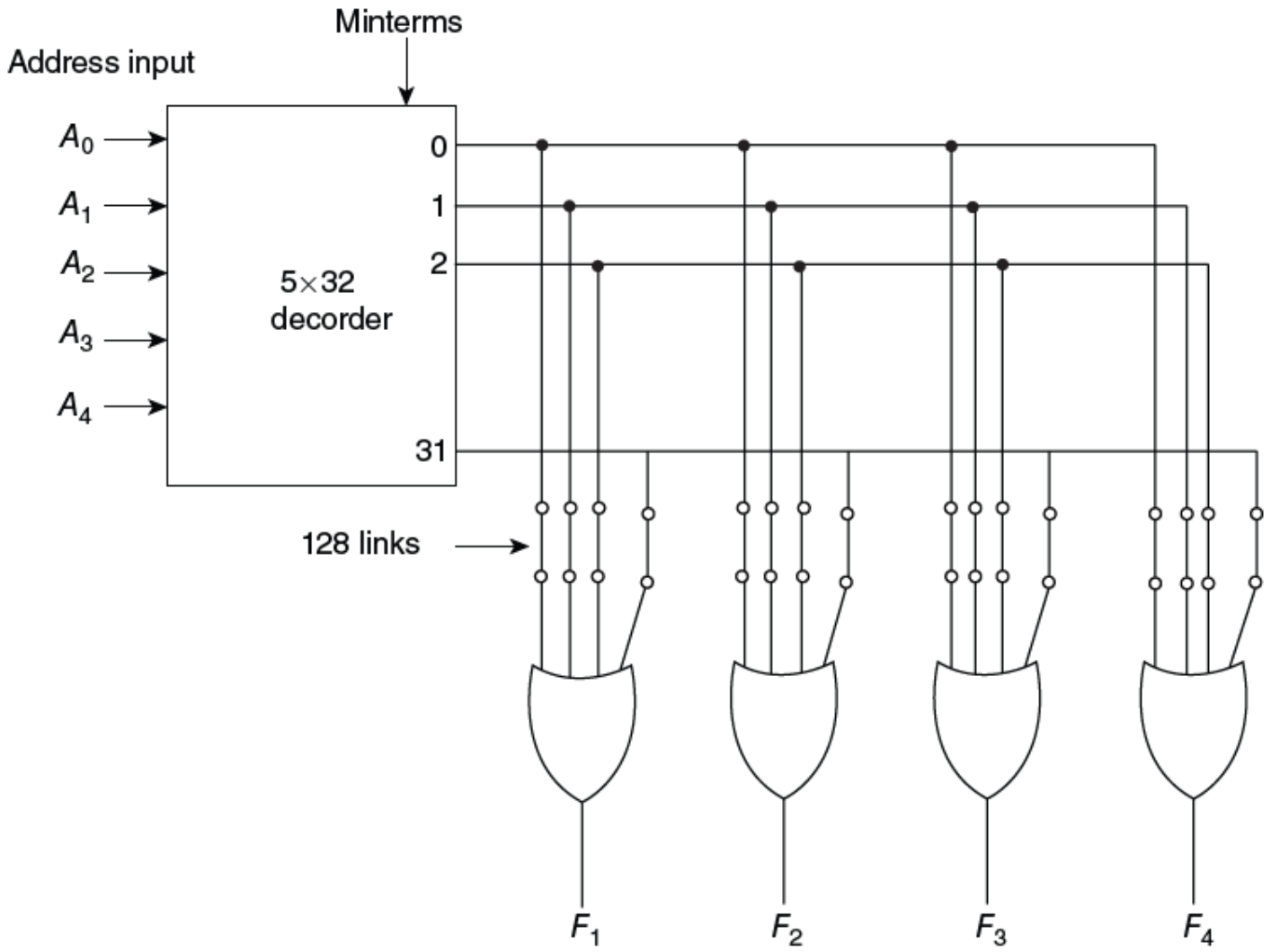


Figure 5-22 Logic construction of a 32 × 4 ROM

Programmable Logic Array (PLA)

- A combinational circuit may occasionally have don’t-care conditions. When implemented with a ROM, a don’t-care condition becomes an address input that will never occur.
- The words at the don’t-care addresses need not be programmed and may be left in their original state (all 0’s or all 1’s). The result is that not all the bit patterns available in the ROM are used, which may be considered a waste of available equipment.

Block Diagram of PLA

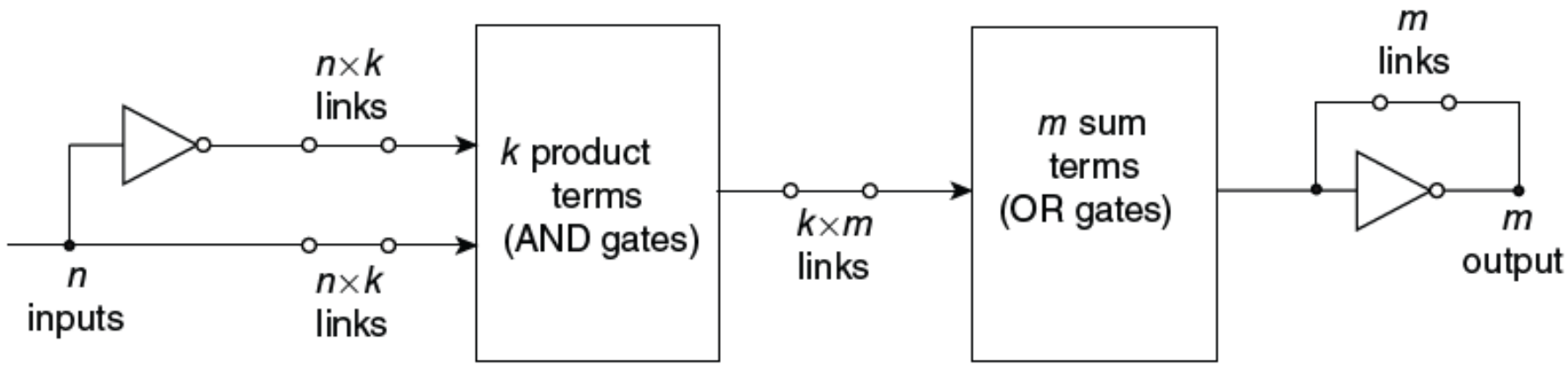


Figure 5-25 PLA block diagram

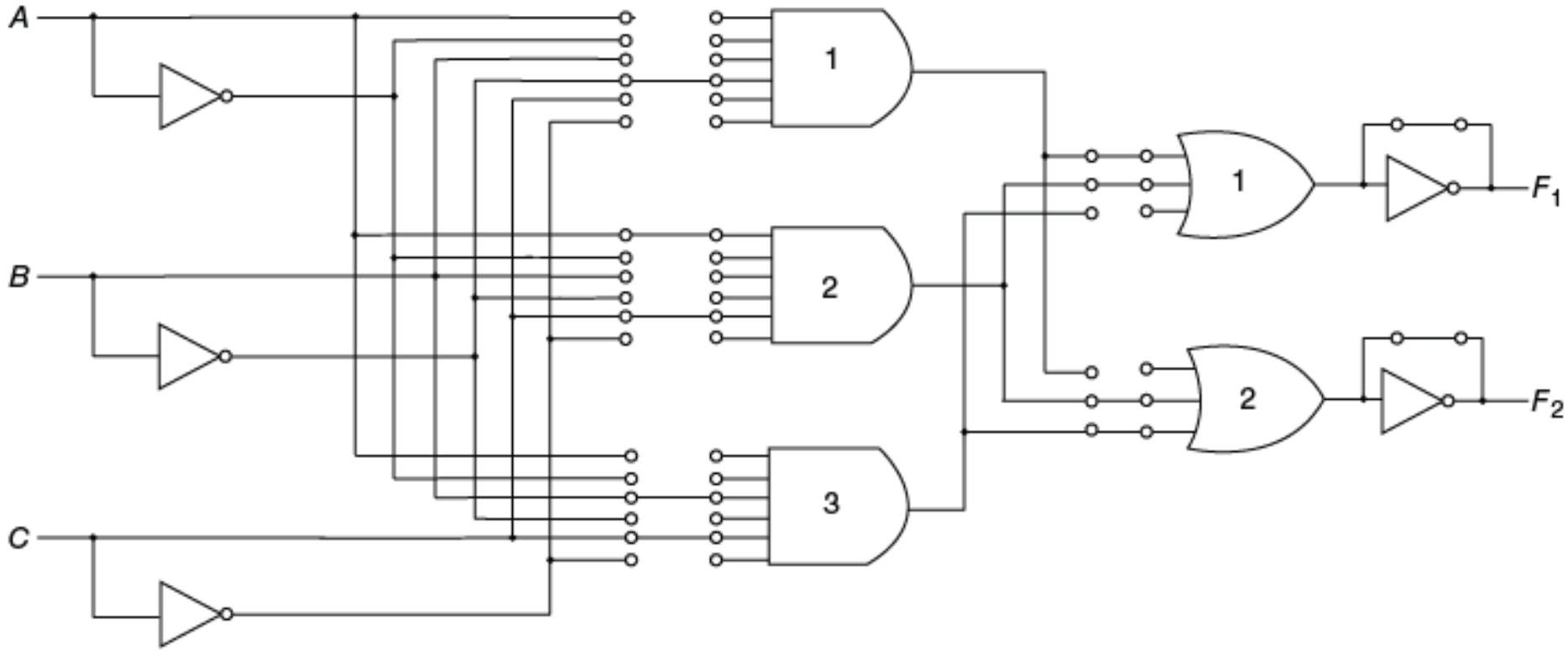
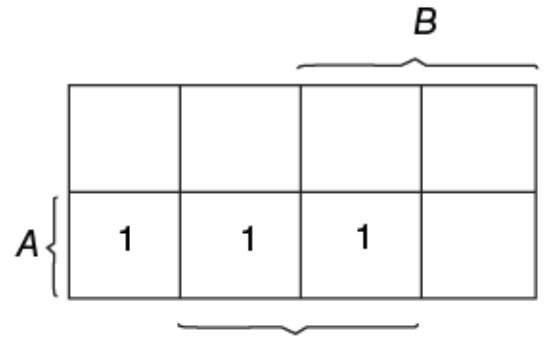


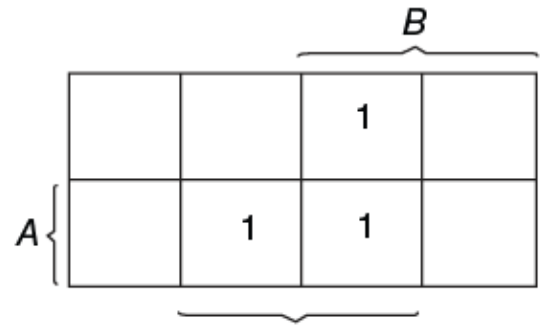
Figure 5-26 PLA with 3 inputs, 3 product terms, and 2 outputs; it implements the combinational circuit specified in Fig. 5-27

A	B	C	F_1	F_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1

(a) Truth table



$F_1 = AB' + AC$



$F_2 = AC + BC$

(b) Map simplification.

	Product term	Inputs A	B	C	Outputs F_1	F_2	
AB'	1	1	0	-	1	-	
AC	2	1	-	1	1	1	
BC	3	-	1	1	-	1	
					T	*T*	*T/C*

(c) PLA program table.

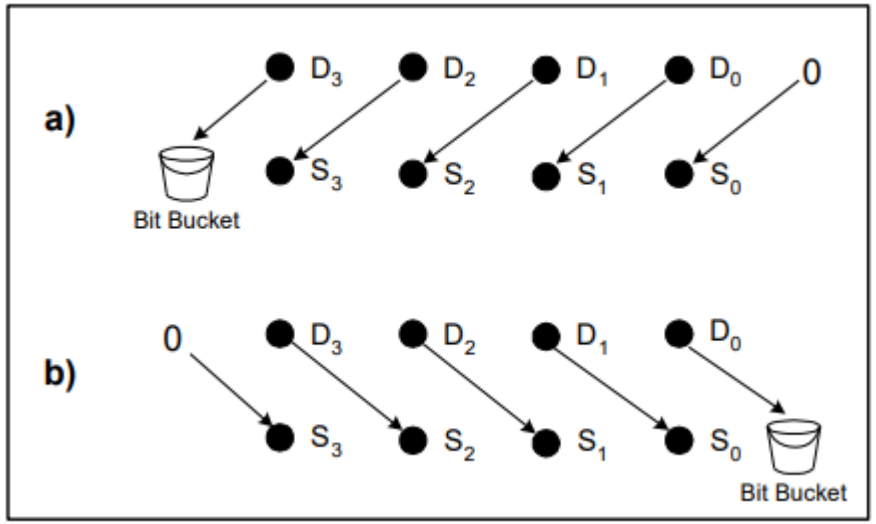
Figure 5-27 Steps required in PLA implementation

Shifter

- The shift unit attached to a processor transfers the output of the ALU onto the output bus.
- The shifter may transfer the information directly without a shift, or it may shift the information to the right or left.
- Provision is sometimes made for no transfer from the ALU to the output bus.
- The shifter provides the shift micro-operations commonly not available in an ALU.

Shifter

- A shifter is a combinational circuit with one or more inputs and an equal number of outputs.
- The outputs are shifted with respect to the inputs.
- If only a shift left or a shift right is required, no gates are needed; such a shift can be accomplished with wires.



4-bit Combinational Shifter

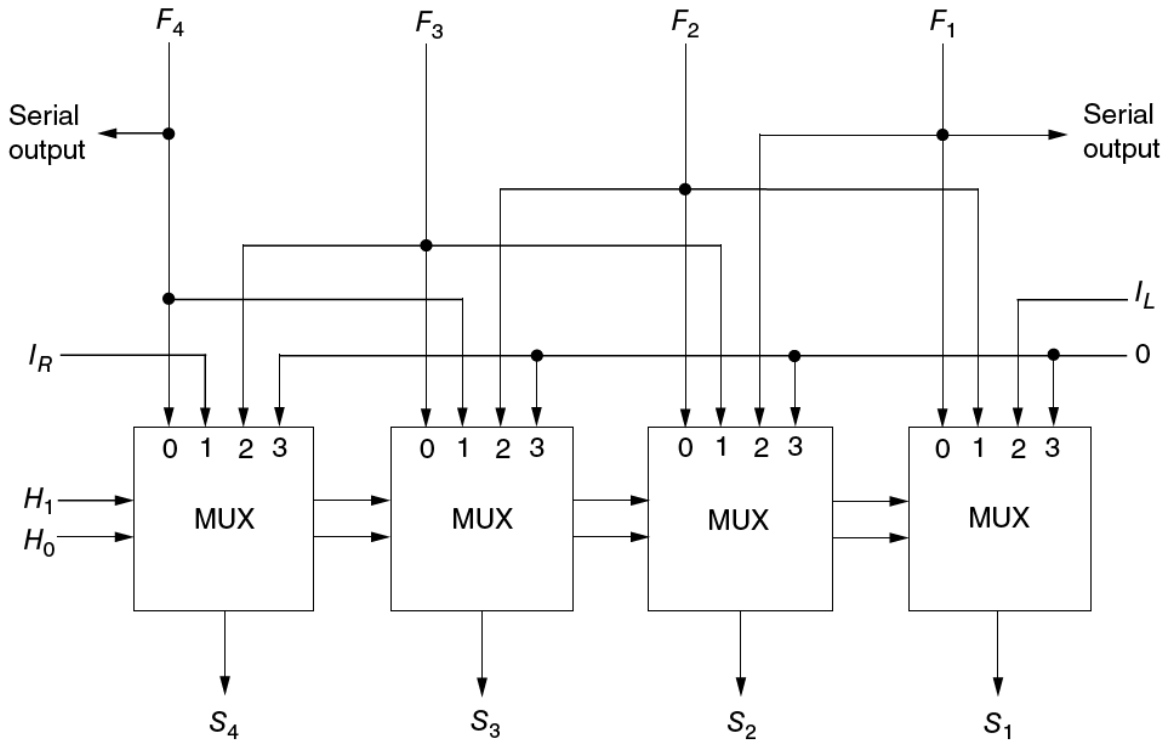


Figure 9-15 4-bit combinational-logic shifter

Comparator

- A magnitude digital Comparator is a combinational circuit that compares two digital or binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number.
- We logically design a circuit for which we will have two inputs one for A and other for B and have three output terminals, one for A > B condition, one for A = B condition and one for A < B condition.

1-Bit Magnitude Comparator

- A comparator used to compare two bits is called a single bit comparator. It consists of two inputs each for two single bit numbers and three outputs to generate less than, equal to and greater than between two binary numbers.

A	B	A<B	A=B	A>B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

2-Bit Magnitude Comparator

- A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator.
- It consists of four inputs and three outputs to generate less than, equal to and greater than between two binary numbers.

Truth Table for 2-bit Comparator

INPUT				OUTPUT		
A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

Circuit Diagram of 2-bit Comparator