East West University
Department of Computer Science and Engineering
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Course Code: CSE345
Course Title: Digital Logic Design
Section: 01

Experiment Number: 01
Experiment Title: Schematic and Structural Verilog Simulation of Combinational Logic Circuits

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Schematic Diagram:

The schematic diagram represents the combinational logic circuit described in Figure 1. Figure-01 is given below:

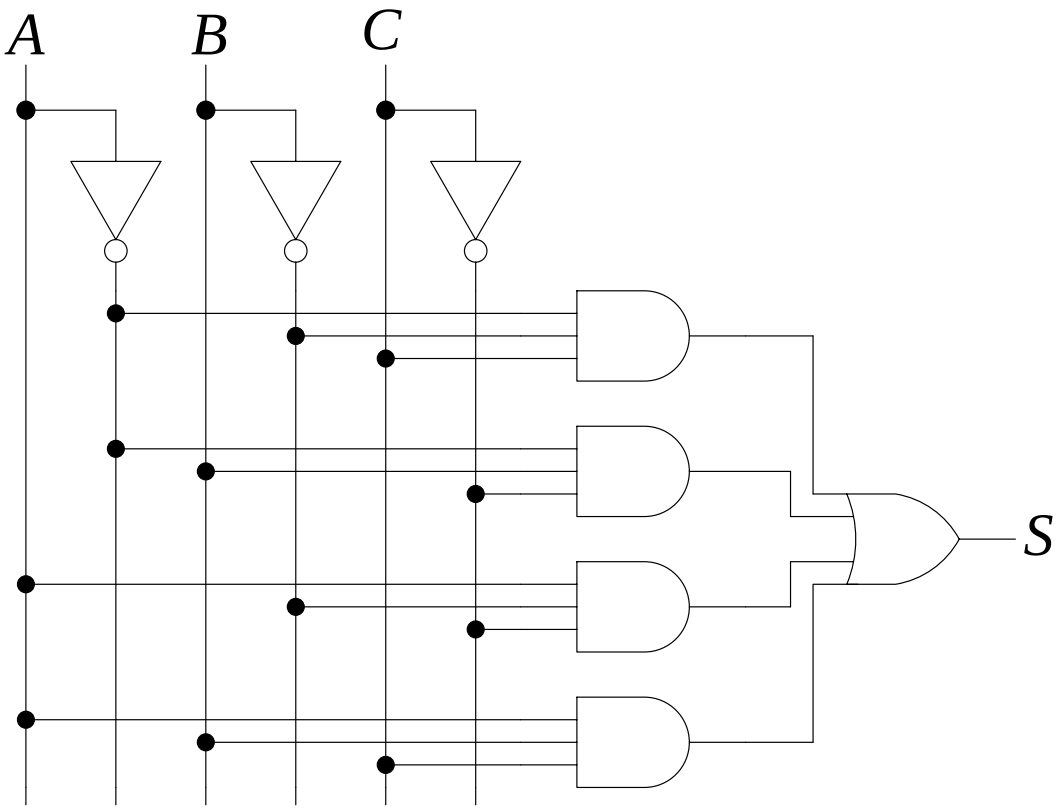
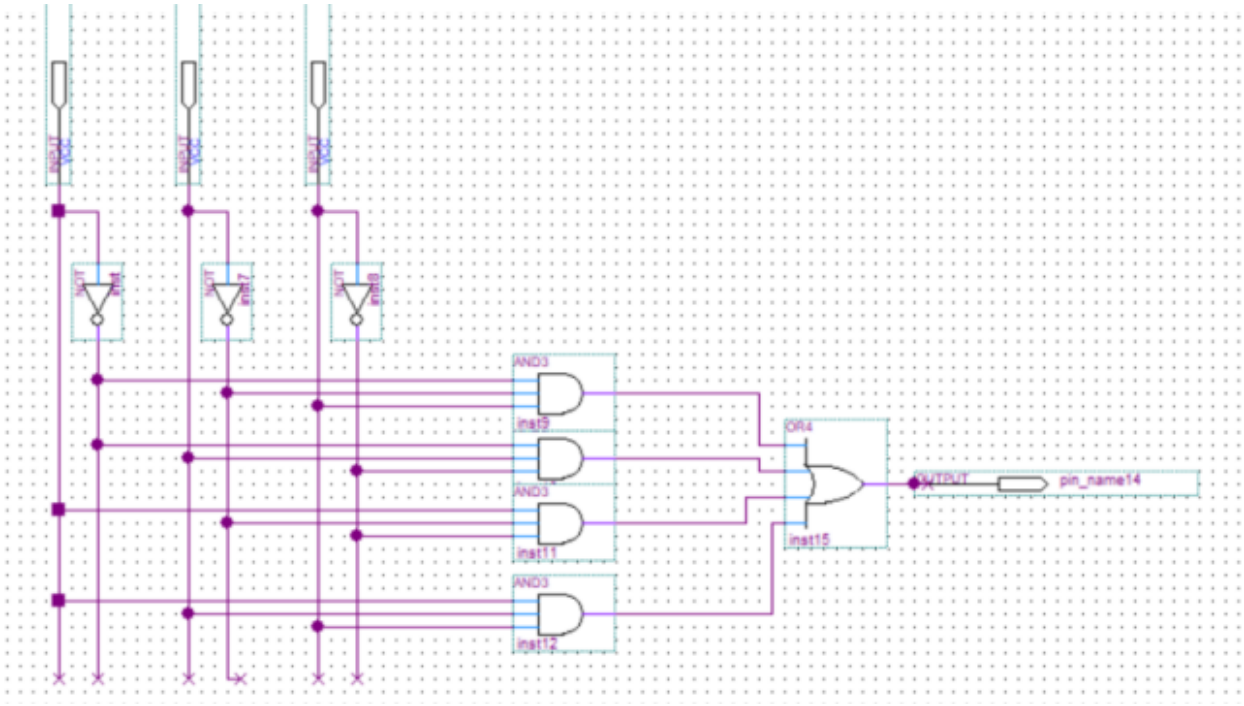


Figure -01: Combinational circuit for lab practice

The design includes the following components:

- AND gates to compute partial products of the Boolean equation.
- OR gate to combine the outputs of the AND gates.
- NOT gates for input inversion.

The design was created using Quartus II. The design of figure 7 in Quatrus II app is given below:



Result:

The simulation verified the functionality of the combinational logic circuit. The output S was consistent with the truth table:

A	B	C	S
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

We can determine Boolean expression from this table of this combinational circuit which is:

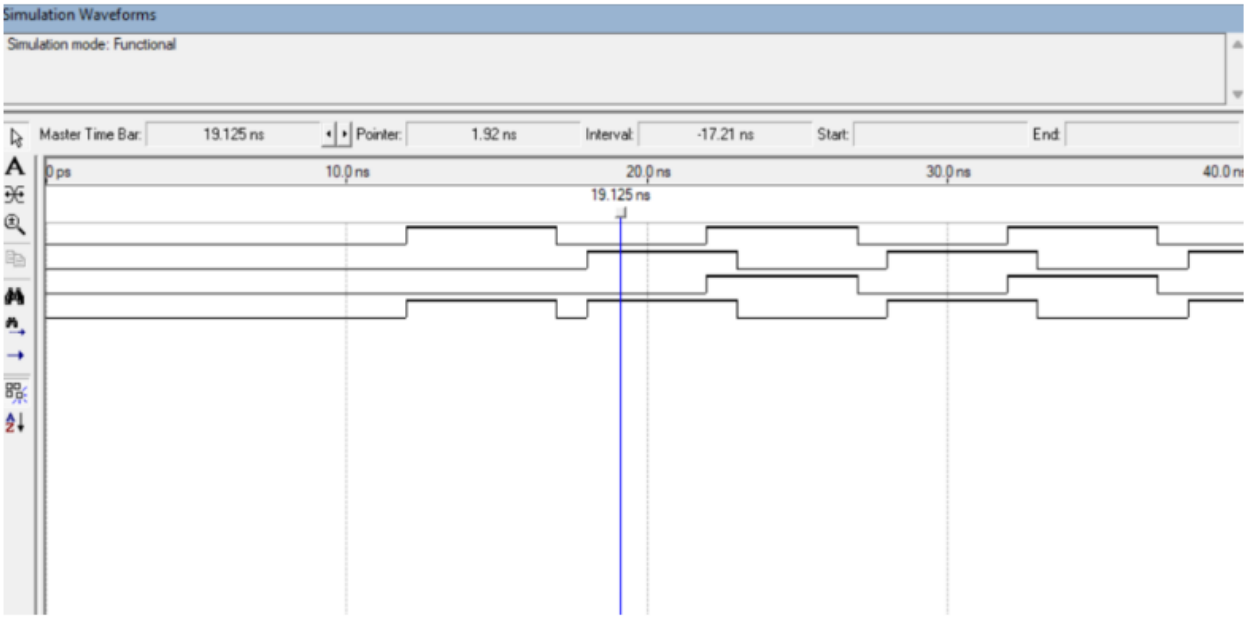
□ = □. □. □ + □. □. □+ □. □. □+ □. □. □

Both schematic and Verilog simulations matched these expected results, validating the design.

Response:

The simulation response was accurate. Both input signals A, B and C demonstrated the expected behavior when passed through the gates, producing the correct output S. The waveform of the simulation confirmed consistency with the truth table and Boolean equation, proving the circuit's functionality.

The simulation waveform of this combinational circuit is given below:



Brief Explanation:

This lab experiment aimed to provide practical experience in designing and simulating combinational logic circuits using schematic in Quartus II. The procedure involved:

1. Constructing the schematic circuit using basic logic gates.

2. Verifying the results of both methods against the truth table and Boolean equation.

The experiment successfully demonstrated the equivalence of schematic approaches for digital circuit simulation, enhancing understanding of logic design principles.