
# Department of Computer Science and Engineering

## Experiment 1.2

**Course Name:** Digital Logic Design

**Course Code:** CSE 345

**Instructor Name:** Nishat Tasnim

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**Group No:** 04

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**Date of Submission: 10th** March, 2025

## Experiment Name:

Experimenting with NAND gate IC (7400) and NOR gate IC (7402) to Prove their Universality.

## Objectives

- To Understand the concept of NAND and NOR gate
- To verify that NAND and NOR gates can be used to implement all basic logic gates (AND, OR, NOT)
- To compare experimental results using theoretical results.
- To simulate the designed circuits using computer software for verification.

# Tasks

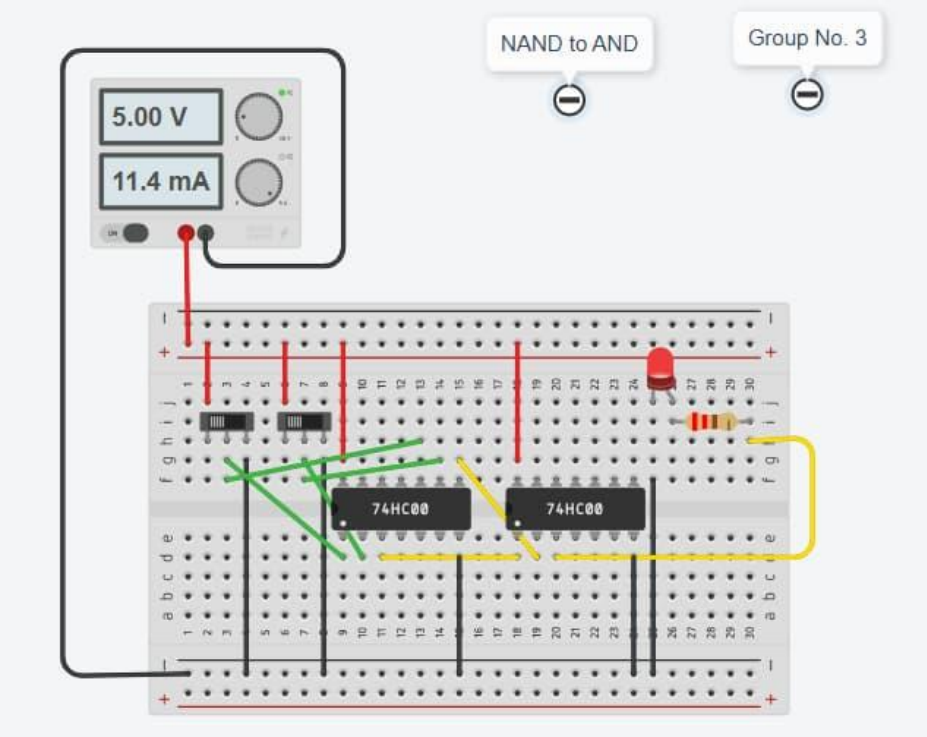
## Universality Prove: NAND Gate

### Task 1

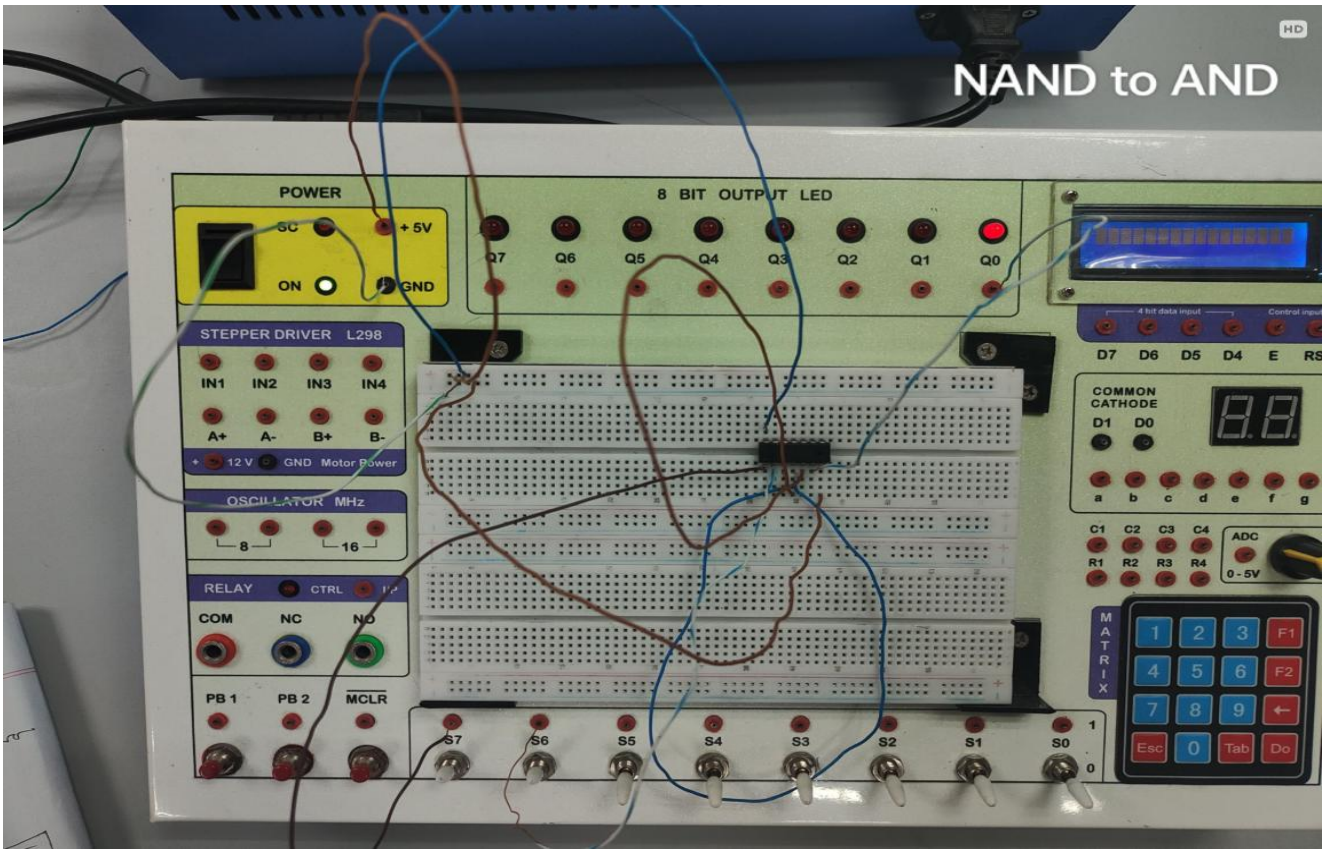
**Description:**

This task involves designing and implementing an AND gate using NAND gates. Since a NAND gate produces the inverse of an AND gate, an AND gate can be constructed by connecting the output of a NAND gate to another NAND operation. The circuit is tested using a simulation tool, and the outputs are verified against the expected AND gate truth table. So, the outputs will be 1 only when both inputs are 1, otherwise it outputs 0.

**Logic Circuit Diagram:**


NAND to AND
Group No. 3
5.00 V
11.4 mA
74HC00
74HC00

## Circuit:


NAND to AND
POWER
8 BIT OUTPUT LED
STEPPER DRIVER L298
OSCILLATOR MHz
RELAY
COMMON CATHODE
MATRIX

## Truth Table (NAND to AND gate):

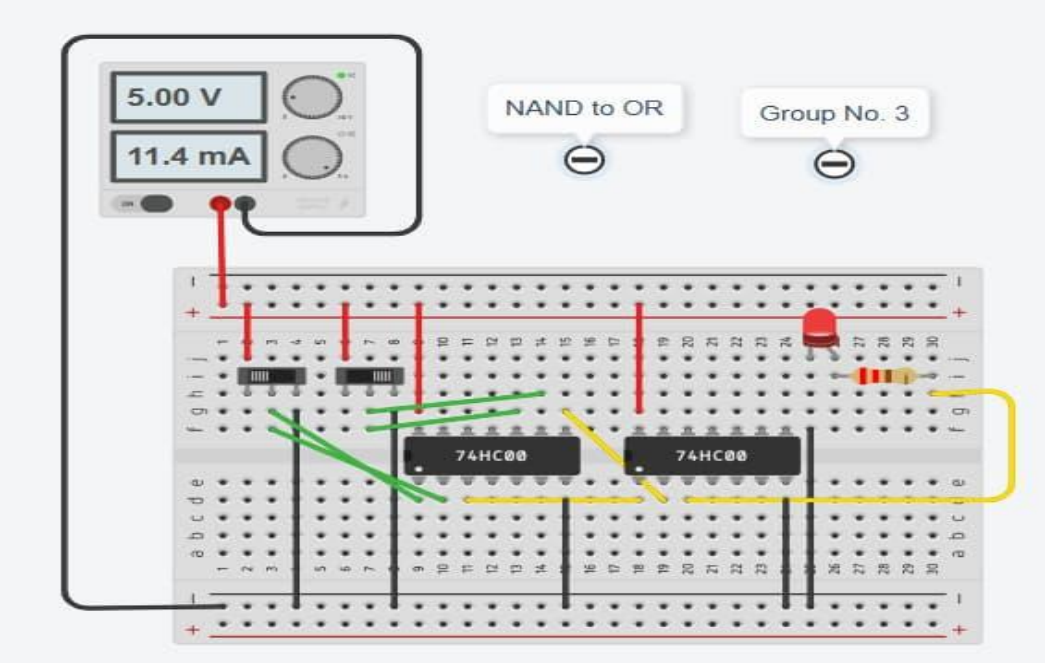
| Input A | Input B | Expected Output | Experimental Output |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

# Task 2

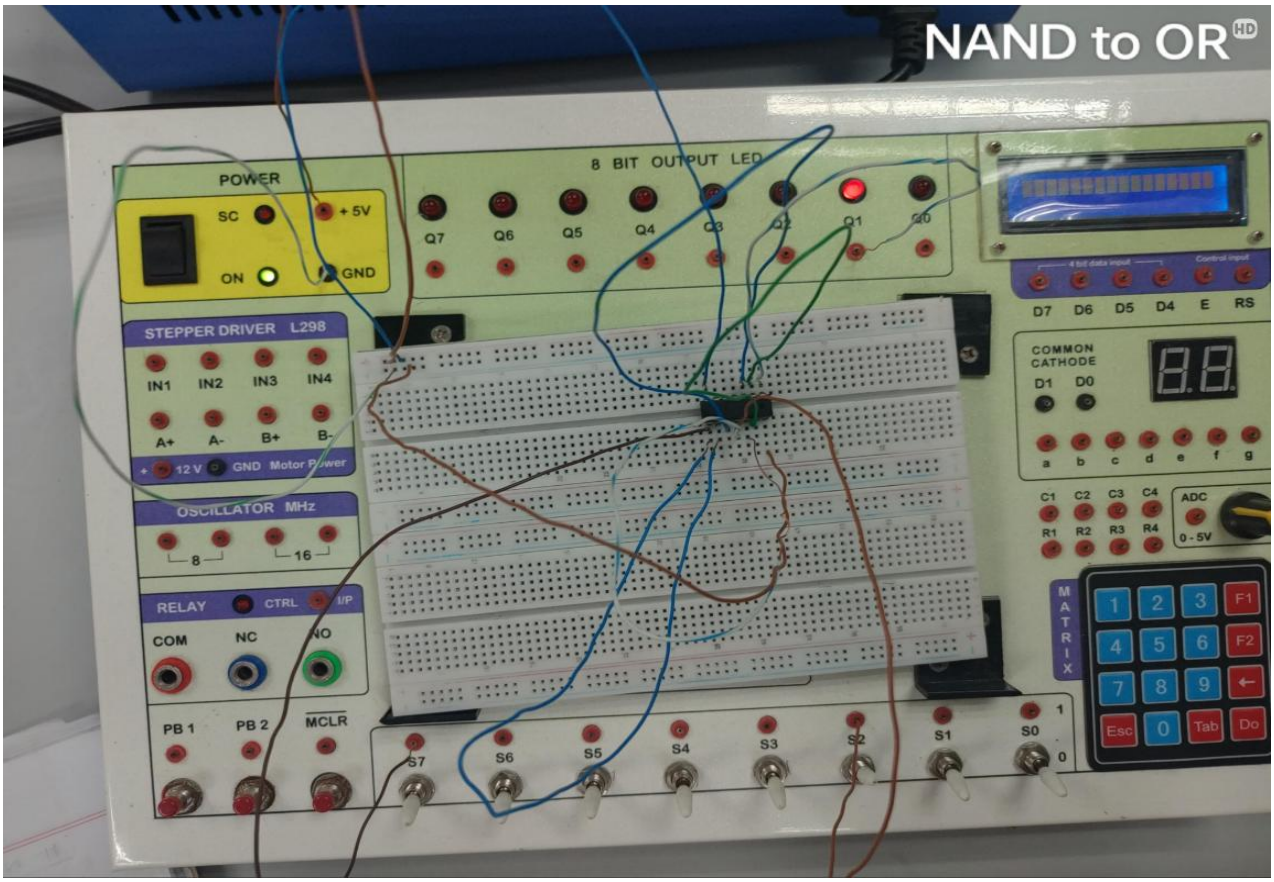
### Description:

This task involves designing and implementing an OR gate using only NAND gates. Since NAND is a universal gate, an OR gate can be constructed by applying De Morgan's theorem. The circuit is tested using a simulation tool, and the outputs are verified against the expected OR gate truth table. The outputs will be 1 when at least one input is 1.

## Logic Circuit Diagram:




## Circuit:



## Truth Table (NAND to OR gate):

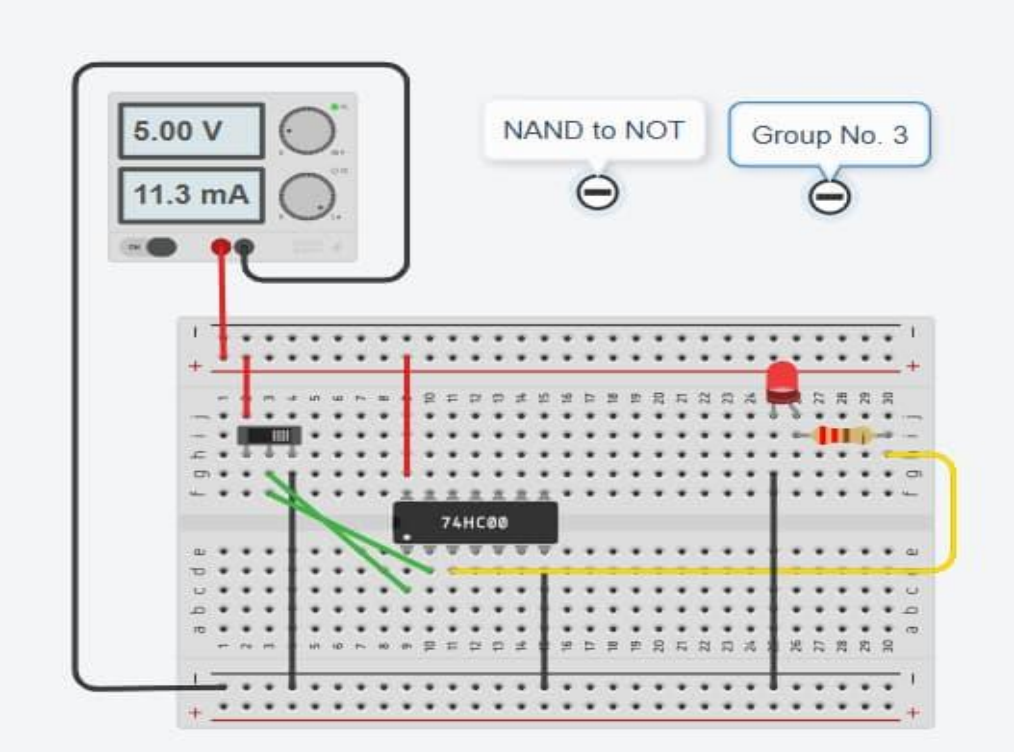
| Input A | Input B | Expected Output | Experimental Output |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

# Task 3

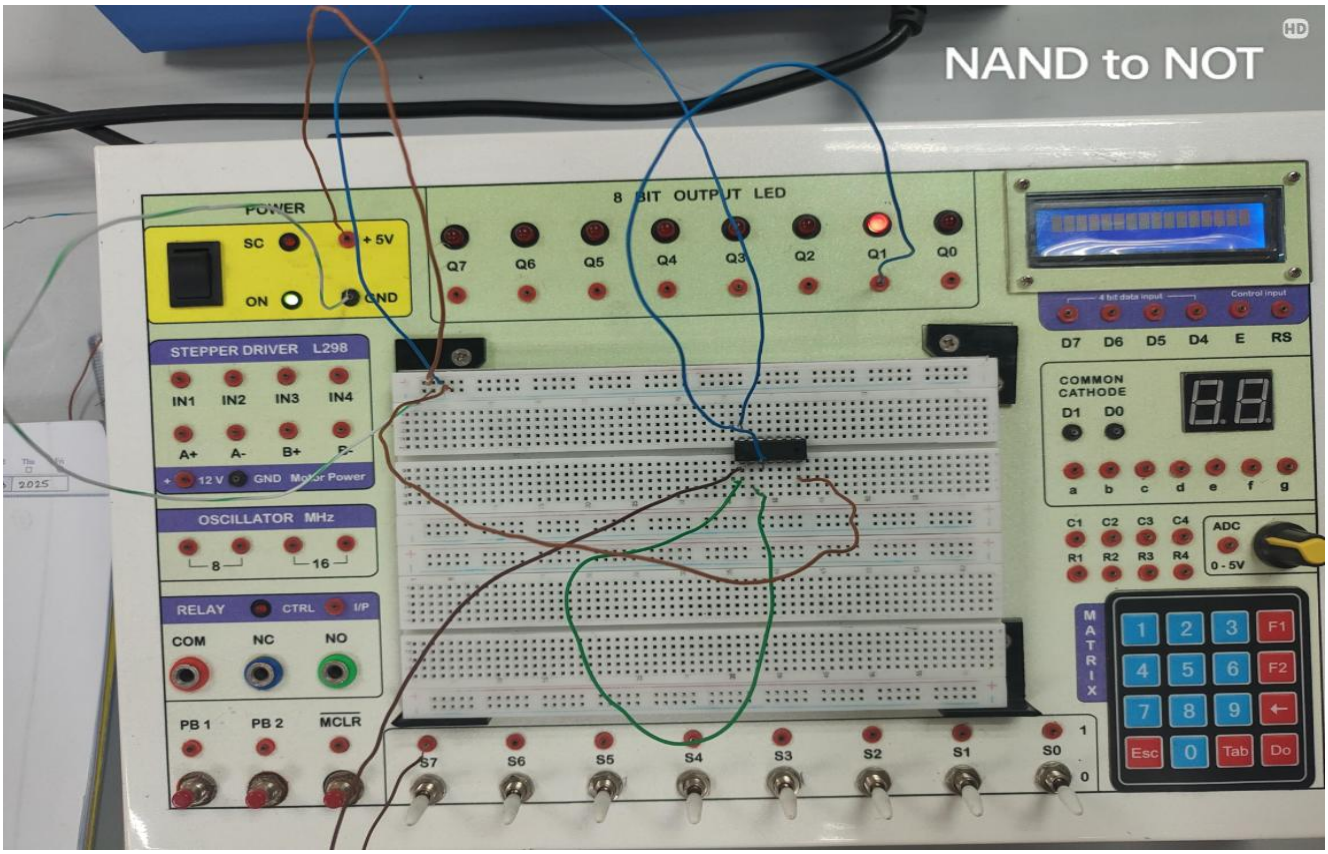
## Description:

This task involves designing and implementing a NOT gate using a single NAND gate. Since a NAND gate outputs the inverse of an AND operation, a NOT gate can be created by connecting both inputs of the NAND gate together. The circuit is tested using a simulation tool, and the outputs are verified against the expected NOT gate truth table. So, if input is 0, output will be 1 and if input is 1, output will be 0.

## Logic Circuit Diagram:


5.00 V
11.3 mA
NAND to NOT
Group No. 3
74HC00

## Circuit:


NAND to NOT
HD
POWER
SC
ON
+ 5V
GND
8 BIT OUTPUT LED
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
STEPPER DRIVER L298
IN1
IN2
IN3
IN4
A+
A-
B+
B-
12 V
GND
Motor Power
OSCILLATOR MHz
8
16
RELAY
CTRL
I/P
COM
NC
NO
PB 1
PB 2
MCLR
S7
S6
S5
S4
S3
S2
S1
S0
D7
D6
D5
D4
E
RS
COMMON CATHODE
D1
D0
a
b
c
d
e
f
g
C1
C2
C3
C4
R1
R2
R3
R4
ADC
0 - 5V
MATRIX
1
2
3
F1
4
5
6
F2
7
8
9
←
Esc
0
Tab
Do

### Truth Table (NAND to NOT gate):

| Input A | Expected Output | Experimental Output |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 0 | 0 |

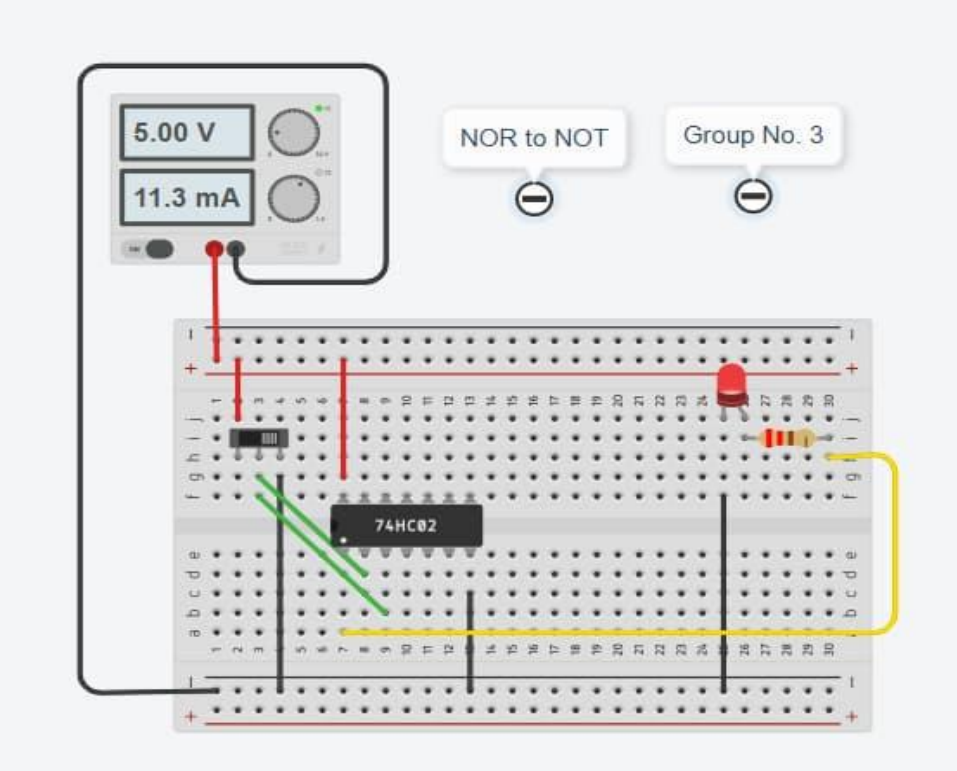
## Universality Prove: NOR Gate

### Task 4

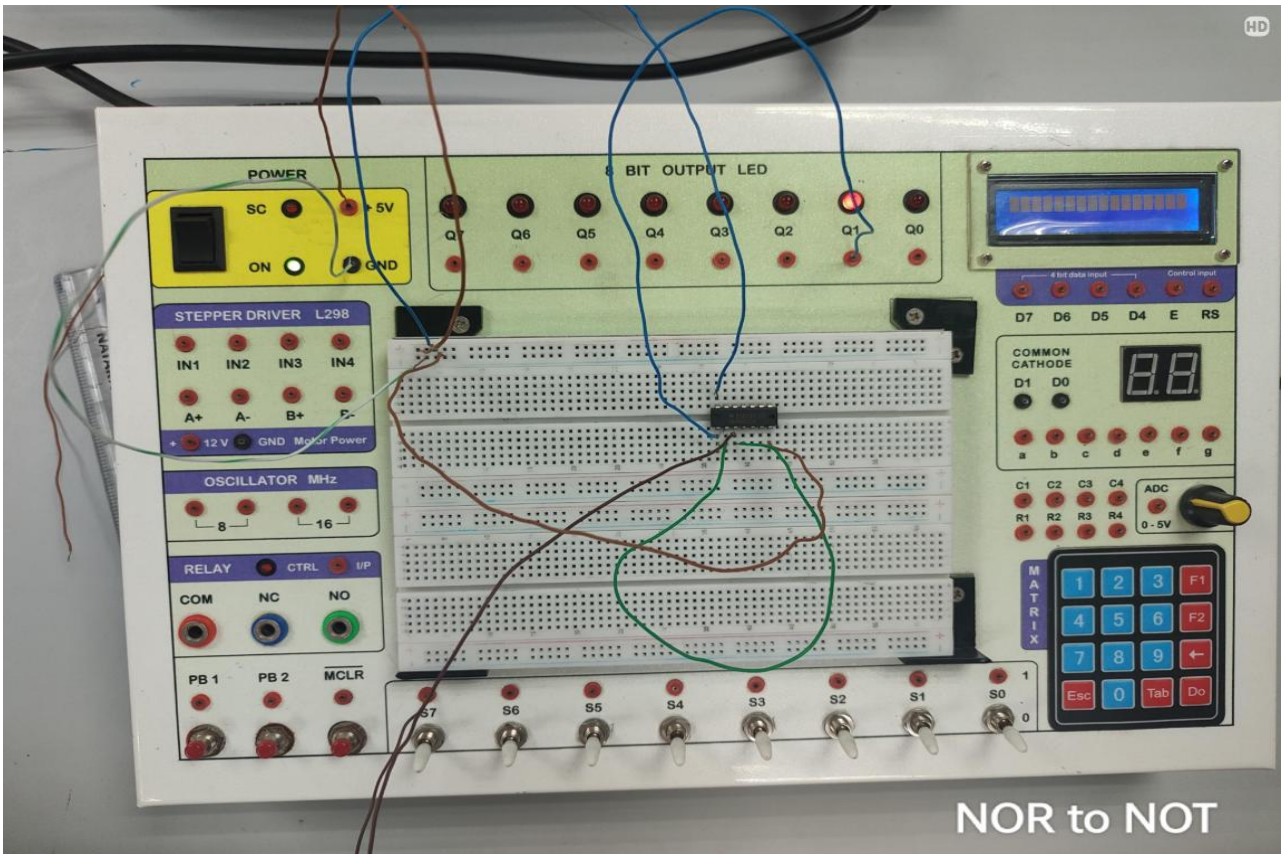
**Description:**

This task involves designing and implementing a NOT gate using a single NOR gate. Since a NOR gate outputs the inverse of an OR operation, a NOT gate can be created by connecting both inputs of the NOR gate together. The circuit is tested using a simulation tool, and the outputs are verified against the expected NOT gate truth table. So, if input is 0, output will be 1 and if input is 1, output will be 0.

**Logic Circuit Diagram:**


5.00 V
11.3 mA
NOR to NOT
Group No. 3
74HC02

## Circuit:


POWER
SC
ON
+5V
GND
8 BIT OUTPUT LED
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
STEPPER DRIVER L298
IN1
IN2
IN3
IN4
A+
A-
B+
B-
12 V
GND
Motor Power
OSCILLATOR MHz
8
16
RELAY
CTRL
I/P
COM
NC
NO
PB 1
PB 2
MCLR
D7
D6
D5
D4
E
RS
COMMON CATHODE
D1
D0
ADC
0 - 5V
MATRIX
S7
S6
S5
S4
S3
S2
S1
S0
NOR to NOT

## Truth Table (NOR to NOT gate):

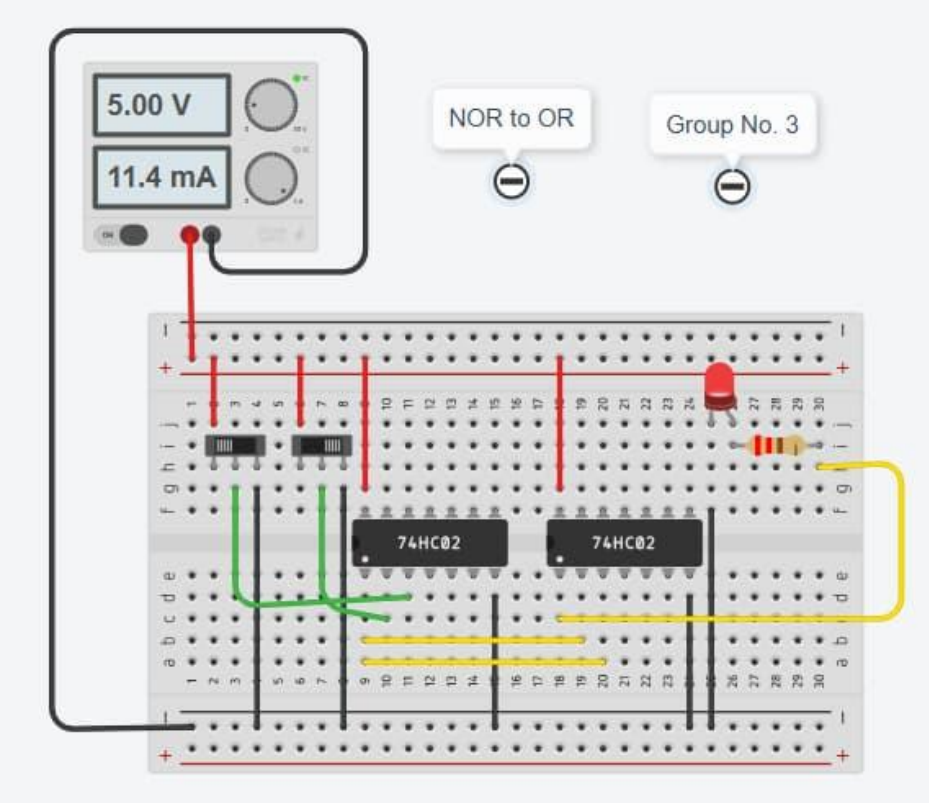
| Input A | Expected Output | Experimental Output |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 0 | 0 |

# Task 5

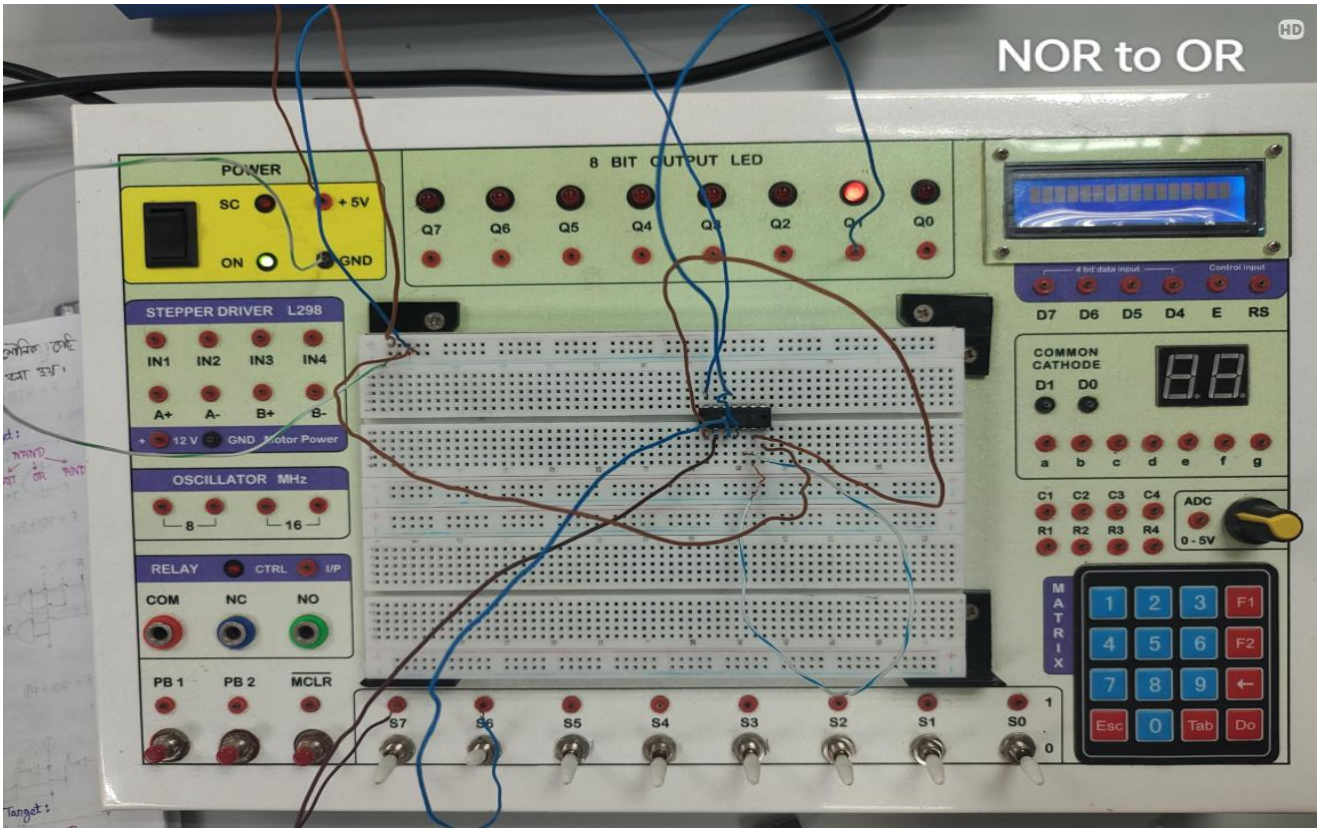
## Description:

This task involves designing and implementing an OR gate using only NOR gates. By applying De Morgan's theorem, an OR gate can be constructed using multiple NOR gates. The circuit is tested using a simulation tool, and the outputs are verified against the expected OR gate truth table. The outputs will be 1 when at least one input is 1.

## Logic Circuit Diagram:


5.00 V
11.4 mA
NOR to OR
Group No. 3
74HC02
74HC02

## Circuit:


NOR to OR
HD
POWER
SC
+ 5V
ON
GND
8 BIT OUTPUT LED
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
STEPPER DRIVER L298
IN1
IN2
IN3
IN4
A+
A-
B+
B-
12 V
GND
Motor Power
OSCILLATOR MHz
8
16
RELAY
CTRL
I/P
COM
NC
NO
PB 1
PB 2
MCLR
4 bit data input
Control input
D7
D6
D5
D4
E
RS
COMMON CATHODE
D1
D0
a
b
c
d
e
f
g
C1
C2
C3
C4
R1
R2
R3
R4
ADC
0 - 5V
MATRIX
1
2
3
F1
4
5
6
F2
7
8
9
Esc
0
Tab
Do
S7
S6
S5
S4
S3
S2
S1
S0
1
0

## Truth Table (NOR to OR gate):

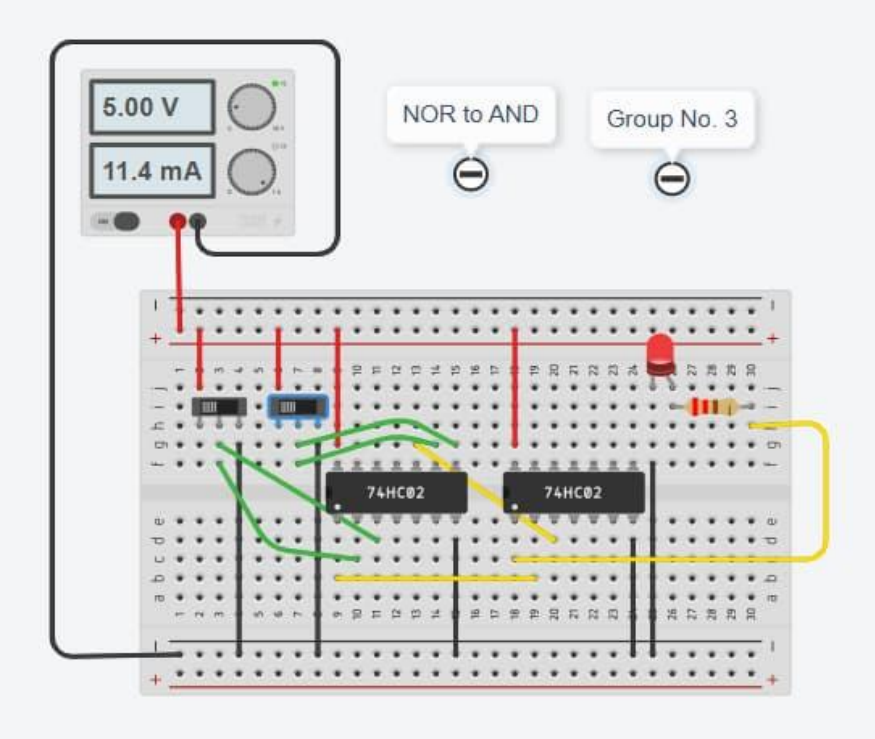
| Input A | Input B | Expected Output | Experimental Output |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

# Task 6

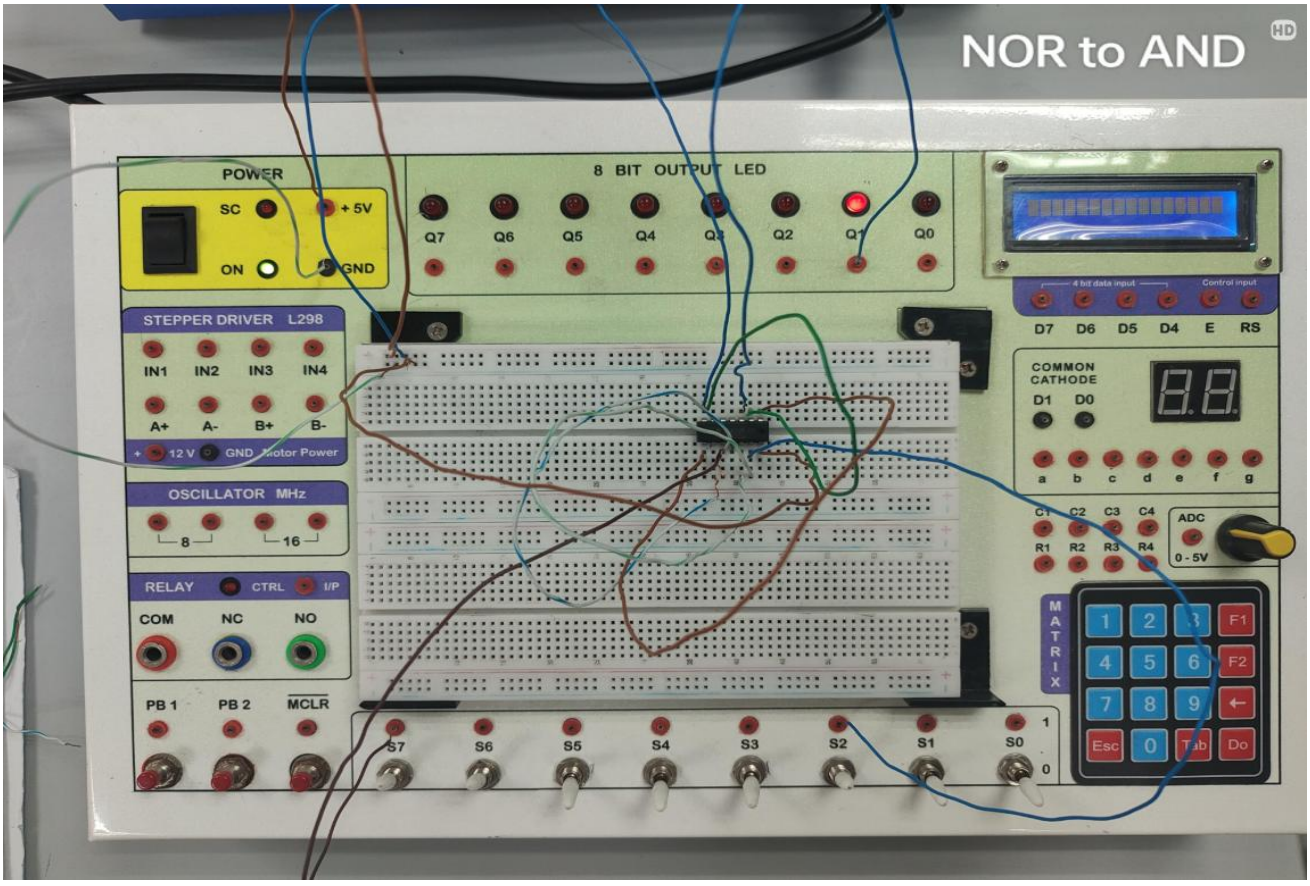
## Description:

This task involves designing and implementing an AND gate using only NOR gates. By applying De Morgan's theorem, an AND gate can be constructed using multiple NOR gates. The circuit is tested using a simulation tool, and the outputs are verified against the expected AND gate truth table. So, the outputs will be 1 only when both inputs are 1, otherwise it outputs 0.

## Logic Circuit Diagram:


5.00 V
11.4 mA
NOR to AND
Group No. 3
74HC02
74HC02

## Circuit:


NOR to AND
HD
POWER
SC
ON
+ 5V
GND
8 BIT OUTPUT LED
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
STEPPER DRIVER L298
IN1
IN2
IN3
IN4
A+
A-
B+
B-
12 V
GND
Motor Power
OSCILLATOR MHz
8
16
RELAY
CTRL
I/P
COM
NC
NO
PB 1
PB 2
MCLR
S7
S6
S5
S4
S3
S2
S1
S0
D7
D6
D5
D4
E
RS
COMMON CATHODE
D1
D0
a
b
c
d
e
f
g
C1
C2
C3
C4
R1
R2
R3
R4
ADC
0 - 5V
MATRIX
1
2
3
F1
4
5
6
F2
7
8
9
←
Esc
0
Tab
Do

**Truth Table (NOR to AND Gate):**

| Input A | Input B | Expected Output | Experimental Output |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

## Discussion:

During the experiment, the expected results were compared with the actual outcomes, and the constructed logic gates behaved as anticipated, aligning with their respective truth tables. Some minor discrepancies were observed due to factors like faulty components, voltage variations, and improper wiring. Challenges included debugging circuit errors, ensuring proper gate functionality, and handling unstable outputs. Despite these difficulties, the experiment successfully validated the universality of NAND and NOR gates, reinforcing their importance in digital logic design and providing a deeper understanding of fundamental logic operations.

Subject : CSE 345(LAB)

Sat Sun Mon Tue Wed Thu Fri

Time | Date 04 03 2025

Group → 03

1. 2022 - 3 - 60 - 064

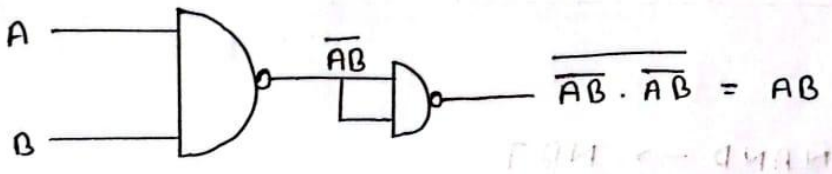
2. 2022 — 3-60- 221

3. 2023 - 1 - 60 - 121

4.

## NAND Gate Universality Prove:

① NAND → AND



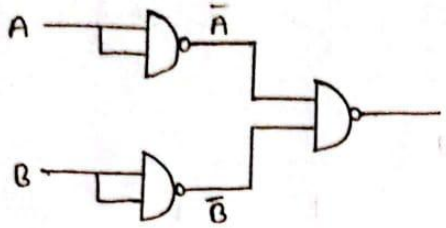

| A | B | Y (Expected) | Y (Experiment) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

Subject :.....

Sat Sun Mon Tue Wed Thu Fri

Time Date

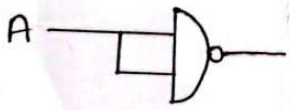
(2) NAND → OR




$\overline{\bar{A}.\bar{B}} = A+B$

| A | B | Y (Expected) | Y (Experiment) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

(3) NAND → NOT




$\overline{A.A} = \bar{A}$

| A | Y (Expected) | Y (Experiment) |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 0 | 0 |

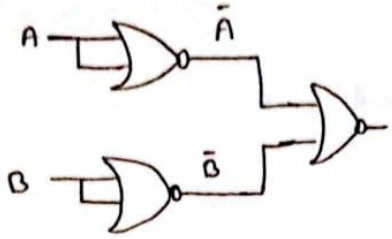
Subject :.....

Sat Sun Mon Tue Wed Thu Fri

Time Date

# NOR Gate Universality Prove:

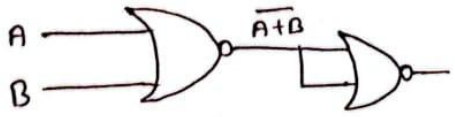
## ① NOR → AND




$\overline{\bar{A}+\bar{B}} = AB$

| A | B | Y (Expected) | Y (Experiment) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

## ② NO R → OR




$\overline{\overline{A+B} + \overline{A+B}} = A+B$

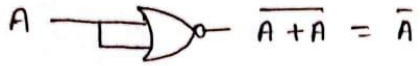
| A | B | Y (Expected) | Y (Experiment) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 |

Subject :.....

Sat Sun Mon Tue Wed Thu Fri

Time Date

③ NOR → NOT




| A | Y (Expected) | Y (Experiment) |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 0 | 0 |

4/3/25