East West University

Department of Computer Science and Engineering

Course Name: Digital Logic Design

Course Code: CSE345

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Project Name: 4-bit Binary to Even Parity Code Converter

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Group No: 03

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1. Problem Statement

1.1 Mini-Project Name:

4-bit Binary to Even Parity Code Converter

1.2 Objectives

1. To learn about parity bit.
2. To generate the even parity bit for a 4-bit data.
3. To develop skill in data collection analysis.

1.3 Introduction

What is **Parity bit**?

- A *parity bit* is a basic way to check for errors in digital communications and data storage, used to make sure data stays accurate. It's an extra binary digit added to a string of binary code. In digital systems, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s (of data bits) to 1s and 1s to 0s.

The sum of the data bits and parity bits can be **even** or **odd**.

In this mini-project, we will understand the functionality of Even Parity.

Even Parity: The parity bit is adjusted so that the total number of 1s in the code, including the parity bit, is even. If there are already an even number of 1s, the parity bit is 0. If there are an odd number of 1s, the parity bit is 1.

2. Design Details

2.1 Truth Table:

Input Variable				Parity Bit	Output Variable			
A	**B**	**C**	**D**	**P**	**E**	**F**	**G**	**H**
0	0	0	0	**0**	0	0	0	0
0	0	0	1	**1**	0	0	0	1
0	0	1	0	**1**	0	0	1	0
0	0	1	1	**0**	0	0	1	1
0	1	0	0	**1**	0	1	0	0
0	1	0	1	**0**	0	1	0	1
0	1	1	0	**0**	0	1	1	0
0	1	1	1	**1**	0	1	1	1
1	0	0	0	**1**	1	0	0	0
1	0	0	1	**0**	1	0	0	1
1	0	1	0	**0**	1	0	1	0
1	0	1	1	**1**	1	0	1	1
1	1	0	0	**0**	1	1	0	0
1	1	0	1	**1**	1	1	0	1
1	1	1	0	**1**	1	1	1	0
1	1	1	1	**0**	1	1	1	1

2.2 K-Map and Function for Output P

AB \ CD	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

2.3 Logical Expression:

$$P = A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D}$$

$$= (\bar{A}B + A\bar{B})\bar{C}\bar{D} + \bar{A}\bar{B}(\bar{C}D + C\bar{D}) + CD(\bar{A}B + A\bar{B}) + AB(\bar{C}D + C\bar{D})$$

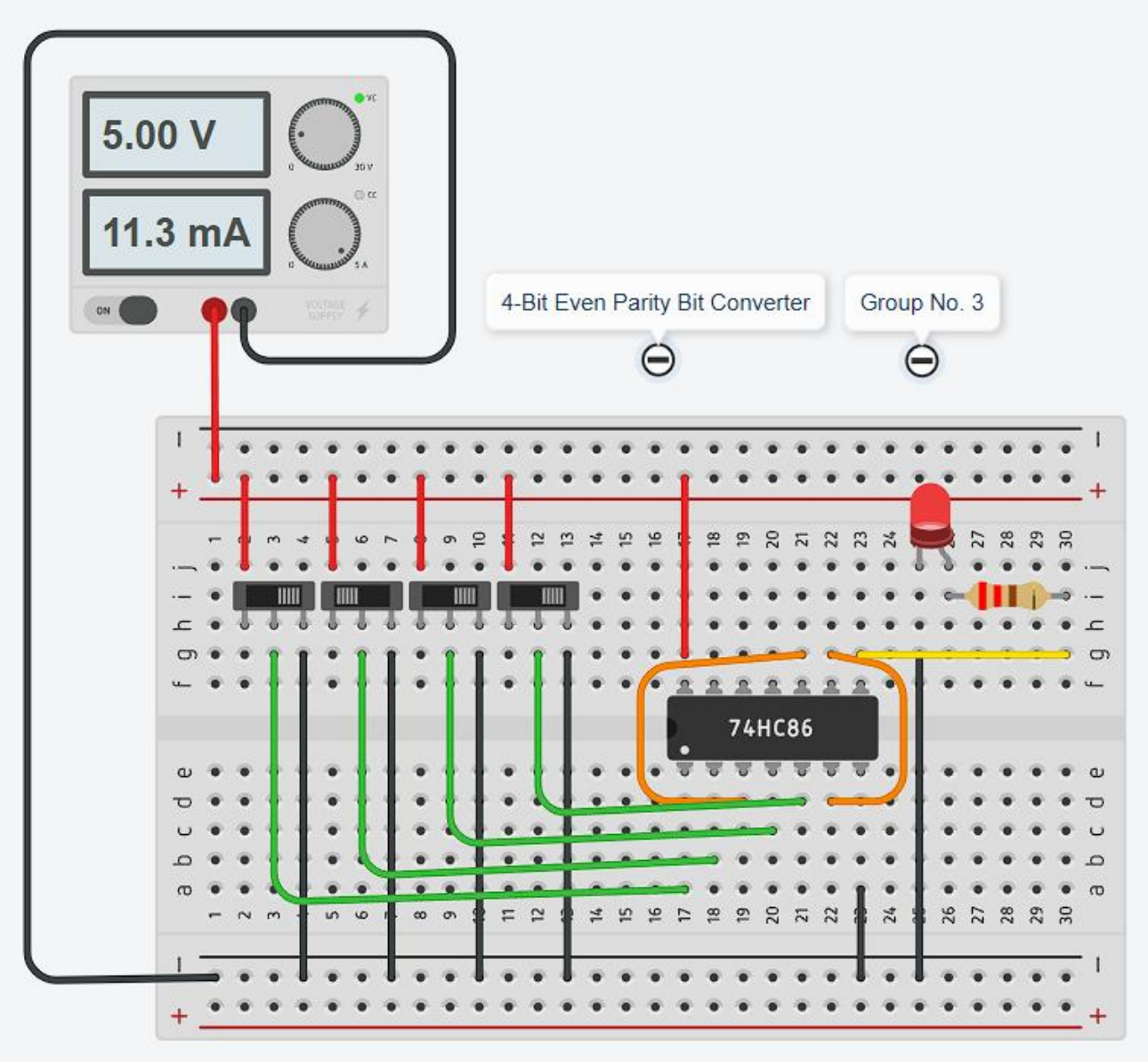
$$= (\bar{A}B + A\bar{B})(\bar{C}\bar{D} + CD) + (\bar{A}\bar{B} + AB)(\bar{C}D + C\bar{D})$$

$$= (A \oplus B)(\overline{C \oplus D}) + (\overline{A \oplus B})(C \oplus D)$$

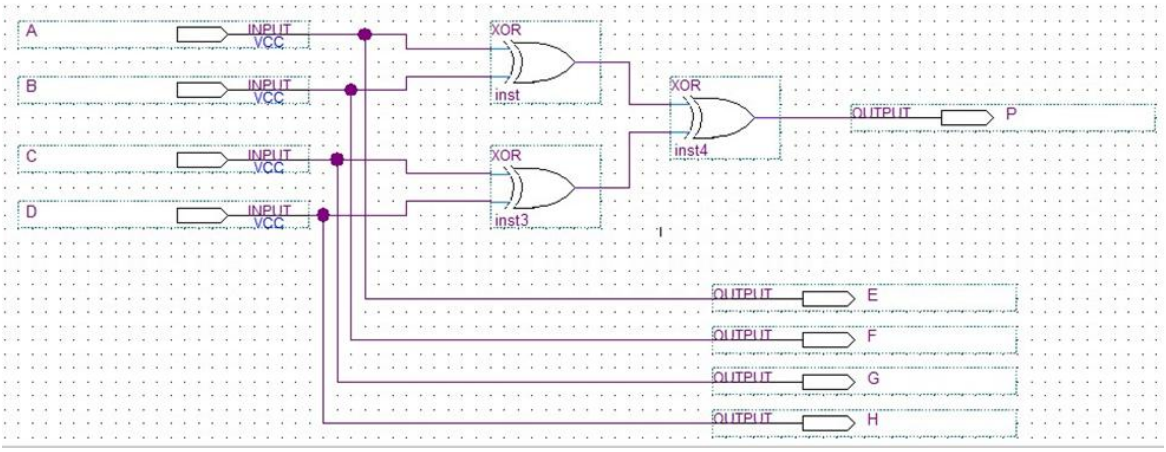
$$= A \oplus B \oplus C \oplus D$$

3. Circuit Diagram

3.1 TinkerCAD:



3.2 Quartus II:



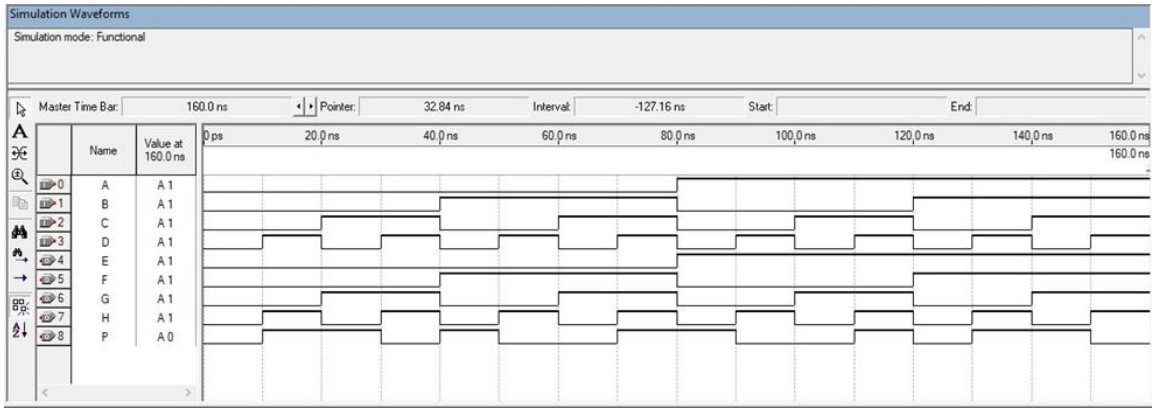
3.2.1 Verilog Code

ex1

Simulation Report

```
1   module ex1 (input A,B,C,D, output P,E,F,G,H);
2     wire w1,w2;
3     xor g1(W1,A,B),
4         g2(W2,C,D),
5         g3(P,W1,W2);
6     and g4(E,A),
7         g5(F,B),
8         g6(G,C),
9         g7(H,D);
10  endmodule
```

3.2.2 Simulation

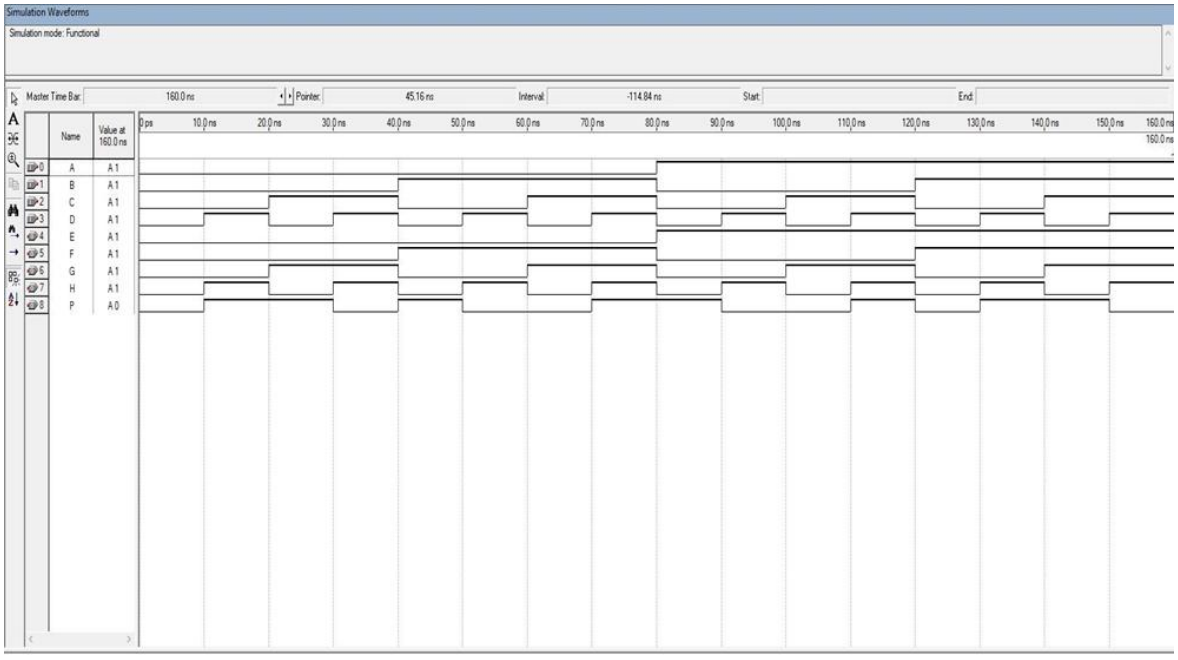


4. Behavioral Verilog Code

4.1 Procedural Model Statement:

```
1  module expt2 (input A,B,C,D,output reg P,E,F,G,H);
2  always@(A,B,C,D) begin
3   P=0;
4   if(~A&~B&~C&D)P=1;
5   if(~A&~B&C&~D)P=1;
6   if(~A&B&~C&~D)P=1;
7   if(~A&B&C&D)P=1;
8   if(A&~B&~C&~D)P=1;
9   if(A&~B&C&D)P=1;
10  if(A&B&~C&D)P=1;
11  if(A&B&C&~D)P=1;
12  if (A==0)
13  E=0;
14  else E=1;
15  if (B==0)
16  F=0;
17  else F=1;
18  if (C==0)
19  G=0;
20  else G=1;
21  if (D==0)
22  H=0;
23  else H=1;
24
25  end
26  endmodule
27
```

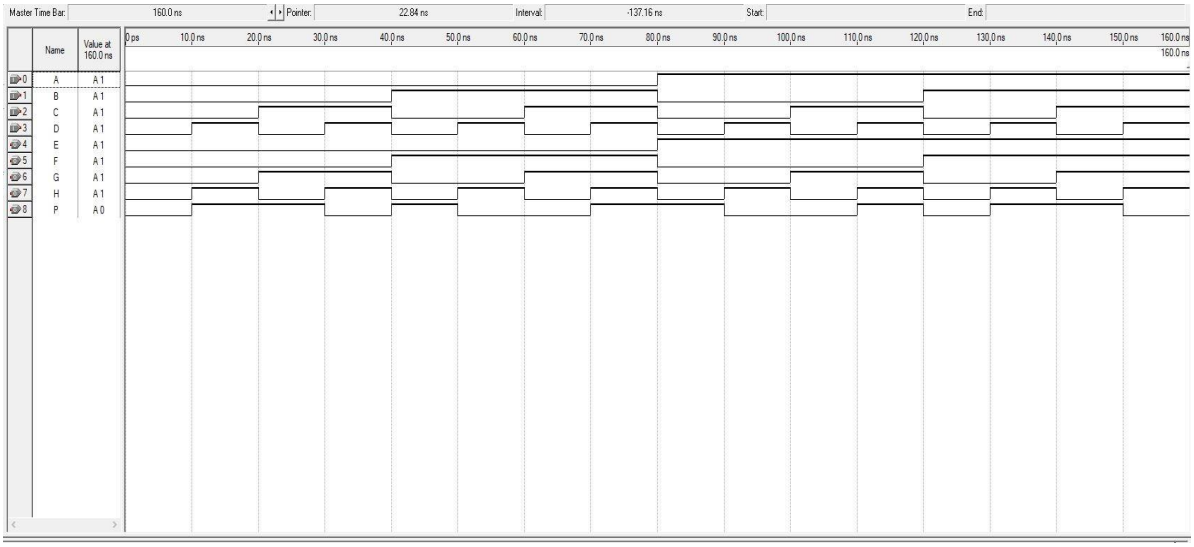
Simulation Result:



4.2 Continuous Assign Statement:

```
module ex1 (input A,B,C,D, output P,E,F,G,H);
assign P=(~A&~B&~C&D)|(~A&~B&C&~D)|(~A&B&~C&~D)|(~A&B&C&D)|(A&~B&~C&~D)|(A&~B&C&D)|(A&B&~C&D)|(A&B&C&~D);
assign E=A;
assign F=B;
assign G=C;
assign H=D;
endmodule
```

Simulation Result:



5. Conclusion

In this project, we designed and implemented a 4-bit binary to even parity bit converter, which calculates a parity bit for a given 4-bit input to ensure that the total number of 1s (including the parity bit) is even. The logic used—a series of XOR gates—efficiently determines the parity bit based on the binary input values.

Overall, the 4-bit parity bit generator is a simple yet powerful application of combinational logic and serves as a foundational building block in digital communication and fault-tolerant systems.