Department of Computer Science and Engineering

Course Name: Digital Logic Design

Course Code: CSE 345

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Date of Submission: 6th March, 2025

Experiment No: 1.1

Experiment Name

Experimenting and Simulating Basic, Universal, and Exclusive Logic Gates

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Objectives

- To understand the operation of basic logic gates (AND, OR, NOT), universal gates (NAND, NOR).
- To study the behavior of exclusive gates (X-OR, X-NOR).
- To simulate and verify the performance of these gates using computer software.
- To construct and test logic gates using gate ICs.

Required Equipments

1. NOT Gate (IC No. 7404)
2. OR Gate (IC No. 7432)
3. AND Gate (IC No. 7408)
4. NAND Gate (IC No. 7400)
5. NOR Gate (IC No. 7402)
6. XOR Gate (IC No. 7486)
7. XNOR Gate (IC No. 74266)
8. Connecting Wires
9. Breadboard
10.

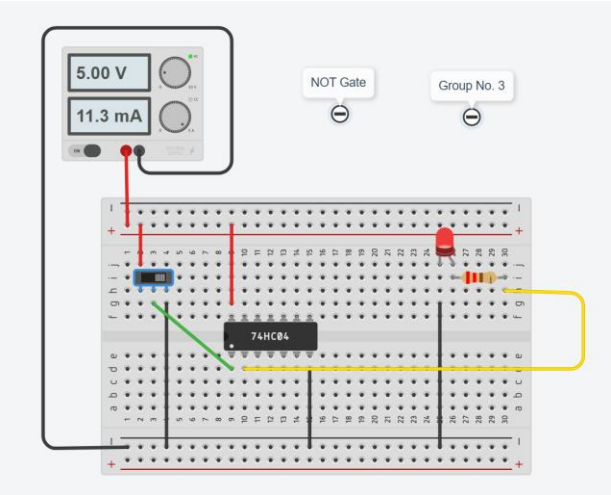
Tasks

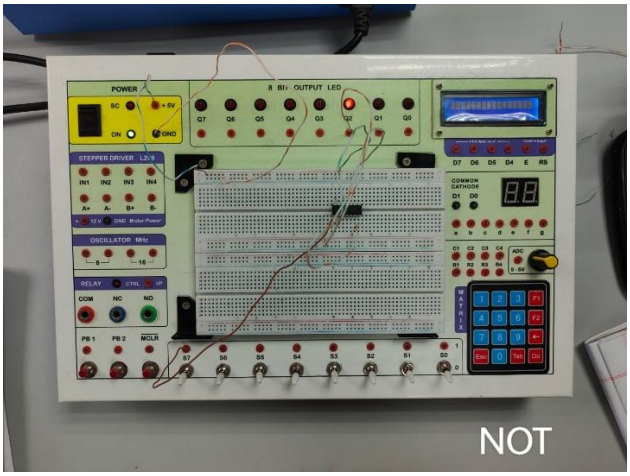
Task 1

Description:

Task 1 involves the understanding of the basic function of the NOT gate, where the output is HIGH (1) only if the input is LOW (1).

Logic Circuit Diagram:





Truth Table (Experimental Results):

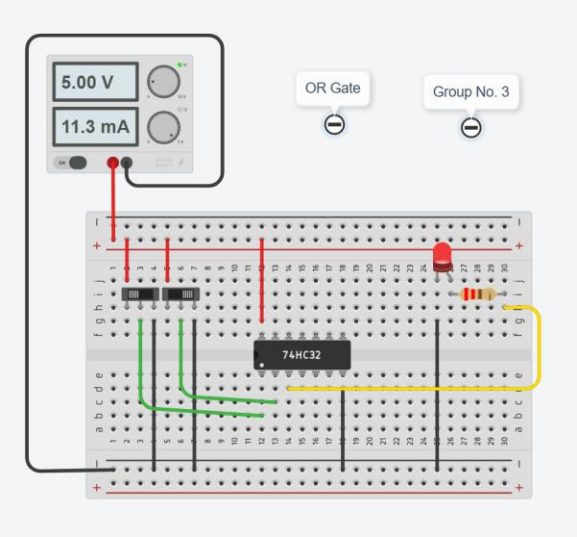
Input B	Expected Output	Experimental Output
0	1	1
1	0	0

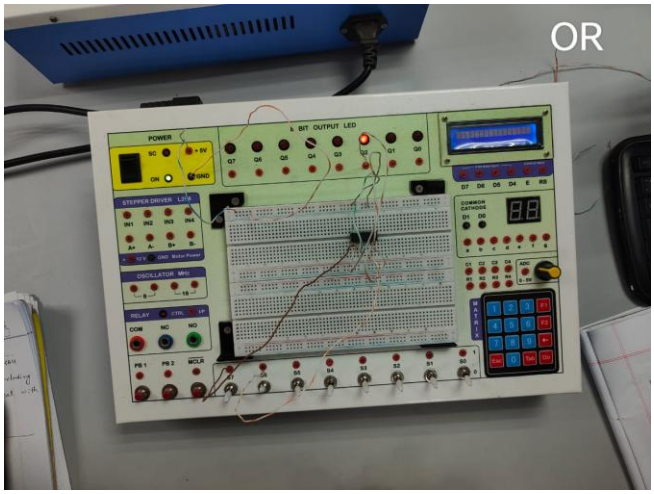
Task 2

Description:

Task 2 involves the understanding of the basic function of the OR gate, where the output is HIGH (1) only if either both inputs are HIGH (1) or just one input is HIGH (1).

Logic Circuit Diagram:





Truth Table (Experimental Results):

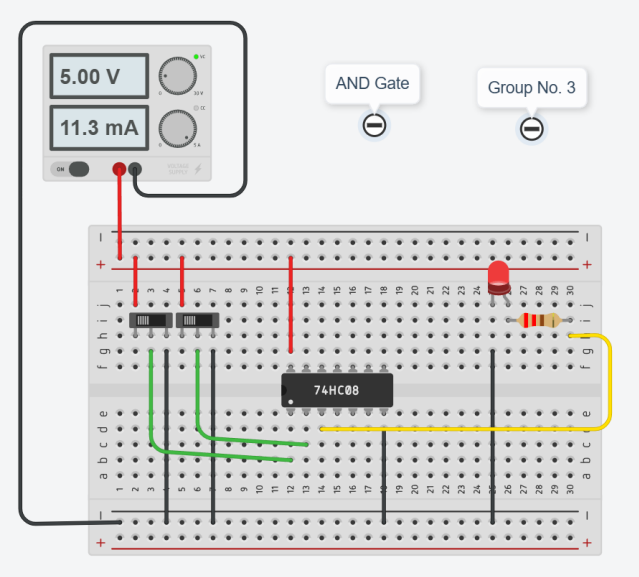
Input A	Input B	Expected Output	Experimental Output
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

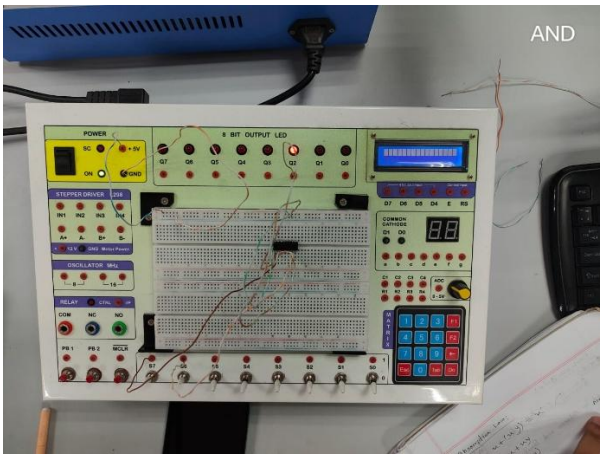
Task 3

Description:

Task 3 involves the understanding of the basic function of the AND gate, where the output is HIGH (1) only if both inputs are HIGH (1).

Logic Circuit Diagram:





Truth Table (Experimental Results):

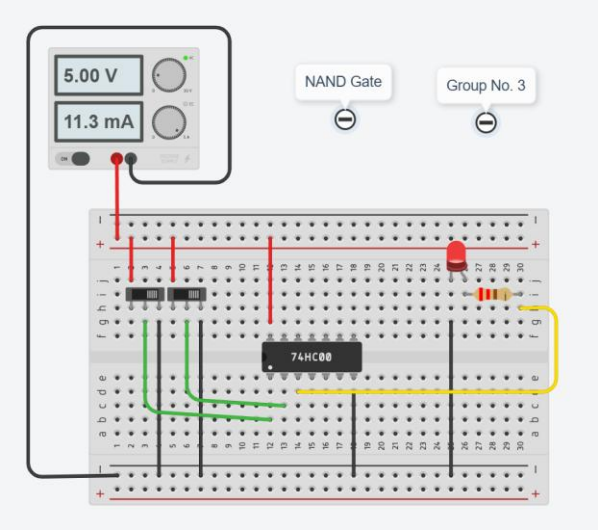
Input A	Input B	Expected Output	Experimental Output
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

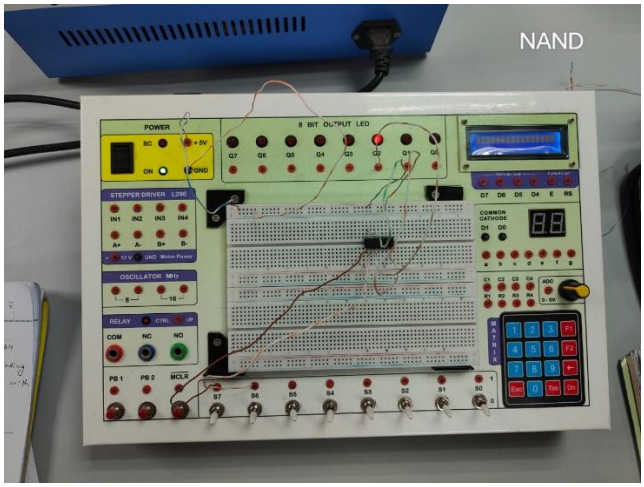
Task 4

Description:

Task 4 involves the understanding of the universal gate – NAND Gate, where the output is HIGH (1) only if either both inputs are LOW (0) or just one input is HIGH (1).

Logic Circuit Diagram:





Truth Table (Experimental Results):

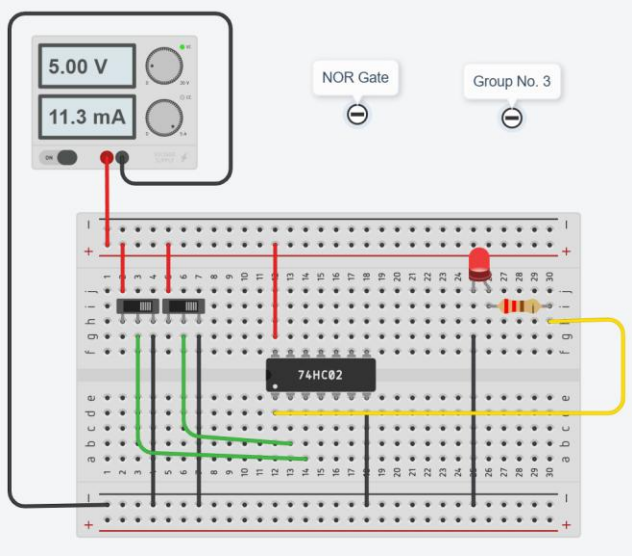
Input A	Input B	Expected Output	Experimental Output
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

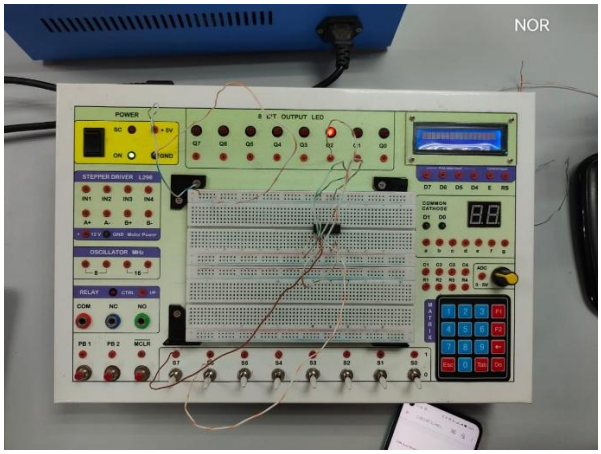
Task 5

Description:

Task 5 involves the understanding of the universal gate – NOR Gate, where the output is HIGH (1) only if both inputs are LOW (0).

Logic Circuit Diagram:





Truth Table (Experimental Results):

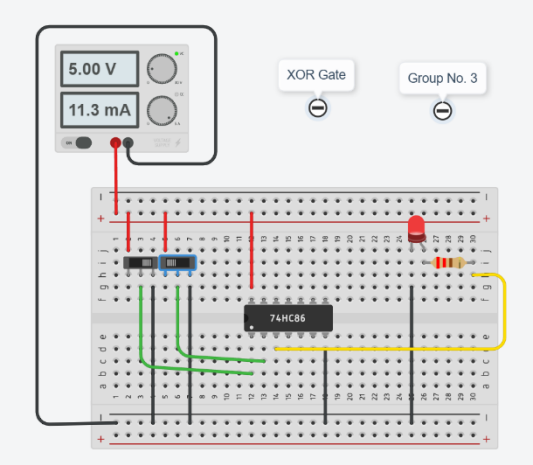
Input A	Input B	Expected Output	Experimental Output
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

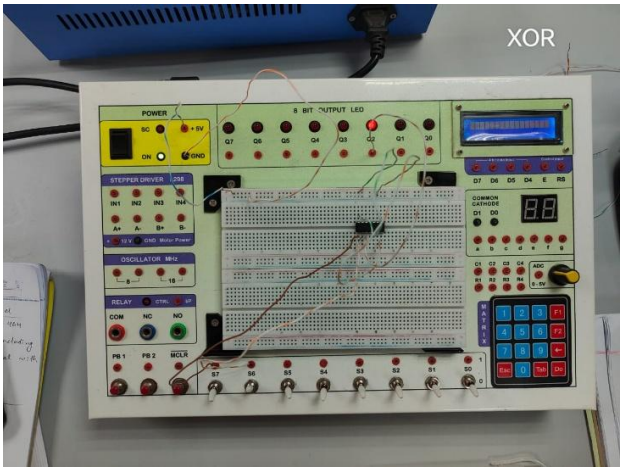
Task 6

Description:

Task 6 involves behavior of exclusive function of the XOR gate, where the output is HIGH (1) only if just one input is HIGH (1).

Logic Circuit Diagram:





Truth Table (Experimental Results):

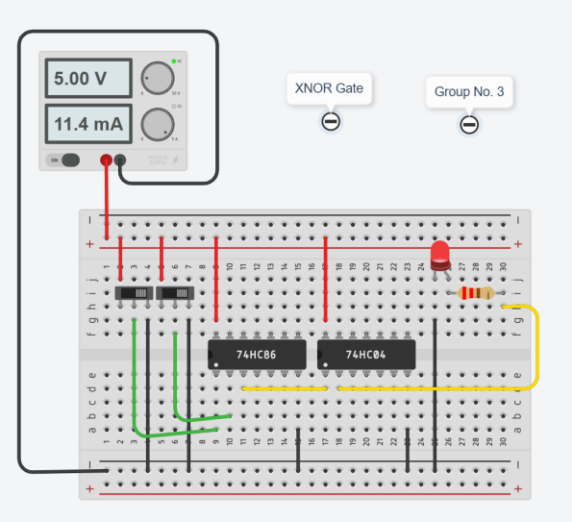
Input A	Input B	Expected Output	Experimental Output
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

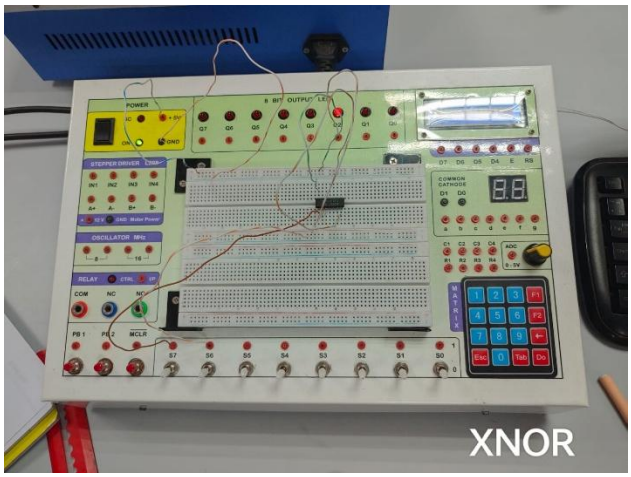
Task 7

Description:

Task 7 involves behavior of exclusive function of the XNOR gate, where the output is HIGH (1) only if both inputs are either LOW (0) or HIGH (1).

Logic Circuit Diagram:





Truth Table (Experimental Results):

Input A	Input B	Expected Output	Experimental Output
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1

Discussion

During the experiment, the expected results were compared with the actual outcomes, and most logic gates functioned as anticipated, producing outputs that matched their respective truth tables. However, some inconsistencies were caused by components, voltage fluctuations, and improper connections on the breadboard. Challenges included identifying malfunctioning components, troubleshooting unstable outputs, and verifying complex logic gates like NOR and XNOR. Despite minor variations, the experiment successfully demonstrated the fundamental operations of logic gates, reinforcing a deeper understanding of digital logic principles.