# Department of Computer Science and Engineering
# Experiment No-01

**Course Title : Digital Logic Design**
**Course Code : CSE345**
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**Date of Submission: 01/03/2025**

**Experiment Name:-**

Schematic and Structural Verilog Simulation of Combinational Logic Circuits

**Objectives:-**

- To Learn schematic simulation of combinational logic circuits using Quartas II software
- To learn structural Verilog simulation of combinational logic circuits using Quartas II software

**Schematic Diagram:-**

The Schematic diagram represents the combinational logic circuit which described in the following Figure-01

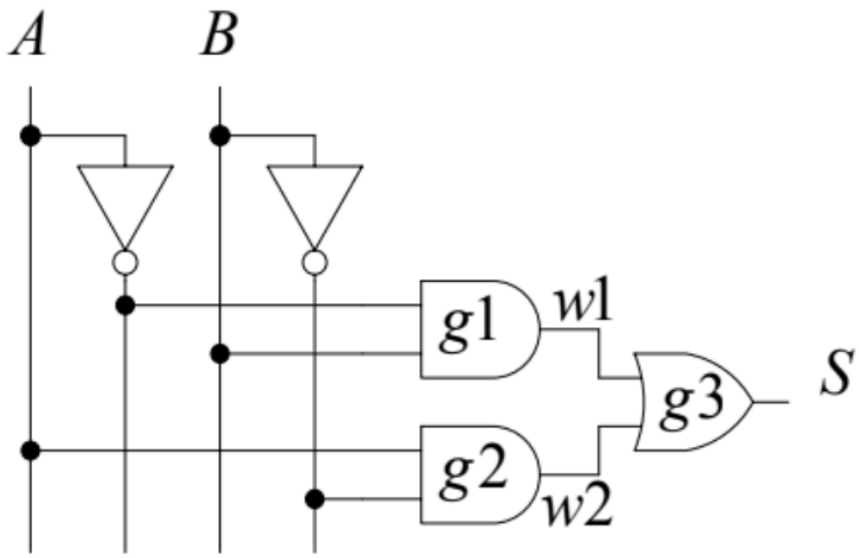


Figure-01: Combinational Circuit

The design includes the following components:
• AND gates to compute partial products of the Boolean equation.
• OR gate to combine the outputs of the AND gates.
• NOT gates for input inversion.

The design was created in Quartas II software. The design of the given circuit in Quartas II software-

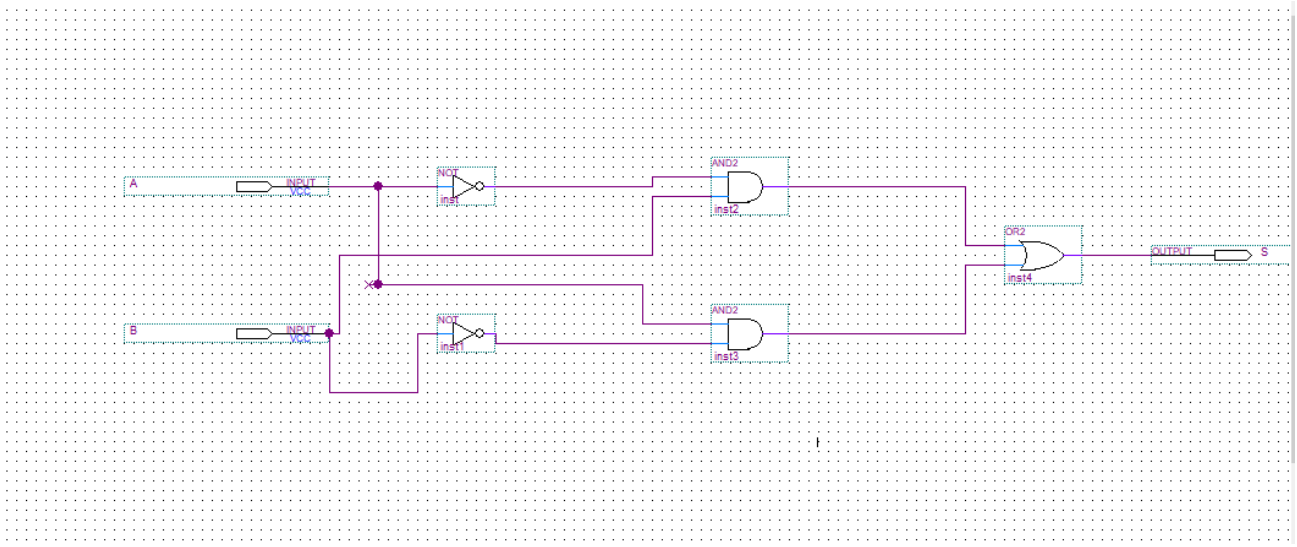


Figure-02: Combinational Circuit Design in Quartas II app.

**Result:-**

The simulation verified the functionality of the combinational logic circuit.The Output S
was consists with the following truth table.

| A | B | S |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The boolean expression of the following truth table is
$S = A'B + AB'$.

Both schematic and Verilog simulations matched these expected results, validating the design.

**Response:-**

The simulation response was accurate. Both input signals A and B demonstrated the expected behavior when passed through the gates, producing the correct output S. The waveform of the simulation confirmed consistency with the truth table and Boolean equation, proving the circuit's functionality.

The simulation waveform of this combinational circuit is given below:

**Input:**

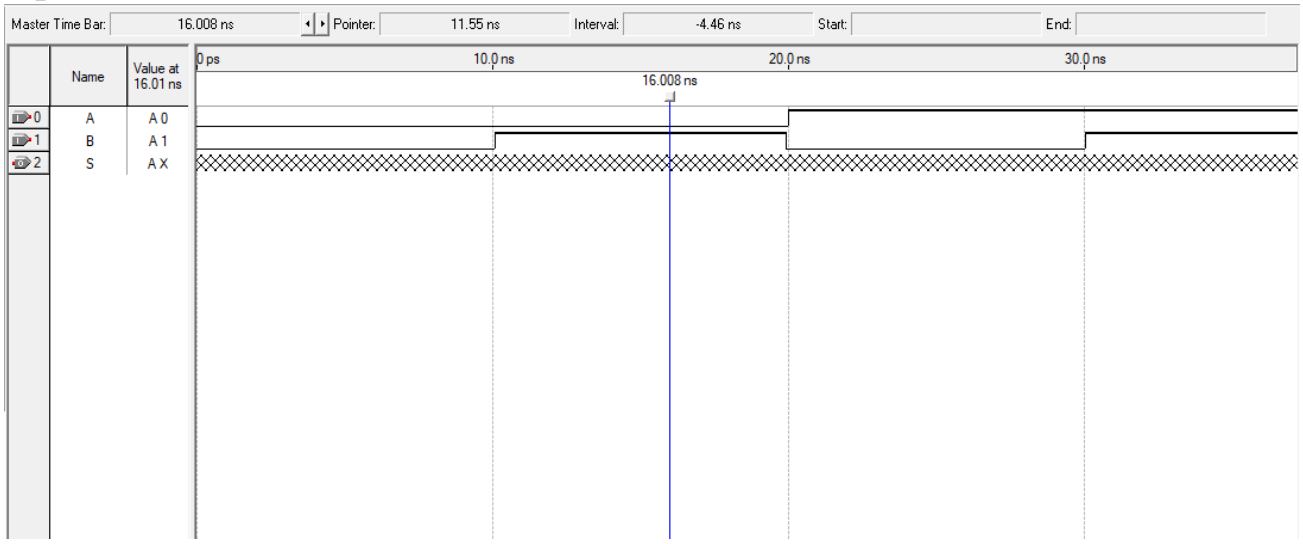


Figure-03: Giving input in the simulation.

**Output:**

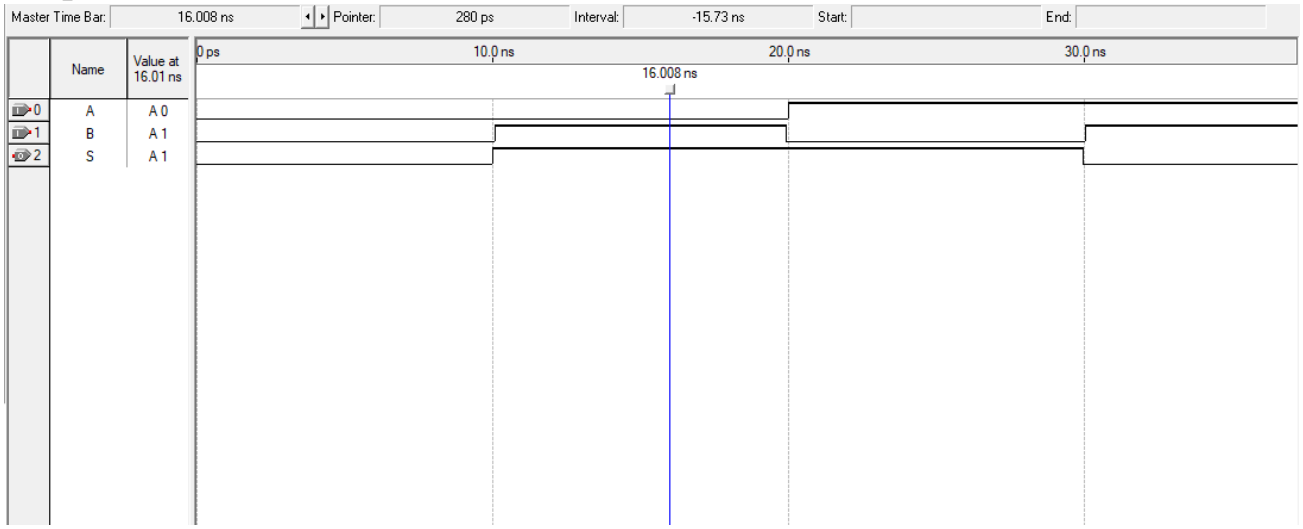


Figure-04: Output of the simulation.

**Verilog Code:-**

We also used Verilog code in Quartas II software for simulating the given circuit. Here is the Verilog code-

```
1  module exptl_2(input A, B,
2                 output S);
3
4          wire w1, w2;
5          and g1(w1,~A,B),
6              g2(w2,A,~B);
7          or  g3(S,w1,w2);
8  endmodule
```

Figure-05:Verilog Code.

It also worked on the simulation.

**Discussion:-**

This lab experiment aimed to provide practical experience in designing and simulating combinational logic circuits using schematic in Quartus II. The procedure involved:
1. Constructing the schematic circuit using basic logic gates.
2. Verifying the results of both methods against the truth table and Boolean equation.
3. Verifying verilog code for simulating the circuit.
The experiment successfully demonstrated the equivalence of schematic approaches for digital circuit simulation, enhancing understanding of logic design principles.

## Discussion

- Explain observations and compare expected vs. actual results.
- Discuss possible reasons for discrepancies.
- Mention any difficulties faced and how they were overcome.