Lab Report No 2

Digital Logic Design

Submitted By:

Abdul Ahad

22-CS-071

Muhammad Afzal

22-CS-035

Muhammad Zain Ali

22-CS-015

Faisal Khan

22-CS-039

Bilal Asghar

22-CS-107

Submitted to:

Engr. Bushra Fiaz

Dated:
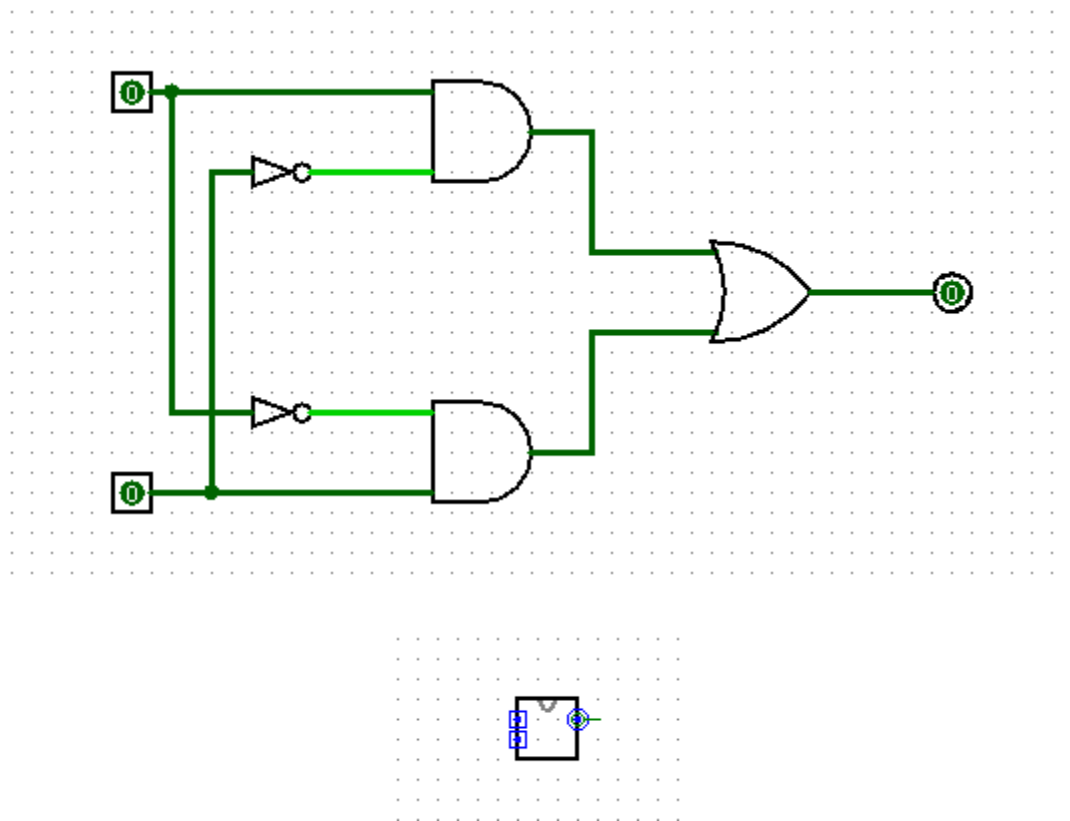
Week 01

Department of Computer Science,

HITEC University, Taxila

Solution:

Brief description (3-5 lines)
Build the circuit od the XOR gate and present it as an IC

The code

The results (Screenshot)

a	b	x
0	0	0
0	1	1
1	0	1
1	1	0

Solution:

Brief description (3-5 lines)
Build AND Gate and Verify its truth table.
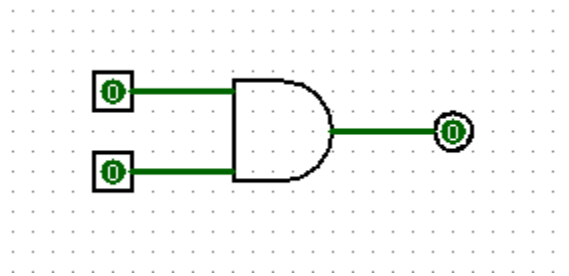
The code

The results (Screenshot)

A	B	Oputpu
0	0	0
0	1	0
1	0	0
1	1	1

Solution:

Brief description (3-5 lines)
Build NAND Gate and Verify its truth table.
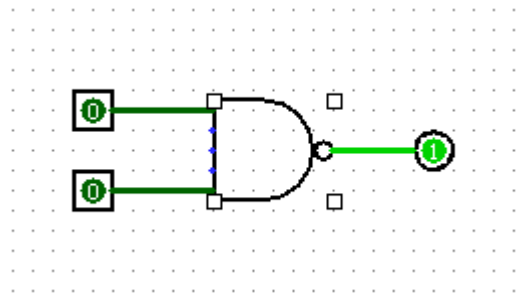
The code

The results (Screenshot)

A	B	Oputpu
0	0	1
0	1	1
1	0	1
1	1	0

Solution:

Brief description (3-5 lines)
Build NOR Gate and Verify its truth table.
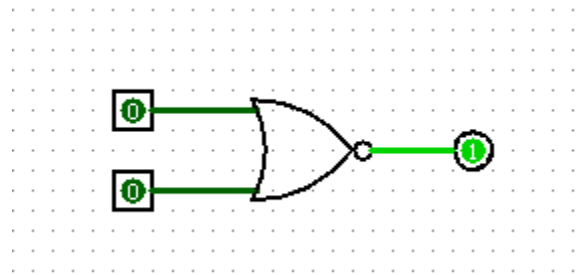
The code

The results (Screenshot)

A	B	Oputpu
0	0	1
0	1	0
1	0	0
1	1	0

Solution:

Brief description (3-5 lines)
Build NOT Gate and Verify its truth table.
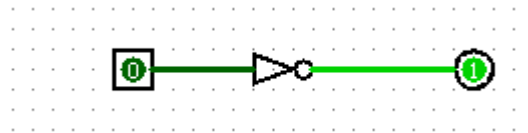
The code

The results (Screenshot)

A	B	Oputpu
0	0	1
0	1	0
1	0	0
1	1	0

Solution:

Brief description (3-5 lines)
Build OR Gate and Verify its truth table.
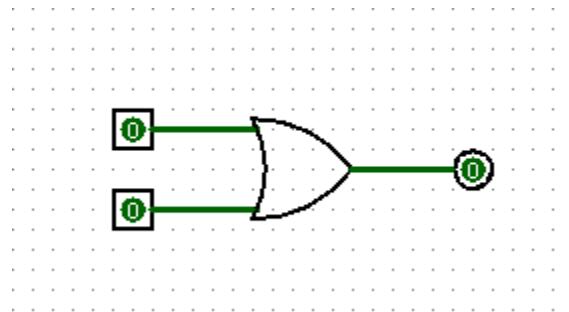
The code

The results (Screenshot)

A	B	Oputpu
0	0	0
0	1	1
1	0	1
1	1	1

Solution:

Brief description (3-5 lines)
Build XOR Gate and Verify its truth table.

The code

The results (Screenshot)

A	B	Oputpu
0	0	0
0	1	1
1	0	1
1	1	0