Lab Report No 6

Digital Logic Design

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Submitted to:

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Dated:

Week 01

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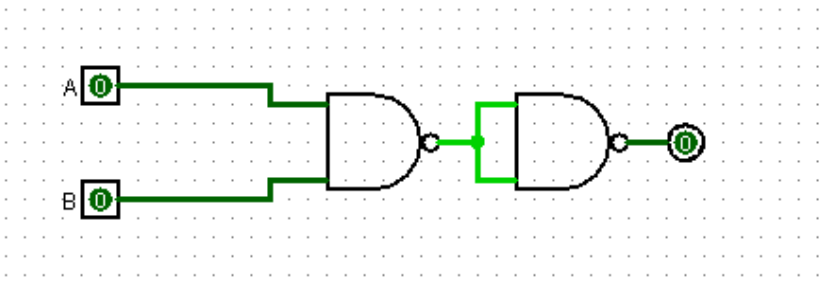
AND Gate from NAND Gate:

The code

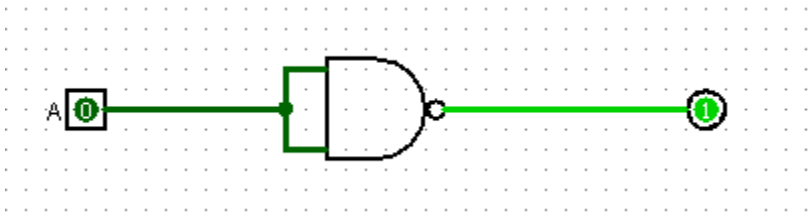


The results (Screenshot)

A	B	x
0	0	0
0	1	0
1	0	0
1	1	1

NOT Gate from NAND Gate:

The code

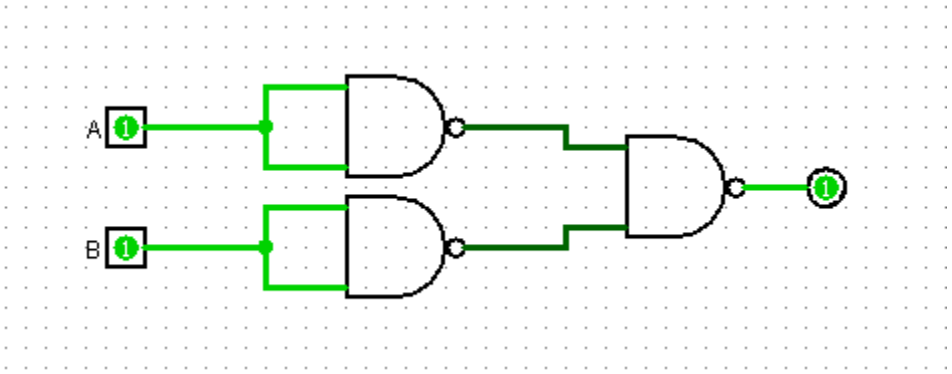


The results (Screenshot)

A	x
0	1
1	0

OR Gate from NAND Gate:

The code

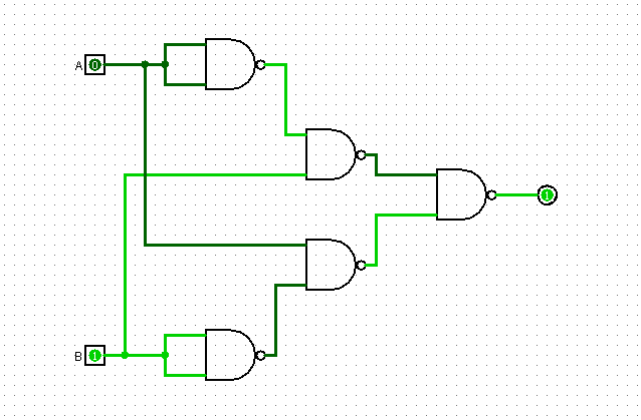


The results (Screenshot)

A	B	x
0	0	0
0	1	1
1	0	1
1	1	1

XOR Gate from NAND Gate:

The code

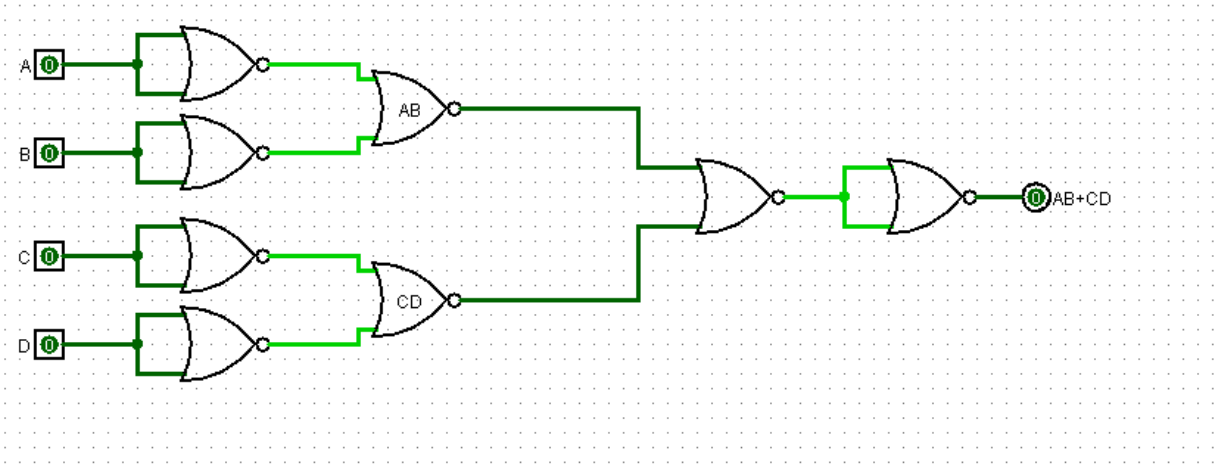


The results (Screenshot)

A	B	x
0	0	0
0	1	1
1	0	1
1	1	0

Boolean expression AB + CD using NOR gate only :

The code



The results (Screenshot)

A	B	C	D	ABorCD
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1