Lab Report No 7

Digital Logic Design

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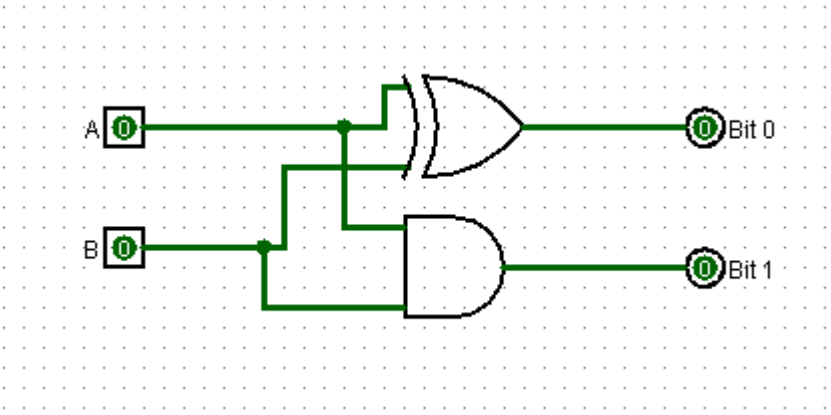
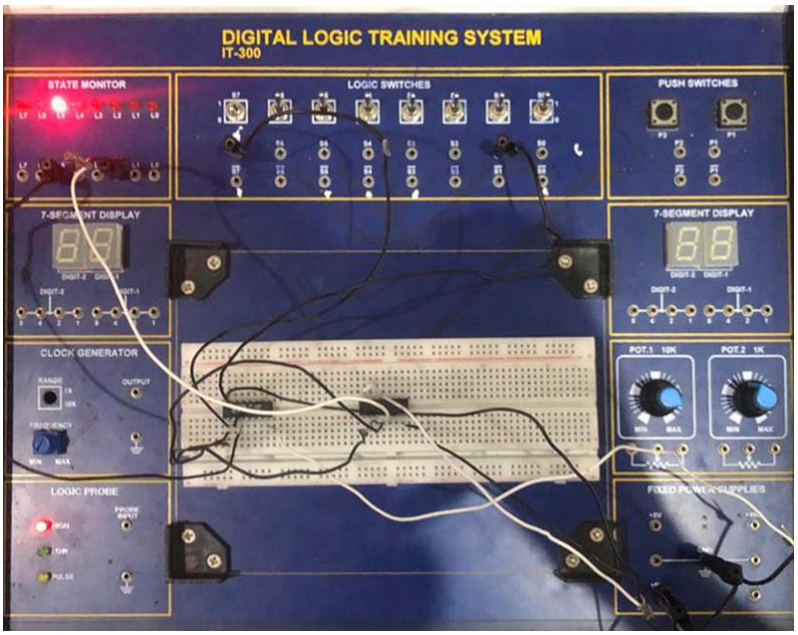
Half Adder:

Solution:

Brief description
Implement and verify the Half Adder Boolean expression by basic logic gates on trainer board and simulate the circuit with Logisim.
The code
Half Adder is combinational logic circuit that generates the sum of two binary numbers (each having 1-bit length). The logic circuit has two inputs and two outputs
The results (Screenshot)



A	B	x	y
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

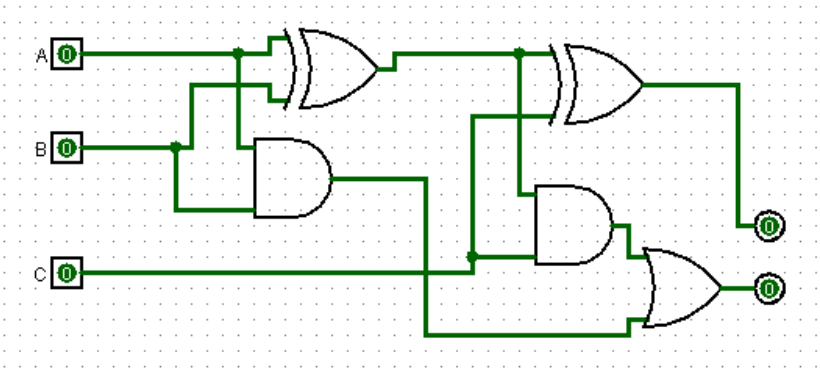


A	B	x	y
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

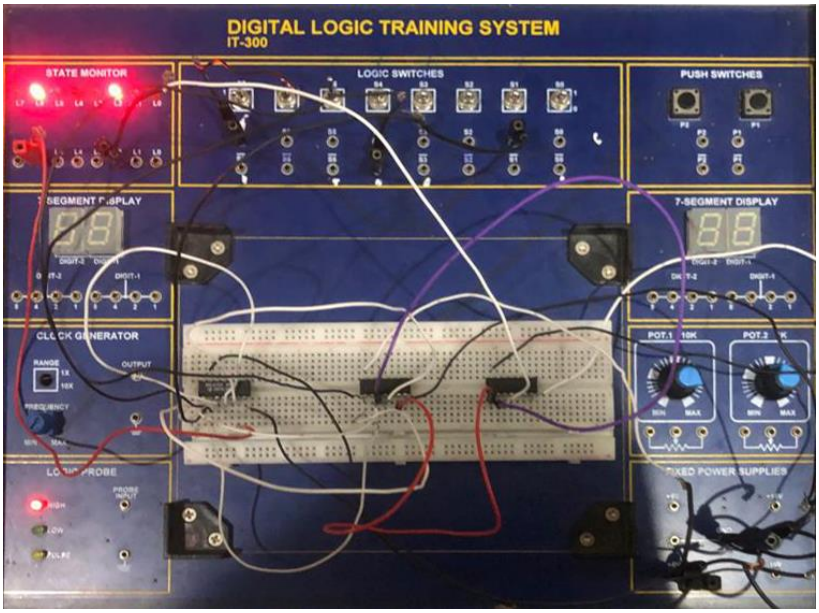
Full Adder:

Solution:

Brief description
Implement and verify the Full Adder Boolean expression by basic logic gates on trainer board and simulate the circuit with Logisim.
The code
Full Adder is combination logic circuit that performs the sum of 3 input binary numbers, (each having 1-bit length). Two of the binary input variables are x and y represent the two significant bits to be added the third input z, represents the carry from previous lower significant position.
The results (Screenshot)



A	B	C	x	y
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



A	B	C	x	y
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1