TFE4152 Exercise 2

Drain current of NMOS transistor:

$\mu_n C_{ox} = 92\,\mu A/V^2$

$\frac{W}{L} = \frac{20\,\mu m}{2\,\mu m}$, $V_{Tn} = 0,8V$, $\lambda = 95,3 \cdot 10^{-3} V^{-1}$

a) $V_{GS} = 1,2\,V$ $V_{DS} = 0,2\,V$

V_{tn}: threshold voltage (terskel spenning)

$V_{GS} > V_{tn} \Rightarrow 1,2V > 0,8V$ ✓

$V_{DS} \leq V_{eff} \Rightarrow 0,2V \leq 0,4V$ ✓

$[(V_{eff} = V_{GS} - V_{tn}) = 1,2 - 0,8 = 0,4\,V]$

$\Rightarrow$ triode region:

$$I_D = \mu_n C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$I_D = 92\frac{\mu A}{V^2} \cdot 10 \left[(0,4V) \cdot 0,2V - \frac{0,04V^2}{2}\right]$$

$$I_D = 55,2\,mA$$

b) $V_{GS} = 1,2V$ $V_{DS} = 0,6V$

$V_{GS} > V_{tn} \Rightarrow 1,2V > 0,8V$ ✓

$V_{DS} \leq V_{eff} \Rightarrow 0,6 \leq 0,4$ ✗

$V_{DS} \geq V_{eff} \Rightarrow 0,6V \geq 0,4V$ ✓

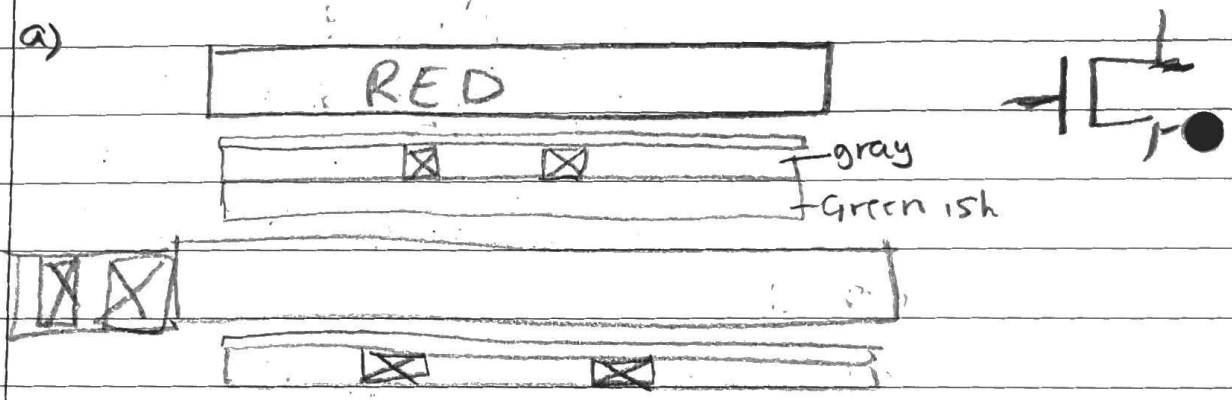
$\Rightarrow$ Active Region

[1] b) $I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2 [1 + \lambda(V_{DS} - V_{tH})]$

$I_D = \frac{1}{2} 92 \frac{mA}{V^2} \cdot 10(0,16) \cdot [1 + 95,3 \cdot 10^{-5} V^{-1}(0,2)]$

$I_D = 15\ mA$ in Aktive Region

[2] a)

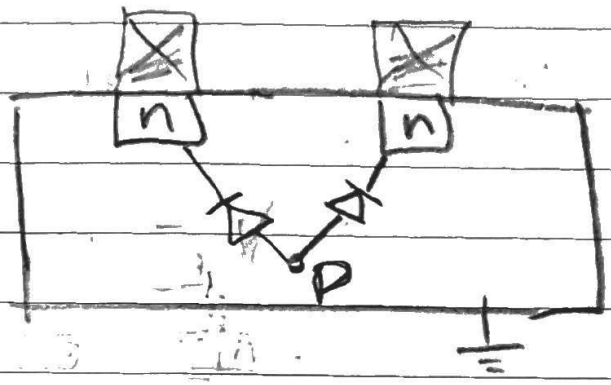


* Red: is gate
* Gray: Doped material. the gray area is when n^+ or P^+ are plus the channel. also n^+ n^+ or P^+ P^+ The doped metal/material.
* ⊠ is the metal or cantact mask
* Blue/greenish are is the active region mask.

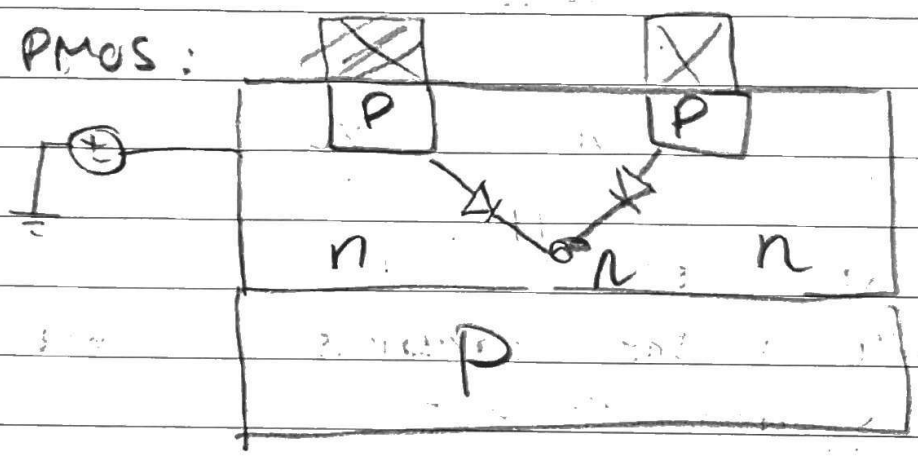
[2] b) This is a PMOS transister :

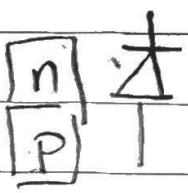
N-well is PMOS
P-well is NMOS.

NMOS :

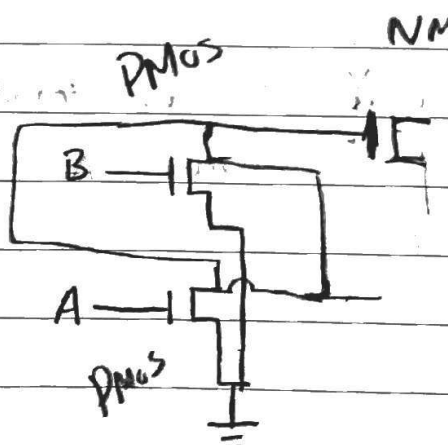


PMOS :

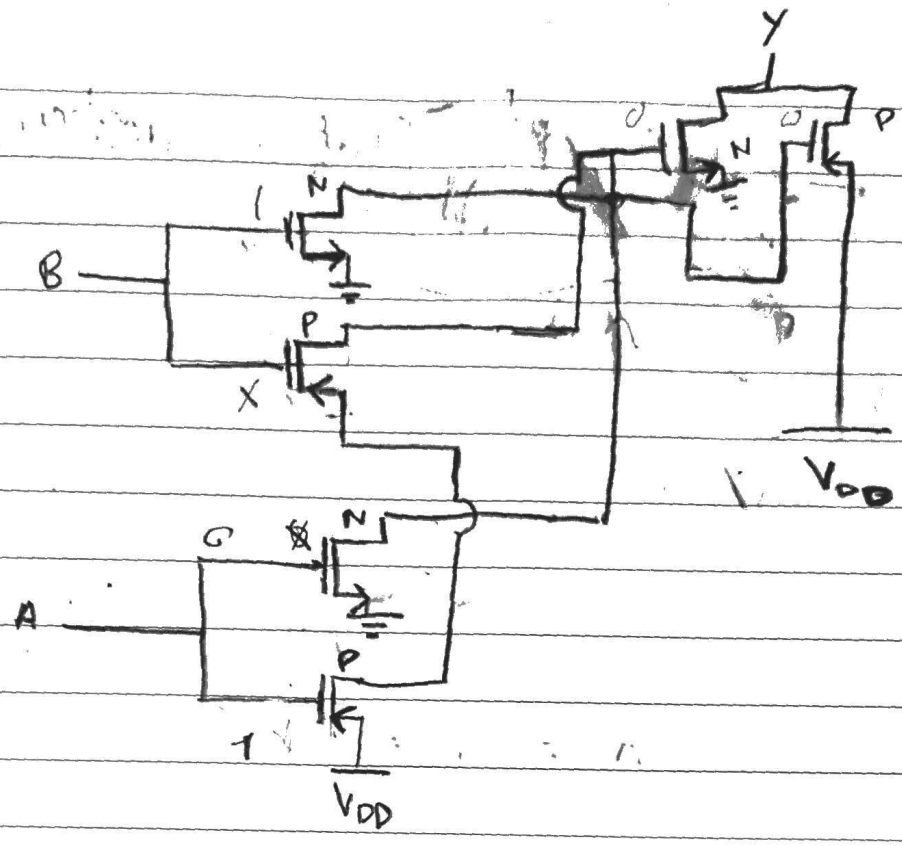




c)



c)



1 PMOS = ikke ledende

1 NMOS = ledende

A	B	Y
1	1	1
0	0	0
1	0	1
0	1	1

this is an OR-GATE

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(4) 1) From the plot we get the relation between:

gm / Vdd (y-aksis) plot 1

rds/ Vdd (y-aksis) plot 2

id / Vdd (y-aksis) plot 3

plot 1: We get a liner graph to Vdd ≈ 0.4V and then it looks more constant. This means that the current will only be linear increased to a certain point wher it will be constant.

From the plot we get the relationship:

Plot 4: rds/vgs

Plot 5: id/vgs

Plot 6: gm/vgs

Plot 4: we see that the Impedance rds is so large. that there is no current or voltage from gate. It act like a isolator.

plot 5: thre we see that that as soon as the rds decreases the current start to flow throu the transistor and it grows expenentially.

Plot 6: the gm start increasing as rds decreases. It increases linearly but then it get more constant. this is because of the current. gm or how much voltage we get per current.

3

$$\sigma^2(\Delta P) = \frac{(A_p)^2}{WL} + (S_{p\cdot})^2 D^2$$

$$S_D = \sqrt{\sigma^2} \Rightarrow \sqrt{\frac{(A_p)^2}{WL_{new}}} = 0,25 \sqrt{\frac{(A_p)^2}{WL}}$$

$$\frac{A_p^2}{WL_{new}} = 0,25^2 \frac{A_p^2}{WL}$$

$$WL_{new} = \frac{WL}{0,25^2} = \frac{WL}{(1/4)^2} = 16\,WL$$

We can see that we have make WL 16 times larger