EXCERCISE 4

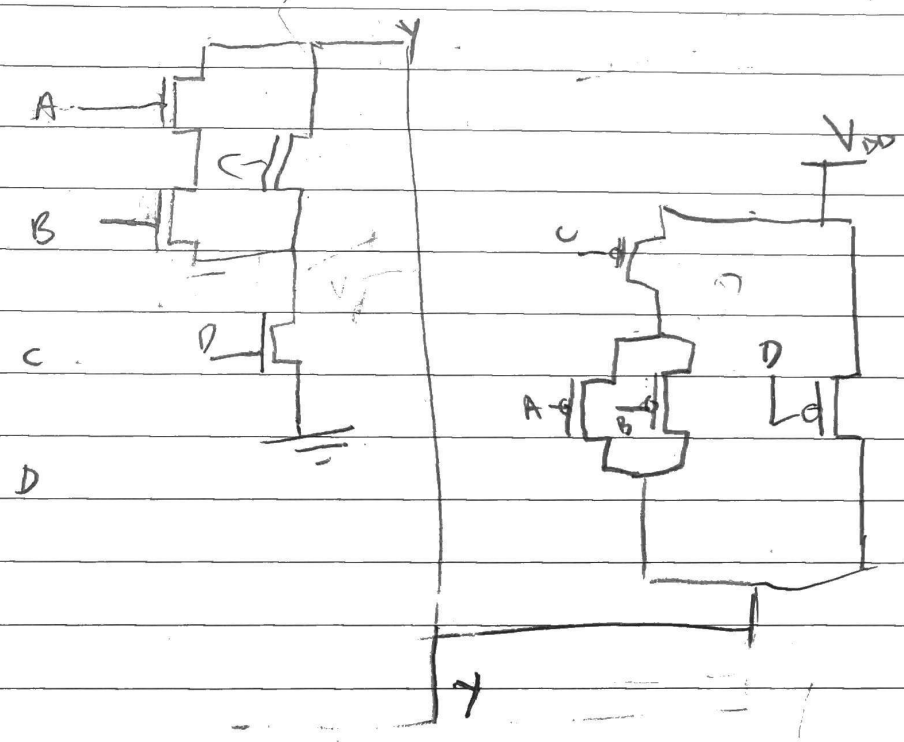
inverter

A+B (OR) => transistors in parallell } Nmos
A·B (AND) => transistors in series }

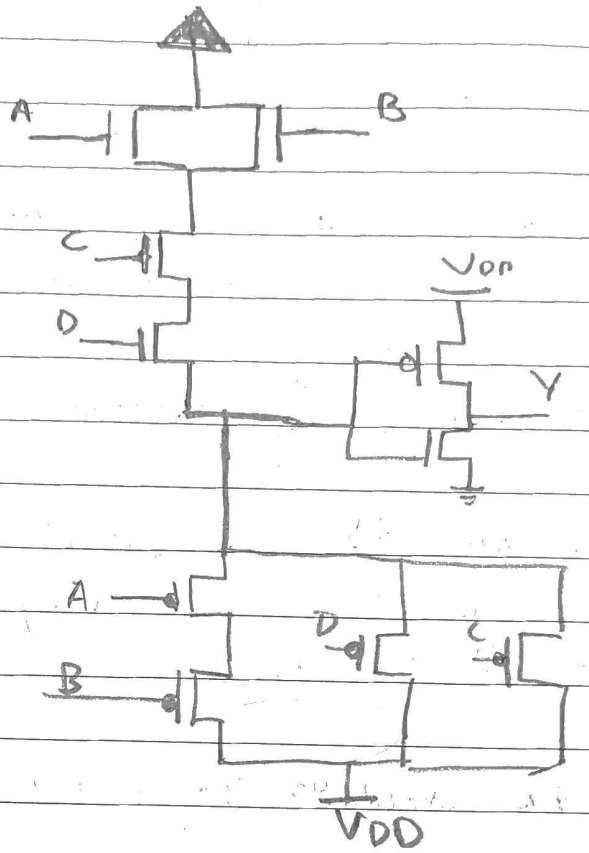
like inverter

$\overline{A+B}$ => transistors in series } Nmos
$\overline{A \cdot B}$ => transistor in parallell }

$$Y = \left[(AB + C) D \right]'$$

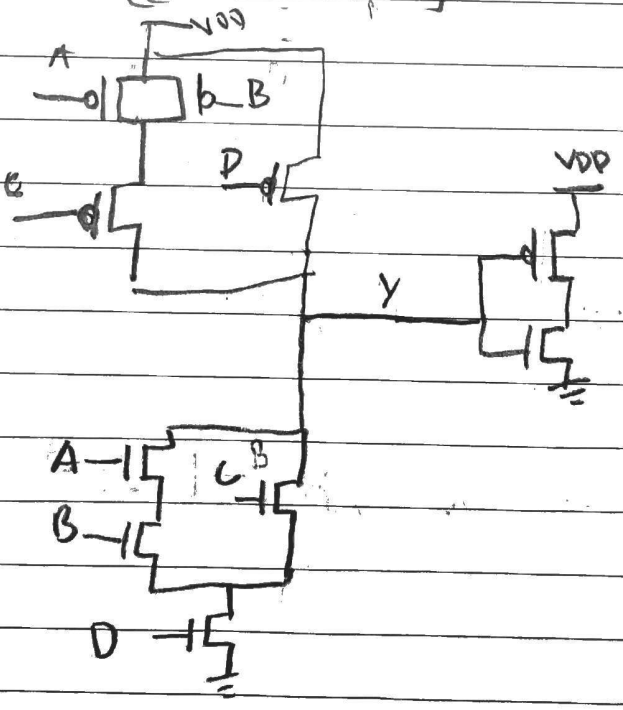


b) $Y = (A+B)CD$



A B C D	Y
0 0 0 0	0
1 1 1 1	1

c) $Y = \overline{[(A+B)C+D]}$



2 a)

$$\left(\frac{W}{L}\right)_{nmos} \left(\frac{\rho_n}{\rho_p}\right) = \left(\frac{W}{L}\right)_{pmos}$$

We assume that L is the same for Nmos and pMos transister.

$$W_{nmos} \cdot X = W_{pMos}$$

this means that Width of the Pmos has to be x-times bigger than Width of the Nmos

From the definition of a symmetric inverter we need $|V_{tp}| = V_{tn}$ and $\frac{B_p}{B_n} = 1$

$$\frac{B_p}{B_n} = \frac{\mu_p C_{ox} \frac{W_p}{L_p}}{\mu_n C_{ox} \frac{W_n}{L_n}} = 1$$

$$\frac{B_p}{B_n} = \frac{\frac{W_n}{L_n}}{\frac{W_p}{L_p}} \Rightarrow \frac{\mu_p}{\mu_n} \frac{C_{ox}}{C_{ox}}$$

$$\frac{B_p}{B_n} = \frac{W_n}{L_n} = \frac{W_p}{L_p} \cdot \frac{\mu_p}{\mu_n} \frac{C_{ox}}{C_{ox}}$$

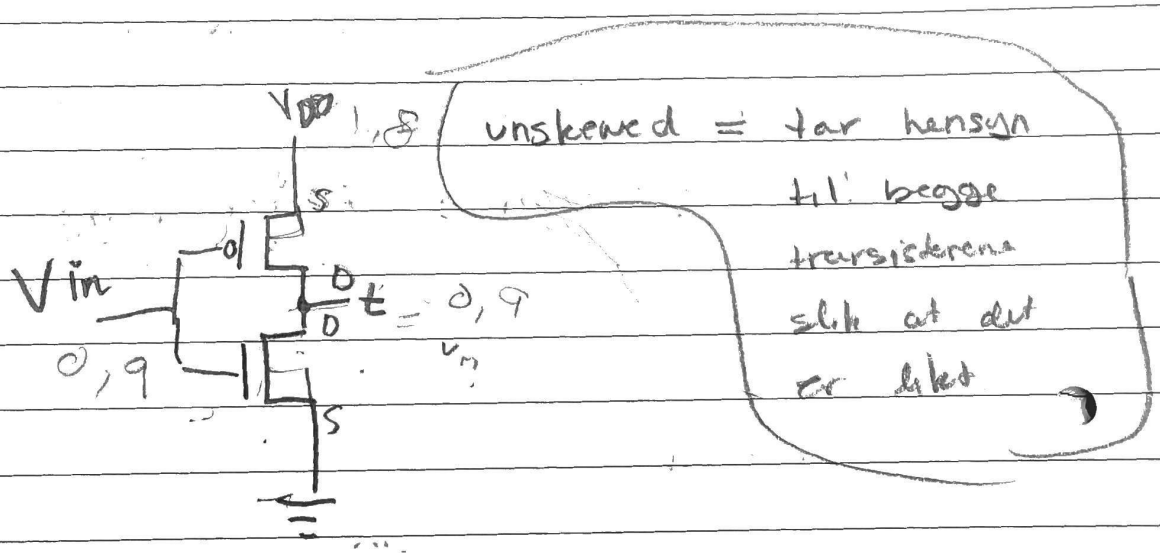
a) $\frac{W_n}{L_n} \cdot \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = \frac{W_p}{L_p}$

$\frac{W_n}{L_n} \cdot k = \frac{W_p}{L_p}$, $L_n = L_p$

$W_n \cdot k = W_p$

$k = \frac{\mu_n C_{ox}}{\mu_p C_{ox}} = \frac{270\ nm}{76\ nm} = 3,8571$

b)



unskewed = tar hensyn til begge transistorene slik at det er likt

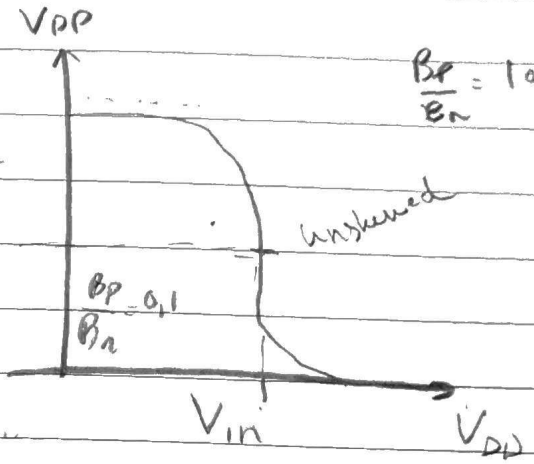
$\frac{W_p}{L_p} = 5$, $L_p = 0,18\mu m$

$W_p = 5 \cdot 0,18\mu m = 0,9\mu m$

b) Midpoint V_m:

$$V_m = \frac{V_{DD} - |V_{tp}| + \sqrt{\frac{B_n}{B_p}} V_{tn}}{\left(\sqrt{\frac{B_n}{B_p}} + 1\right)}$$

$$V_m = \frac{V_{DD}}{2}$$



K = 3,57 in Aimspice using OP

c) using Xdown function in Aimspice we get that the period is:

$$T = \frac{4,678 \cdot 10^{-10}}{100} = 4,678 \cdot 10^{-12}$$

$$F = \frac{1}{T} = \frac{1}{4,678 \cdot 10^{-12}} = 213,7\,GHz$$

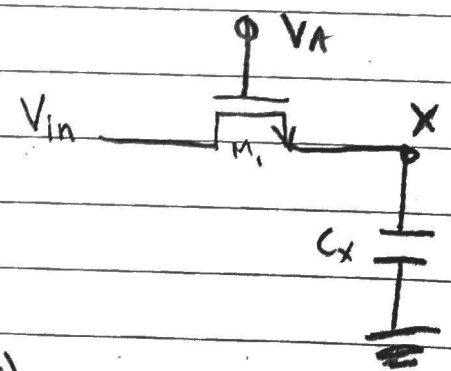
d) Varying $\left(\frac{W}{L}\right)$ means varying the area of the transistor, Hence bigger area means more resistance which means it takes long time for the capacitor to charge up. V_{OD} affects the r_{out} resistance which means it affects the current running trough it which means higher frequency when V_{OD} decreases.

$n = 100$

e)

	n_0	$fT = \left(\frac{I}{n}\right)$	f
tt	100	$4,4,65 \cdot 10^{-12}$ s	215 GHz
ss	100	$5,99 \cdot 10^{-11}$ s	16,7 GHz
ff	100	$3,758\ 10^{-12}$ s	266,09 GHz

3



$V_A = V_{dd} = 1,8\,V$

$C_x = 12\,fF$

$M_1 \Rightarrow L = 0,18\,\mu m \quad W = 0,5\,\mu m$

a)

$V_x = V_{in} - V_{th}$, $V_{in} = 0,9 V_{dd}$

$V_x = 0,9 V_{dd} - V_{th}$

[3] b) if we want the capacitor to charge up quickly. | We can change the dimension of the transistor. Small area means small resistance => quicker charging over the capacitor. If we want to decrese the time for the charge of capacitor, we can make the width and the length of the transister larger => slower chargin over the capacitor.