ECED 3403 – Computer Architecture

Quiz 2

24 July 2024

The following quiz is closed book and notes. Internet-connected computing devices may not be used. You may use notes written or printed on both sides of a letter-sized paper (8.5” by 11” or 21.59 cm by 27.94 cm). Calculators are permitted. Answers are to be written directly on the quiz. State any assumptions made. Time allotted for quiz is 60 minutes. The mark associated with each question is written in parenthesis beside the question number.

The quiz has five questions on four pages (two sheets).

1. (2) Some machines have their stack inside the CPU. Give one example of an advantage of this design and one example of a shortcoming.

2. (2) An ISA has four index registers. Instructions using an index register represent the register using two bits, with the MSBit stored in bit 2 and the LSBit stored in bit 5. If you were to design an emulator for this ISA, how would you determine which register is being accessed in an instruction? (That is, the register number, 0 through 3.)

3. (2) XM23 uses a 10-bit encoded offset for branching instructions, for example:

   ```
   SELF    BR    SELF
   ```

   What is the value of the 10-bit encoded offset if the address of SELF is #1FEC?

4. (2) Conditional branches sometimes bubble, whereas unconditional branches always bubble. When do conditional branches bubble? Why?

5. (2) The following XM23 code fragment accesses a well-known type of data structure (you may assume that subroutine `PRINT_R1_R2` exists):

```
WHILE
    CMP   #0,R0
    BEQ   ENDWHILE
    LDR   R0,#0,R1
    LDR   R0,#2,R2
    BL    PRINT_R1_R2
    LDR   R0,#4,R0
    BRA   WHILE
ENDWHILE
```

Please answer the following questions:

a) (0.5) What is the name of this type of data structure?
b) (0.5) How do you know this?
c) (1) How many words does the data structure occupy and how many elements does it contain?