

CS311 Project 4: Cache Design for MIPS Architecture

Due 11:59pm, December 22nd

1. Purpose

This project is intended to help you understand the principle of caching by implementing a data cache.

2. Overview

The main part of this project is to add a data cache to the five stage pipeline implemented for the project 3. The cache should be configurable to adjust capacity, associativity, and block size with command-line options. You must support extra options to print out the content of the cache.

3. Cache Implementation

3.1 Adding Data Cache

In this project, you must add a data cache to the pipelined MIPS simulator. Assume the memory reads from IF, access the memory directly in a cycle in the same way as the project 3 model assumes. You only need to add a data cache. We do not support self-modifying code, so stores cannot update instructions. The write policy of the cache must be *write-allocate* and *write-back*. The replacement policy must be the perfect LRU.

If an access is a cache hit, it takes a cycle to finish the MEM stage. If an access is a cache miss, it takes 30 cycles to finish the MEM stage. While the miss is handled, the pipeline must be stalled. During the 30 cycle period, the missed block is moved from the memory to the cache, and the access is completed.

Hit : IF-DE-EX-MEM-WB

Miss: IF-DE-EX-MEM1- ... -MEM30-WB

3.2 Cache Parameters

The capacity, associativity, and block size of the cache must be configurable. The parameters are specified with “-c” option: -c <capacity>:<assoc>:<blocksize>

Configurable parameters:

- Capacity: 4B (one word) - 8KB
- Associativity: 1 – 16 way
- Block size: 4B – 32B .

When you specify both capacity and block size, you should specify the number with byte granularity and power of two.

Ex) Capacity 4KB, Associativity 4way, Block size 32B → **4096:4:32**

4. Simulator Option

```
cs311sim [-nobp] [-f] [-m addr1:addr2] [-c cap:assoc:bsize] [-d] [-p]
[-x] [-X] [-n num_instr] inputBinary
```

- -nobp : branch prediction is disabled. All conditional branches must add three-cycle bubbles.

- -f : Data forwarding support is on
- -m : dump the memory content at the end of simulation
- -d : print the register file content, and the current PC at every cycle
- -p : print the PCs of instructions in each pipeline stage at every cycle
CYCLE N: x3004 | x3003 | x3002 | x3001 | x3000
- -c : cache configuration
- -x : dump the cache content only at the end of simulation
- -X: dump the cache content every cycle

The TAs will provide the skeleton code for displaying output format like lab3.

The example of output format are attached as below.

```
Cache Configuration:
-----
Capacity: 512B
Associativity: 4way
Block Size: 32B

Current Cache state:
-----
SET[0]:  WAY[0]  WORD[0]: 0x00000000 WORD[0]: 0x00000000 WORD[0]: 0x00000000 WORD[0]: 0x00000000
        WORD[1]: 0x00000000 WORD[1]: 0x00000000 WORD[1]: 0x00000000 WORD[1]: 0x00000000
        WORD[2]: 0x00000000 WORD[2]: 0x00000000 WORD[2]: 0x00000000 WORD[2]: 0x00000000
        WORD[3]: 0x00000000 WORD[3]: 0x00000000 WORD[3]: 0x00000000 WORD[3]: 0x00000000
        WORD[4]: 0x00000000 WORD[4]: 0x00000000 WORD[4]: 0x00000000 WORD[4]: 0x00000000
        WORD[5]: 0x00000000 WORD[5]: 0x00000000 WORD[5]: 0x00000000 WORD[5]: 0x00000000
        WORD[6]: 0x00000000 WORD[6]: 0x00000000 WORD[6]: 0x00000000 WORD[6]: 0x00000000
        WORD[7]: 0x00000000 WORD[7]: 0x00000000 WORD[7]: 0x00000000 WORD[7]: 0x00000000

SET[1]:  WORD[0]: 0x00000000 WORD[0]: 0x00000000 WORD[0]: 0x00000000 WORD[0]: 0x00000000
        WORD[1]: 0x00000000 WORD[1]: 0x00000000 WORD[1]: 0x00000000 WORD[1]: 0x00000000
        WORD[2]: 0x00000000 WORD[2]: 0x00000000 WORD[2]: 0x00000000 WORD[2]: 0x00000000
        WORD[3]: 0x00000000 WORD[3]: 0x00000000 WORD[3]: 0x00000000 WORD[3]: 0x00000000
        WORD[4]: 0x00000000 WORD[4]: 0x00000000 WORD[4]: 0x00000000 WORD[4]: 0x00000000
        WORD[5]: 0x00000000 WORD[5]: 0x00000000 WORD[5]: 0x00000000 WORD[5]: 0x00000000
        WORD[6]: 0x00000000 WORD[6]: 0x00000000 WORD[6]: 0x00000000 WORD[6]: 0x00000000
        WORD[7]: 0x00000000 WORD[7]: 0x00000000 WORD[7]: 0x00000000 WORD[7]: 0x00000000

SET[2]:  WORD[0]: 0x00000000 WORD[0]: 0x00000000 WORD[0]: 0x00000000 WORD[0]: 0x00000000
        WORD[1]: 0x00000000 WORD[1]: 0x00000000 WORD[1]: 0x00000000 WORD[1]: 0x00000000
        WORD[2]: 0x00000000 WORD[2]: 0x00000000 WORD[2]: 0x00000000 WORD[2]: 0x00000000
        WORD[3]: 0x00000000 WORD[3]: 0x00000000 WORD[3]: 0x00000000 WORD[3]: 0x00000000
        WORD[4]: 0x00000000 WORD[4]: 0x00000000 WORD[4]: 0x00000000 WORD[4]: 0x00000000
        WORD[5]: 0x00000000 WORD[5]: 0x00000000 WORD[5]: 0x00000000 WORD[5]: 0x00000000
        WORD[6]: 0x00000000 WORD[6]: 0x00000000 WORD[6]: 0x00000000 WORD[6]: 0x00000000
        WORD[7]: 0x00000000 WORD[7]: 0x00000000 WORD[7]: 0x00000000 WORD[7]: 0x00000000

SET[3]:  WORD[0]: 0x00000000 WORD[0]: 0x00000000 WORD[0]: 0x00000000 WORD[0]: 0x00000000
        WORD[1]: 0x00000000 WORD[1]: 0x00000000 WORD[1]: 0x00000000 WORD[1]: 0x00000000
        WORD[2]: 0x00000000 WORD[2]: 0x00000000 WORD[2]: 0x00000000 WORD[2]: 0x00000000
        WORD[3]: 0x00000000 WORD[3]: 0x00000000 WORD[3]: 0x00000000 WORD[3]: 0x00000000
        WORD[4]: 0x00000000 WORD[4]: 0x00000000 WORD[4]: 0x00000000 WORD[4]: 0x00000000
        WORD[5]: 0x00000000 WORD[5]: 0x00000000 WORD[5]: 0x00000000 WORD[5]: 0x00000000
        WORD[6]: 0x00000000 WORD[6]: 0x00000000 WORD[6]: 0x00000000 WORD[6]: 0x00000000
        WORD[7]: 0x00000000 WORD[7]: 0x00000000 WORD[7]: 0x00000000 WORD[7]: 0x00000000
```

Figure 1 Cache Configuration & Initial Cache state

5. Hand in

You should submit the compressed file of the source files through tar or zip program.

Please make the compressed file name with your team name. (team_name.tar or team_name.zip)

Ex) If you are team14, you should make the compressed file with “team14.tar” or “team14.zip”

Please send the email to cs311_ta@calab.kaist.ac.kr with attaching the compressed file until the due date.