RISC V ARCH TEST
TASK 3

Task Description : Handle illegal instruction exception in supervisor mode rather than in mode
As all exception by default handle in m mode

Sol : For handling the exception in supervisor mode mdeleg csr's 4th bit should be set and stvec set with address of supervisor exception handler.

Note: if exception occur while Hart is in m mode it will not delegated So switch to supervisor mode and cause illegal instruction

```
    li a0,0
    jal ra ,function
   // C.add a0, a6
   .word 0x8542
    li t1,1
```

c.add cause illegal exception and will handle in supervisor handler :

spike log:

```
core   0: >>>>  $d
core   0: 0x80000050 (0x00008542) c.mv    a0, a6
core   0: exception trap_illegal_instruction, epc 0x80000050
core   0:           tval 0x00008542
core   0: >>>>  supervisor_trap_handler
core   0: 0x800000cc (0x143022f3) csrr    t0, stval
core   0: 1 0x800000cc (0x143022f3) x5  0x00008542
core   0: 0x800000d0 (0x00008337) lui     t1, 0x8
core   0: 1 0x800000d0 (0x00008337) x6  0x00008000
core   0: 0x800000d4 (0x54230313) addi    t1, t1, 1346
core   0: 1 0x800000d4 (0x54230313) x6  0x00008542
core   0: 0x800000d8 (0x00530c63) beq     t1, t0, pc + 24
core   0: 1 0x800000d8 (0x00530c63)
core   0: 0x800000f0 (0x00a484b3) add     s1, s1, a0
core   0: 1 0x800000f0 (0x00a484b3) x9  0x00000000
core   0: 0x800000f4 (0x00100513) li      a0, 1
core   0: 1 0x800000f4 (0x00100513) x10 0x00000001
core   0: 0x800000f8 (0x14102373) csrr    t1, sepc
core   0: 1 0x800000f8 (0x14102373) x6  0x80000050
core   0: 0x800000fc (0x00430313) addi    t1, t1, 4
core   0: 1 0x800000fc (0x00430313) x6  0x80000054
core   0: 0x80000100 (0x14131073) csrw    sepc, t1
core   0: 1 0x80000100 (0x14131073) c321_sepc 0x80000054
core   0: 0x80000104 (0x10200073) sret
core   0: 1 0x80000104 (0x10200073) c768_mstatus 0x000000a0
core   0: >>>>  $x
core   0: 0x80000054 (0x00100313) li      t1, 1
```

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Time stamp: 4 hours 1 mint