Vector multiplier based on Vedic Multiplication Algorithm

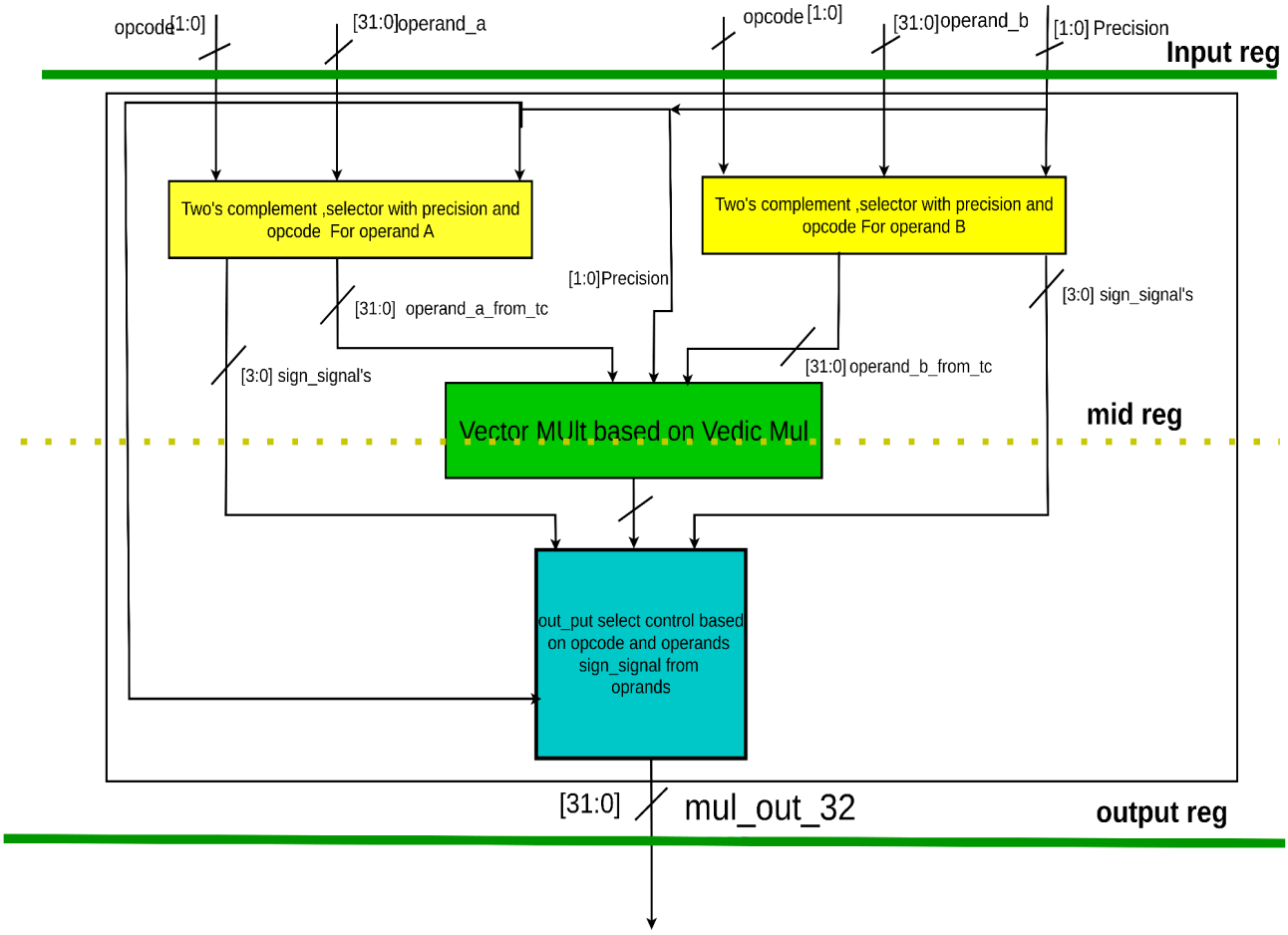
Author : Abdullah Jhatial Associate Engineer at 10x Engineers
Tech lead : Ahmed Shahid Senior Engineer at 10x Engineers

Subject : The purpose of this IP doc is to understand how it works at a higher abstraction level . so v_mult IP can be integrated into systems

Introduction : This Vector multiplier IP supports **MUL , MULH , MULHU,MULHSU** instructions.and supported precisions are **BYTE, HALF WORD,WORD**. It is three stages pipelined. A 2GHz frequency was observed at the synthesis stage.

Terminology : 2'C , tc :: Two's complement , r_: remaining

Higher level abstraction



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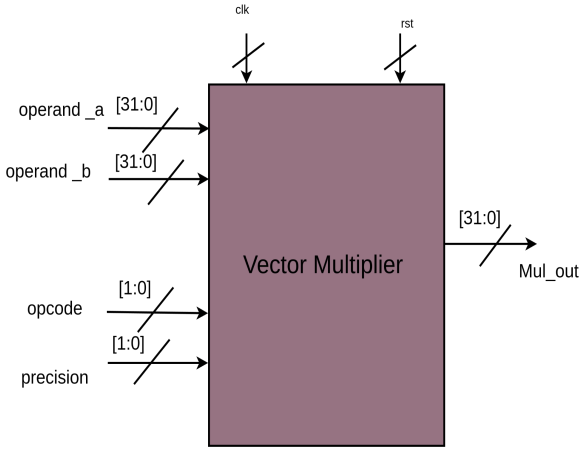

Top module interface signals: v_mult_su

Signal	Width	Description
operand_a	32 bit	Operand_a is a 32-bit vector. Its element sizes interpret on precision signal
operand_b	32 bit	Operand_a is a 32 bit vector. Its element sizes interpret on precision signal
precision	2 bit	precision signal define element size in vector, Supported precisions are 4 byte size elements (00) 2 half word size element (01) Word size element (10)
opcode	2 bit	opcode signal used for type of operation Supported operation are MUL,MULH,MULHU,MULHSU, (00,01,10,11)
Mul_out	32 bit	Mul_out is operation's result as precision and opcode signal are driven

3_Cycles : at first pos edge clk input reg load operands and opcode and precision , at 2nd pos edge mid reg in multiplier load with intermediate signals and at 3rd posedg output reg loads the result of multiplication

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Git hub repo :

RTL:

Operands tow's complement

tc_selcet_8_16.sv // // parametrized N-WIDTH

tc_bit_stream_with_precision.sv

operand_tc_contorl.sv

v_mul_u:

two_bit_multiplier.sv

multiplier_4bit.sv

multiplier_8bit.sv

multiplier_16bit.sv

multiplier_32bit.sv

adder_RTL:

prefix_adder.sv // kogge_stone parameterized up N-WIDTH

carry_save_adder.sv

carry_select_adder.sv // Using BEC

half_adder.sv

full_adder.sv // using majority circuit

output_control:

v_mul_su_output_control.sv

v_mul_su_top_module:

v_mul_su.sv // top module

Synthesis:

tcl_scripts:

tcl_run.tcl

tcl_arg.arg

Verif:

Self_checking:

tcl_verif.tcl

tcl_arg.arg

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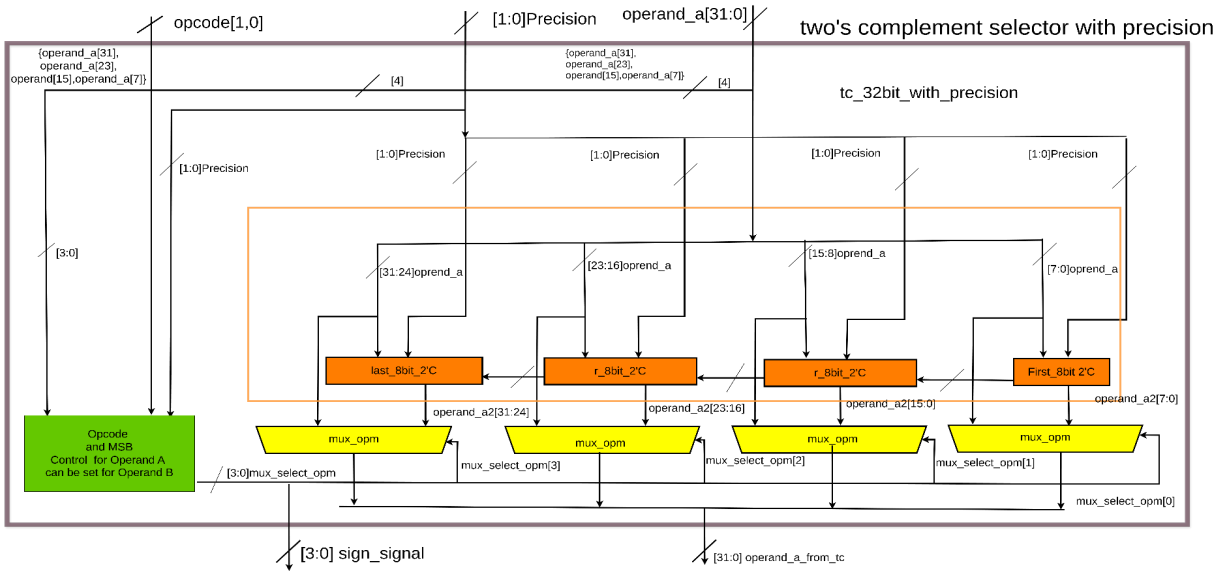
Operands Tow's Complement control

First_8bit_tc : First_8bit_tc, is responsible for computing the two's complement of the first 8 bits of the operand. This block is parameterized in NWidth, Modified tow's complement circuit is used in parallel prefix calculation Architecture.

r_8bits_tc : r_8bits_tc, handles the two's complement for intermediate segments This block has dependencies on two critical signals: the previous carry propagate signal and precision signals. The carry propagate signal is essential because the result of the first 8-bit block can influence the carry into the next 8-bit segment.
The precision signals dictate how the operand is processed in terms of the operand size or precision.

last_8bit_tc : only difference between this and r_tc circuit is carry out signal.

control block : This control block generates the sign signals which are used as mux select. Whether we selects tow's complement of element or used as unsigned Sign signal dependence on the opcode ,precision and MSB's. These generated sign signals are also used in output control.



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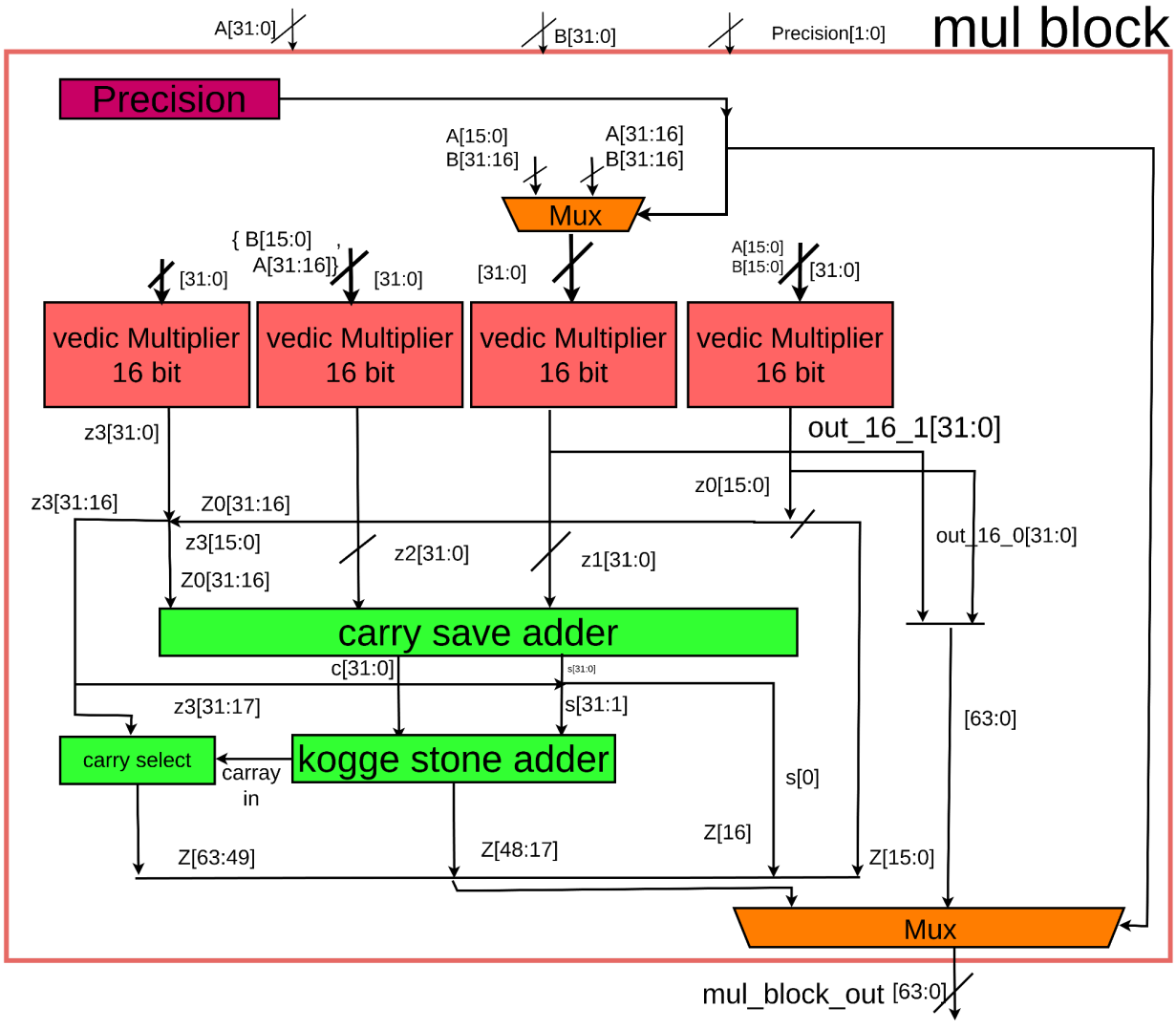
Vector Multiplier : This multiplier based on vedic multiplication for understanding vedic Multipliers refer to this Research paper Ref[1].
For vector support we have to control the input vector bit's pattern Which is controlled by precision signal for 32 bit multiplication. Second 16 bit multiplier got first 16 bits of operand A and last 16 bit of --operand B.For 16bit multiplication Second 16bit multiplier will get upper 16 bits of operand A and B .
this control also implemented in 16bit multiplier which is used for control 16bit Multiplication or 8bit multiplication . this implement only second placed 16bit multiplier.



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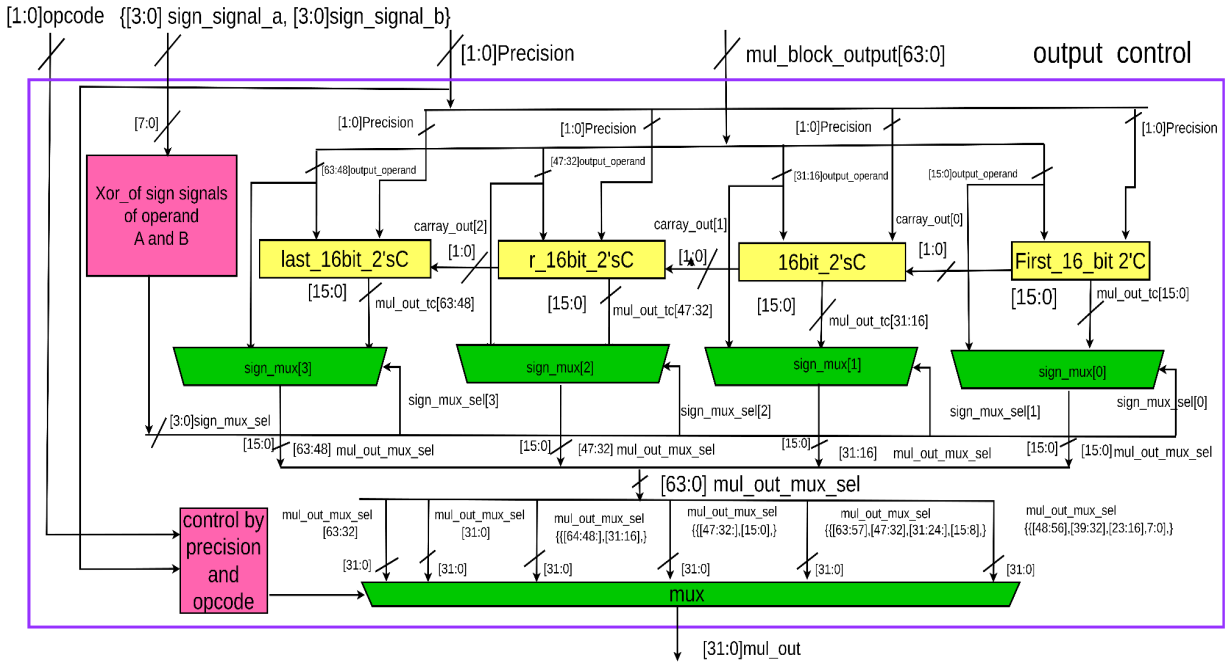
Output control : This control is designed for signed multiplication with opcode support For instruction sign_mux select whether taking tc of mul out or not . that depends on sign signals which are generated from Operand tow's complement block . mux is used for instruction's support with precision control



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Ref[1]: Ganjikunta, G. K., Khan, S. I., & Basha, M. M. (2019). A high-performance signed-unsigned multiplier using Vedic mathematics. *Journal of Low Power Electronics, 15*(5), 302-308. American Scientific Publishers.

Ref[2] : kogge stone adder

System_diagram: Vector Multiplier based on Vedic multiplication

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