

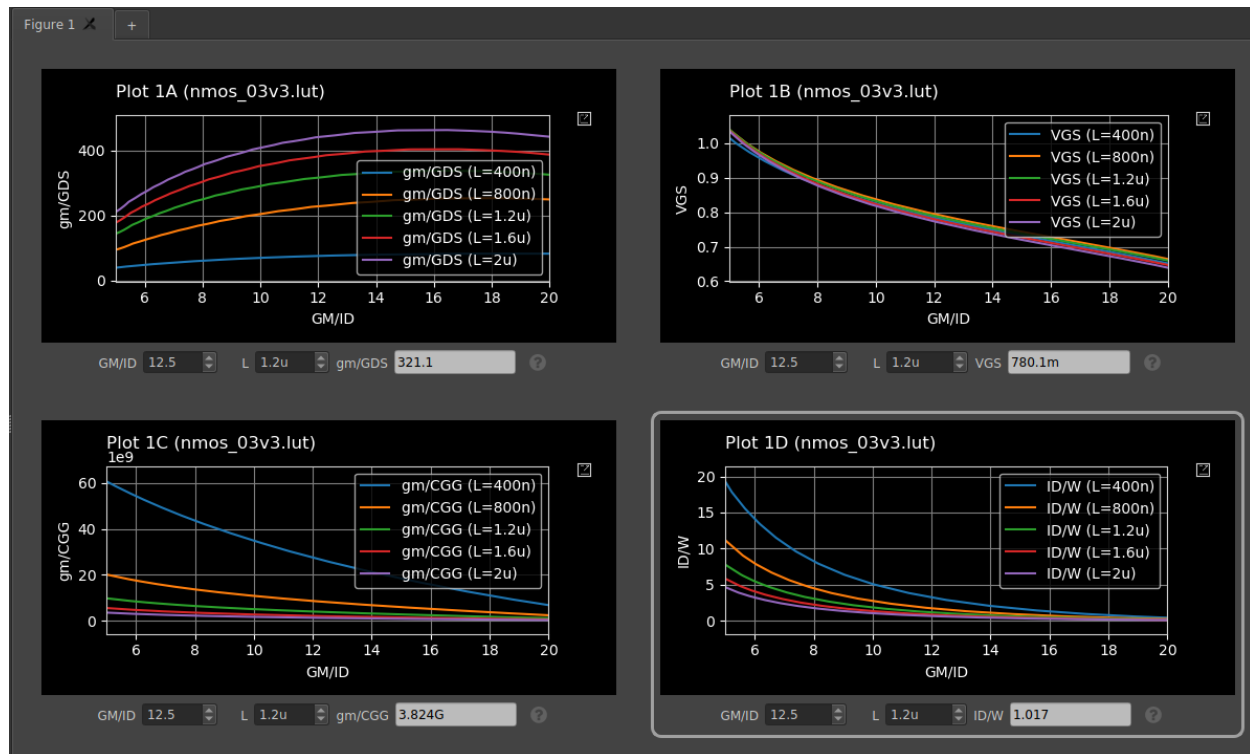
ITI  
LAB  
gm/ID Design Methodology

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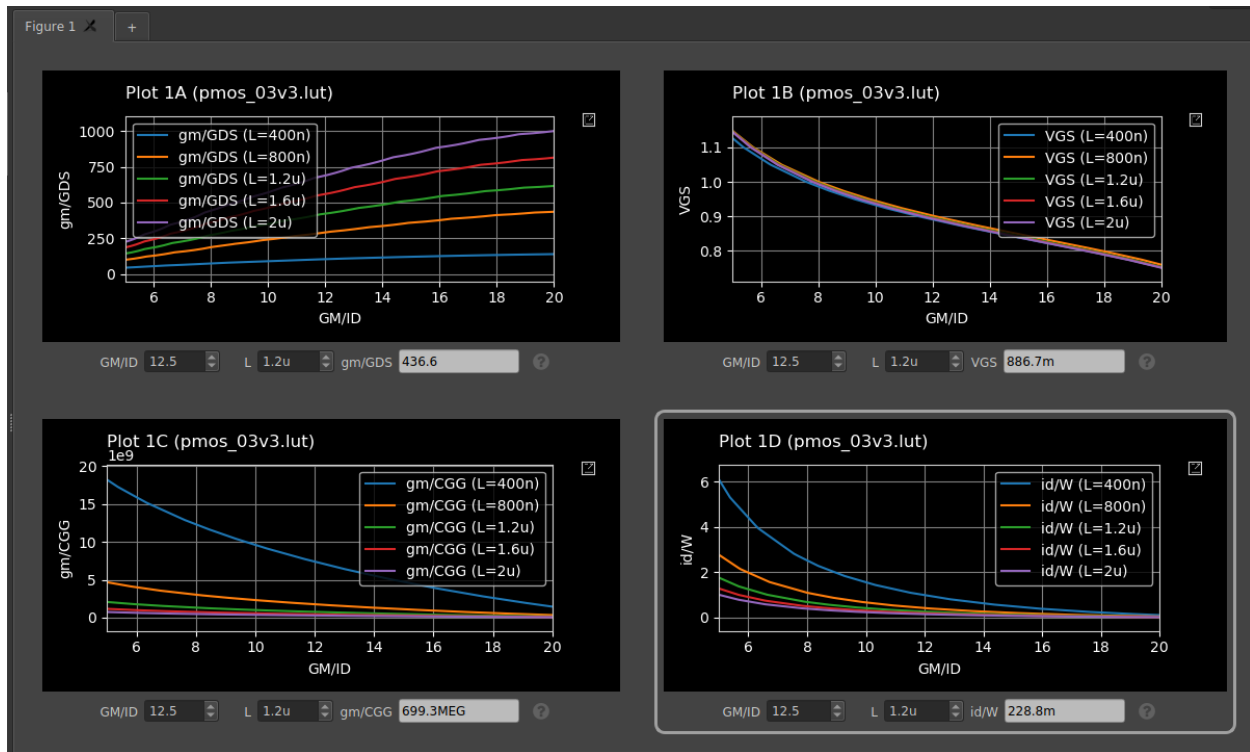
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# Part 1: gm/ID Design Charts

## NMOS



# PMOS



## Part 2: OTA Design

### Detailed hand analysis

$$GBW = \frac{g_m}{2\pi C_L}$$

And it was given that the GBW should be  $\geq 10MHz$ ,  $C_L = 5 pF$

$$g_m \leq 314 \mu S$$

And the current was given to be  $=10 \mu A$

Which means that  $\frac{g_m}{I_D} > 15.7$

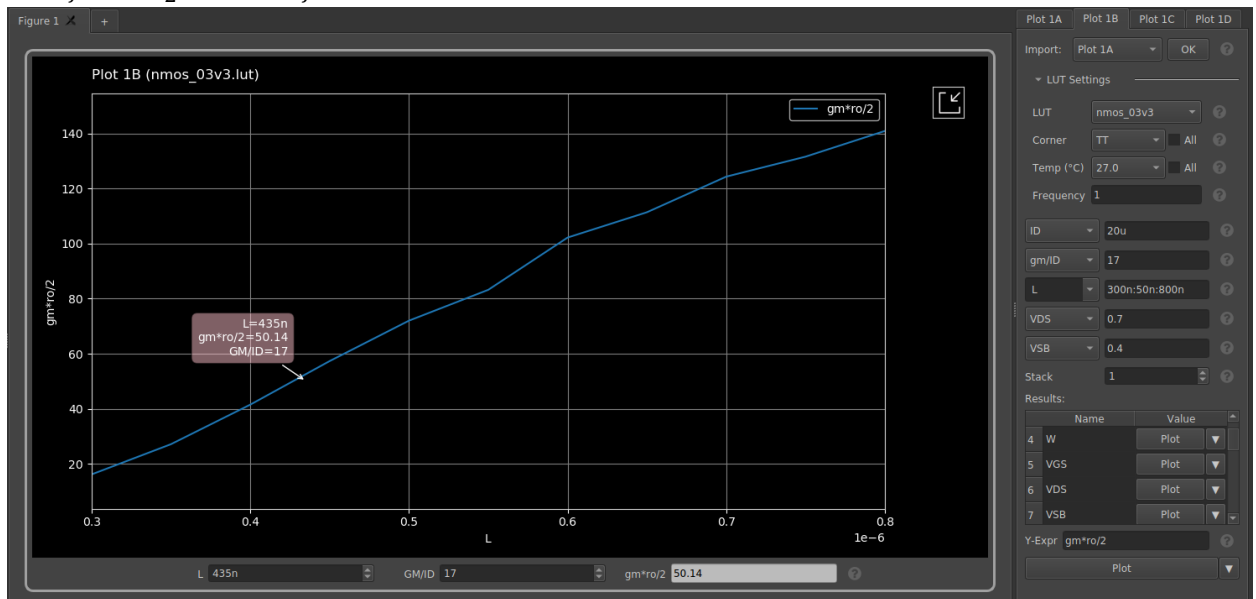
So we will use a reasonable number of  $\frac{g_m}{I_D}$  that will ensure meeting of the specifications

$$\frac{g_m}{I_D} = 17$$

We will be using  $V_{DS} = 0.7 V$  for all transistors except the transistors of the tail current which we will be using  $V_{DS} = 0.4 V$

- Input pair

$$A_{V_{Dif}} = \frac{g_m N r_{oN}}{2}, A_{V_{Dif}} \geq 50$$



Now we will use the value of L to find the value of W



$$W_{input\ pair} = 22.51\mu m, L_{input\ pair} = 435nm$$

5	VGS	828.3m
6	VDS	700m
7	VSB	400m

- Active load

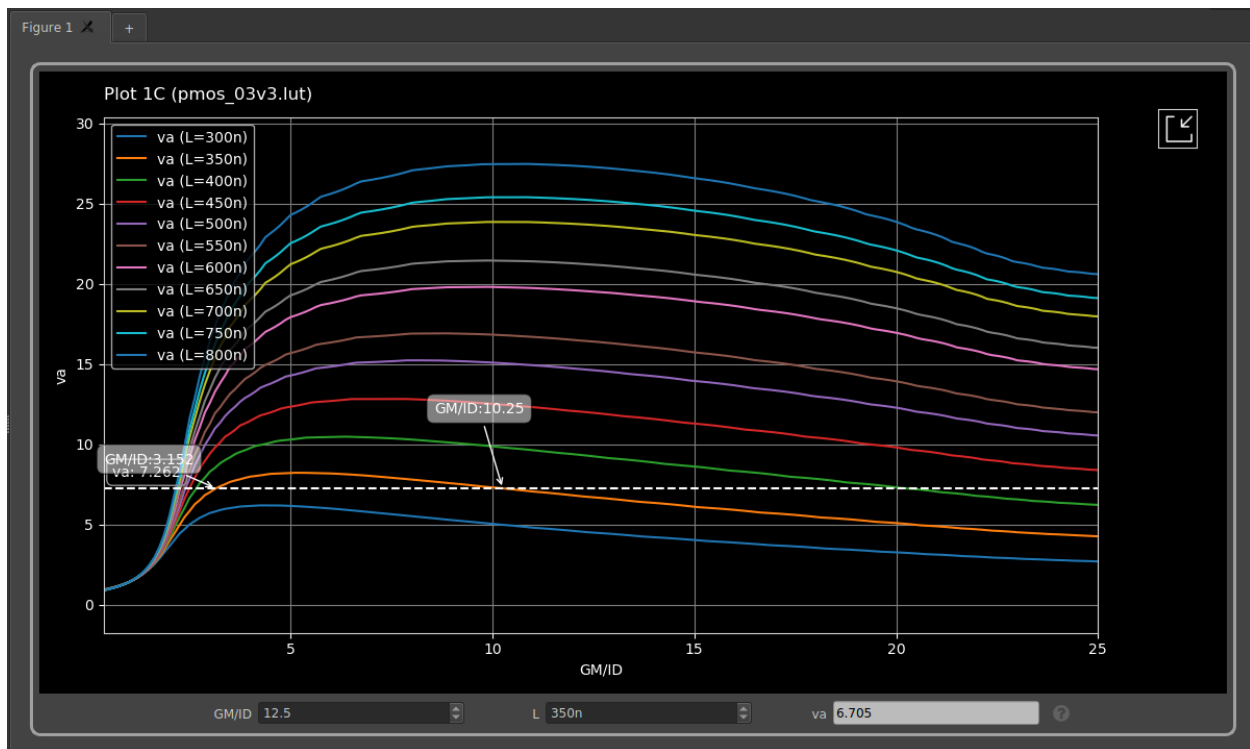
$$r_o = \frac{V_A}{I_D}, \text{ assuming that } r_{oN} = r_{oP}$$

$$A_{V_{Dif}} \geq 50, g_{mN} = 314 \mu S, A_{V_{Dif}} = \frac{g_{mN}}{2} \times r_o$$

$$r_o = 2 \times \frac{50}{g_{mN}},$$

$$\frac{V_A}{I_D} \geq 2 \times \frac{50}{g_{mN}}, V_A \geq \frac{2 \times 50 \times I_D}{g_{mN}}$$

$$V_A \geq 6,368$$



Now we will use the value of L to find the value of W

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1A OK ?

▼ LUT Settings

LUT pmos\_03v3 ?

Corner TT All ?

Temp (°C) 27.0 All ?

Frequency 1 ?

ID 20u ?

gm/ID 10 ?

L 350n ?

VDS 0.7 ?

VSB 0 ?

Stack 1 ?

Results:

	Name	TT-27.0
1	ID	20u
2	IG	N/A
3	L	350n

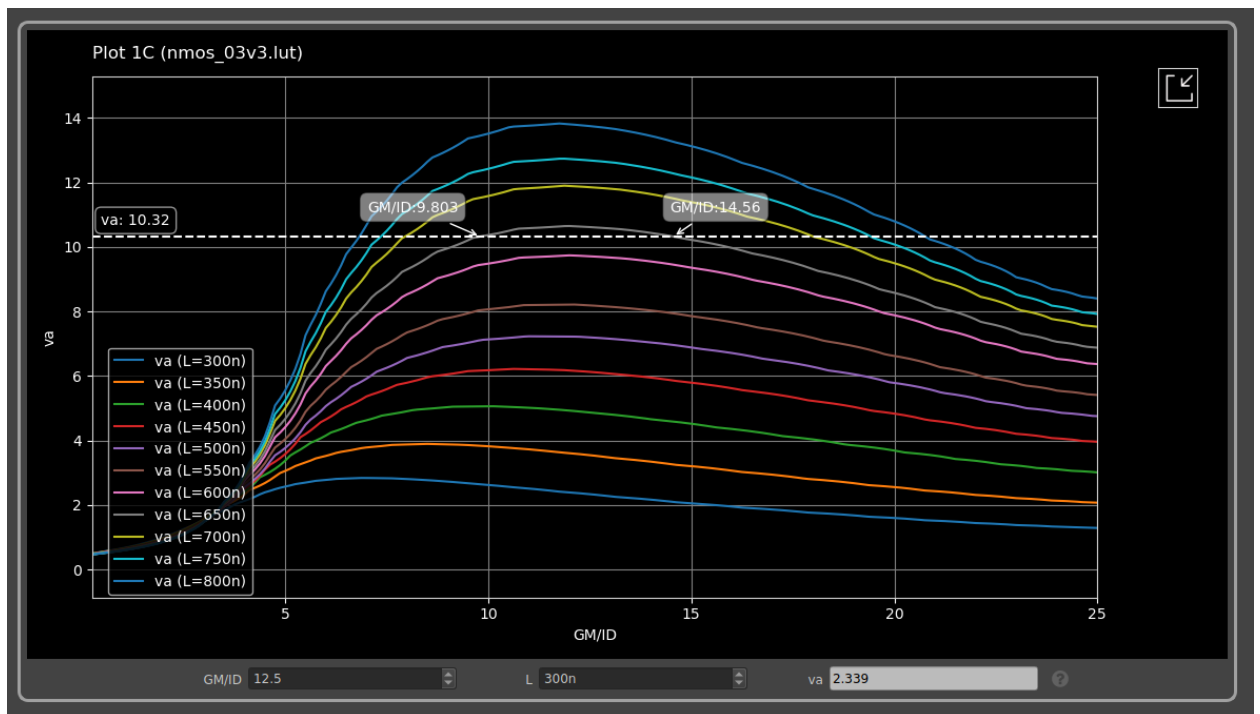
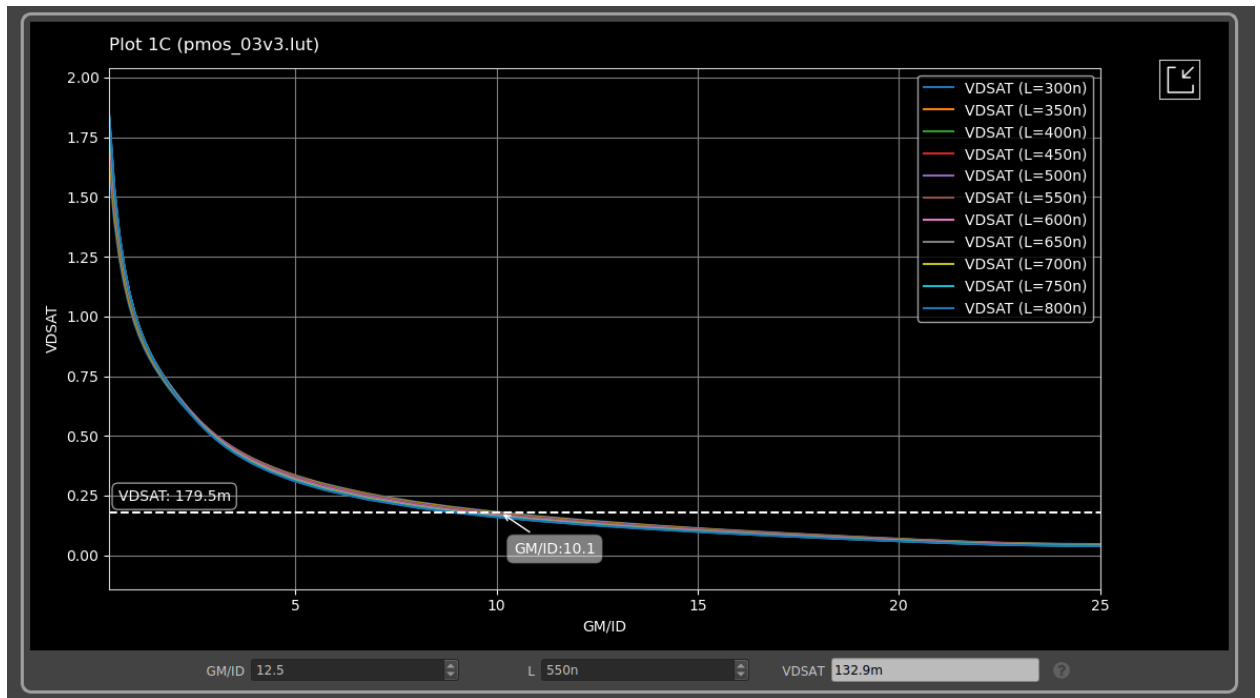
$$W_{Active\ load} = 22.51\mu m, L_{Active\ load} = 435nm$$

- Tail current source

Assume  $\frac{g_m}{I_D} = 10$

$$V_{DSSat} \approx V_{ov}, V_{ov} = \frac{2}{g_m/I_D}$$

$$V_{DSSat} \approx 0.2V$$



Now we will use the value of L to find the value of W

Plot 1A Plot 1B Plot 1C Plot 1D

Import: Plot 1A OK ?

▼ LUT Settings

LUT nmos\_03v3 ?

Corner TT All ?

Temp (°C) 27.0 All ?

Frequency 1 ?

ID 10u ?

gm/ID 10 ?

L 650n ?

VDS 0.4 ?

VSB 0 ?

Stack 1 ?

Results:

	Name	TT-27.0
1	ID	10u
2	IG	N/A
3	L	650n
4	W	3.03u

$$W_{tail} = 3.03\mu m, L_{tail} = 650nm$$

W, L,  $gm$ ,  $ID$ ,  $gm/ID$ ,  $VDS_{sat}$ ,  $V_{ov}=V_{GS}-V_{TH}$ , and  $V^*=2ID/gm$  of all transistors

- Input pair

```
[10-08-2025 20:39:29] - Info: [Sizing Assistant] The resultant point 'w = 22.5u'
[10-08-2025 20:39:32] - Info: [Sizing Assistant] The resultant point 'l = 440n'
[10-08-2025 20:39:33] - Info: [Sizing Assistant] The resultant point 'l = 440n'
[10-08-2025 20:39:39] - Info: [Sizing Assistant] The resultant point 'id = 20u'
[10-08-2025 20:39:45] - Info: [Sizing Assistant] The resultant point 'gm/id = 16.85'
[10-08-2025 20:39:56] - Info: [Sizing Assistant] The resultant point 'VDSAT = 92.64m'
[10-08-2025 20:40:15] - Info: [Sizing Assistant] The resultant point 'vgs-VTH = 8.475m'
[10-08-2025 20:40:24] - Info: [Sizing Assistant] The resultant point 'vstar = 118.7m'
```

- Active load

```
[10-08-2025 20:43:54] - Info: [Sizing Assistant] The resultant point 'w = 10.88u'
[10-08-2025 20:43:56] - Info: [Sizing Assistant] The resultant point 'l = 350n'
[10-08-2025 20:44:01] - Info: [Sizing Assistant] The resultant point 'gm = 198.2u'
[10-08-2025 20:44:11] - Info: [Sizing Assistant] The resultant point 'id = 20u'
[10-08-2025 20:44:24] - Info: [Sizing Assistant] The resultant point 'gm/id = 9.912'
[10-08-2025 20:44:34] - Info: [Sizing Assistant] The resultant point 'VDSAT = 179.7m'
[10-08-2025 20:44:40] - Info: [Sizing Assistant] The resultant point 'Vgs-vth = 155m'
[10-08-2025 21:01:04] - Info: [Sizing Assistant] The resultant point 'Vstar = 201.8m'
```

- Tail current source

```
10-08-2025 20:35:36] - Info: [Sizing Assistant] The resultant point 'w = 3.03u'
10-08-2025 20:35:38] - Info: [Sizing Assistant] The resultant point 'l = 650n'
10-08-2025 20:35:45] - Info: [Sizing Assistant] The resultant point 'gm = 98.94u'
10-08-2025 20:35:52] - Info: [Sizing Assistant] The resultant point 'gm/id = 9.894'
10-08-2025 20:36:27] - Info: [Sizing Assistant] The resultant point 'VDSAT = 172.9m'
10-08-2025 20:36:37] - Info: [Sizing Assistant] The resultant point 'Vgs-VTH = 142.5m'
10-08-2025 20:36:46] - Info: [Sizing Assistant] The resultant point 'VSTAR = 202.1m'
```

- Input pair

<i>parameter</i>	<i>Value</i>
$W$	$22.5\mu m$
$L$	$440nm$
$g_m$	$198.2\mu S$
$g_m/I_D$	$9.912V$
$V_{DSAT}$	$179.7mV$
$V_{ov}$	$155mV$
$V^*$	$201.8mV$

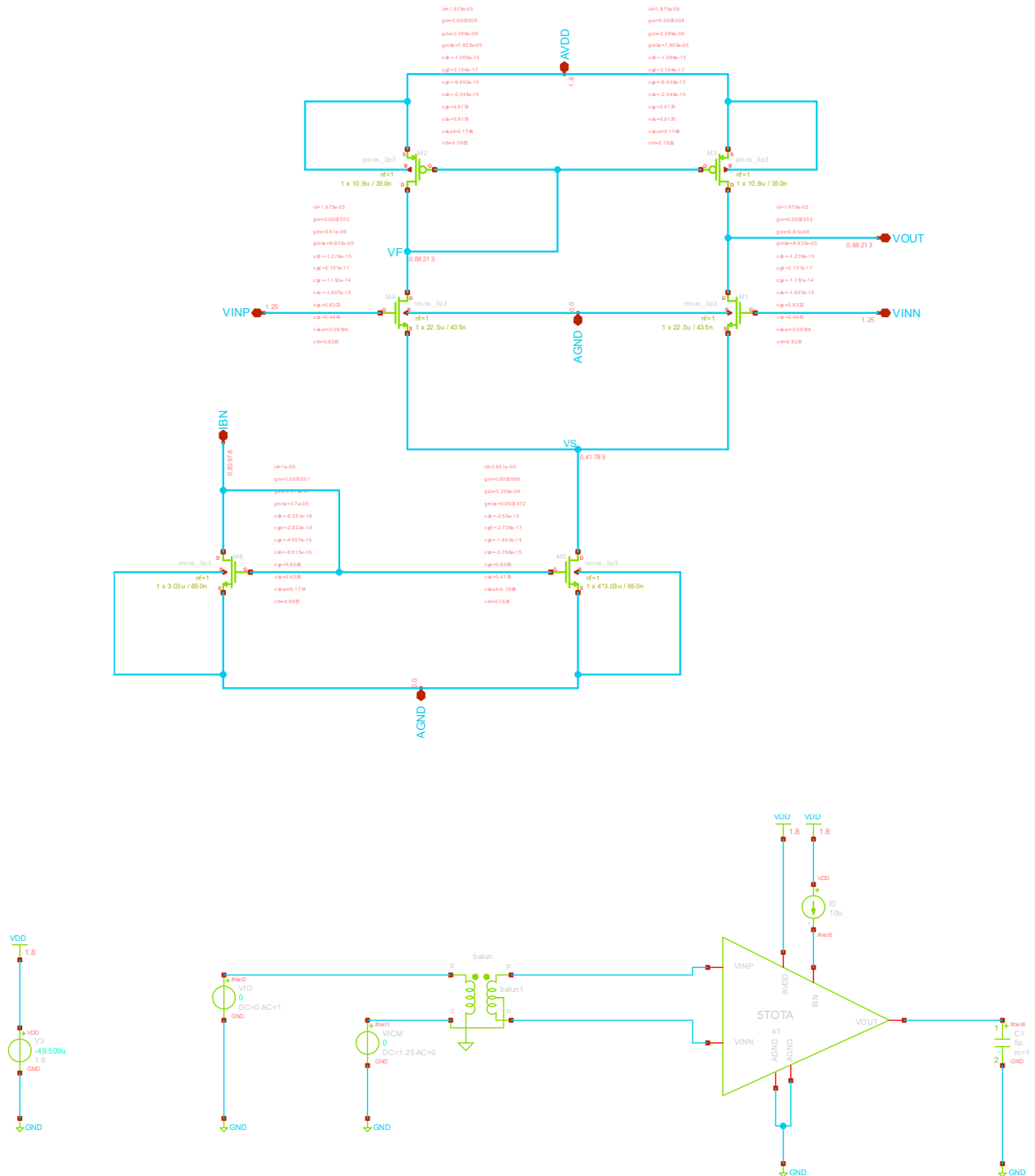
- Active load

<i>parameter</i>	Value
$W$	$10.88\mu m$
$L$	$350nm$
$g_m$	$192.2\mu S$
$g_m/I_D$	$16.75V$
$V_{DSAT}$	$92.64mV$
$V_{ov}$	$8.475mV$
$V^*$	$118.7mV$

- Tail

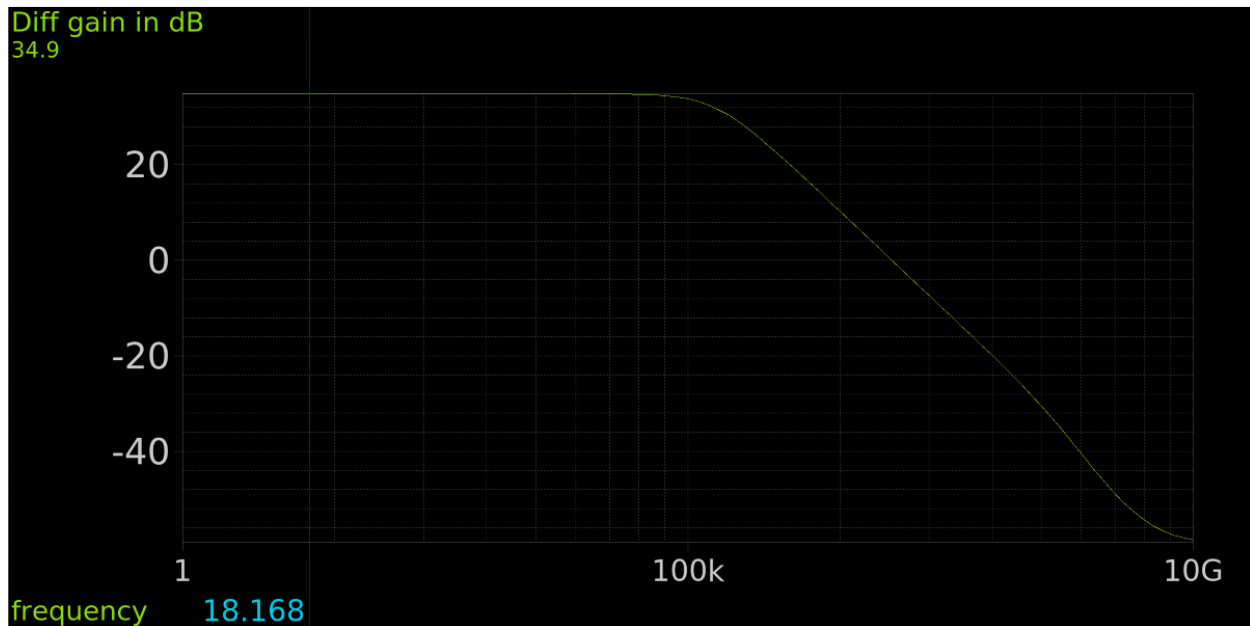
<i>parameter</i>	Value
$W$	$3.03\mu m$
$L$	$650n$
$g_m$	$98.94\mu S$
$g_m/I_D$	$9.894V$
$V_{DSAT}$	$172.9mV$
$V_{ov}$	$142.5mV$
$V^*$	$202.1mV$

# Part 3: Open-Loop OTA Simulation



- Since both transistors have the same dimensions and the same  $V_{DS}$  and  $V_{GS}$ , they operate at the same overdrive voltage  $V_{ov}$ . This gives them the same drain current,  $g_m = \frac{2I_D}{V_{ov}}$  which means that they both have the same  $g_m$  too
- $V_{OUT}=0.88213$  V in DC steady state.  
 $V_{OUT}=V_F$  because M2 and M3 form a current mirror that forces the drain currents of the inputs to match. In the bias condition, the mirror forces M2's source node to settle at the voltage that makes the two branches have equal currents .

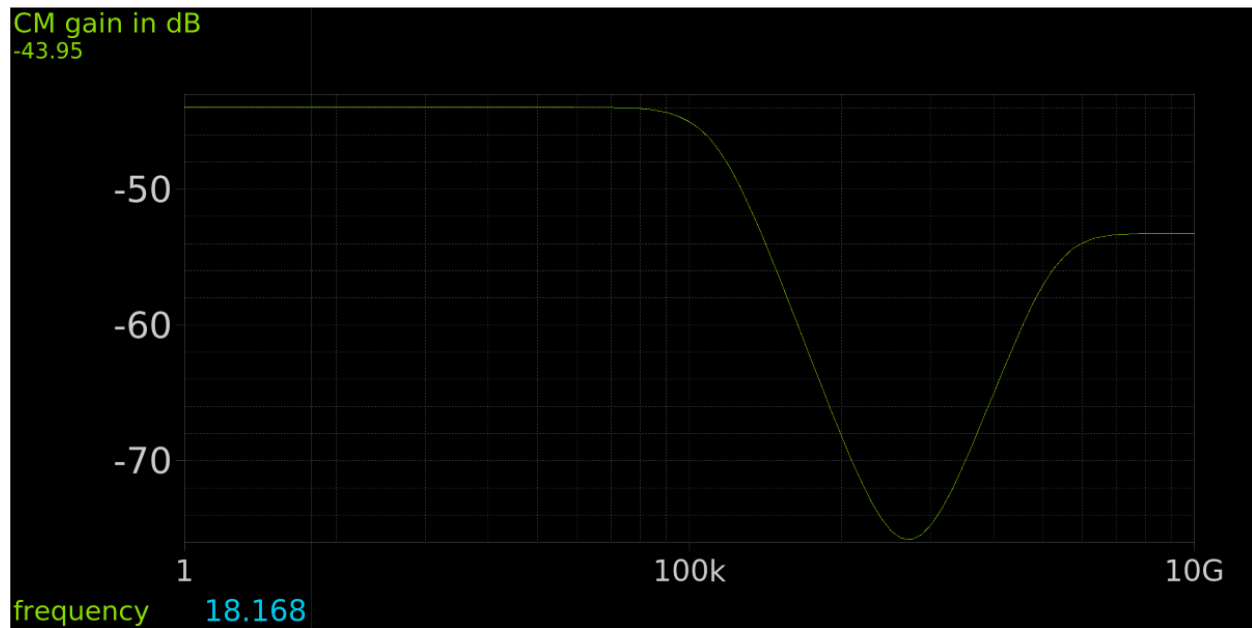
### Diff small signal ccs



$$A_v = g_{m1}(r_{o1} // r_{o3}), A_v = 55.89$$

$$A_v = 34.95 \text{ dB}$$

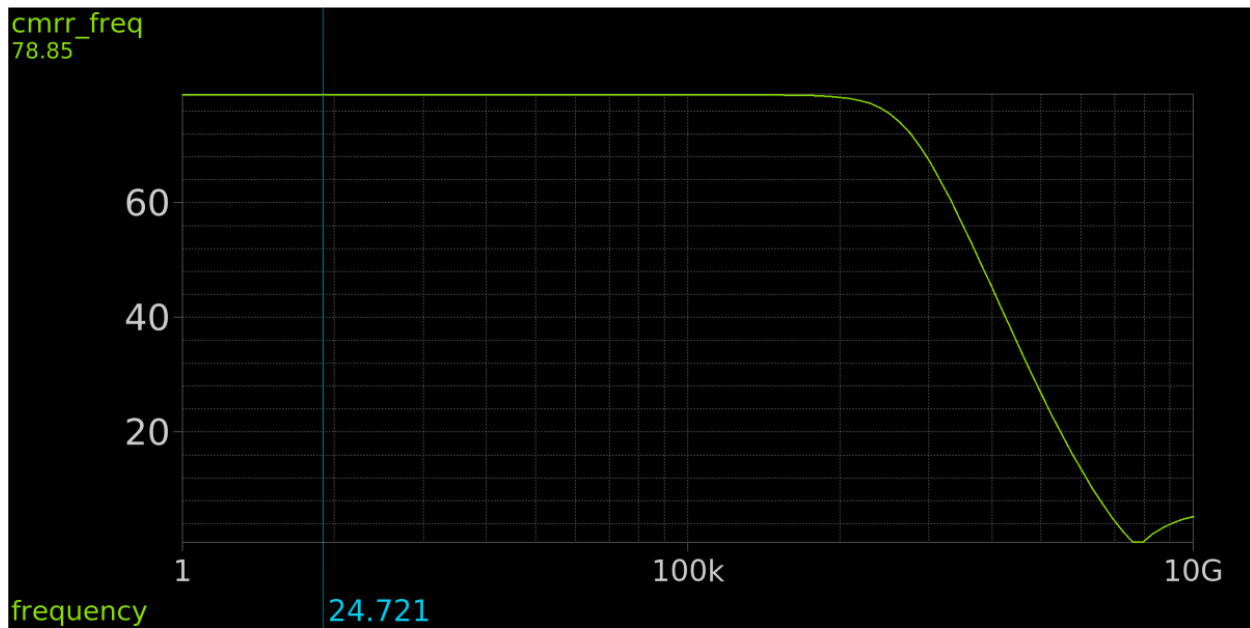
## CM small signal ccs



$$A_v = -\frac{1}{2 \times g_{m3} \times r_{o5}}, A_v = -8.237 \times 10^{-3}$$

$$A_v = -41.684 \text{ dB}$$

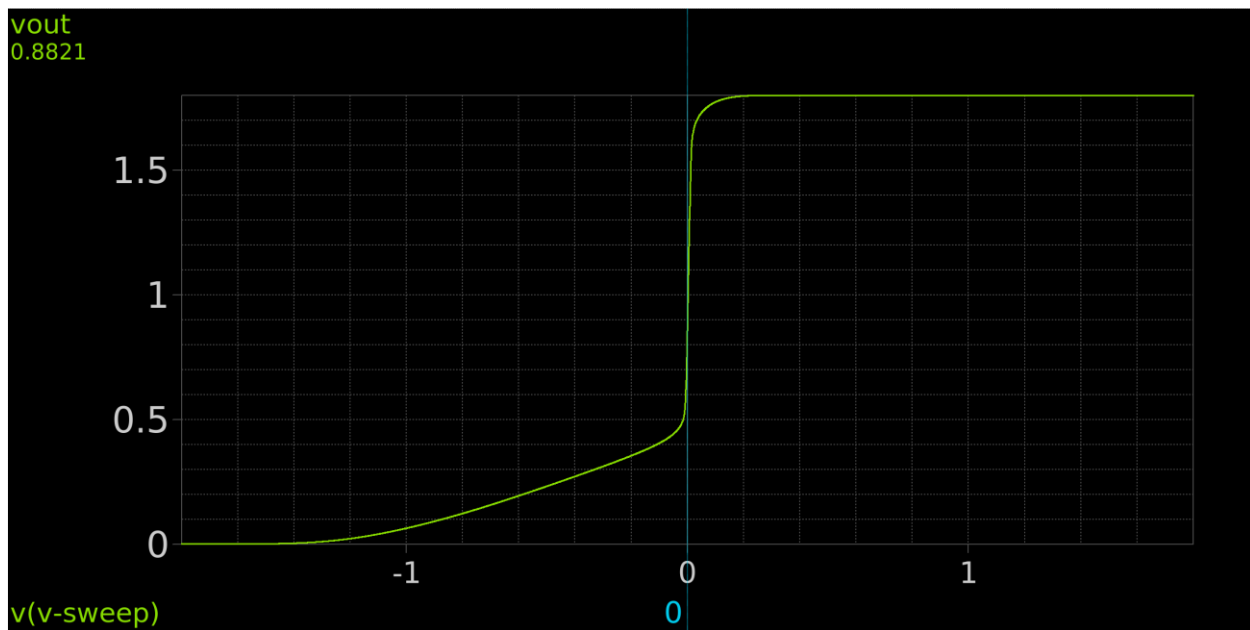
## CMRR

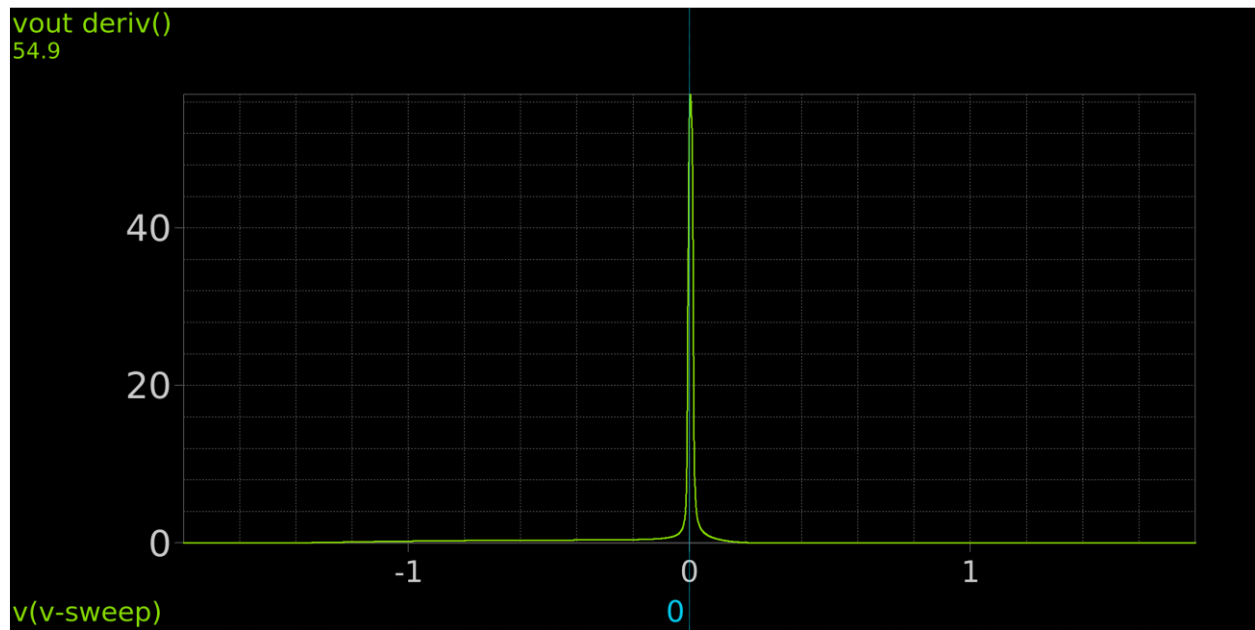


$$CMRR = \frac{A_{vd}}{A_{vcm}}, CMRR = 6785.3$$

$$CMRR = 76.6 \text{ dB}$$

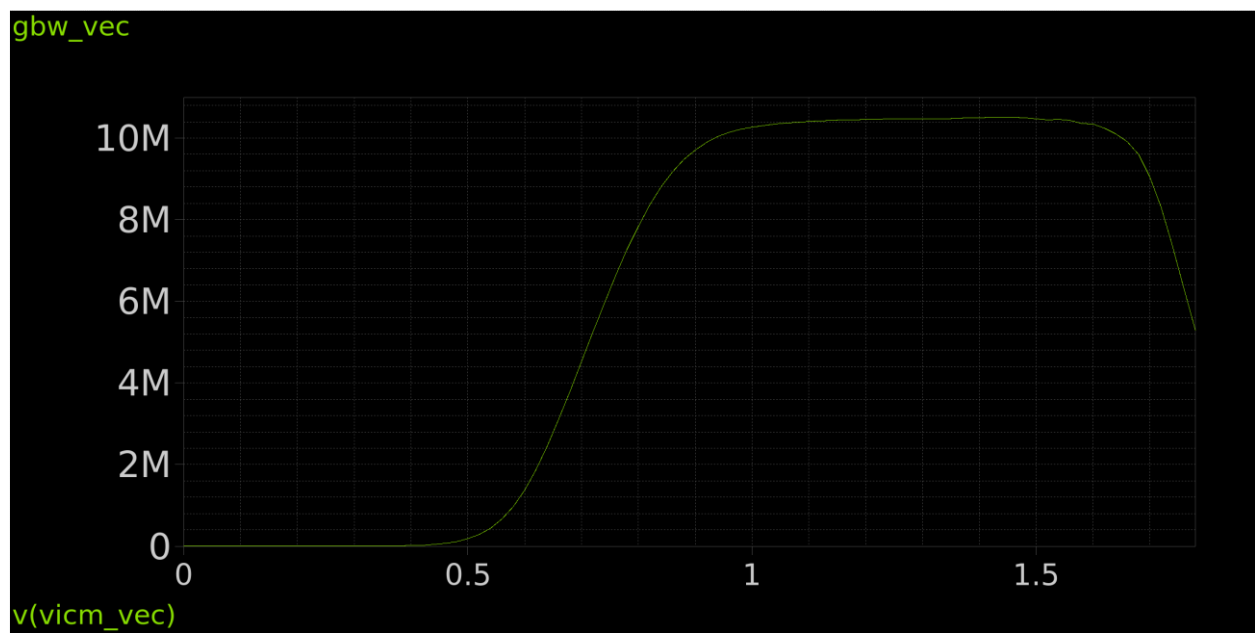
## Diff large signal ccs





Peak  $A_v=54.9$

CM large signal ccs (GBW vs VICM)

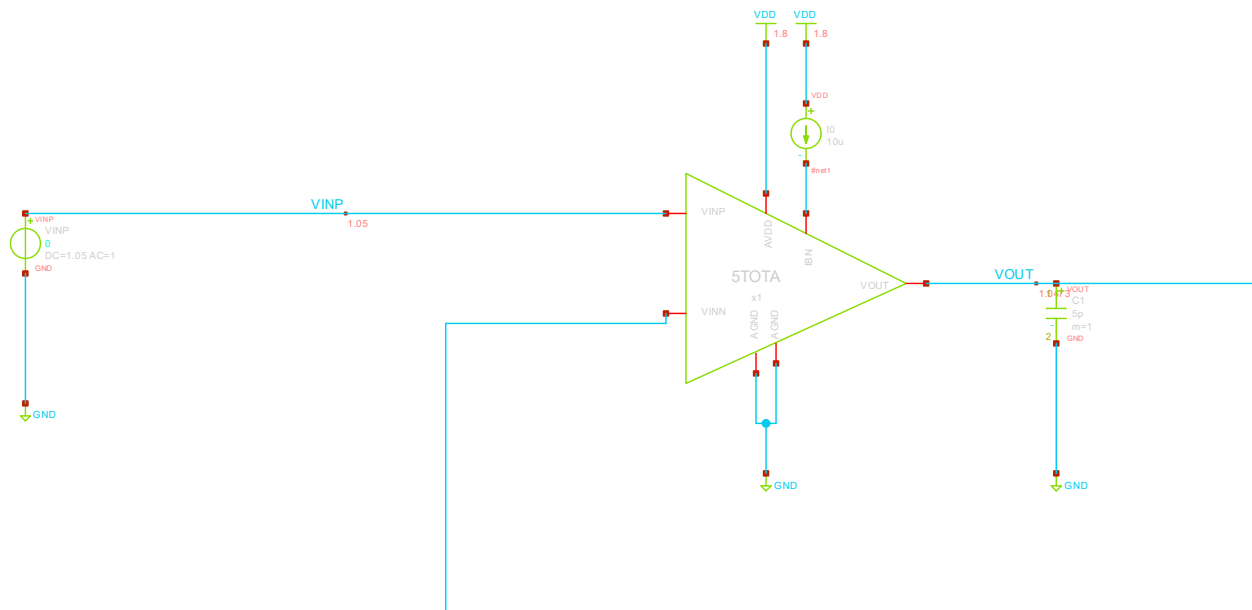


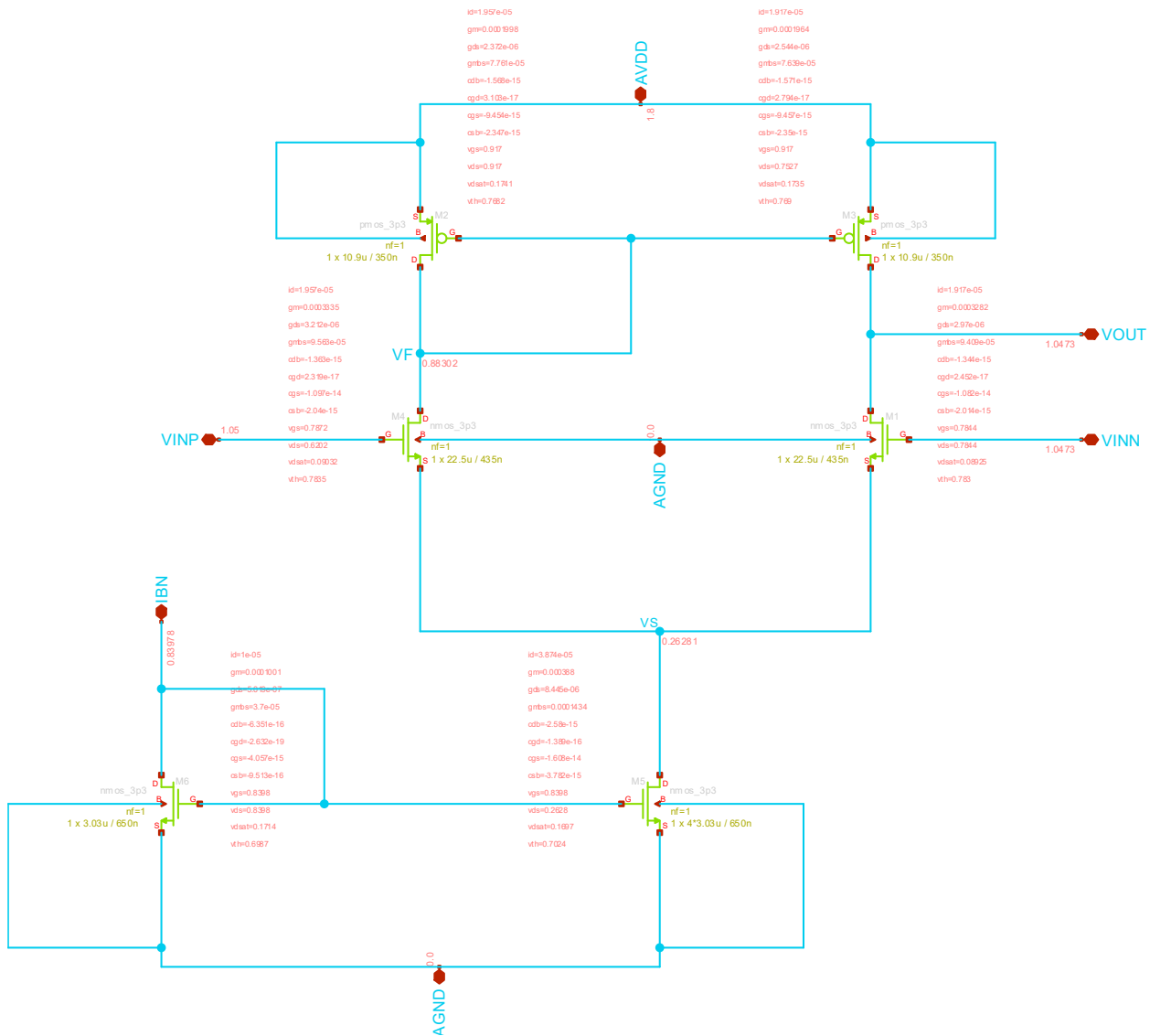
```

No. of Data Rows : 101
gain          = 1.175206e+00 at= 1.000000e+00
bw            = 4.504954e+06
max_gbw       = 1.050943e+07 at= 1.584893e+07
min_vincm     = 8.788375e-01
max_vincm     = 1.685160e+00
min_vincm     = 8.788375e-01
max_vincm     = 1.685160e+00
cmir          = 8.063225e-01
binary raw file "5t ota tb cmir.raw"

```

## PART 4: Closed-Loop OTA Simulation





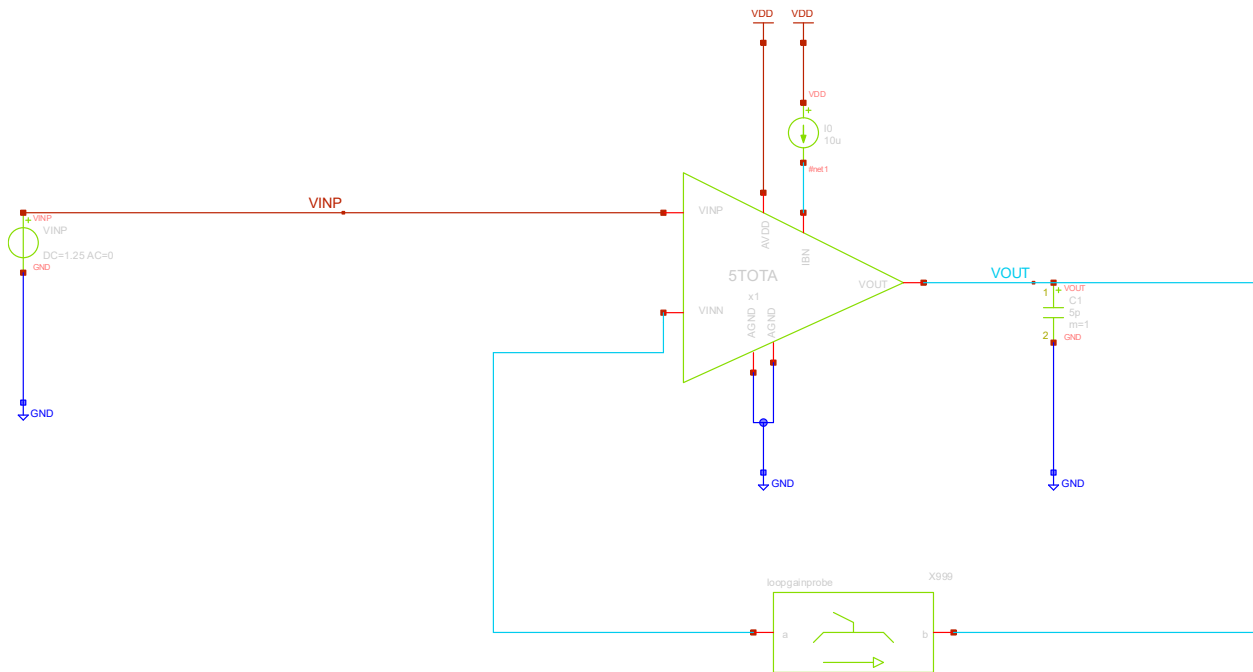
- Comment:  
Before closing the loop, VINP and VINN were equal at DC, so the two input transistors had identical gate voltages and matched operating points. After closing the loop, VOUT is connected to VINN , and the feedback action drives VINP and VINN to different DC values to satisfy the closed-loop bias condition. This DC difference in gate voltage between the two input transistors changes their overdrive voltages, leading to unequal drain currents and  $g_m$  values, hence creating a mismatch in the input pair parameters.

- Mismatch

$$I_{D1} = 1.957 \times 10^{-5}$$

$$I_{D4} = 1.917 \times 10^{-5}$$

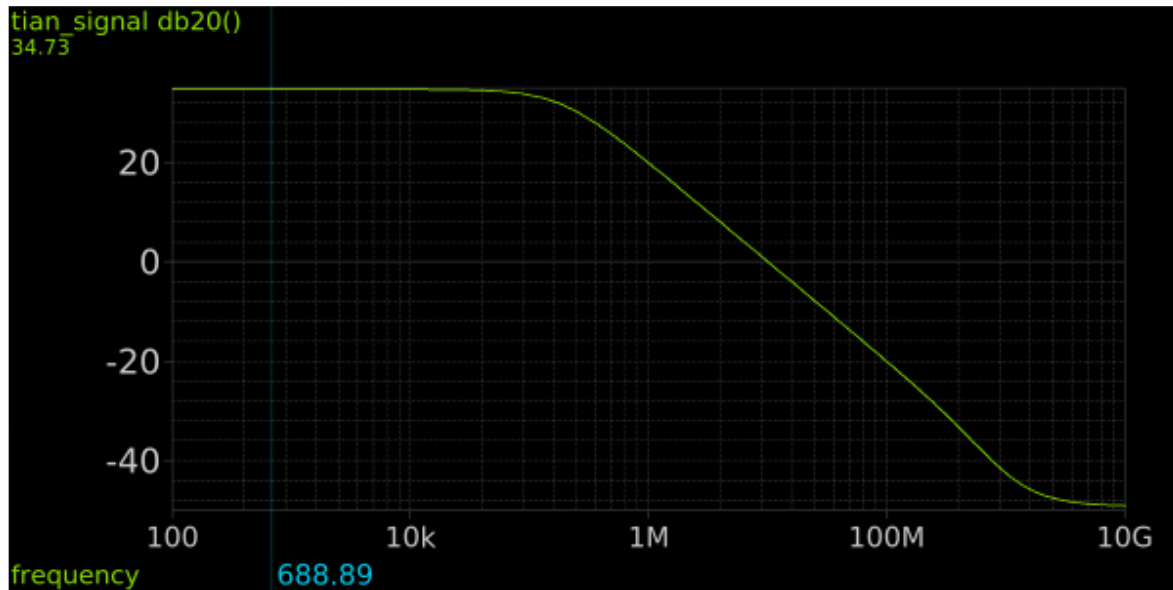
$$Mismatch = 0.04$$

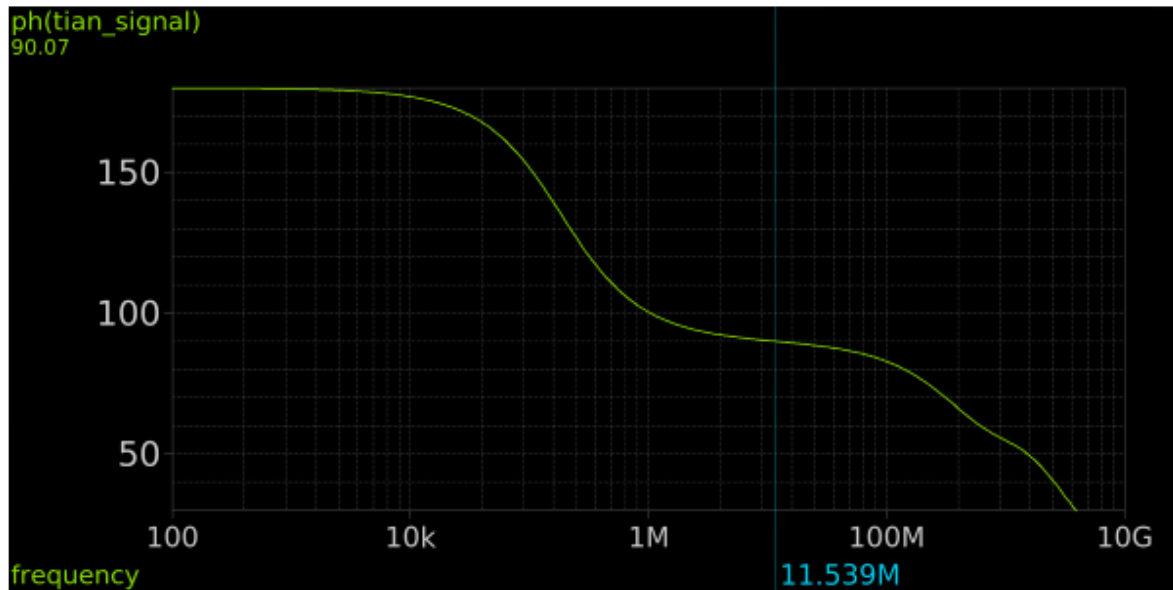


```

No. of Data Rows : 401
gain_crossover_freq = 1.008672e+07
phaseatzerogain    = 9.031005e+01
pm = 8.968995e+01
binary raw file "stb.raw"

```





<i>parameter</i>	Open loop value	Closed loop value
<i>DC gain</i>	34.9 dB	34.73 dB
<i>GBW</i>	10.05MHz	10.09MHz

$$A_v = g_{m1}(r_{o1} // r_{o3}), A_v = 55.89$$

$$A_v = 34.95 \text{ dB}$$

$$GBW = \frac{g_m}{2\pi C_L}, GBW = 10.4 \text{ MHz}$$

<i>parameter</i>	Simulation value	Hand-analysis value
<i>DC gain</i>	34.73 dB	34.94 dB
<i>GBW</i>	10.09MHz	10.4MHz