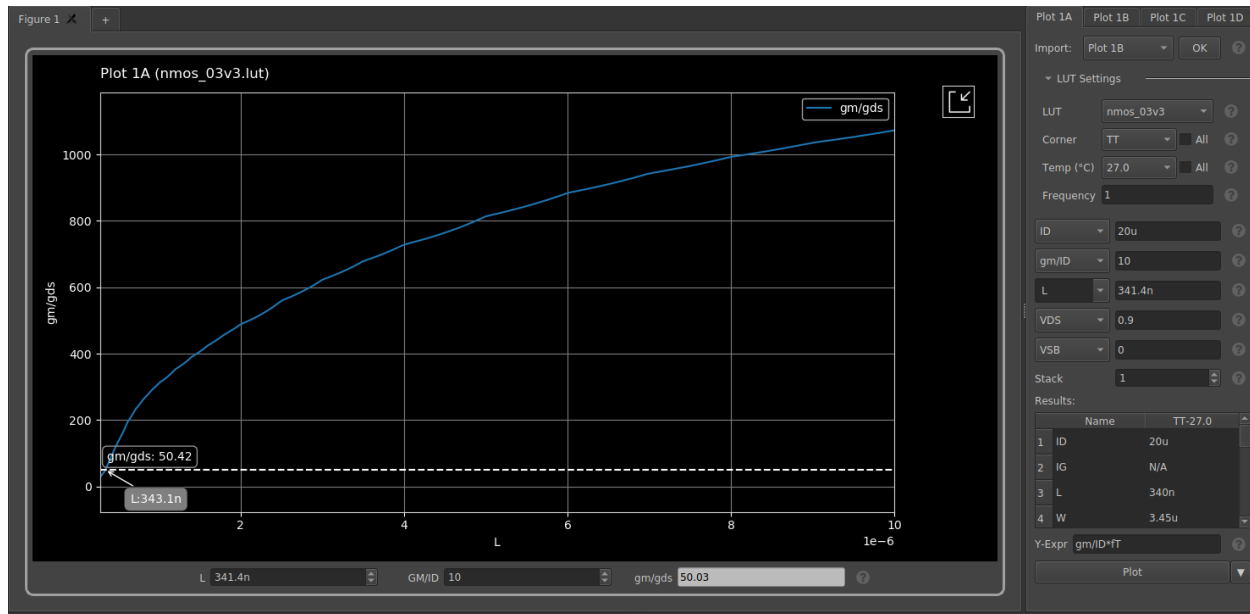


ITI
LAB3
Cascode Amplifier

Contents

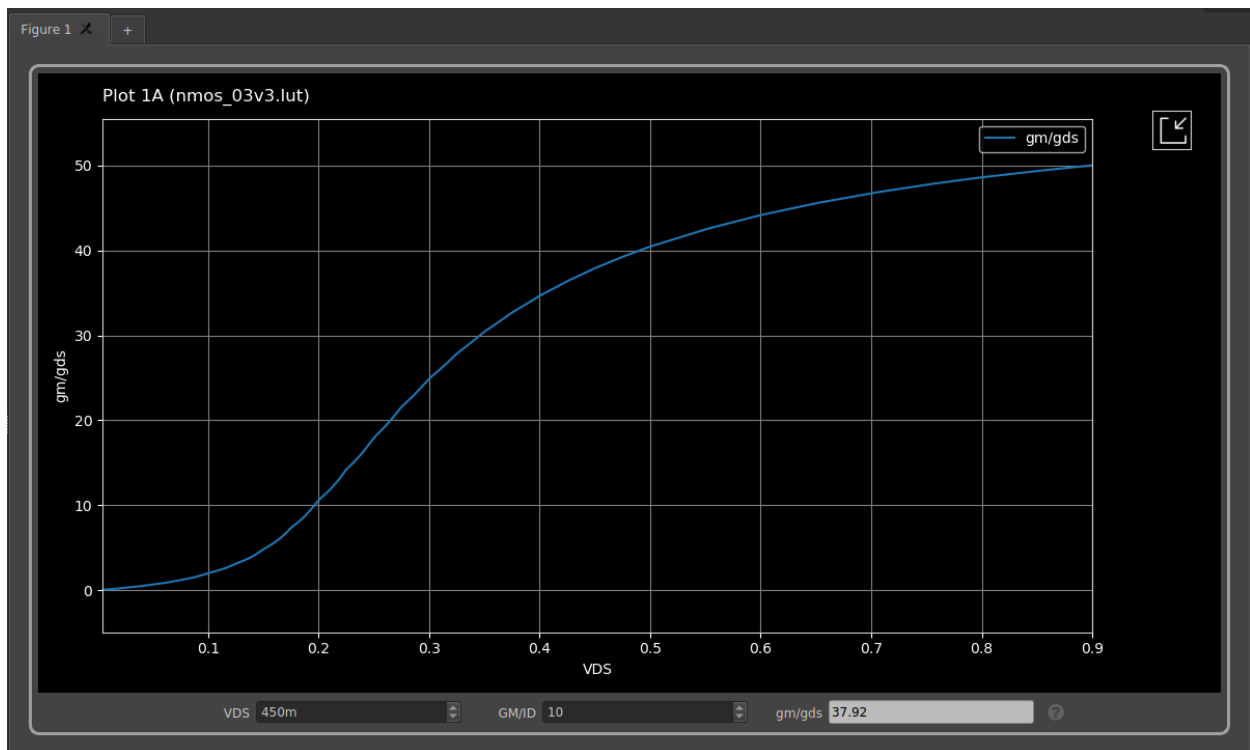
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Part 1: Device Sizing Using SA



$W=3.45\mu\text{m}$, $L=343.1 \text{ nm}$

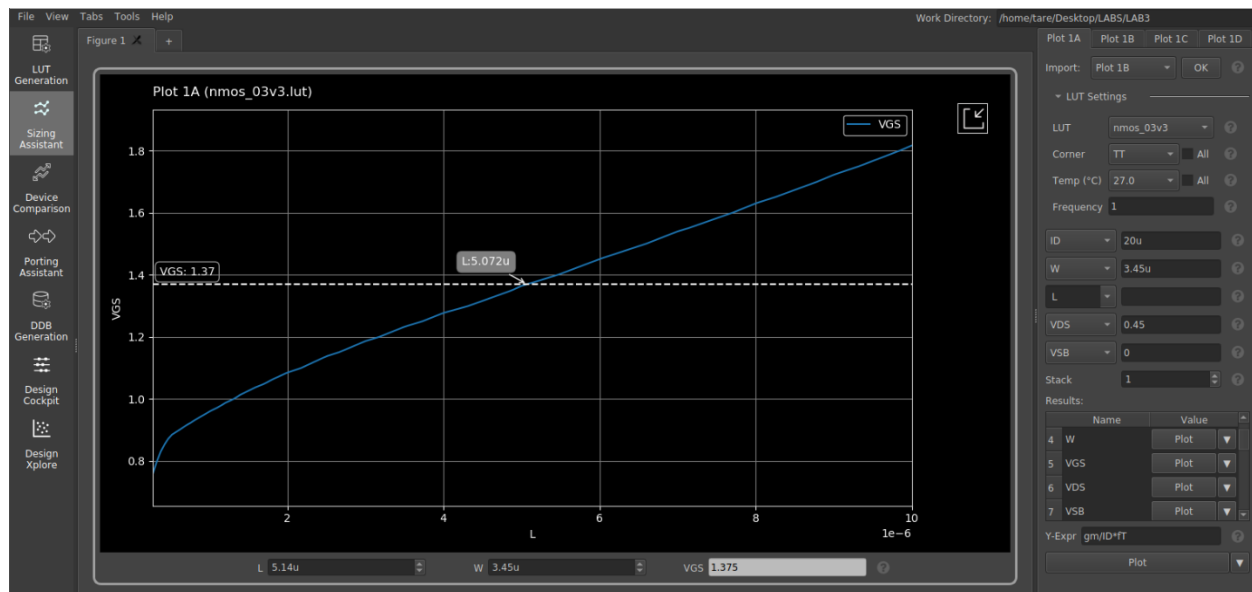
g_m/g_{ds} graph



- In a cascode amplifier using the same transistor sizing, the drain-source voltage (V_{DS}) is split between the two stacked transistors. Since the drain current and W/L ratio remain the same, the transconductance stays approximately constant. However, each transistor now operates with a lower V_{ds} , which increases its output resistance, thereby reducing g_{ds} . As a result, the overall $\frac{g_m}{g_{ds}}$ ratio increases, leading to a higher intrinsic gain for the cascode configuration.

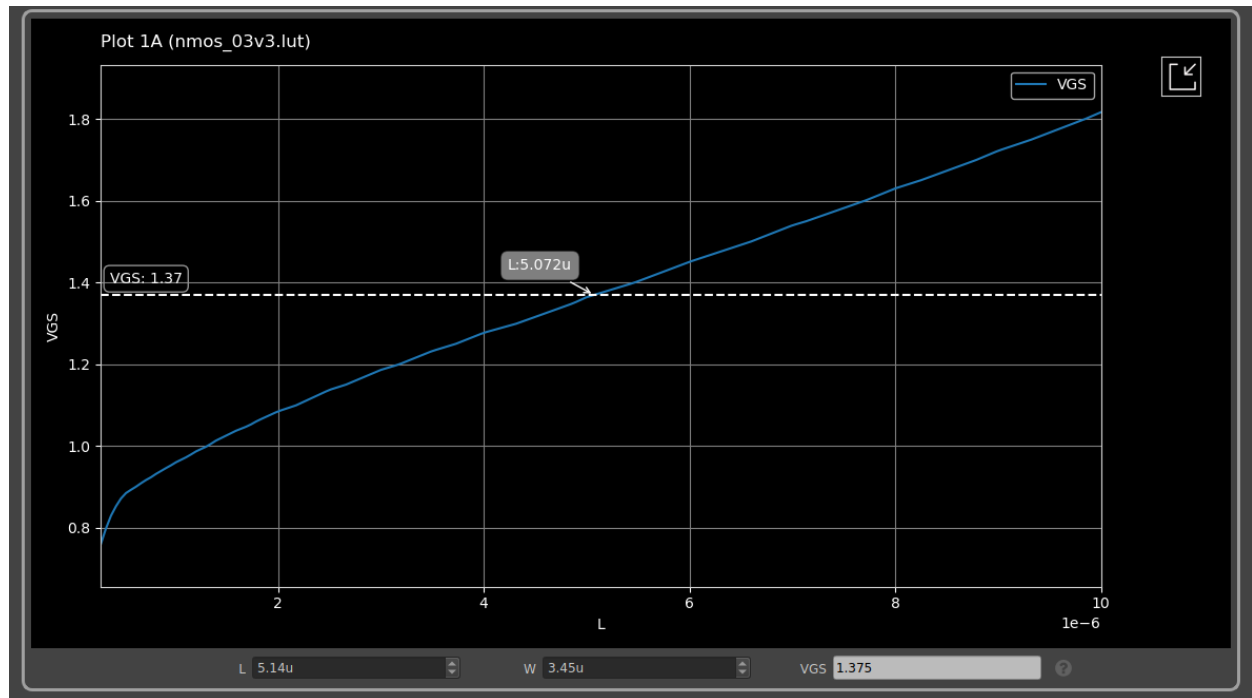
Part 2: Cascode for Gain

Sizing of M3 in the magic battery



$W=3.45\mu m$, $L \approx 5\mu m$

Calculating V_B



Calculating the value of the two voltage sources

The image shows two side-by-side screenshots of a circuit simulation software interface, likely LTspice, showing the MOSFET model settings and results for two different plots.

Left Screenshot (Plot 1A):

- Import: Plot 1B
- LUT Settings: LUT: nmos_03v3, Corner: TT, Temp (°C): 27.0, Frequency: 1
- Parameters: ID: 20u, W: 3.45u, L: 341.4n, VDS: 0.9, VSB: 0, Stack: 1
- Results table:

	Name	TT-27.0
3	L	340n
4	W	3.45u
5	VGS	797.5m
6	VDS	900m

- Y-Expr: gm/ID*fT
- Plot button

Right Screenshot (Plot 1B):

- Import: Plot 1B
- LUT Settings: LUT: nmos_03v3, Corner: TT, Temp (°C): 27.0, Frequency: 1
- Parameters: ID: 20u, W: 3.45u, L: 341.4n, VDS: 0.45, VSB: 0, Stack: 1
- Results table:

	Name	TT-27.0
3	L	340n
4	W	3.45u
5	VGS	808.2m
6	VDS	450m

- Y-Expr: gm/ID*fT
- Plot button

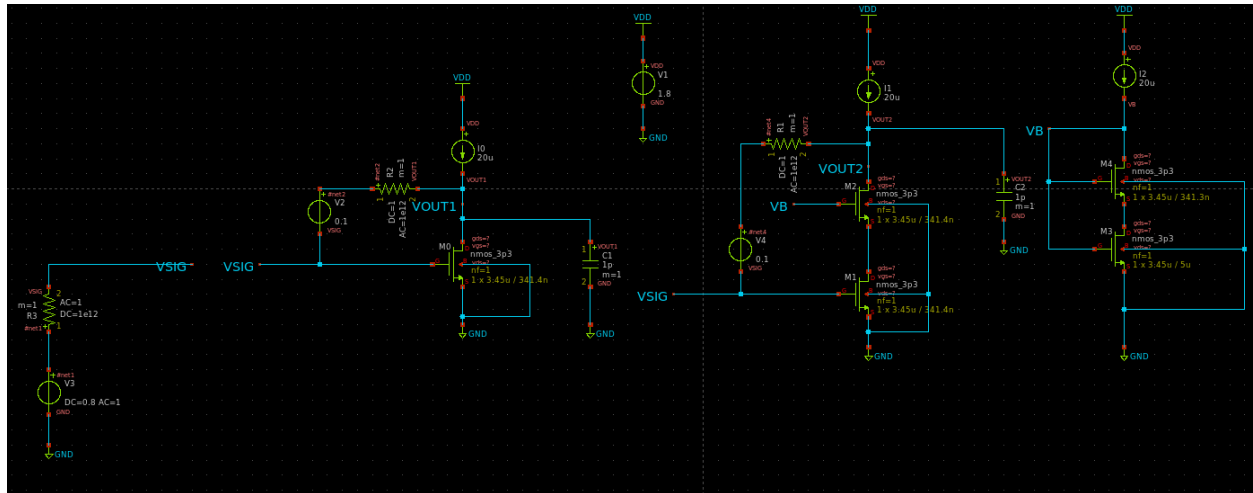
$$V1 = 0.9 - 0.7975$$

$$V1 \approx 0.1 \text{ V}$$

$$V2 = 0.9 - 0.8082$$

$$V2 \approx 0.1 \text{ V}$$

Schematic



DC OP

```
ngspice 1 -> print all
@m.xm0.m0[cdb] = -2.90578e-16
@m.xm0.m0[cgd] = 1.779221e-17
@m.xm0.m0[cgs] = -2.48655e-15
@m.xm0.m0[csb] = -4.35300e-16
@m.xm0.m0[gds] = 3.888824e-06
@m.xm0.m0[gm] = 2.039092e-04
@m.xm0.m0[gmb] = 5.714676e-05
@m.xm0.m0[id] = 2.066932e-05
@m.xm0.m0[vds] = 9.061490e-01
@m.xm0.m0[vdsat] = 1.632016e-01
@m.xm0.m0[vgs] = 8.061572e-01
@m.xm0.m0[vth] = 6.766916e-01
@m.xm1.m0[cdb] = -2.94132e-16
@m.xm1.m0[cgd] = 1.253252e-17
@m.xm1.m0[cgs] = -2.48879e-15
@m.xm1.m0[csb] = -4.37851e-16
@m.xm1.m0[gds] = 4.916997e-06
@m.xm1.m0[gm] = 1.935629e-04
@m.xm1.m0[gmb] = 5.451958e-05
@m.xm1.m0[id] = 1.933068e-05
@m.xm1.m0[vds] = 4.501752e-01
@m.xm1.m0[vdsat] = 1.622247e-01
@m.xm1.m0[vgs] = 8.061577e-01
@m.xm1.m0[vth] = 6.780967e-01
```

```
@m.xm2.m0[cdb] = -2.27062e-16
@m.xm2.m0[cgd] = 1.793869e-17
@m.xm2.m0[cgs] = -2.54632e-15
@m.xm2.m0[csb] = -3.38055e-16
@m.xm2.m0[gds] = 5.154783e-06
@m.xm2.m0[gm] = 1.930104e-04
@m.xm2.m0[gmb] = 4.186040e-05
@m.xm2.m0[id] = 1.933069e-05
@m.xm2.m0[vds] = 4.559620e-01
@m.xm2.m0[vdsat] = 1.657858e-01
@m.xm2.m0[vgs] = 9.155188e-01
@m.xm2.m0[vth] = 7.850566e-01
@m.xm3.m0[cdb] = -8.97291e-15
@m.xm3.m0[cgd] = -5.26285e-15
@m.xm3.m0[cgs] = -4.85722e-14
@m.xm3.m0[csb] = -1.17382e-14
@m.xm3.m0[gds] = 1.351783e-05
@m.xm3.m0[gm] = 4.525358e-05
@m.xm3.m0[gmb] = 1.758662e-05
@m.xm3.m0[id] = 2.000000e-05
@m.xm3.m0[vds] = 4.553435e-01
@m.xm3.m0[vdsat] = 5.503163e-01
@m.xm3.m0[vgs] = 1.365708e+00
@m.xm3.m0[vth] = 6.553700e-01
```

```

@m.xm4.m0[cdb] = -2.22234e-16
@m.xm4.m0[cgd] = 2.305510e-17
@m.xm4.m0[cgs] = -2.53164e-15
@m.xm4.m0[csb] = -3.32920e-16
@m.xm4.m0[gds] = 4.082919e-06
@m.xm4.m0[gm] = 1.996196e-04
@m.xm4.m0[gmb] = 4.288360e-05
@m.xm4.m0[id] = 2.000000e-05
@m.xm4.m0[vds] = 9.103425e-01
@m.xm4.m0[vdsat] = 1.646558e-01
@m.xm4.m0[vgs] = 9.103498e-01
@m.xm4.m0[vth] = 7.816275e-01
net1 = 8.000000e-01
net2 = 9.061648e-01
net3 = 4.501893e-01
net4 = 9.061648e-01
net5 = 4.553581e-01
v1#branch = -6.000000e-05
v2#branch = -6.69317e-07
v3#branch = 6.164777e-15
v4#branch = 6.693174e-07
vb = 1.365715e+00

```

Checking if all transistors are in saturation

Transistor	Vds	Vds sat	Vth	Region
M0	0.9	0.163	0.67	Saturation
M1	0.45	0.162	0.67	Saturation
M2	0.45	0.162	0.785	Saturation
M3	0.455	0.55	0.66	Triode
M4	0.9	0.165	0.78	Saturation

- From the above table, M3 is operating in the triode region as The gate and drain of M4 are connected together, ensuring M4 operates in saturation. However , M3's drain is at a lower voltage than its gate, since it's connected to the source of another NMOS below it. This causes VDS3 to drop significantly while VGS3 remains the same as M4 (since the gates are shared). When VDS3 becomes less than VGS3 - Vth, M3 enters the triode region.

- M2 and M4 have different V_{th} from M0, M1 and M3.
Transistors M2 and M4 exhibit a higher effective threshold voltage V_{th} due to the body effect. In the cascode configuration, their sources are elevated (at ~ 0.45 V) rather than grounded, resulting in a nonzero source-to-bulk voltage V_{SB} . Since the gate is biased at a fixed voltage, the increased V_{SB} leads to an increase in V_{th} according to the body effect equation.

Transistor	g_m	g_{ds}	Comparison
M0	2.04×10^{-4}	3.88×10^{-6}	$g_m \gg g_{ds}$
M1	1.95×10^{-4}	4.9×10^{-6}	$g_m \gg g_{ds}$
M2	1.93×10^{-4}	5.15×10^{-6}	$g_m \gg g_{ds}$
M3	4.52×10^{-5}	1.35×10^{-5}	$g_m > g_{mb}$
M4	2×10^{-4}	4.1×10^{-6}	$g_m \gg g_{mb}$

Transistor	g_m	g_{mb}	Comparison
M0	2.04×10^{-4}	5.71×10^{-5}	$g_m > g_{mb}$
M1	1.93×10^{-4}	5.45×10^{-5}	$g_m > g_{mb}$
M2	1.93×10^{-4}	4.186×10^{-5}	$g_m > g_{mb}$
M3	4.52×10^{-5}	1.75×10^{-5}	$g_m > g_{mb}$
M4	2×10^{-4}	4.3×10^{-5}	$g_m > g_{mb}$

Transistor	egs	egd	Comparison
M0	2.49×10^{-15}	1.78×10^{-17}	Cgs >> Cgd
M1	2.49×10^{-15}	1.25×10^{-17}	Cgs >> Cgd
M2	2.54×10^{-15}	1.79×10^{-17}	Cgs >> Cgd
M3	4.857×10^{-14}	5.26×10^{-15}	Cgs > Cgd
M4	2.53×10^{-15}	2.3×10^{-17}	Cgs >> Cgd

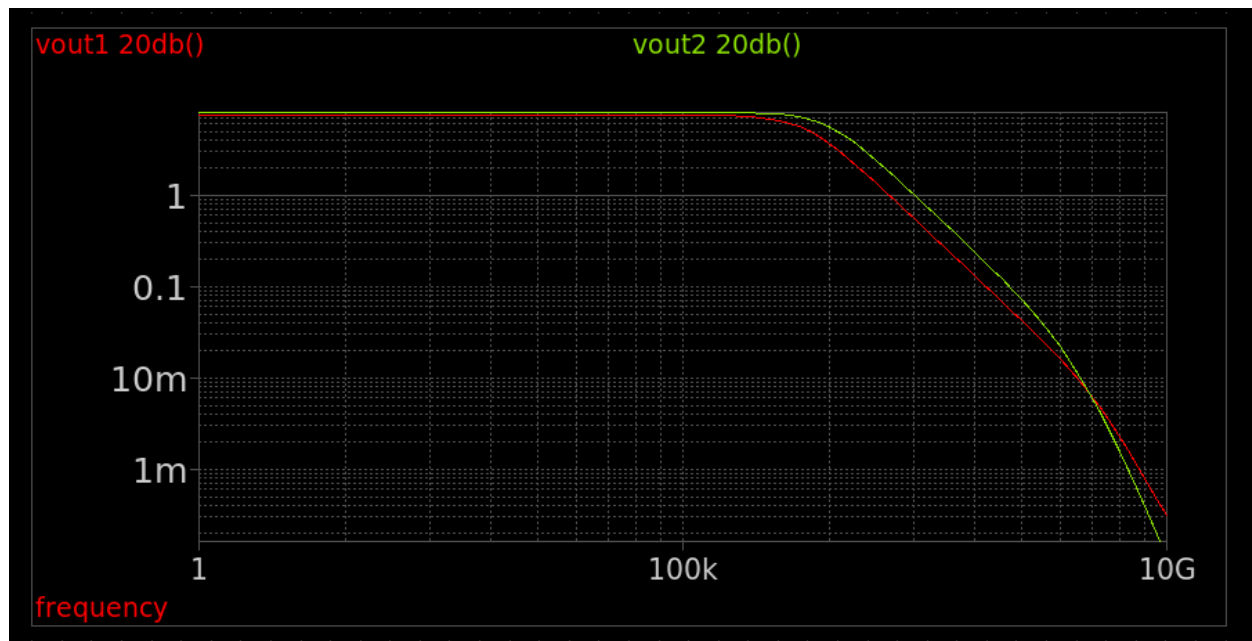
Transistor	csb	cdb	Comparison
M0	4.35×10^{-16}	1.25×10^{-17}	Csb >> Cdb
M1	4.37×10^{-16}	2.49×10^{-15}	Csb >> Cdb
M2	3.38×10^{-16}	2.27×10^{-16}	Csb > Cdb
M3	1.17×10^{-14}	8.97×10^{-15}	Csb >> Cdb
M4	3.33×10^{-16}	2.22×10^{-16}	Csb > Cdb

AC analysis

DC gain, BW, GBW, and UGF

```
gain_cs = 5.243463e+01
bw_cs = 6.176208e+05
gbw_cs = 3.238472e+07
ugf_cs = 3.241994e+07
gain_casc = 1.832993e+03
bw_casc = 1.644846e+04
gbw_casc = 3.014991e+07
ugf_casc = 3.020803e+07
binary raw file "lab3_1.raw"
ngspice 1 -> █
```

Bode plot



Hand analysis for DC gain, BW, GBW, and UGF

1. Common source

$$\text{DC gain(Common source amplifier)} = \frac{g_{m0}}{g_{ds0}}$$

$$\text{DC gain(Common source amplifier)} = \frac{2.04 \times 10^{-4}}{3.88 \times 10^{-6}}$$

$$\text{DC gain} = 52.577$$

$$\text{BW} = \frac{1}{2\pi RC}, R = 257K\Omega, C = 1pF$$

$$\text{BW} = 6.19 \times 10^5 \text{ Hz}$$

$$\text{UGF} = \text{BW} \times A_v, \text{GBW} = \text{BW} \times A_v$$

$$\text{UGF} = 3.254 \times 10^7$$

$$\text{GBW} = 3.254 \times 10^7$$

Parameter	Simulation Value	Analysis Value
DC gain	52.43	52.577
BW	6.17×10^5	6.19×10^5
GBW	3.23×10^7	3.254×10^7
UGF	3.24×10^7	3.254×10^7

2. Cascode

$$\text{DC gain(Cascode)} = r_{o2} \left(1 + (g_{m2} + g_{mb2}) r_{o1} \right) g_{m1}$$

$$\text{DC gain(Cascode)} = 194 \times 10^3 (1 + (1.93 \times 10^{-4} + 4.186 \times 10^{-5}) 205 \times 10^3) 1.95 \times 10^{-4}$$

$$\text{DC gain (Cascode)} \approx 1859$$

$$\text{BW} = \frac{1}{2\pi RC}, R = r_{o2} \left(1 + (g_{m2} + g_{mb2}) r_{o1} \right) R = 9.53 \text{M}\Omega, C = 1 \text{pF}$$

$$\text{BW} = 1.67 \times 10^4 \text{ Hz}$$

$$\text{UGF} = \text{BW} \times A_v, \text{GBW} = \text{BW} \times A_v$$

$$\text{UGF} = 3.1 \times 10^7$$

$$\text{GBW} = 3.1 \times 10^7$$

Parameter	Simulation Value	Analysis Value
DC gain	1832	1859
BW	1.644×10^4	1.67×10^4
GBW	3.01×10^7	3.1×10^7
UGF	3.02×10^7	3.1×10^7

Comments:

1. The cascode amplifier consistently shows a much higher DC gain than the common source amplifier. This is expected because in a cascode configuration, the output resistance is significantly boosted due to the stacking of two transistors, effectively increasing the overall gain. In contrast, the common source amplifier has limited output resistance, resulting in lower gain. This advantage is clearly reflected in both the simulation and hand analysis results.
2. While the cascode amplifier achieves higher gain, it typically exhibits a narrower bandwidth compared to the common source amplifier. This is due to the increased output impedance and the Miller effect being mitigated only partially. However, the pole formed by the high impedance node limits the bandwidth.

3. Despite the significant difference in DC gain and bandwidth between the common source and the cascode amplifiers, UGF is nearly the same for both. This outcome highlights a fundamental design trade-off: increasing gain typically reduces bandwidth, but their product (GBW) remains fairly constant. It reflects how amplifiers can be optimized for either high gain or wide bandwidth, but not both simultaneously without impacting UGF. The gain-bandwidth product provides an important measure of amplifier speed vs. amplification capability. Both architectures show similar GBW, since increasing gain usually comes at the cost of reduced bandwidth.
4. Both the common source and cascode amplifiers exhibit nearly identical GBW, despite having very different DC gains and bandwidths individually. This suggests that while the cascode configuration boosts gain and narrows bandwidth, and the common source does the opposite, the overall frequency performance in terms of UGF and GBW which remains fundamentally limited by the same technology and biasing conditions. It highlights the inherent trade-off and balance between gain and bandwidth in amplifier design.

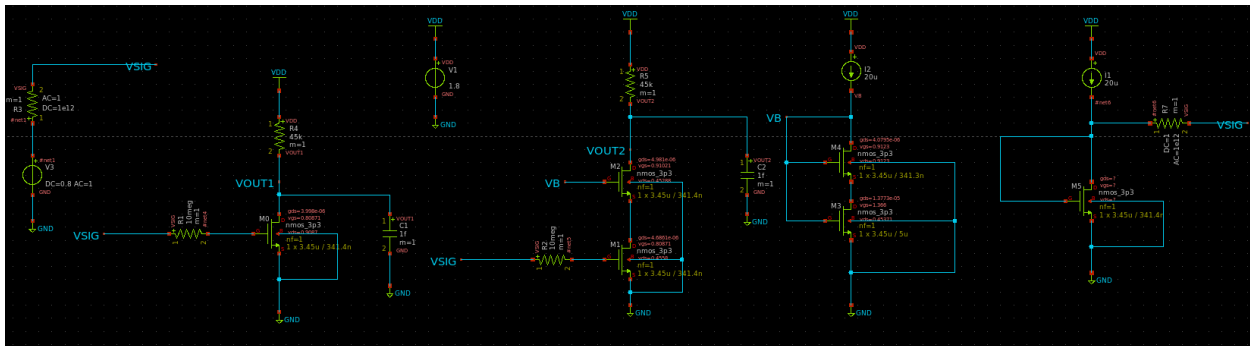
Part 3: Cascode for BW

R_D Calculations

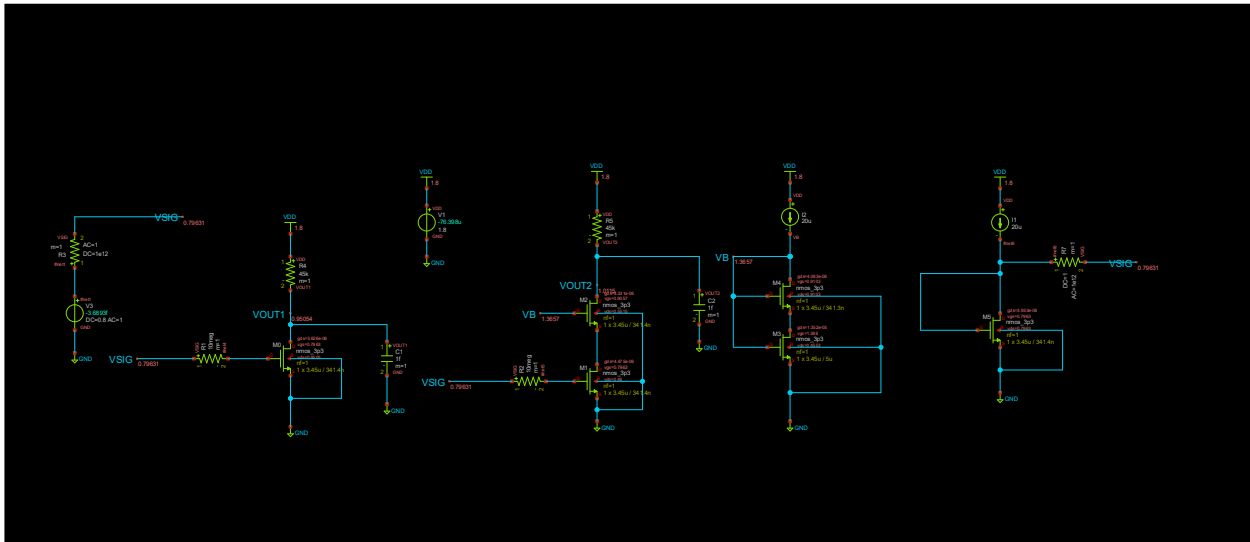
$$R_D = \frac{V_{RD}}{I_{Bias}}, V_{RD} = \frac{V_{DD}}{2}, I_{Bias} = 20\mu A$$

$$R_D = 45K\Omega$$

Schematic



DC OP and Voltages annotated



```
@m.xm0.m0[cdb] = -2.86463e-16
@m.xm0.m0[cgd] = 1.759709e-17
@m.xm0.m0[cgs] = -2.44639e-15
@m.xm0.m0[csb] = -4.29205e-16
@m.xm0.m0[gds] = 3.626094e-06
@m.xm0.m0[gm] = 1.937213e-04
@m.xm0.m0[gmb] = 5.423962e-05
@m.xm0.m0[id] = 1.887692e-05
@m.xm0.m0[vds] = 9.505248e-01
@m.xm0.m0[vdsat] = 1.569109e-01
@m.xm0.m0[vgs] = 7.963038e-01
@m.xm0.m0[vth] = 6.762754e-01
@m.xm1.m0[cdb] = -2.89714e-16
@m.xm1.m0[cgd] = 1.305411e-17
@m.xm1.m0[cgs] = -2.44702e-15
@m.xm1.m0[csb] = -4.31589e-16
@m.xm1.m0[gds] = 4.475188e-06
@m.xm1.m0[gm] = 1.830929e-04
@m.xm1.m0[gmb] = 5.153802e-05
@m.xm1.m0[id] = 1.752123e-05
@m.xm1.m0[vds] = 4.600457e-01
@m.xm1.m0[vdsat] = 1.557254e-01
@m.xm1.m0[vgs] = 7.963043e-01
@m.xm1.m0[vth] = 6.780040e-01
```

```
@m.xm2.m0[cgd] = 2.059451e-17
@m.xm2.m0[cgs] = -2.49930e-15
@m.xm2.m0[csb] = -3.30322e-16
@m.xm2.m0[gds] = 4.330907e-06
@m.xm2.m0[gm] = 1.832361e-04
@m.xm2.m0[gmb] = 3.948523e-05
@m.xm2.m0[id] = 1.752123e-05
@m.xm2.m0[vds] = 5.514734e-01
@m.xm2.m0[vdsat] = 1.584529e-01
@m.xm2.m0[vgs] = 9.056503e-01
@m.xm2.m0[vth] = 7.860711e-01
@m.xm3.m0[cdb] = -8.97291e-15
@m.xm3.m0[cgd] = -5.26285e-15
@m.xm3.m0[cgs] = -4.85722e-14
@m.xm3.m0[csb] = -1.17382e-14
@m.xm3.m0[gds] = 1.351783e-05
@m.xm3.m0[gm] = 4.525358e-05
@m.xm3.m0[gmb] = 1.758662e-05
@m.xm3.m0[id] = 2.000000e-05
@m.xm3.m0[vds] = 4.553435e-01
@m.xm3.m0[vdsat] = 5.503163e-01
@m.xm3.m0[vgs] = 1.365708e+00
@m.xm3.m0[vth] = 6.553700e-01
```

```
@m.xm3.m0[vdsat] = 5.503163e-01
@m.xm3.m0[vgs] = 1.365708e+00
@m.xm3.m0[vth] = 6.553700e-01
@m.xm4.m0[cdb] = -2.22234e-16
@m.xm4.m0[cgd] = 2.305510e-17
@m.xm4.m0[cgs] = -2.53164e-15
@m.xm4.m0[csb] = -3.32920e-16
@m.xm4.m0[gds] = 4.082919e-06
@m.xm4.m0[gm] = 1.996196e-04
@m.xm4.m0[gmbs] = 4.288360e-05
@m.xm4.m0[id] = 2.000000e-05
@m.xm4.m0[vds] = 9.103425e-01
@m.xm4.m0[vdsat] = 1.646558e-01
@m.xm4.m0[vgs] = 9.103498e-01
@m.xm4.m0[vth] = 7.816275e-01
@m.xm5.m0[cdb] = -2.90221e-16
@m.xm5.m0[cgd] = 1.744742e-17
@m.xm5.m0[cgs] = -2.47820e-15
@m.xm5.m0[csb] = -4.34563e-16
@m.xm5.m0[gds] = 3.932780e-06
@m.xm5.m0[gm] = 1.998791e-04
@m.xm5.m0[gmbs] = 5.607266e-05
@m.xm5.m0[id] = 2.000000e-05
@m.xm5.m0[vds] = 7.962961e-01
@m.xm5.m0[vdsat] = 1.615499e-01
@m.xm5.m0[vgs] = 7.963034e-01
@m.xm5.m0[vth] = 6.692447e-01
net1 = 8.000000e-01
net2 = 4.600585e-01
net3 = 4.553581e-01
net4 = 7.963107e-01
```

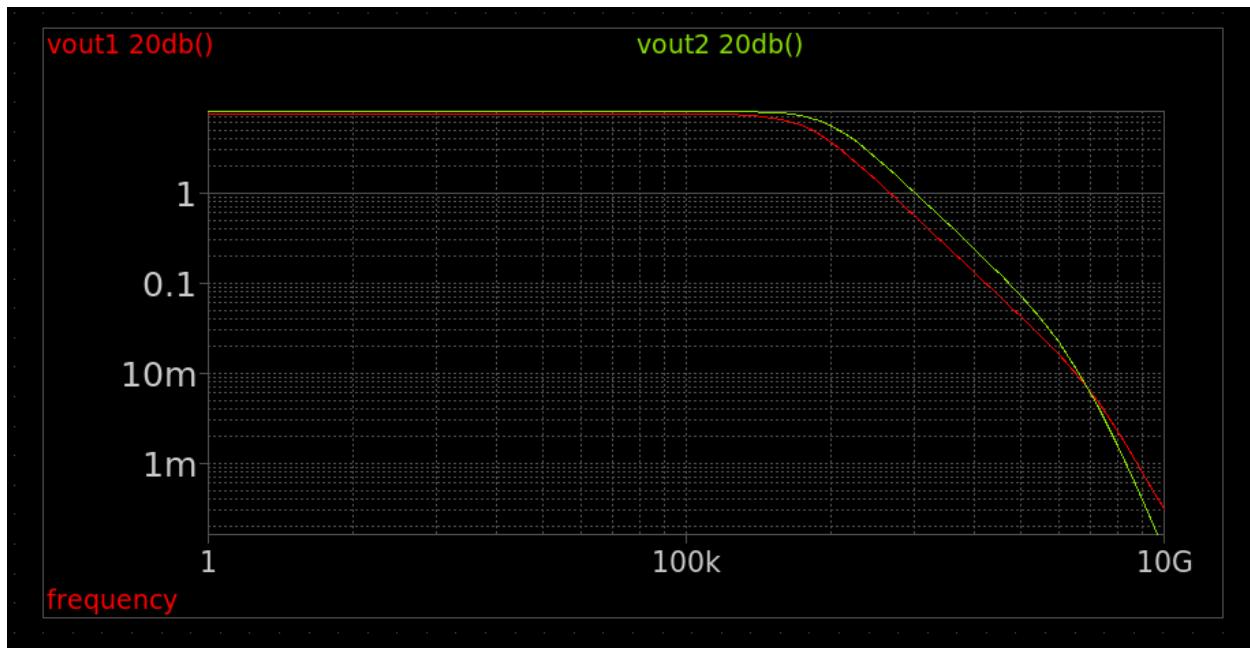
Transistor	Vds	Vds sat	Region
M0	0.95	0.157	Saturation
M1	0.46	0.156	Saturation
M2	0.55	0.158	Saturation
M3	0.455	0.55	Triode
M4	0.9	0.165	Saturation
M5	0.796	0.67	Saturation

AC analysis

DC gain, BW, GBW, and UGF

```
gain_1 = 7.493942e+00
bw_1 = 1.818028e+06
gbw_1 = 1.362420e+07
ugf_1 = 1.352979e+07
gain_2 = 8.048888e+00
bw_2 = 3.105802e+06
gbw_2 = 2.499825e+07
ugf_2 = 2.479168e+07
```

Bode plot



Hand analysis for DC gain, BW, GBW, and UGF

1. Common source

$$\text{DC gain(Common source amplifier)} = g_{m0} \left(\frac{1}{g_{ds0}} \right) // R_D$$

$$\text{DC gain(Common source amplifier)} = 1.937 \times 10^{-4} (275 // 45) \times 10^3$$

$$\text{DC gain} = 7.49$$

$$\text{BW} = \frac{1}{2\pi RC}, \quad R = 10M\Omega, \quad C = C_{gs} + C_{gd}(1 + A_V)$$

$$C = 8.78 \times 10^{-15}$$

[23-07-2025 18:05:53] - Info: [Sizing Assistant] Knob deviation (W) = 0.0%-Condition deviation (L) = 0.4%
 [24-07-2025 16:47:17] - Info: [Sizing Assistant] The resultant point 'CGS = 3.137f'
 [24-07-2025 16:50:02] - Info: [Sizing Assistant] The resultant point 'CGD = 664.1a'
 [24-07-2025 16:50:07] - Info: [Sizing Assistant] The resultant point 'CDB = 2.323f'
 [24-07-2025 16:50:11] - Info: [Sizing Assistant] The resultant point 'CSB = 2.967f'

$$\text{BW} = 1.81 \times 10^6 \text{ Hz}$$

$$\text{UGF} = \text{BW} \times A_v, \text{GBW} = \text{BW} \times A_v$$

$$\text{UGF} = 1.36 \times 10^7$$

$$\text{GBW} = 1.36 \times 10^7$$

Comment: The capacitor values obtained from Xschem simulations were found to produce inaccurate or misleading BW results.

We used ADT to calculate the values of the capacitors, which were then used in the hand analysis. These values gave a bandwidth result close to the simulation value, unlike the ones initially obtained from Xschem.

Parameter	Simulation Value	Analysis Value
DC gain	7.49	7.49
BW	1.81×10^6	1.81×10^6
GBW	1.36×10^7	1.36×10^7
UGF	1.35×10^7	1.36×10^7

2. Cascode

$$\text{DC gain(Cascode)} = R_D // r_{o2} (1 + (g_{m2} + g_{mb2}) r_{o1}) g_{m1}$$

$$\text{DC gain(Cascode)} =$$

$$(45 \times 10^3 // (194 \times 10^3 (1 + (1.93 \times 10^{-4} + 4.186 \times 10^{-5}) 205 \times 10^3))) 1.95 \times 10^{-4}$$

$$\text{DC gain (Cascode)} \approx 8.2$$

$$\text{BW} = \frac{1}{2\pi RC}, R = 10\text{M}\Omega,$$

$$C = C_{gs} + C_{gd}(1 + 1), C = 4.4652 \times 10^{-15}$$

[23-07-2025 18:05:53] - Info: [Sizing Assistant] Knob deviation (W) = 0.0%-Condition deviation (L) = 0.4%
 [24-07-2025 16:47:17] - Info: [Sizing Assistant] The resultant point 'CGS = 3.137f'
 [24-07-2025 16:50:02] - Info: [Sizing Assistant] The resultant point 'CGD = 664.1a'
 [24-07-2025 16:50:07] - Info: [Sizing Assistant] The resultant point 'CDB = 2.323f'
 [24-07-2025 16:50:11] - Info: [Sizing Assistant] The resultant point 'CSB = 2.967f'

$$\text{BW} = 3.55 \times 10^6 \text{ Hz}$$

$$\text{UGF} = \text{BW} \times A_v, \text{GBW} = \text{BW} \times A_v$$

$$\text{UGF} = 2.94 \times 10^7$$

$$\text{GBW} = 2.94 \times 10^7$$

Comment: The capacitor values obtained from Xschem simulations were found to produce inaccurate or misleading BW results.

We used ADT to calculate the values of the capacitors, which were then used in the hand analysis. These values gave a bandwidth result close to the simulation value, unlike the ones initially obtained from Xschem.

Parameter	Simulation Value	Analysis Value
DC gain	8.04	8.2
BW	3.1×10^6	3.55×10^6
GBW	2.5×10^7	2.94×10^7
UGF	2.48×10^7	2.94×10^7

Comments:

1. The bandwidth-enhanced cascode achieves gain equivalent to the common-source amplifier because the cascode transistor operates as a current buffer rather than a voltage amplifier. In this configuration, the upper transistor functions as common-gate amplifier with its gate biased at a fixed DC potential, effectively serving as a current conveyor that transfers the signal current from the input stage to the load without amplification.
2. The bandwidth-enhanced cascode demonstrates substantial superiority over the common-source amplifier due to its effective mitigation of Miller capacitance multiplication. By isolating the input transistor's drain node from the high-impedance output, the cascode C_{gd} from experiencing the full voltage swing, thereby eliminating the $C_{gd}(1 + A_V)$ Miller effect that severely constrains CS bandwidth. Additionally, the low-impedance intermediate node and improved isolation from load capacitance variations result in bandwidth improvements over the conventional CS configuration.
3. The cascode configuration achieves higher unity gain frequency due to its bandwidth advantages while maintaining equivalent DC gain, and the gain terms are comparable, the UGF improvement directly reflects the bandwidth enhancement ratio. This elevated unity gain frequency translates to superior high-frequency performance.
4. The cascode exhibits higher gain-bandwidth product performance, representing an optimal balance between DC gain preservation and AC response maximization.