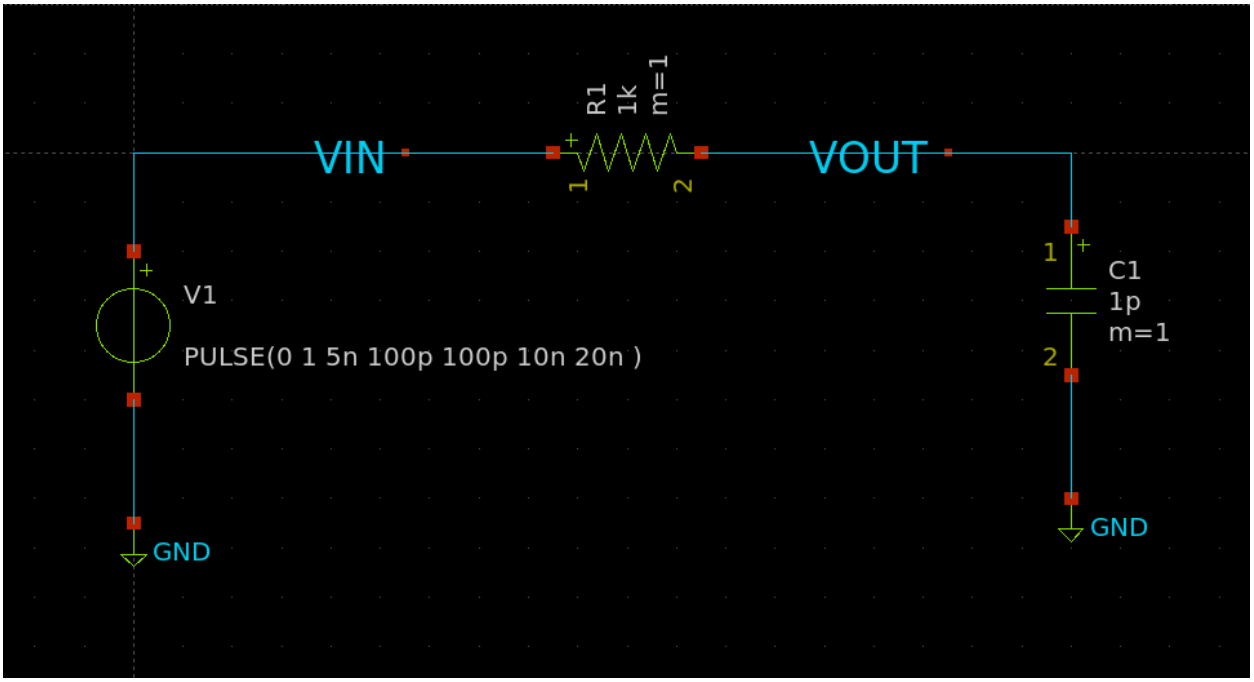
ITI
LAB1

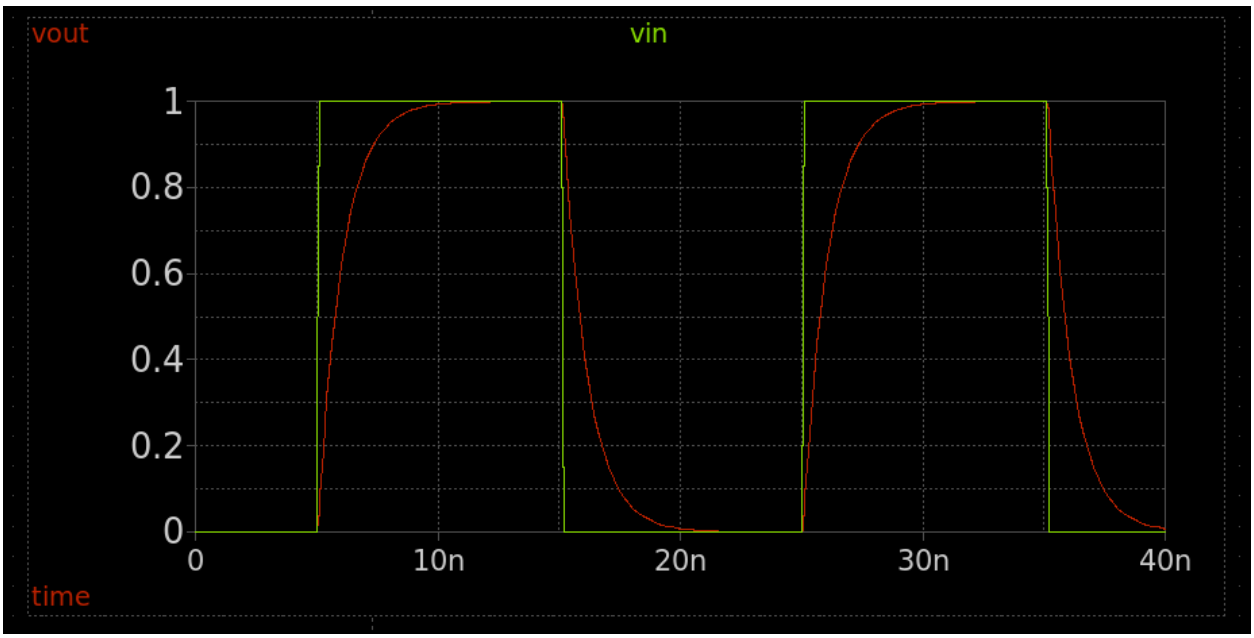
# Contents

# PART 1: Low Pass Filter Simulation (LPF)

## Design




## Transient analysis



## Rise and fall time

*Simulated results*

```
t_rise             =  2.194799e-09 targ=  7.350398e-09 trig=  5.155599e-09
t_fall             =  2.190539e-09 targ=  1.744592e-08 trig=  1.525538e-08
```

Comment : the derived expressions are

Rise time is:  .meas tran t_rise TRIG v(vout) VAL=0.1 RISE=1 TARG v(vout) VAL=0.9 RISE=1

Fall time is:  .meas tran t_fall TRIG v(vout) VAL=0.9 FALL=1 TARG v(vout) VAL=0.1 FALL=1

*Analytical Results*

Since that the value of the R is $1K\Omega$ and the time constant is $1\ ns$

the time constant = R C

then the value of the C will be $1\ pF$

$$Rise\ time \approx 2.2\ RC$$

$$Fall\ time \approx 2.2\ RC$$

From the above obtained formula the analytic value of the rise time=$2.2\ ns$

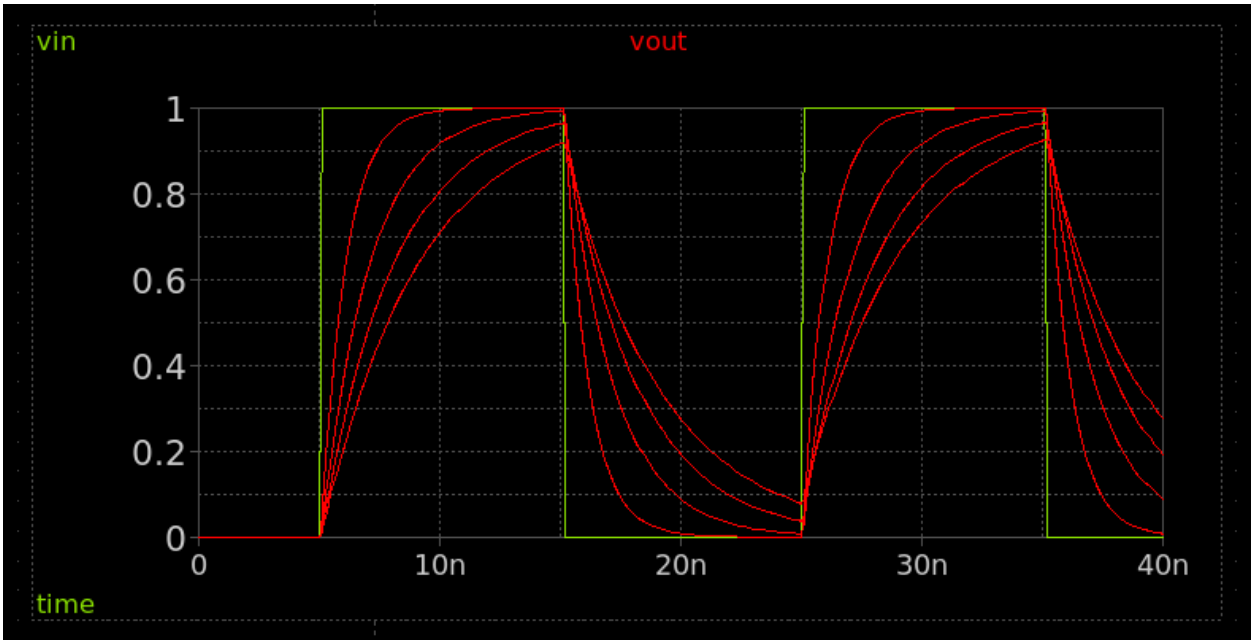
And the analytic value of the fall time=$2.2\ ns$

## Parametric sweep

tran_rise_time.txt
~/Desktop/Xscheme labs/Lab 1

```
const.r_val = 1.000000e+03
tran1.t_rise = 2.194799e-09
const.r_val = 2.000000e+03
tran2.t_rise = 4.392096e-09
const.r_val = 3.000000e+03
tran3.t_rise = 6.589698e-09
const.r_val = 4.000000e+03
tran4.t_rise = 8.787352e-09
const.r_val = 1.000000e+03
tran1.t_rise = 2.194799e-09
const.r_val = 2.000000e+03
tran2.t_rise = 4.392096e-09
const.r_val = 3.000000e+03
tran3.t_rise = 6.589698e-09
const.r_val = 4.000000e+03
tran4.t_rise = 8.787352e-09
const.r_val = 1.000000e+03
tran1.t_rise = 2.194799e-09
const.r_val = 2.000000e+03
tran2.t_rise = 4.392096e-09
const.r_val = 3.000000e+03
tran3.t_rise = 6.589698e-09
```

Comment: As observed from the transient analysis, increasing the resistance R leads to a corresponding increase in both the rise time and fall time of the output waveform. This behavior is expected in a first-order RC low-pass filter, where the time constant $\tau = RC$ governs the rate of charging and discharging of the capacitor. A larger R results in a larger time constant, thus slowing down the circuit's response to input transitions.

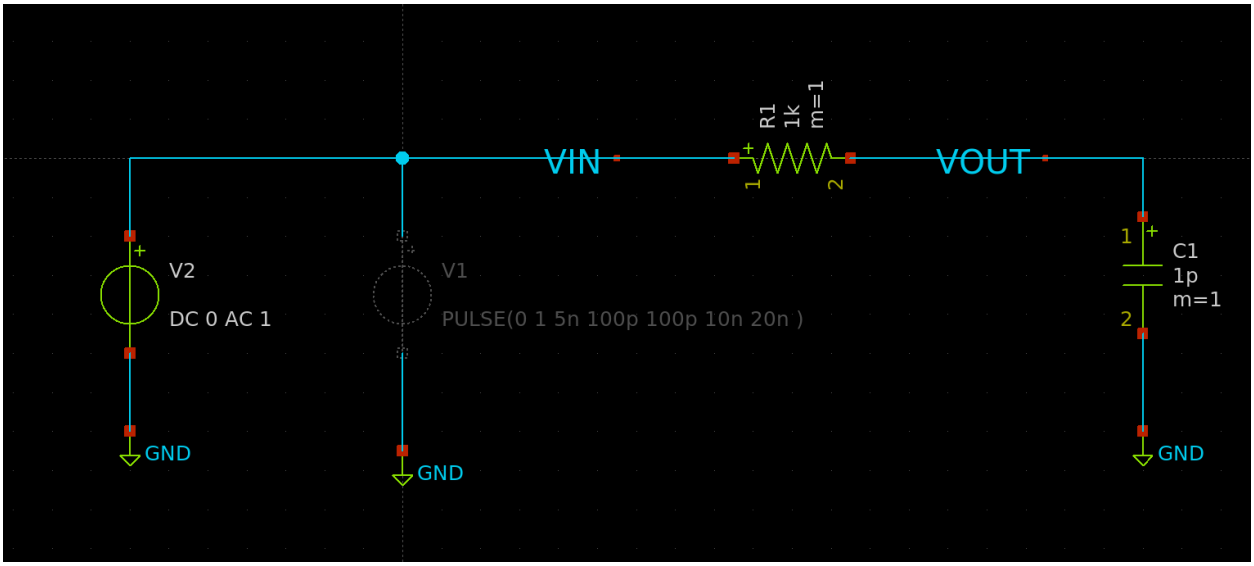



Comment: As the resistance R increases, the output voltage becomes smoother and exhibits slower transitions in response to the input signal. This is due to the increase in the RC time constant, which causes the circuit to filter out high-frequency components more effectively. As a result, the output waveform becomes more delayed and less sharp, demonstrating the low-pass filtering behavior of the circuit.

# AC analysis

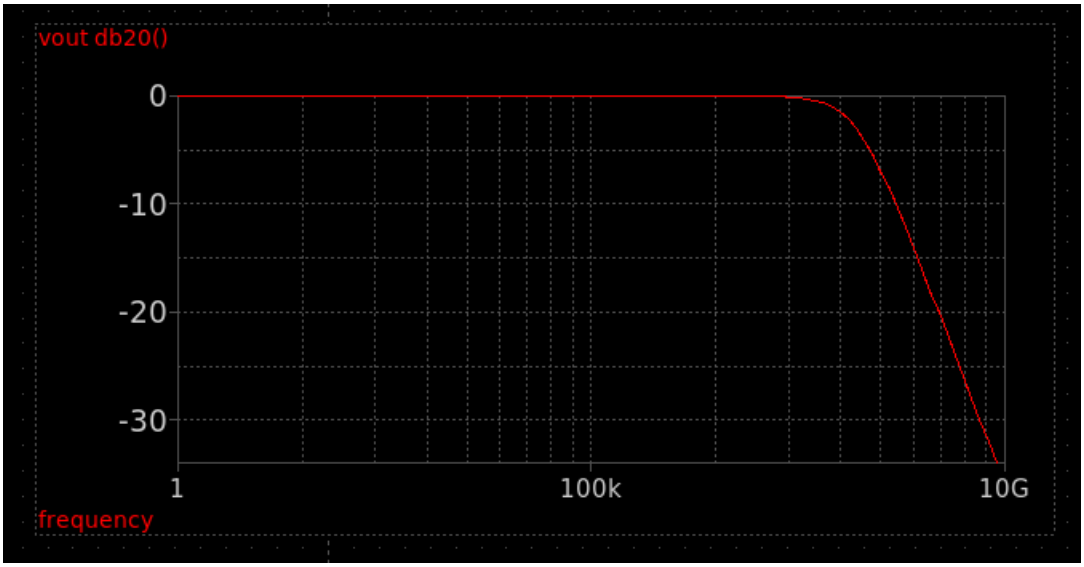
## Design

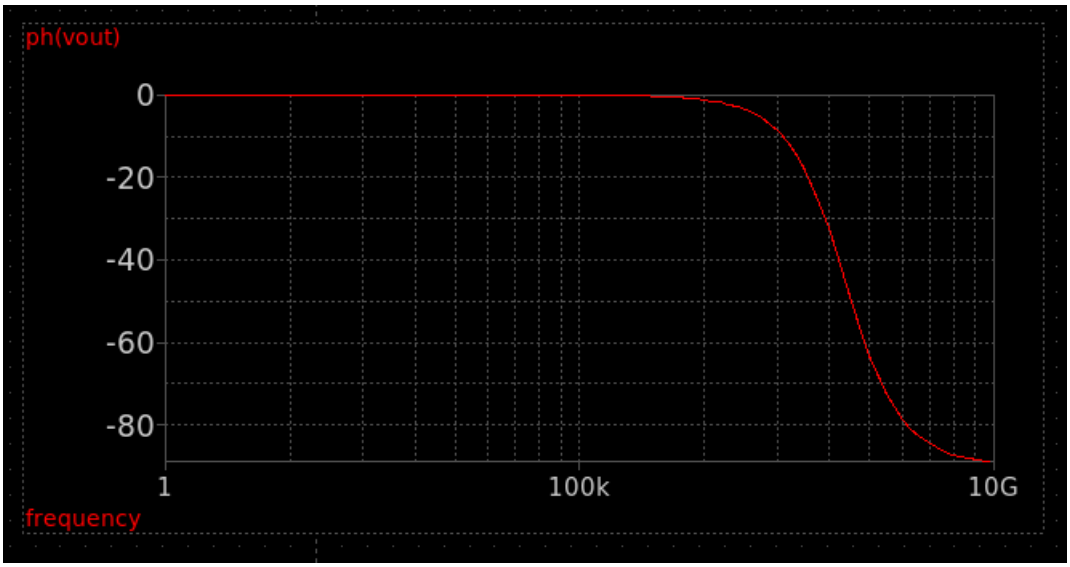
In order to be able to do the AC analysis we need to replace the square wave voltage source by an ac source of voltage 1v
so the circuits design will be




## Bode Plot (Magnitude and phase)

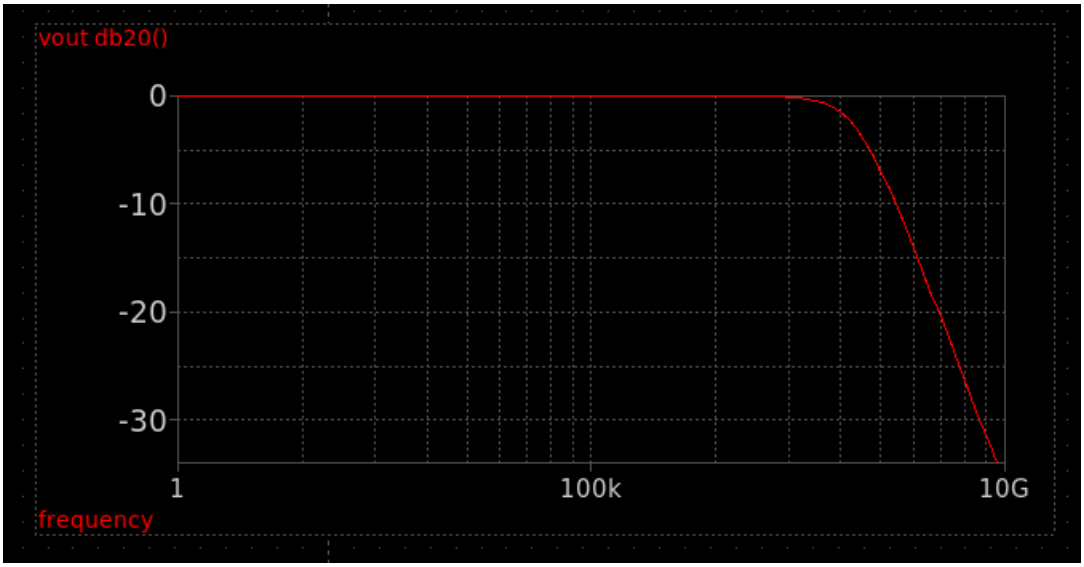
At R=1$K\Omega$






Comment: The Bode plot confirms that the circuit is functioning correctly as a first-order low-pass filter. The magnitude response shows a flat gain at low frequencies, followed by a steady roll-off beyond the cutoff frequency, which is characteristic of such filters. The phase response also exhibits the expected behavior, transitioning smoothly from 0° to −90° as frequency increases. This validates that the circuit effectively attenuates high-frequency components while allowing low-frequency signals to pass with minimal distortion, thus confirming its intended filtering behavior.

## DC gain




Comment: At low frequencies, including DC, the capacitor in the RC low-pass filter behaves as an open circuit, allowing the full input signal to appear across the output resistor. This results in a DC gain of 1, meaning the circuit passes low-frequency signals without attenuation. As the frequency increases, the capacitive reactance decreases, and the capacitor begins to shunt more

of the input signal to ground. This causes the gain to drop significantly. The frequency at which the gain falls to 70.7% of its maximum value (or drops by 3 dB) is known as the cutoff frequency or −3 dB point. Beyond this point, the circuit increasingly attenuates higher frequencies, confirming its low-pass filtering behavior.

## 3-dB bandwidth

```
max_gain              =  1.000000e+00 at=  1.584893e+00
bw                    =  1.592554e+08
```

$$f_{3-dB} = \frac{1}{2\pi RC}$$

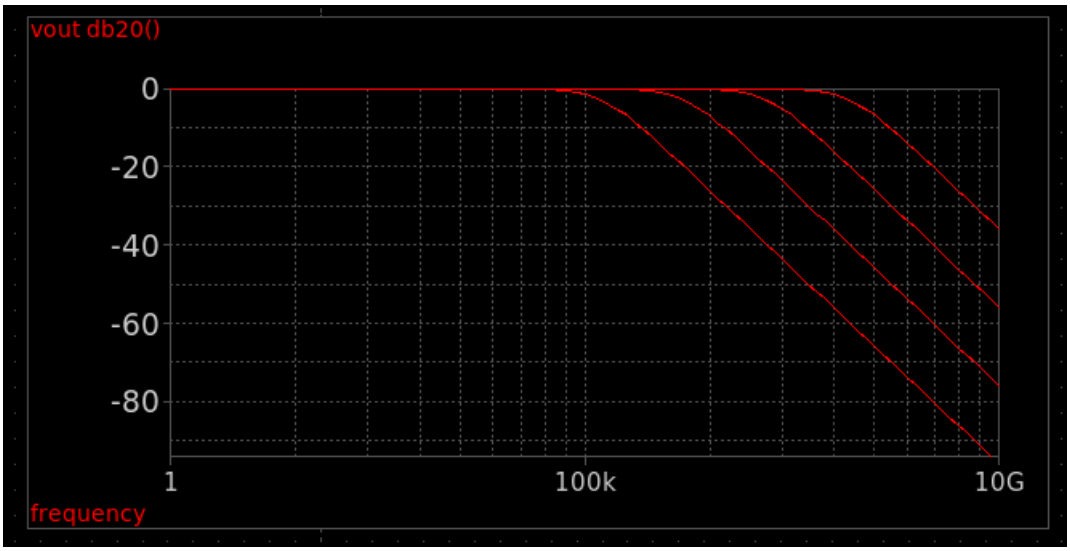
$$f_{3-dB} = \frac{1}{2\pi \times 1000 \times 1 \times 10^{-12}}$$

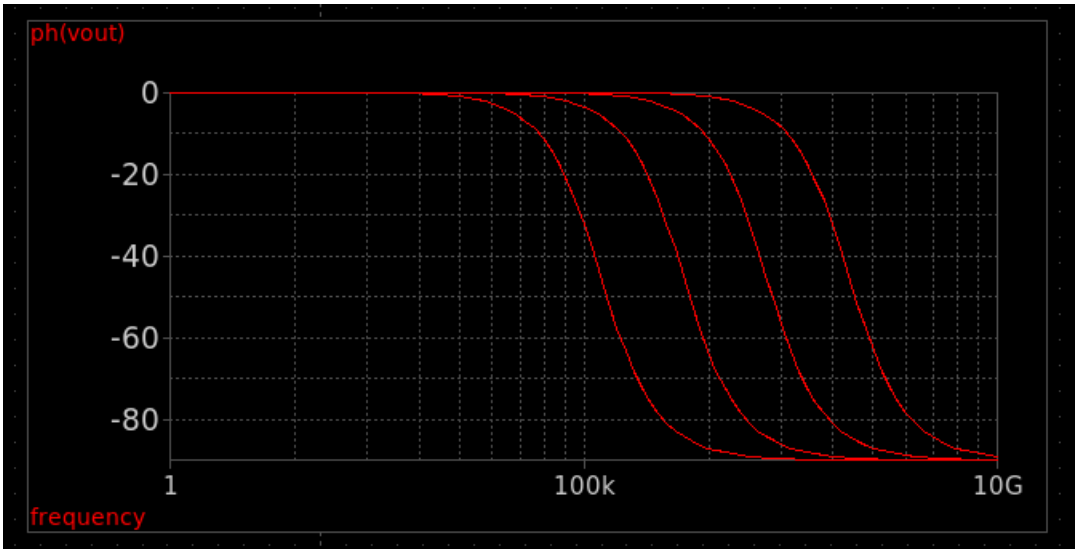
$$f_{3-dB} = 159.155\ MHz$$

Parametric sweep

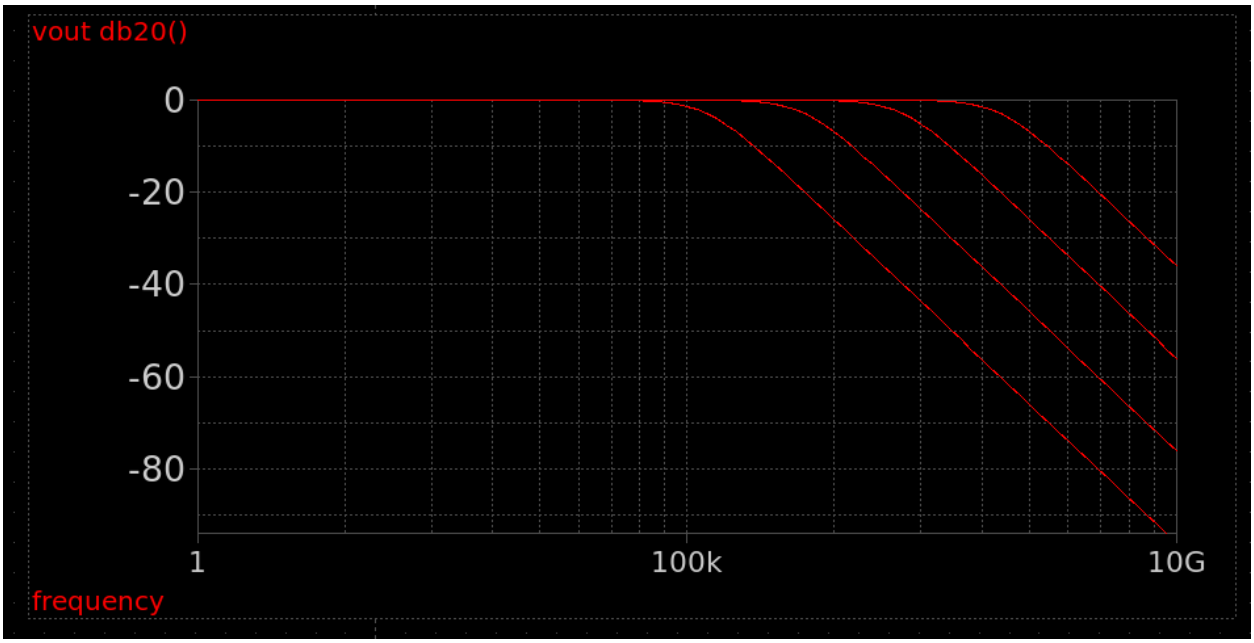
```
No. of Data Rows : 101
max_gain            =  1.000000e+00 at=  1.584893e+00
bw                  =  1.592554e+08
page: no such command available in ngspice
binary raw file "rc_ckt_2.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 101
max_gain            =  1.000000e+00 at=  1.000000e+00
bw                  =  1.592554e+07
page: no such command available in ngspice
binary raw file "rc_ckt_2.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 101
max_gain            =  1.000000e+00 at=  1.000000e+00
bw                  =  1.592554e+06
page: no such command available in ngspice
binary raw file "rc_ckt_2.raw"
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


No. of Data Rows : 101
max_gain            =  1.000000e+00 at=  1.000000e+00
bw                  =  1.592554e+05
```

Comment: The parametric analysis shows that as the resistance R increases, the 3 dB bandwidth of the circuit decreases. This inverse relationship is expected for a first-order RC low-pass filter, where the cutoff frequency $f_{3-dB} = \frac{1}{2\pi RC}$. A larger resistance increases the time constant $\tau = RC$ , causing the filter to respond more slowly and attenuate higher frequencies more aggressively. As a result, the circuit allows a narrower range of frequencies to pass, confirming the reduced bandwidth. This behavior is consistent with the theoretical model and highlights the trade-off between filtering strength and signal bandwidth.



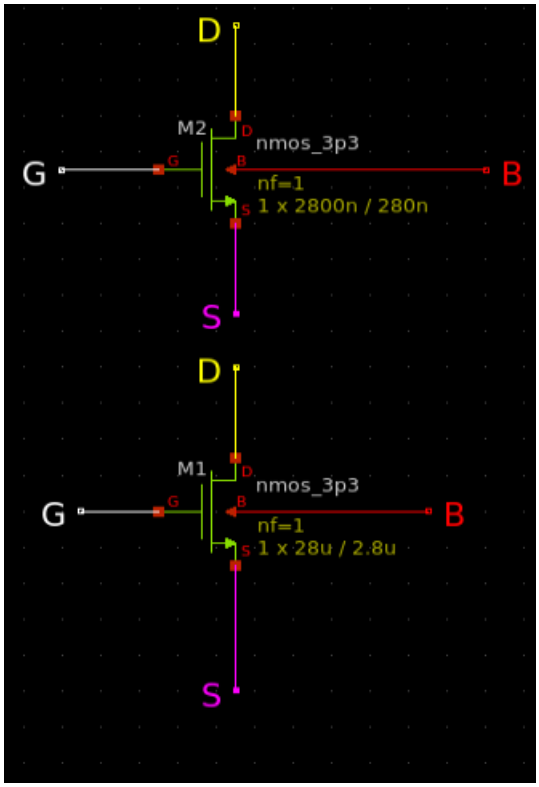

Comment: As resistance R increases, the waveform responds more slowly, with delayed rise and fall transitions. The general shape of the waveform remains the same, but the output takes longer to reach its high and low values. This is due to the increase in the RC time constant, which slows down the charging and discharging of the capacitor. As a result, the circuit introduces more delay in signal response, demonstrating the expected behavior of a low-pass filter with increasing resistance.



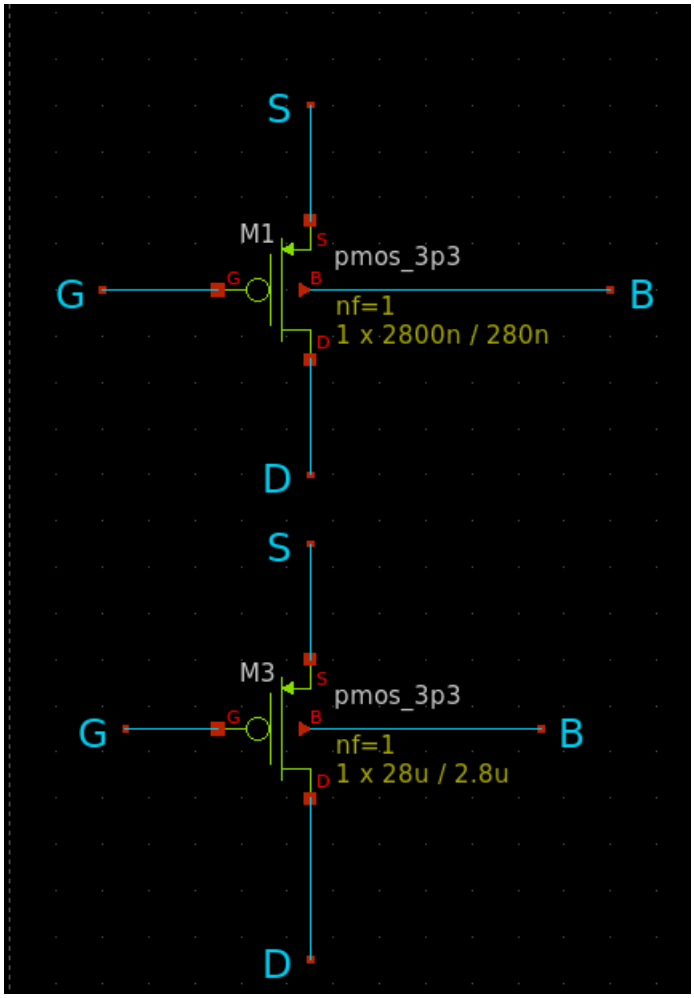

Comment: The analysis of DC gain across different resistance values shows that at low frequencies, including DC, the gain remains approximately constant and equal to 1, regardless of the resistance value. This is because, at very low frequencies, the capacitor behaves like an open circuit, and the output simply follows the input. However, as the frequency increases, the capacitive reactance decreases, allowing more current to bypass the output resistor through the capacitor. This effect becomes more pronounced at higher frequencies, causing the gain to drop. For higher resistance values, the drop in gain occurs at lower frequencies (i.e., the cutoff frequency shifts left), resulting in lower gain at a given frequency beyond the cutoff. Conversely, for lower resistance values, the circuit maintains higher gain over a broader frequency range before it starts to attenuate. This shift is due to the fact that the cutoff frequency is inversely proportional to R, so increasing R reduces the frequency range over which the circuit passes signals without attenuation.

# Part2 : MOSFET Characteristics

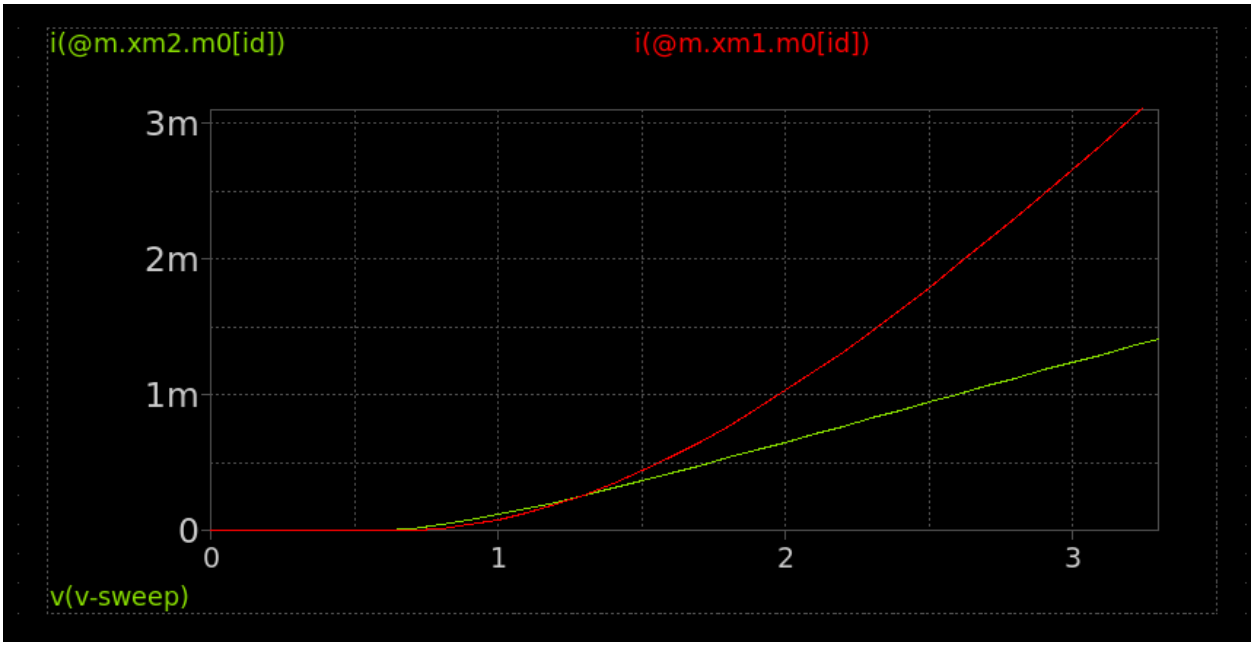
## Design(NMOS)



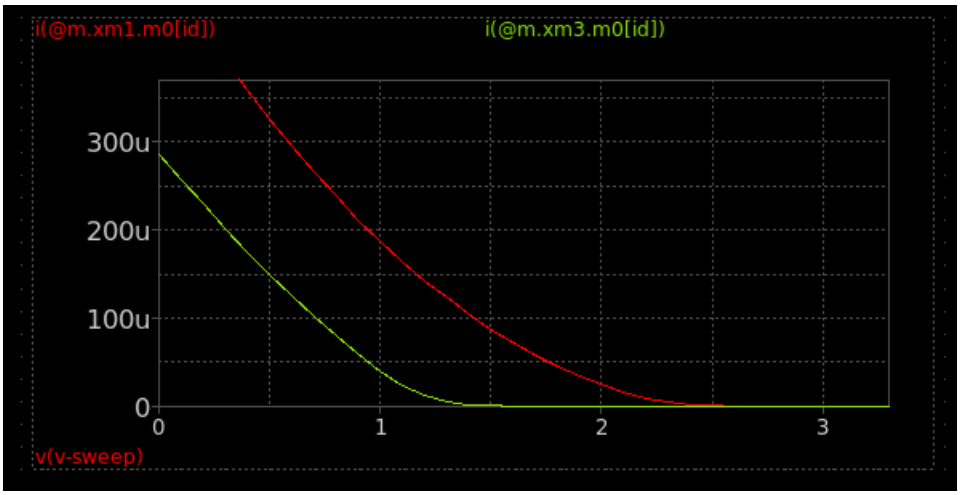
Design(PMOS)


S
M1
S
pmos_3p3
G
G
B
B
nf=1
D
1 x 2800n / 280n
D
S
M3
S
pmos_3p3
G
G
B
B
nf=1
D
1 x 28u / 2.8u
D

## ID vs Vgs(NMOS)




## ID vs Vgs(PMOS)




2) The long-channel device exhibits higher drain current in saturation. This is because it adheres

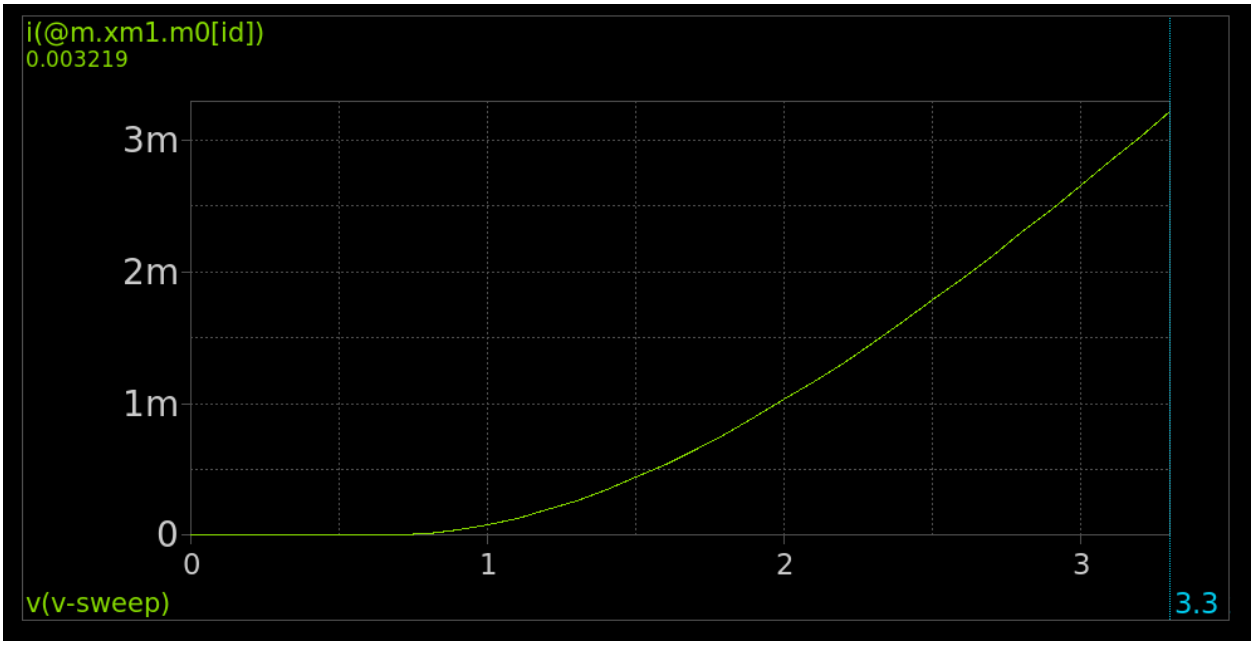
- closely to the ideal square-law behavior and experiences less velocity saturation and weaker channel length modulation (CLM).
  In contrast, short-channel devices suffer from velocity saturation, where carriers reach a maximum drift velocity and current no longer increases significantly with increasing Vov. As a result, the current is often lower than that predicted by the square law, despite the same W/L ratio. Additionally, stronger CLM in short-channel devices reduces output resistance, which may further reduce effective current.

- In long-channel devices, the ID-Vov relationship is quadratic, following the classic square-law model: $ID\ \alpha\ \frac{W}{L}Vov^2$
  However, in short-channel devices, due to velocity saturation, the current exhibits a more linear dependence on Vov : $ID\ \alpha\ Vov^{\gamma}\ where\ \gamma < 2$

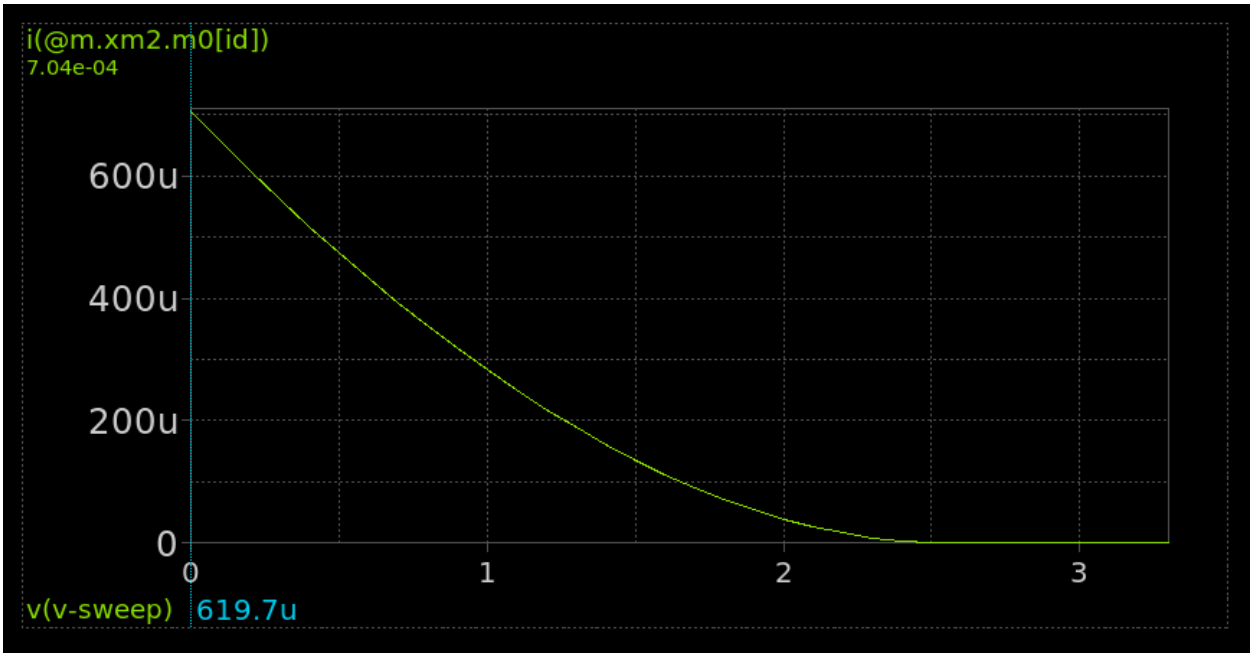
3)

- NMOS transistors typically conduct higher current than PMOS transistors for the same overdrive voltage and dimensions. This is because electrons (NMOS carriers) have higher mobility than holes (PMOS carriers) roughly 4 to 5 times greater in standard CMOS processes. As a result, NMOS devices have a higher drain current (ID) under the same Vgs.
  (Long_channel)

NMOS



PMOS

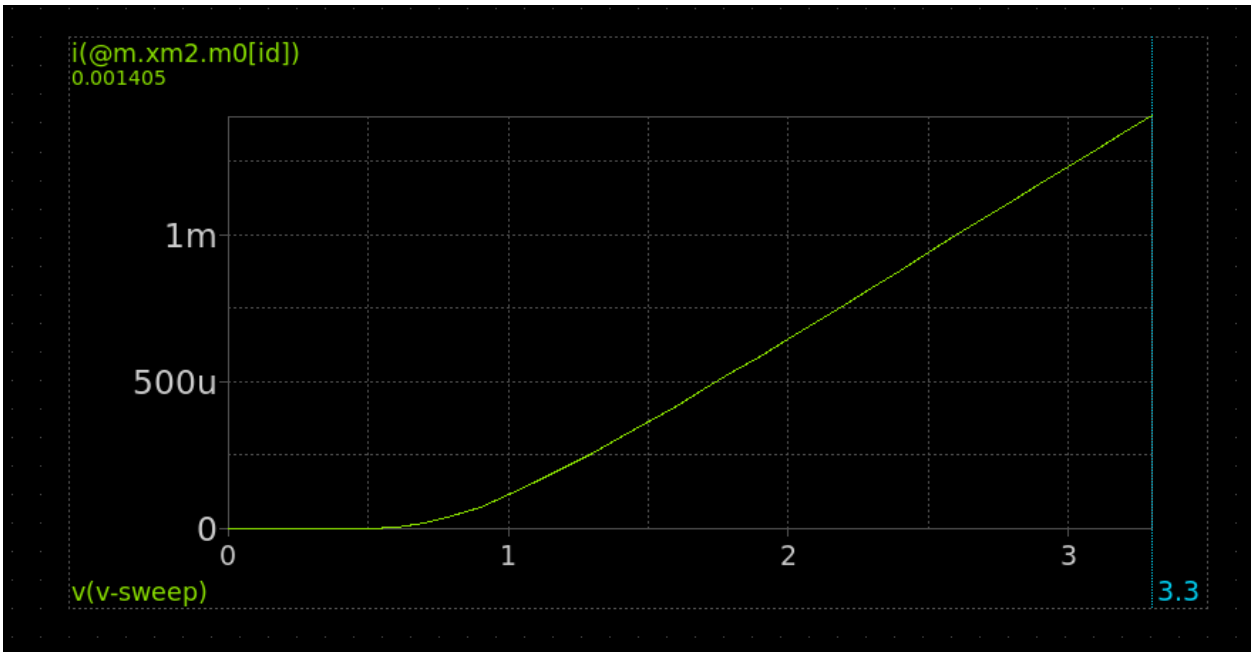



From the graphs

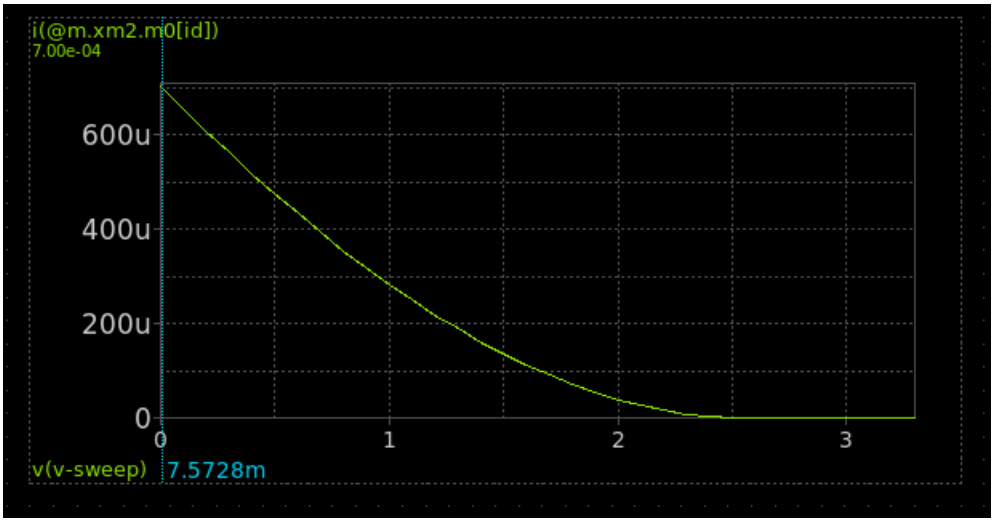
$$\frac{I_{nmos}}{I_{pmos}} = 4.57$$

(Short length)

(NMOS)



(PMOS)



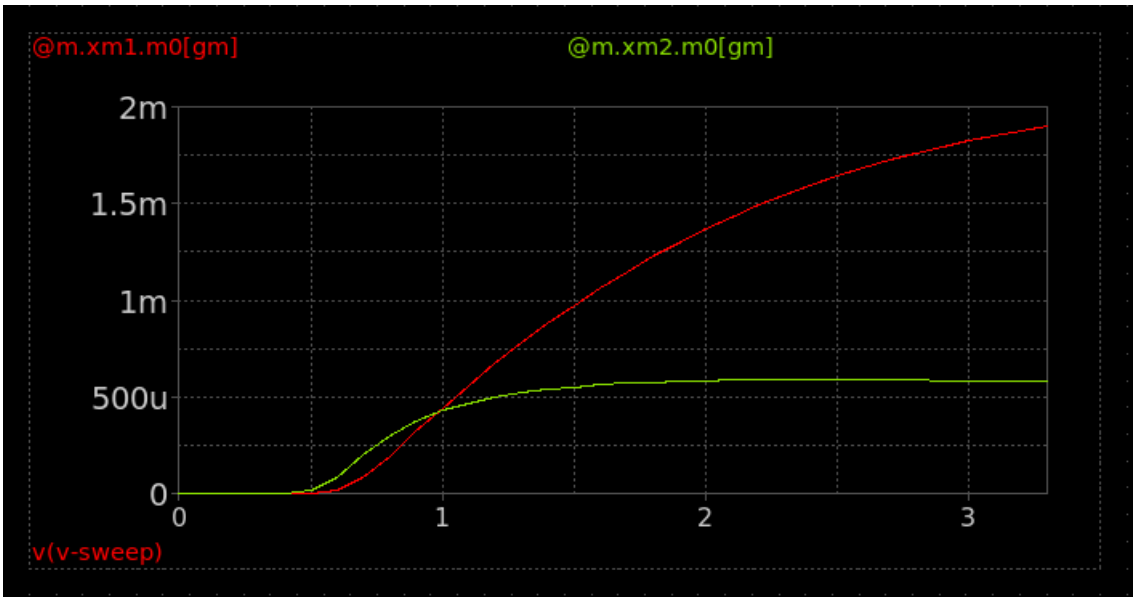

From the graphs

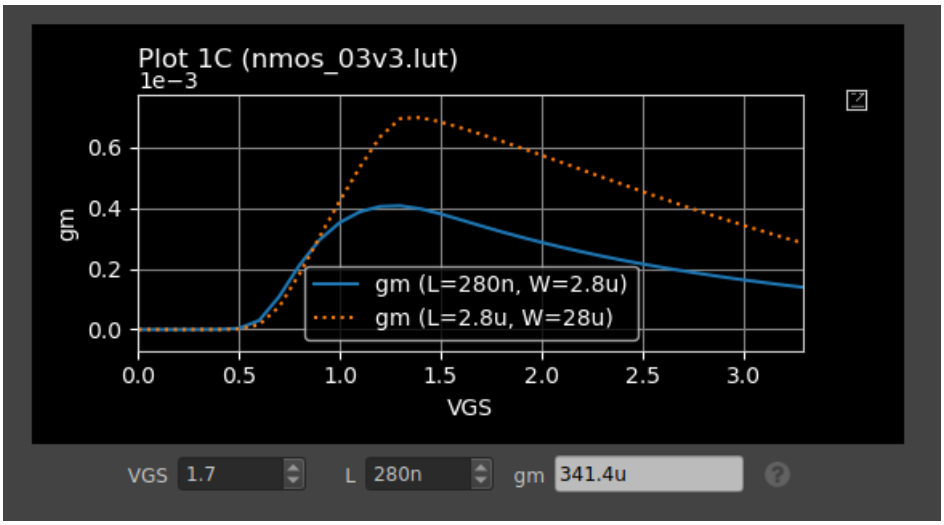
$$\frac{I_{nmos}}{I_{pmos}} = 2$$

Note: The PMOS readings were taken with the gate voltage starting at 0V (instead of 3.3V) because I initially used the same connection setup as the NMOS. As a result, the PMOS terminals were effectively reversed compared to the standard PMOS biasing (i.e., source and drain connected similarly to the NMOS case). This led to the PMOS being measured in an inverted configuration, with the gate sweep starting from 0V rather than from VDD.

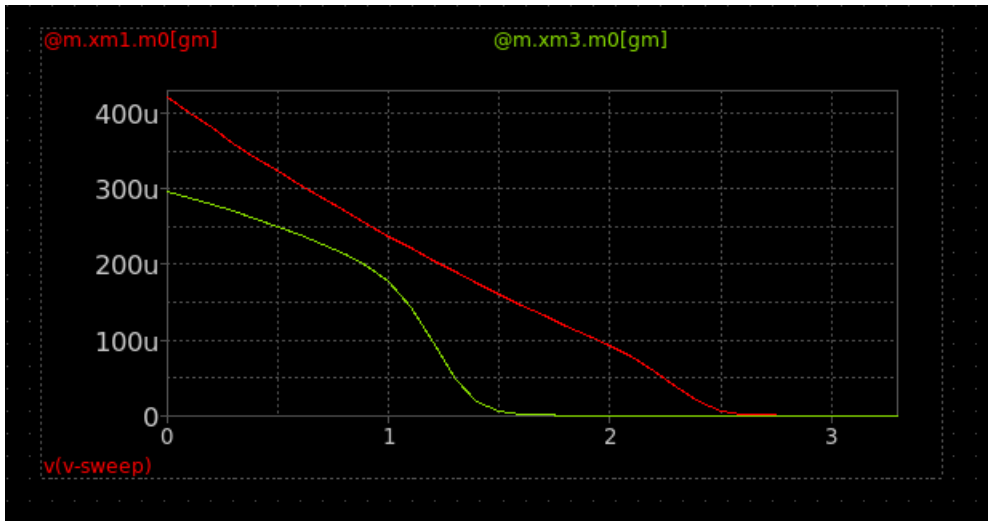
- MOS transistors tend to be more sensitive to short-channel effects. As channel length decreases, PMOS devices show a more noticeable deviation from ideal behavior, such as less predictable threshold voltage and reduced control by the gate. This is largely due to the lower hole mobility, which limits the current.

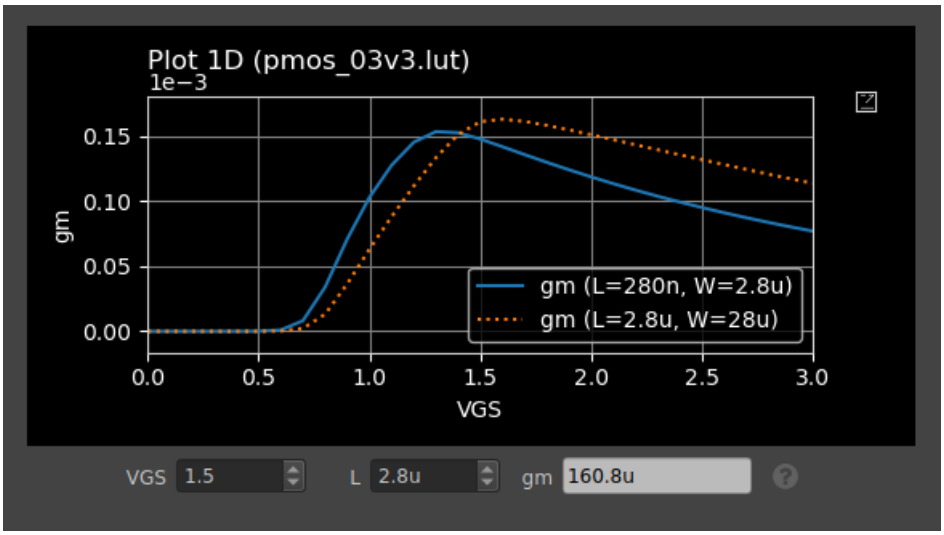
## $g_m$ *vs* $Vgs$(NMOS)



## $g_m$ *vs* $Vgs$(PMOS)



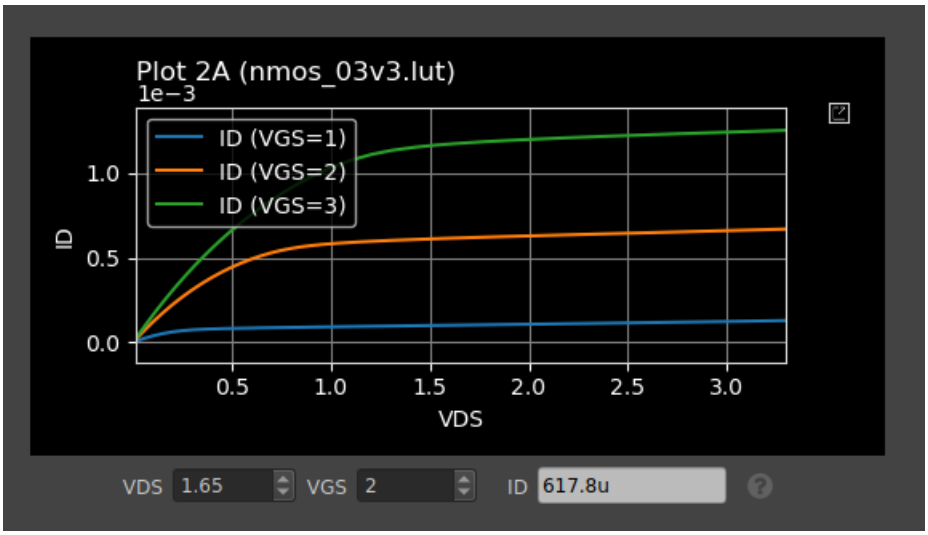




- For the long-channel device, $g_m$ initially increases approximately linearly with Vgs because it follows the square-law model: Since $ID\ \alpha\ (Vgs - Vt)^2$,
  Then $g_m\ \alpha\ (Vgs - Vt)$
- The increase in $g_m$ with Vgs is sub-linear, meaning it rises more slowly compared to the ideal case. This behavior is primarily due to velocity saturation: as the electric field in the channel increases with higher Vgs, the carrier velocity approaches a maximum limit and stops increasing proportionally. As a result, the drain current ID grows more slowly, and since $g_m = \frac{dI_D}{dVgs}$, the transconductance curve begins to flatten out at higher Vgs. This

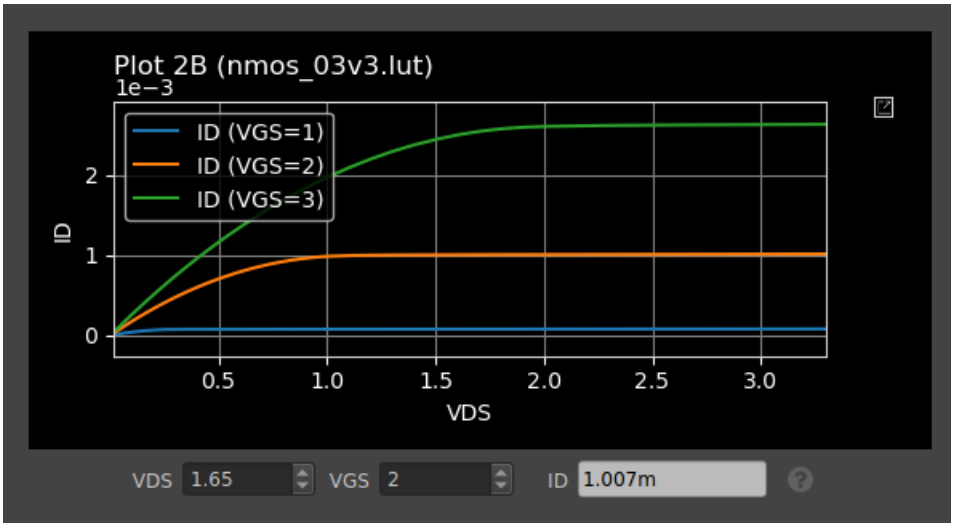
leads to an early saturation in $g_m$ which is a typical short-channel effect not present in longer-channel devices.

## ID vs Vds(NMOS)

Short channel

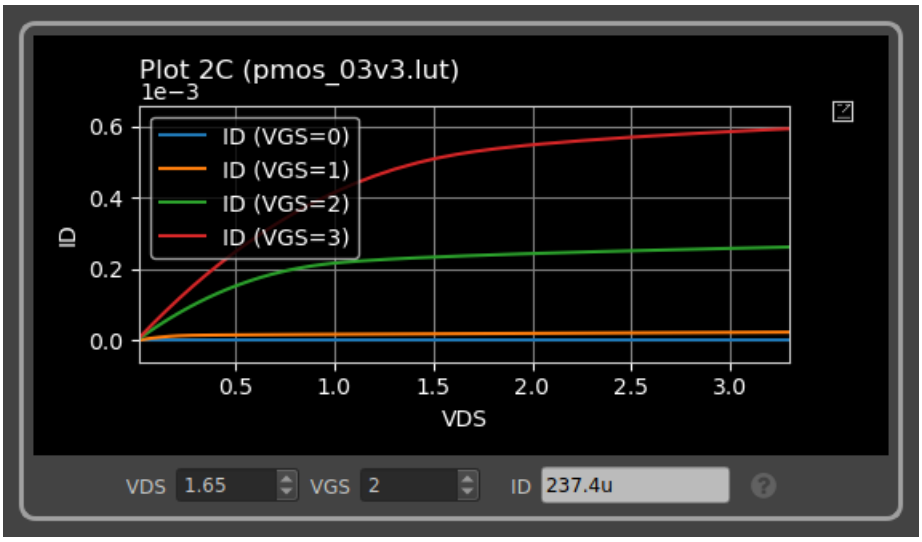



Long channel

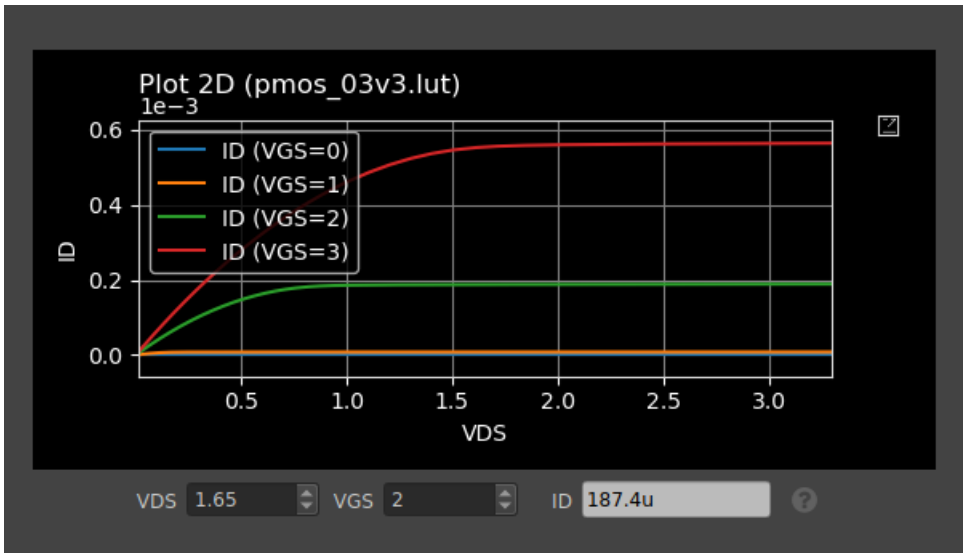


# ID vs Vds(PMOS)

Short chanel




Long channel



- The long-channel device typically exhibits higher drain current in the saturation region for the same Vgs and $\frac{W}{L}$ ratio. This is because long-channel devices follow the ideal square-law model, where current continues to rise smoothly with increasing Vds before saturating, with less impact from short-channel effects such as velocity saturation.
  In contrast, short-channel devices suffer from early velocity saturation, which limits the increase in carrier velocity. As a result, the current tends to saturate earlier and at a lower value compared to the long-channel.
- The short-channel device has a slightly higher slope in the saturation region, meaning its ID still increases more noticeably with Vds, even after saturation. This is due to stronger channel length modulation, which is more prominent in short-channel devices. In MOSFET terms, this corresponds to a lower output resistance $r_o$ and thus a larger $\lambda$.
  On the other hand, long-channel devices exhibit a flatter saturation region, indicating weaker CLM and thus better current saturation behavior, which is desirable in analog applications.