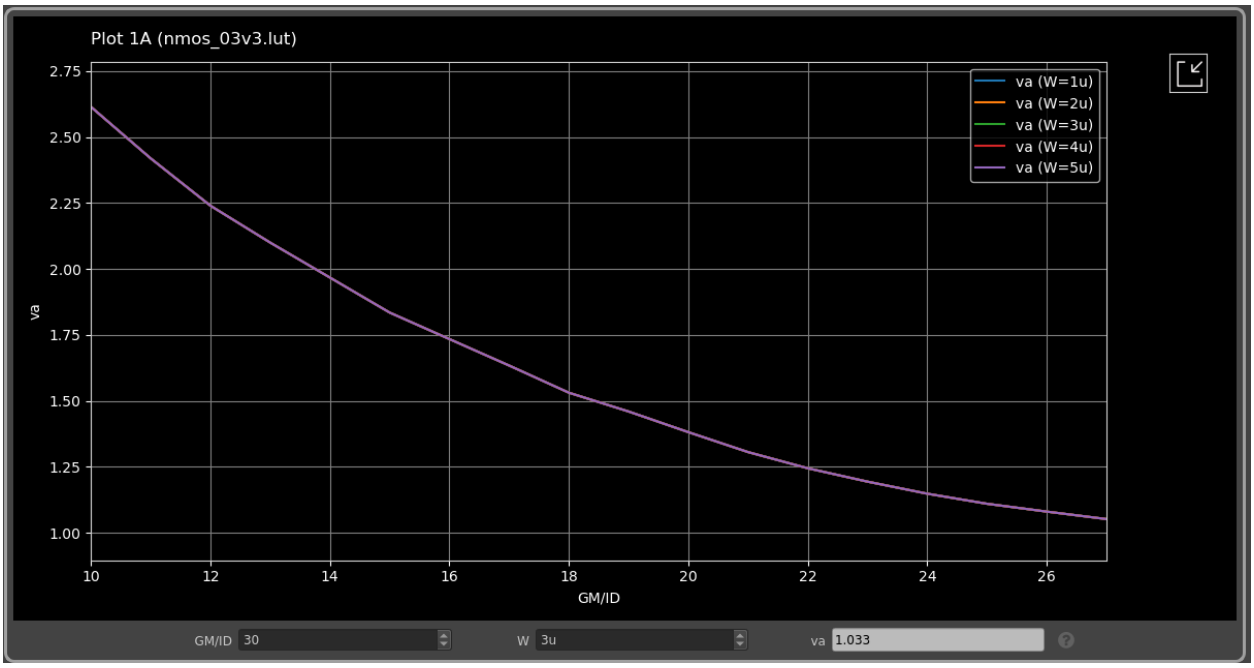
ITI
LAB11
Fully-Differential Folded Cascode OTA

Contents

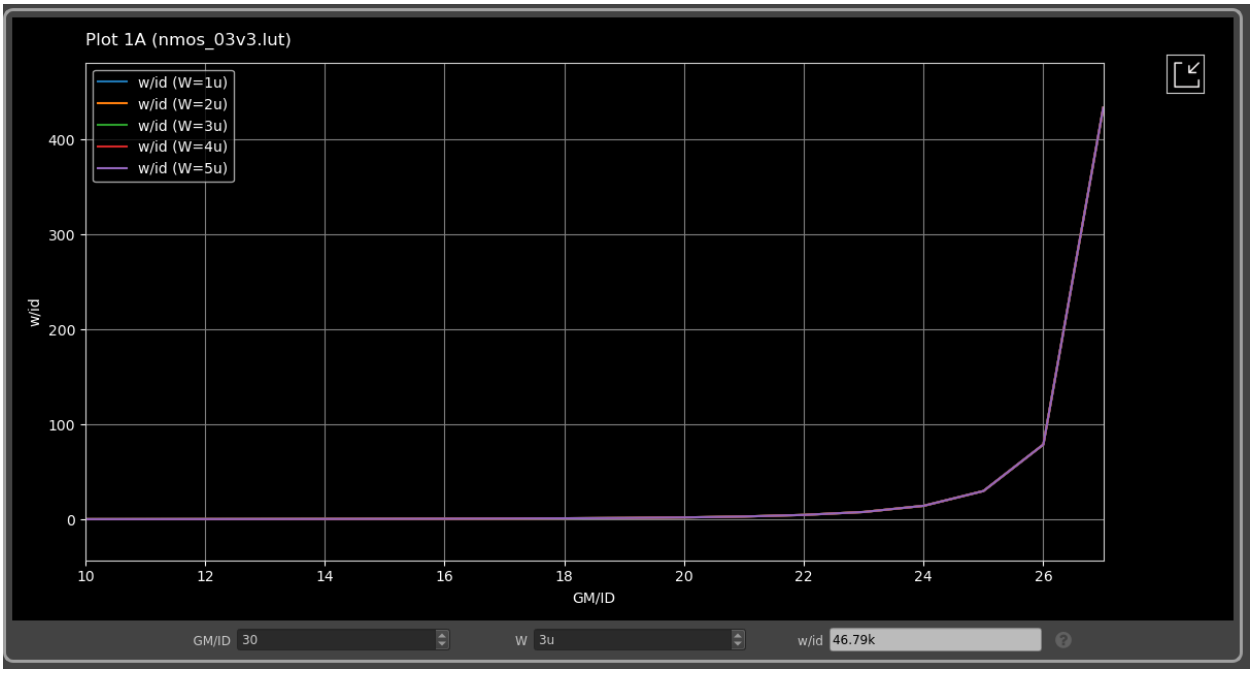
PART 1: gm/ID Design Charts

NMOS

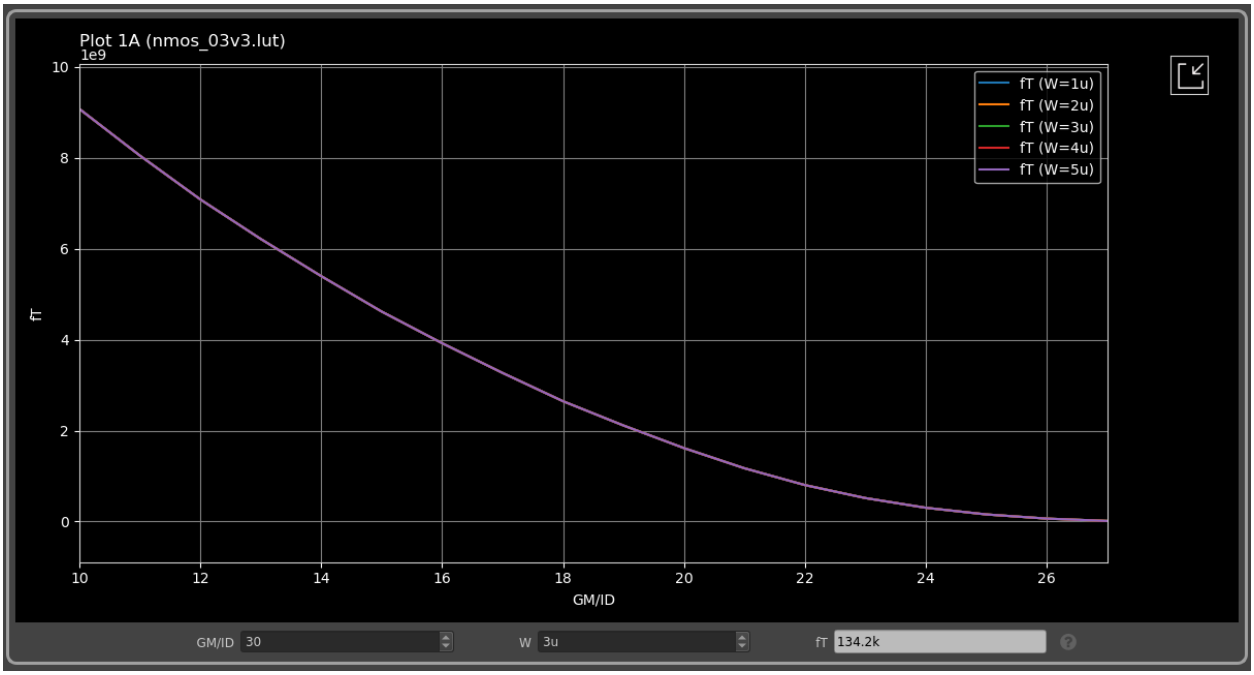
VA



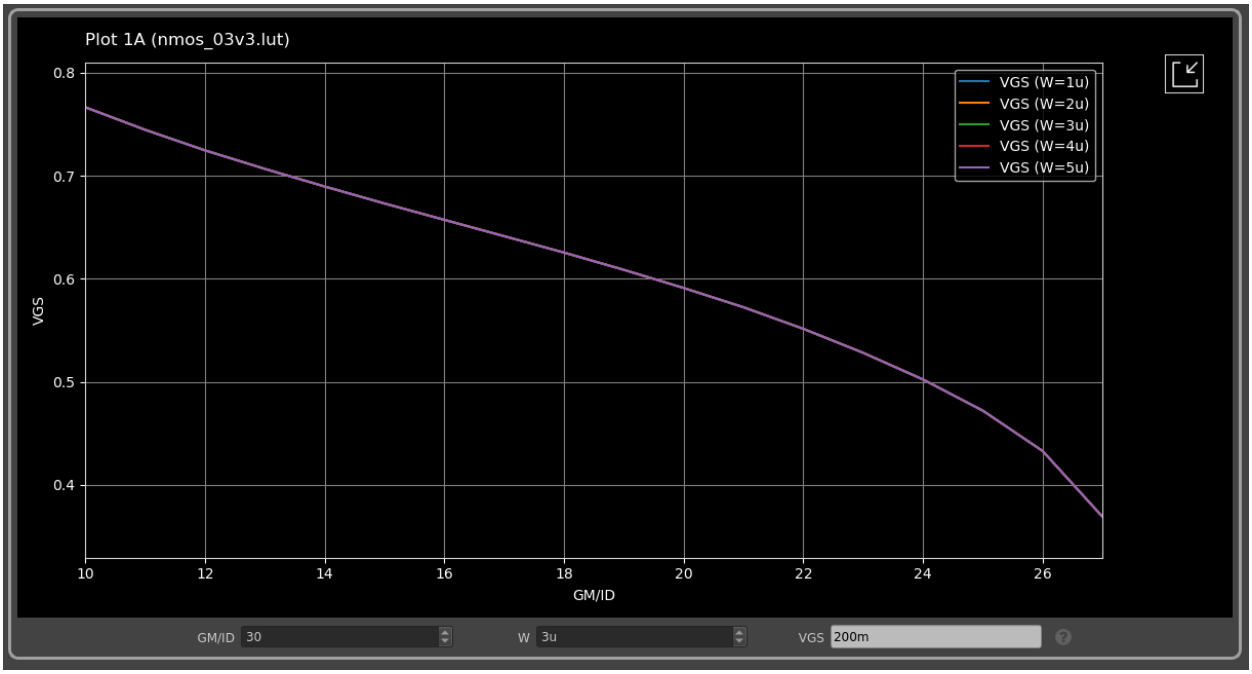
W/ID



fT

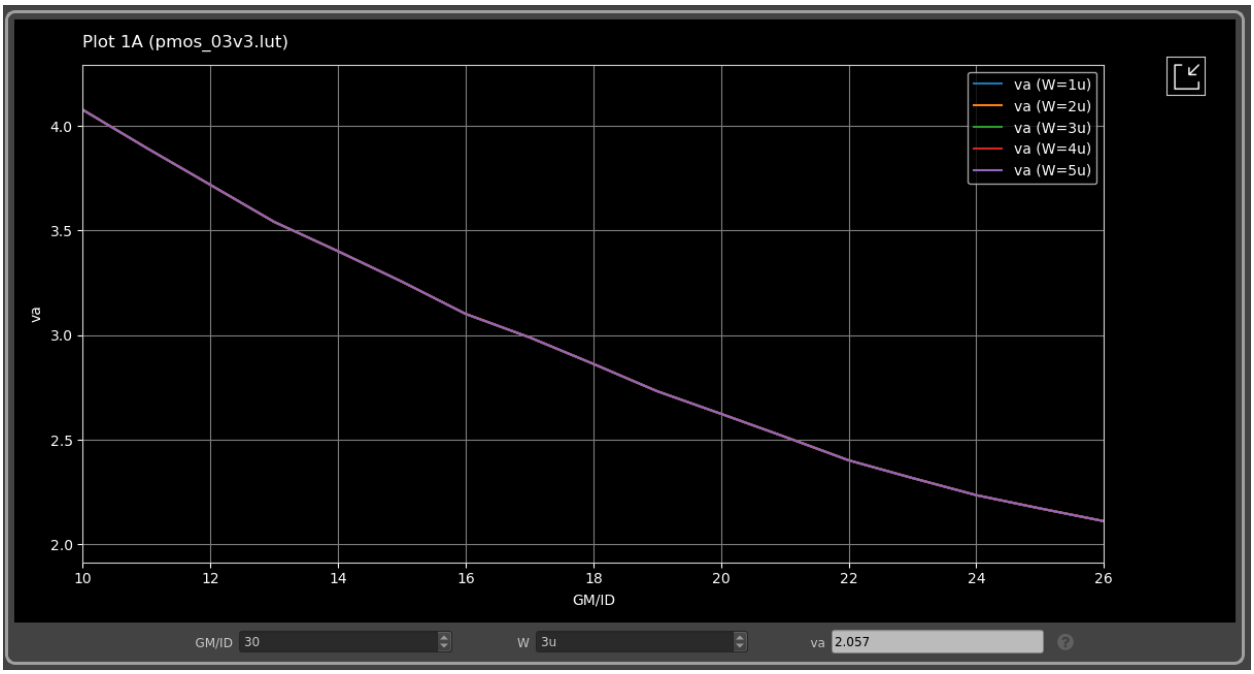

Plot 1A (nmos_03v3.lut)
1e9
fT (W=1u)
fT (W=2u)
fT (W=3u)
fT (W=4u)
fT (W=5u)
fT
GM/ID
GM/ID 30
W 3u
fT 134.2k

VGS

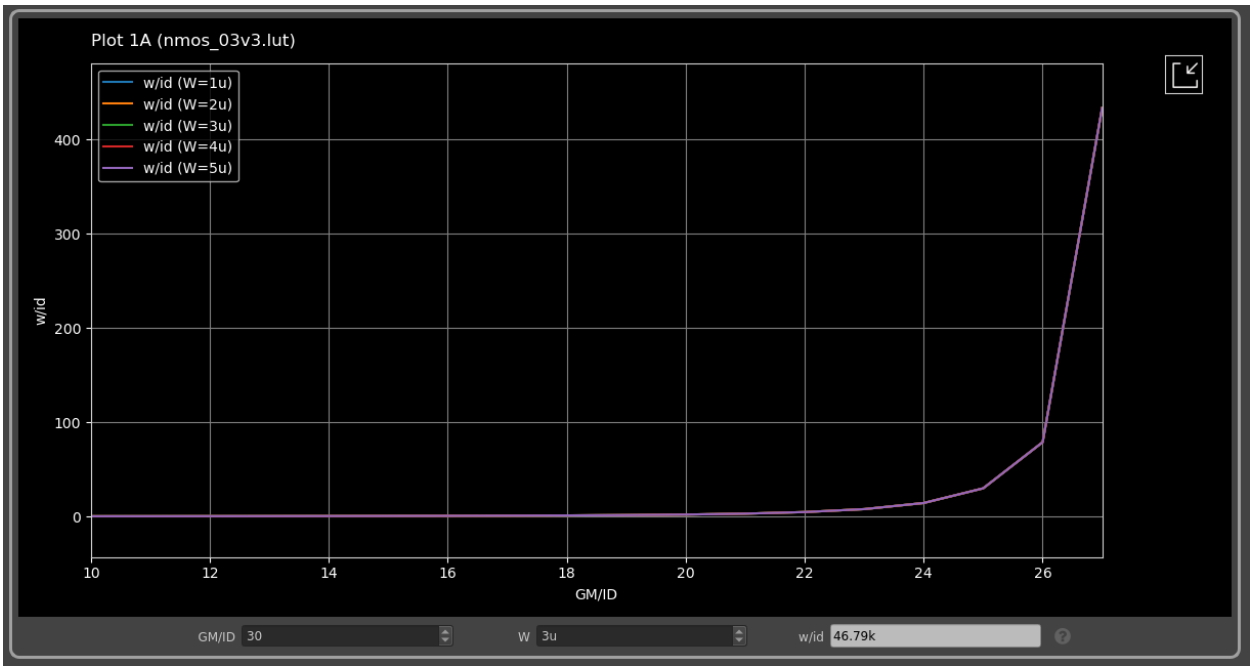

Plot 1A (nmos_03v3.lut)
VGS (W=1u)
VGS (W=2u)
VGS (W=3u)
VGS (W=4u)
VGS (W=5u)
VGS
GM/ID
GM/ID 30
W 3u
VGS 200m

PMOS

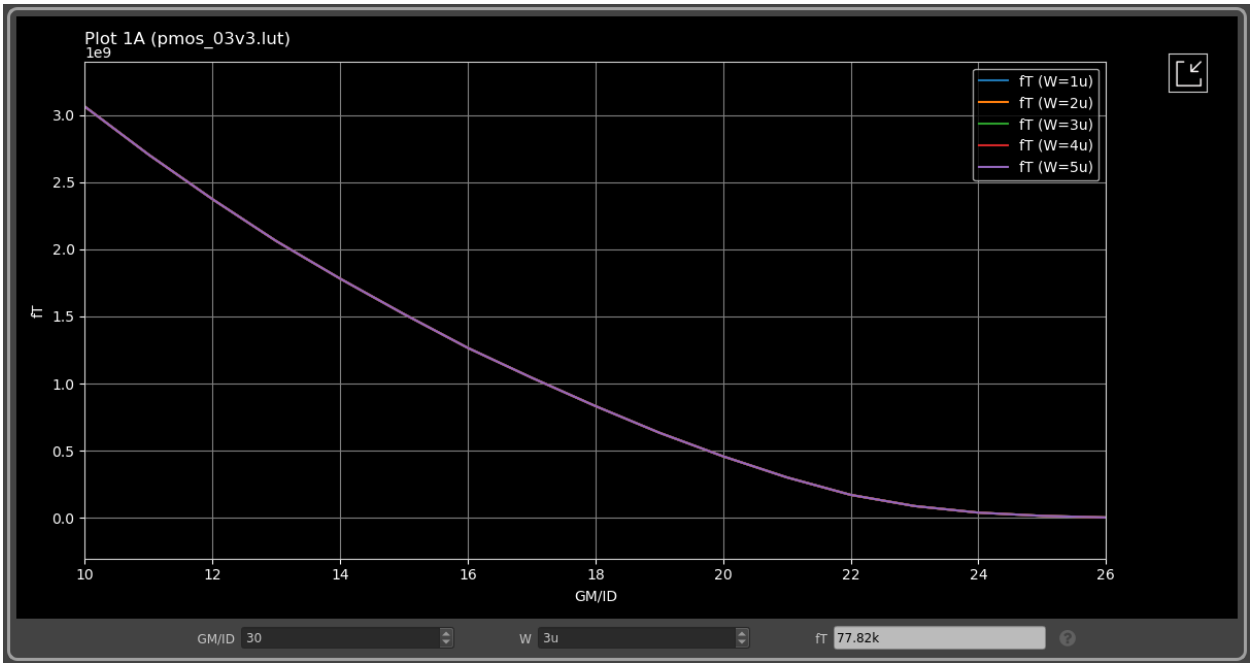
VA


Plot 1A (pmos_03v3.lut)
va (W=1u)
va (W=2u)
va (W=3u)
va (W=4u)
va (W=5u)
va
GM/ID
GM/ID 30
W 3u
va 2.057

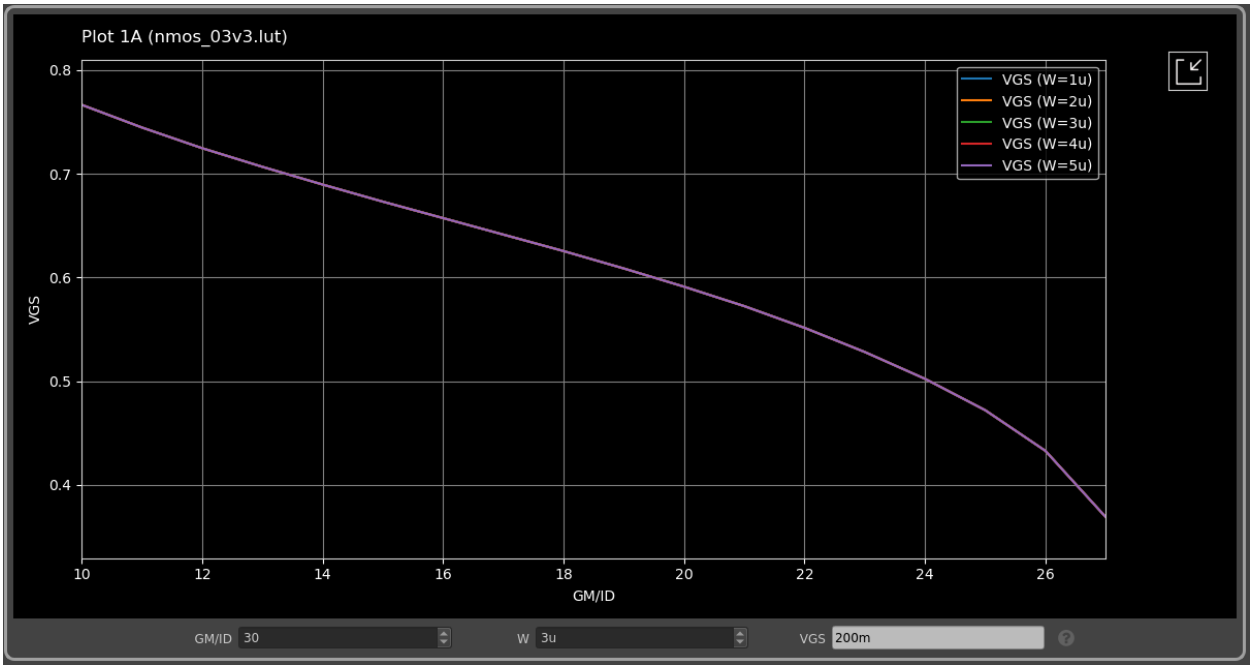
W/ID


Plot 1A (nmos_03v3.lut)
w/id (W=1u)
w/id (W=2u)
w/id (W=3u)
w/id (W=4u)
w/id (W=5u)
w/id
GM/ID
GM/ID 30
W 3u
w/id 46.79k

fT


Plot 1A (pmos_03v3.lut)
1e9
fT (W=1u)
fT (W=2u)
fT (W=3u)
fT (W=4u)
fT (W=5u)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
fT
10
12
14
16
18
20
22
24
26
GM/ID
GM/ID 30
W 3u
fT 77.82k

VGS


Plot 1A (nmos_03v3.lut)
VGS (W=1u)
VGS (W=2u)
VGS (W=3u)
VGS (W=4u)
VGS (W=5u)
0.8
0.7
0.6
0.5
0.4
VGS
10
12
14
16
18
20
22
24
26
GM/ID
GM/ID 30
W 3u
VGS 200m

PART 2: OTA Design

$DC\ loop\ gain$ =$60dB$

$DC\ loop\ gain$=1000

$settling\ time = \frac{4.6}{2\pi BW_{CL}}$, $settling\ time = 100ns$

$BW_{CL} = 7.32MHz$, $A_{OL} = 2000$

$$BW_{OL} = \frac{BW_{CL}}{(1 + A_{OL}\beta)}$$

$BW_{OL} = 7312Hz$, *but we will take a margin of to make sure that the GBW is satisfied*
$A_{OL} = 3000$

$GBW_{OL} = A_{OL}\, BW_{OL}$

$GBW_{OL} \approx 22MHz$

$$GBW_{OL} = \frac{g_{m_{input\_pair}}}{2\pi C_L}$$

$g_{m_{input\_pair}} \approx 207\mu S$

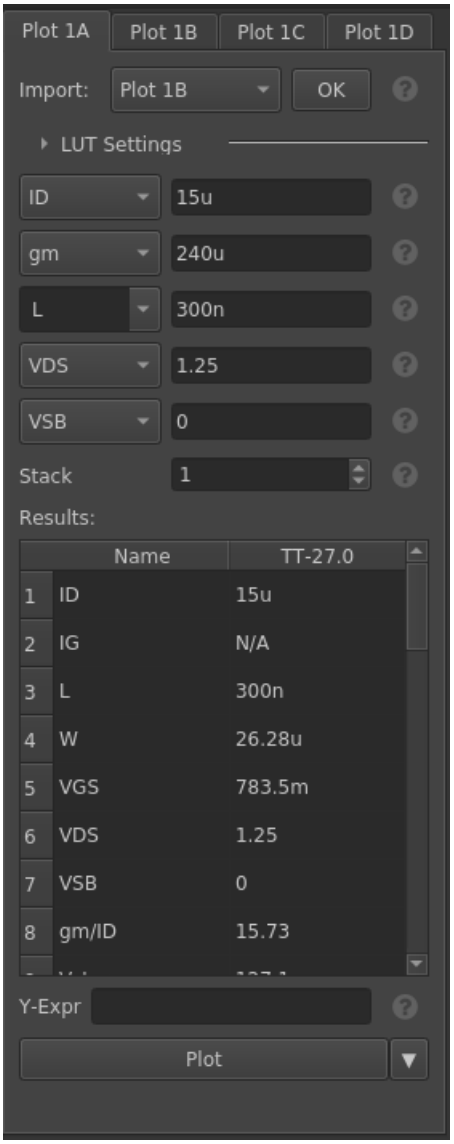
Input pair design

Assume $I_D = 15\mu A$, and we will use a margin for
$g_{m_{input\_pair}}$ *to be*

$g_{m_{input\_pair}} = 240\mu S$

We will use L=300n

$V_{DS} = 1.25V$



$$W_{input\ pair} = 26.28\mu m$$

$$L_{input\ pair} = 300n$$

Current source design

Since $I_{BIAS} = 10\mu A$ and we want each branch to have $15\mu A$ (except the input pair branch $30\mu A$ for each branch of the input pair to have $15\mu A$) we will need to use Multipliers

So I will design the transistor that has I_{BIAS} and make all transistors having the same dimensions

Then adjust the multipliers to obtain the desired current at each branch

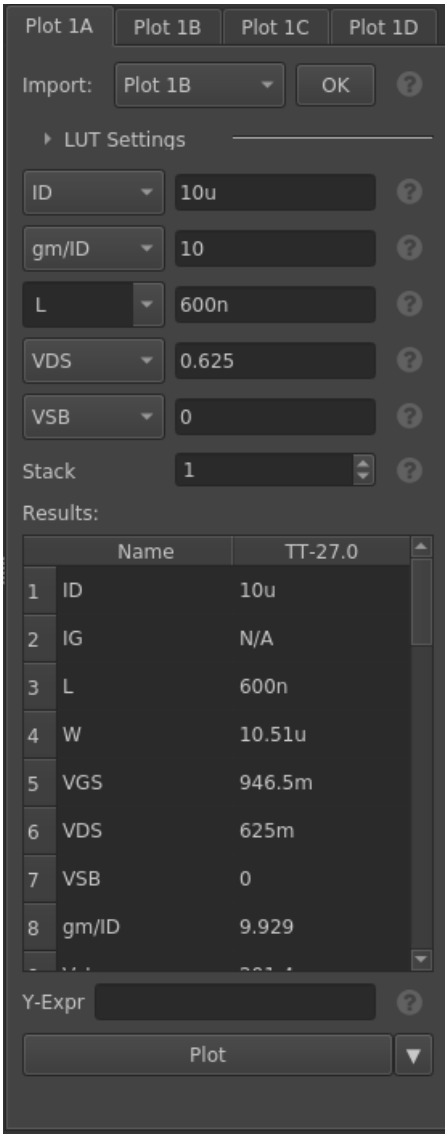
For the transistors that has I_{BIAS}

I= $10\mu A$

use L=$600\mu m$

use $\frac{g_m}{I_D} = 10$

$V_{DS} = 0.625V$



$$W_{current\ source} = 10.51\mu m$$

$$L_{current\ source} = 600n$$

For the multipliers

1. The transistor that is connected to $I_{BIAS} = 10\mu A$ we will use multiplier=2
2. Any transistor that has $I = 15\mu A$ we will use multiplier=3
3. Any transistor that has $I = 30\mu A$ we will use multiplier=6

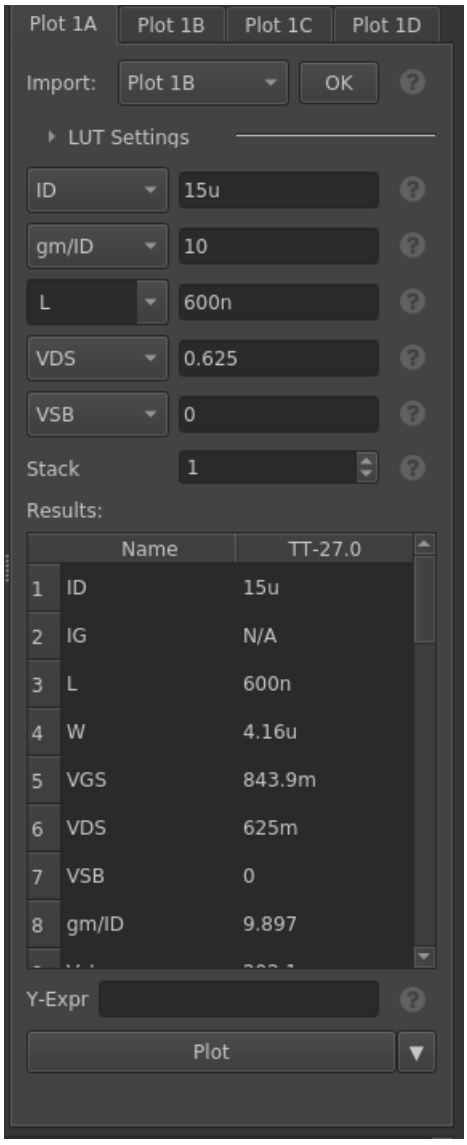
Tail design

$I_D = 15\mu A$

Use $L = 600n$

use $\frac{g_m}{I_D} = 10$

$V_{DS} = 0.625V$



$$W_{tail} = 4.16\mu m$$

$$L_{tail} = 600n$$

Cascode design

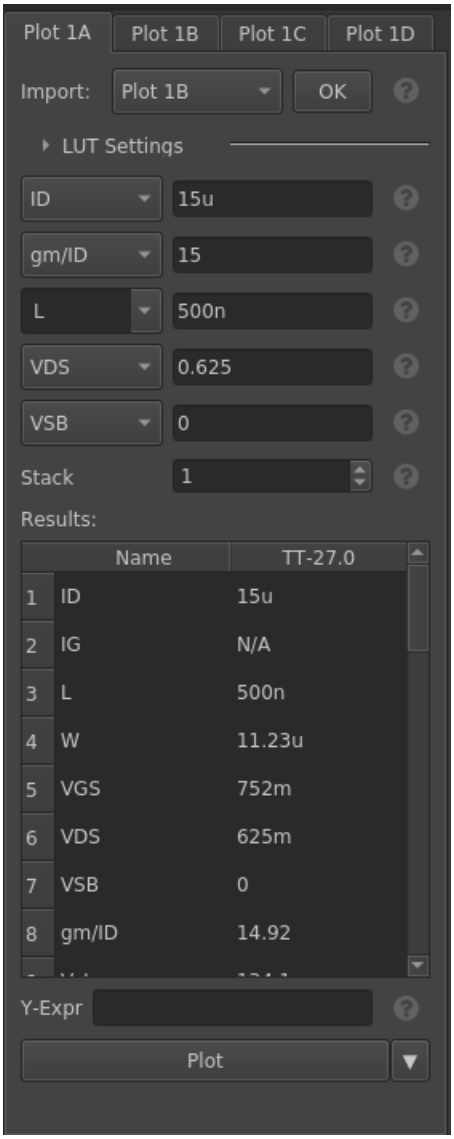
NMOS

$I_D = 15\mu A$

Use $L = 600n$

use $\frac{g_m}{I_D} = 10$

$V_{DS} = 0.625V$



$$W_{NMOS\ cascode} = 11.23\mu m$$

$$L_{NMOS\ cascode} = 500n$$

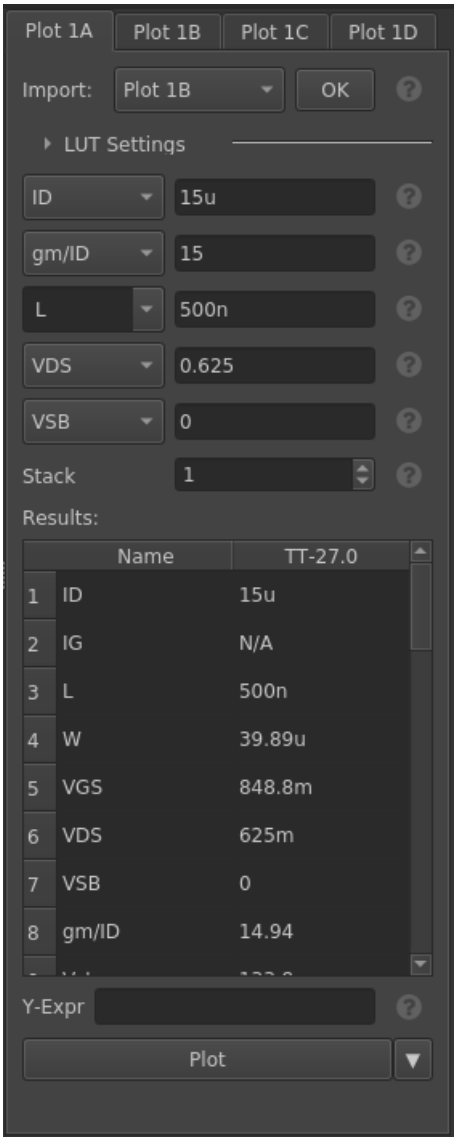
PMOS

$I_D = 15\mu A$

Use $L = 600n$

use $\frac{g_m}{I_D} = 10$

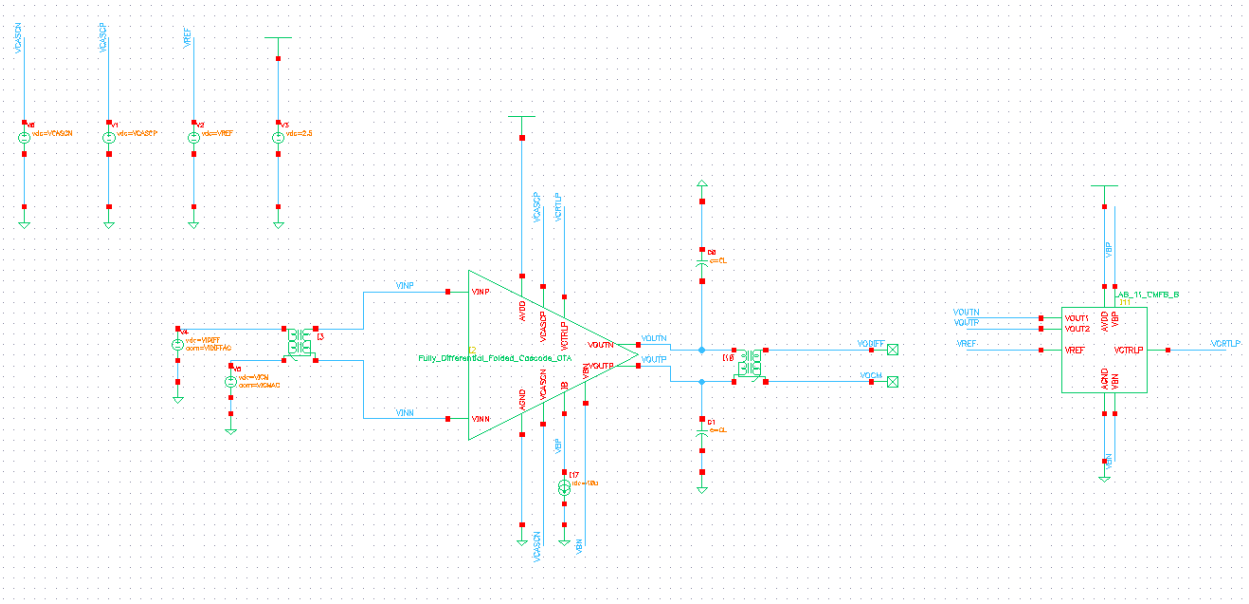
$V_{DS} = 0.625V$

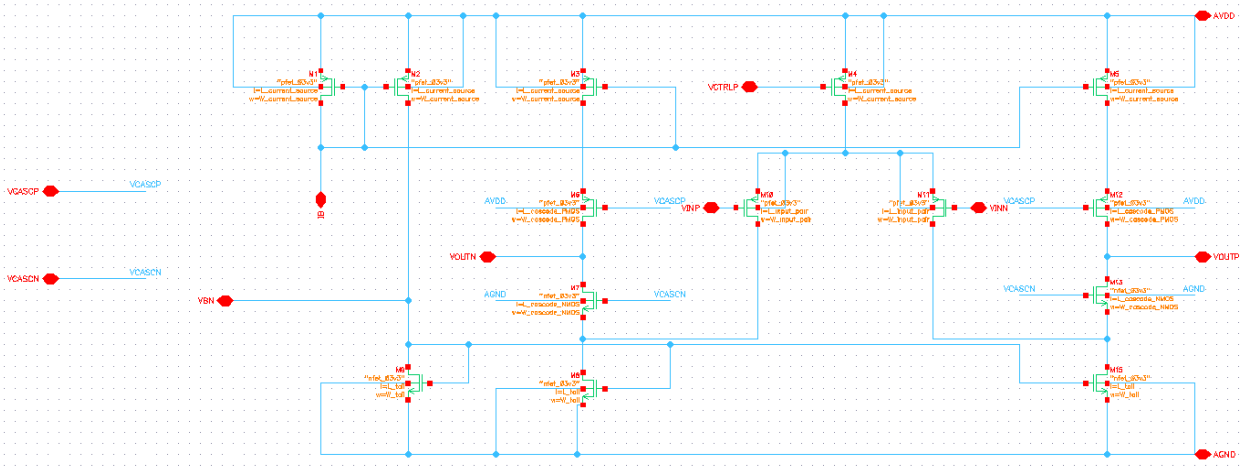


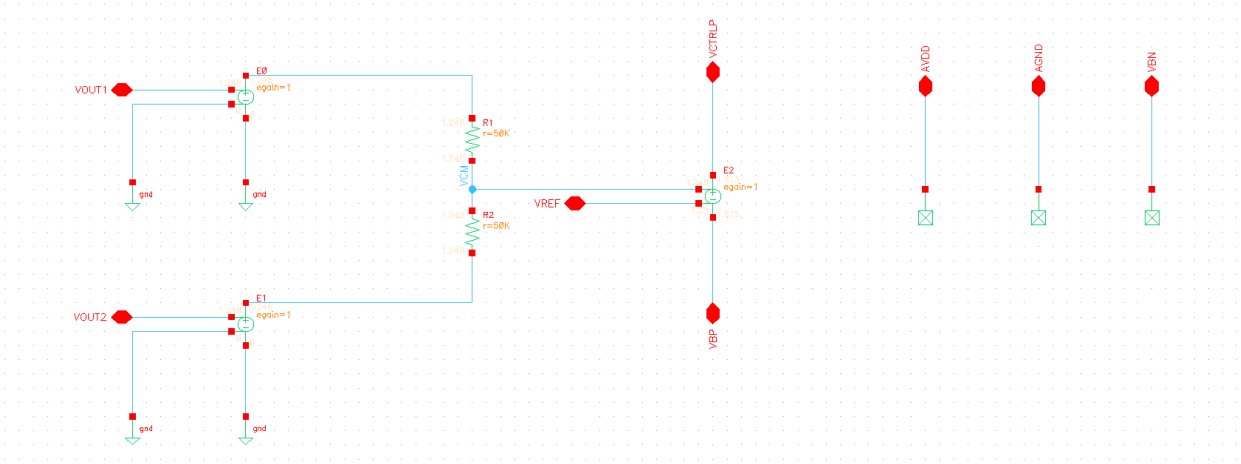
$W_{PMOS\ cascode} = 39.89\mu m$

$L_{PMOS\ cascode} = 500n$

PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

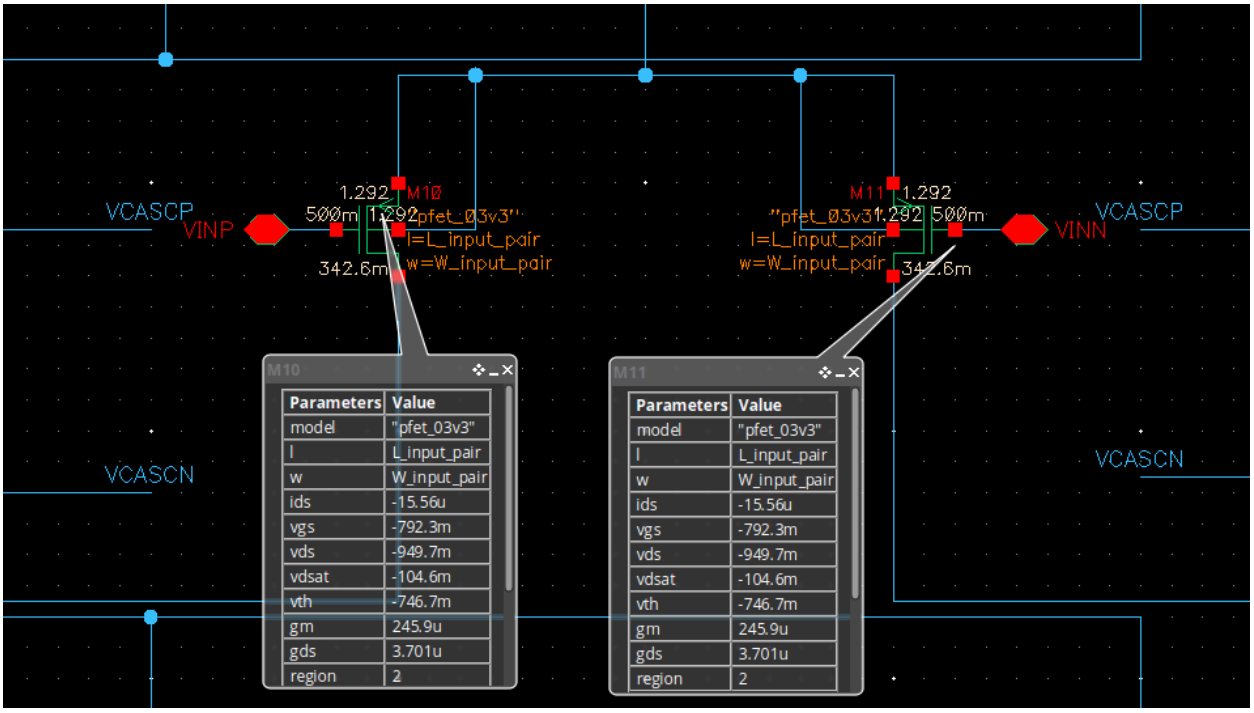




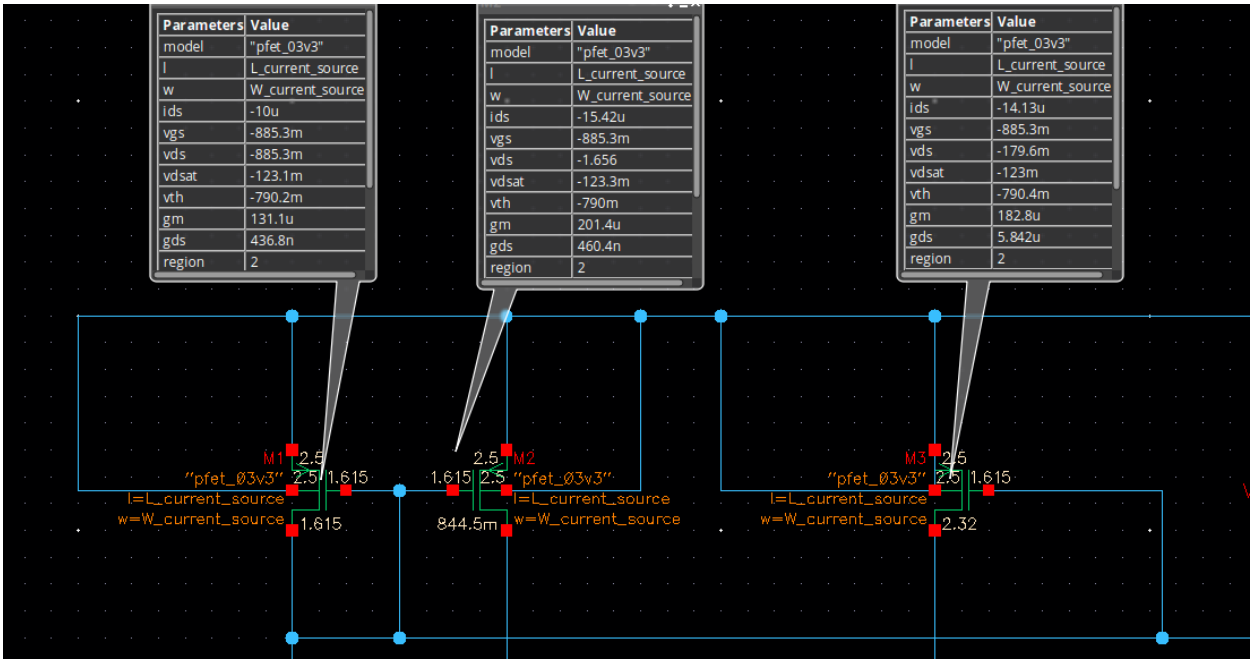


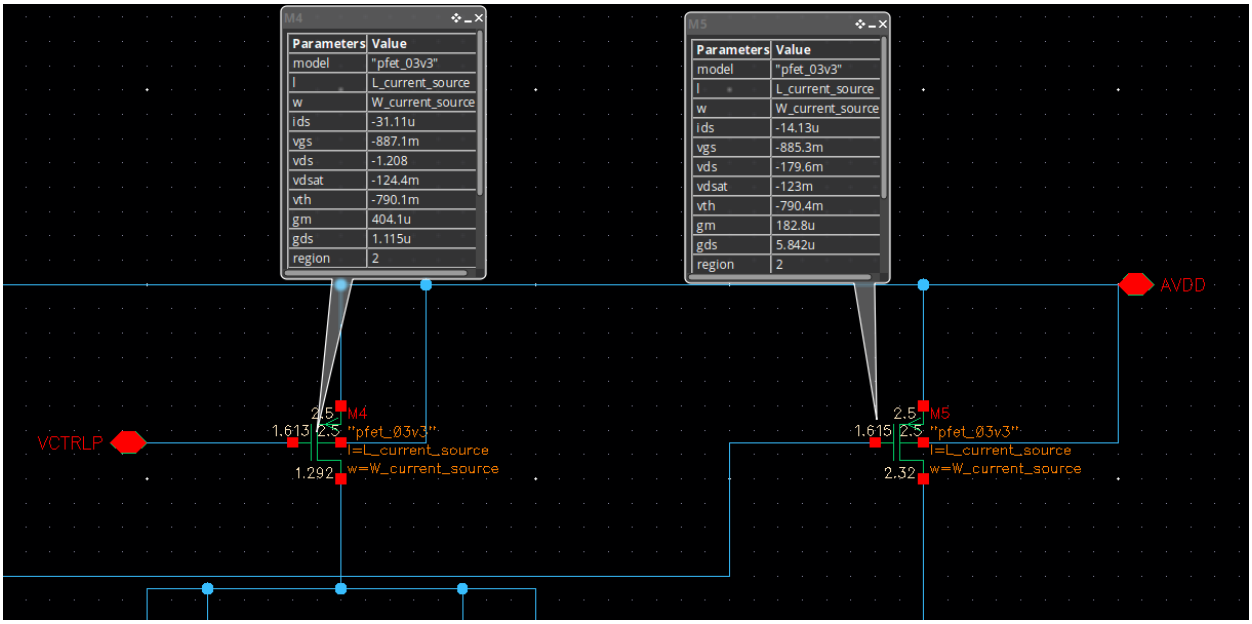
DC OP

Input pair

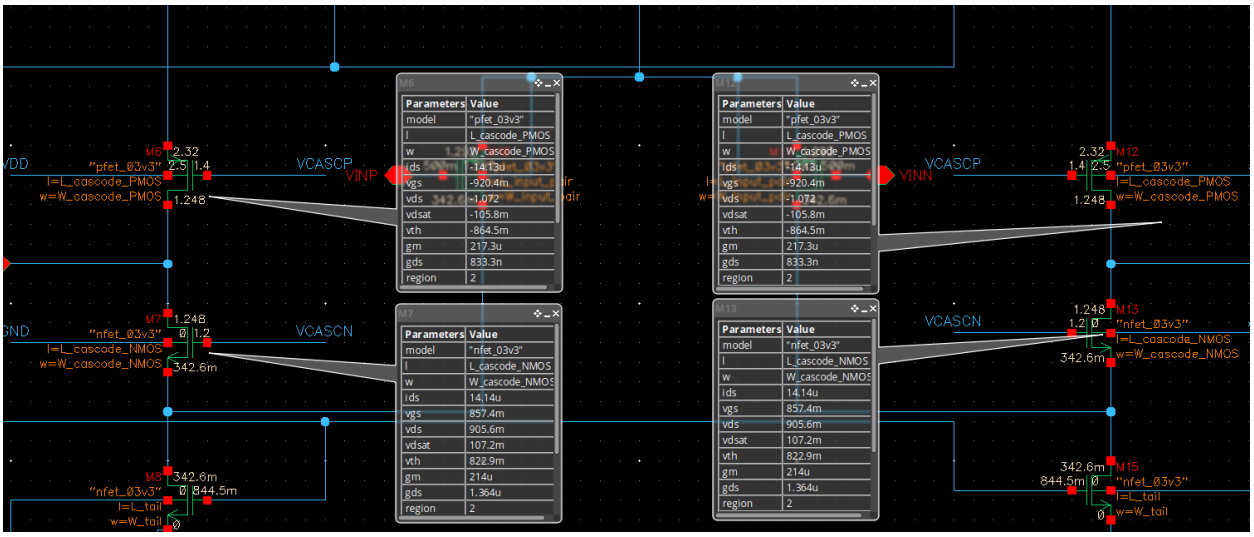


Current source

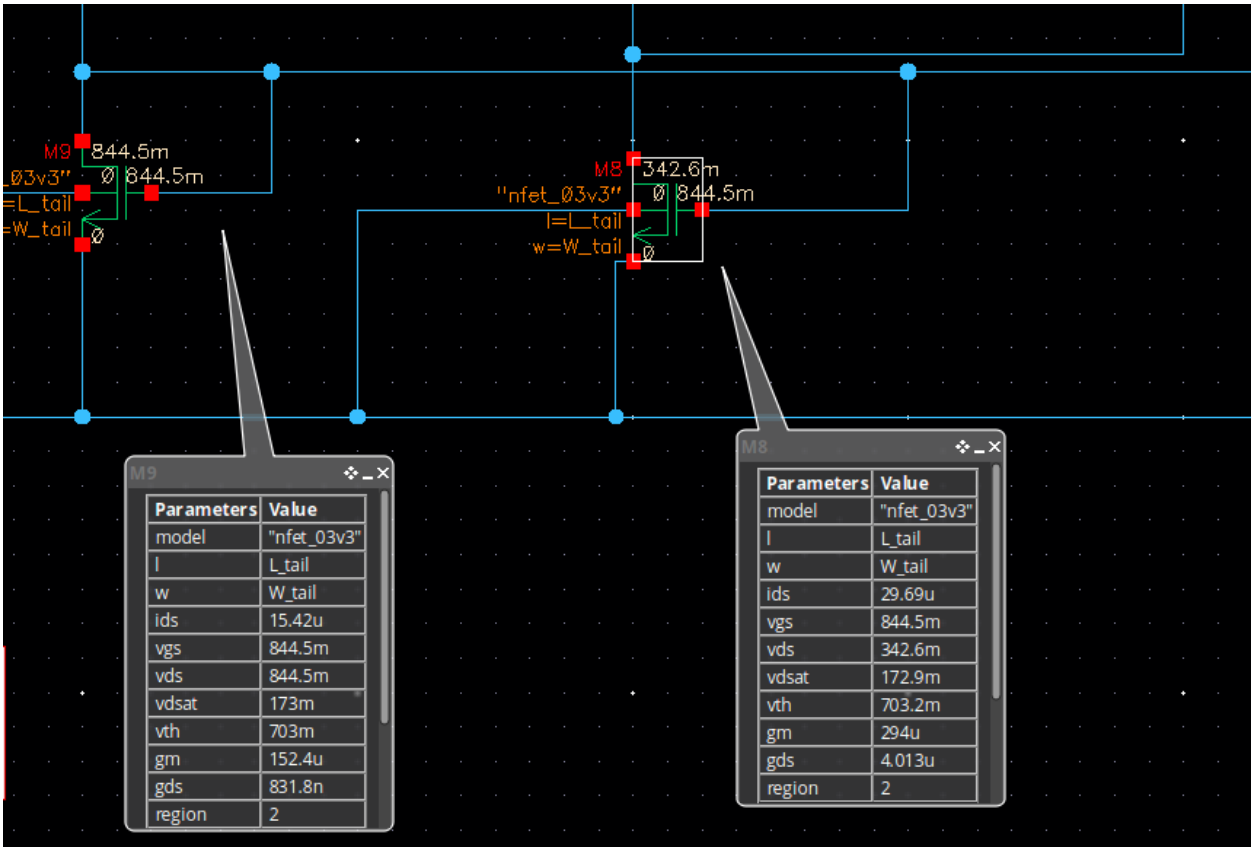


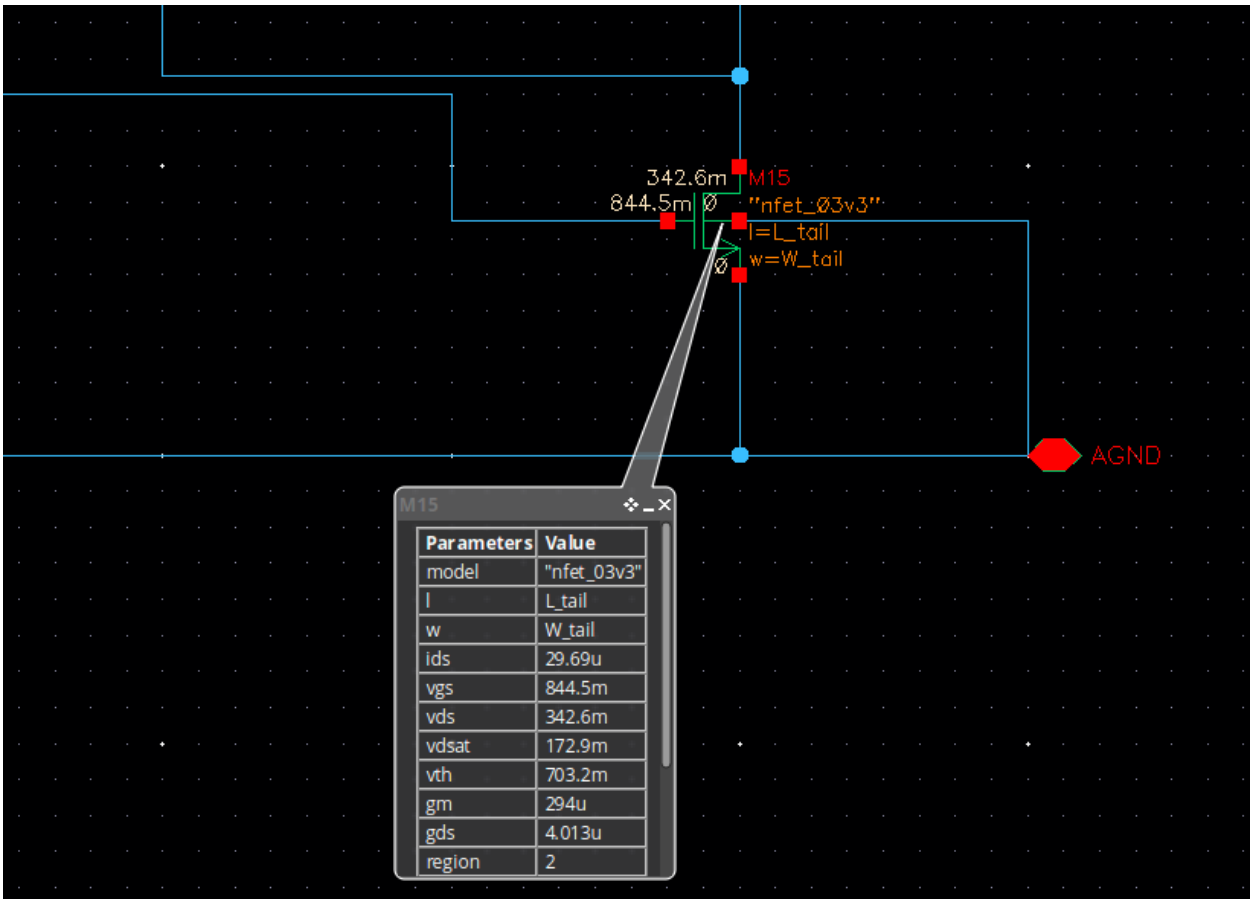


Cascode



Tail





Voltage values calculations

$$V_{ref} = \frac{V_{DD} - V^*_{M3} - V^*_{M6} + V^*_{M7} + V^*_{M8}}{2}$$

$V^* = 0.2\text{V}$

$V_{ref} = 1.25V$

$V_{CASCN} = V_{gs_{cascn}} + V^*_{M8}$, $V^*_{M8} = 0.2V, V_{gs_{cascn}} = 0.984V$

$V_{CASCN} = 1.184V$

$V_{CASCP} = V_{DD} - V^*_{M3} - V_{gs_{cascp}}$, , $V^*_{M3} = 0.2V, V_{gs_{cascp}} = 0.92V$

$V_{CASCP} = 1.4V$

- The common mode level at the output of the OTA is 1.248V which is nearly equal to V_{ref}

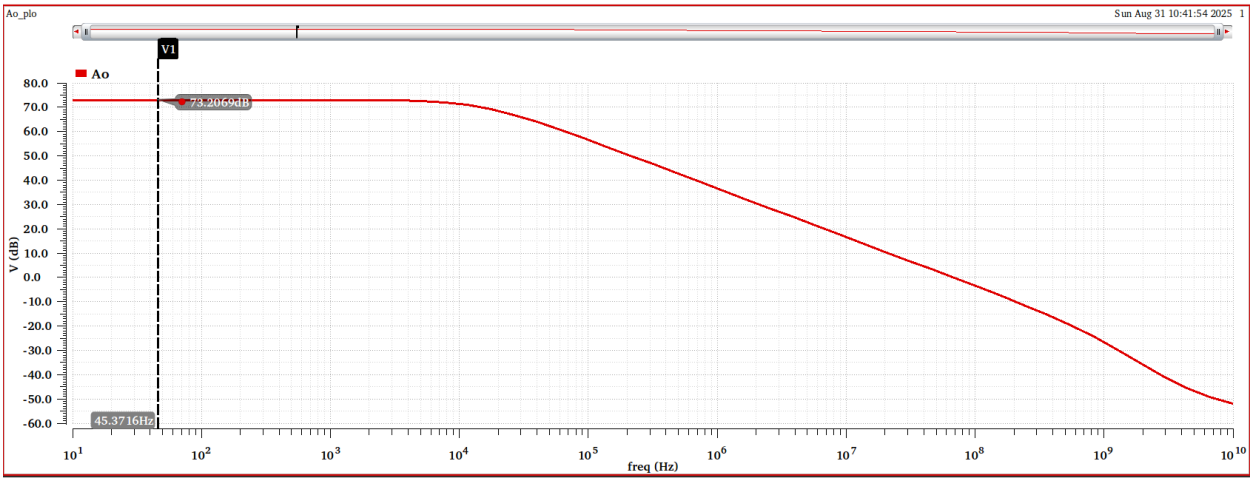
- $\frac{VOUT}{VIN} = \frac{1.615-1.613}{1.25-1.247}$

$$\frac{VOUT}{VIN} = 1$$

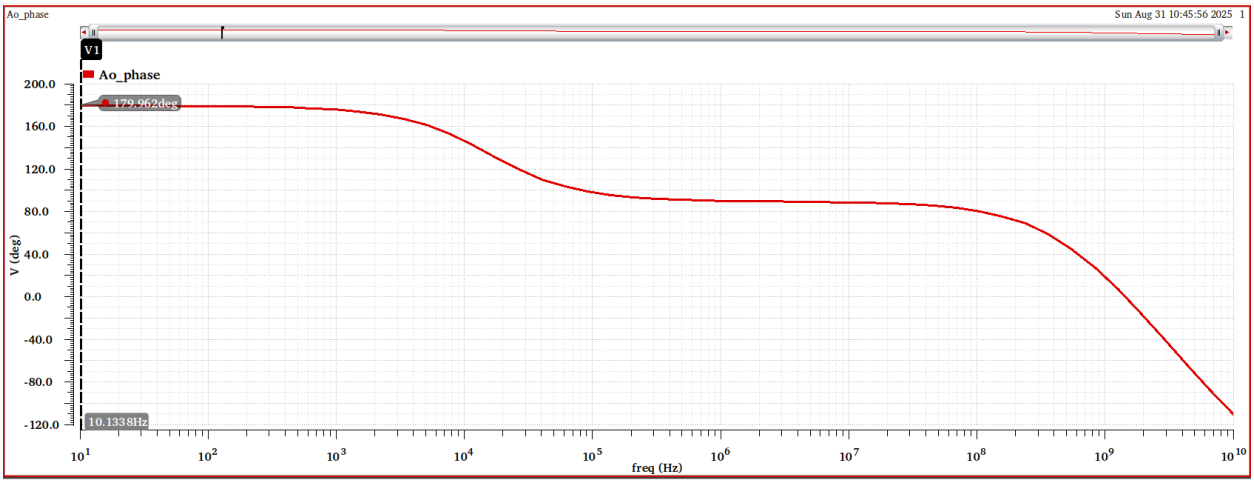
this is because in the behavioral model the value of the gain of all the voltage controlled voltage source is set to 1

Diff small signal ccs

Gain magnitude in dB



Gain phase



Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_NEW:LAB11_Part3:1	Ao_plot				
ITI_NEW:LAB11_Part3:1	Ao	4.575k			
ITI_NEW:LAB11_Part3:1	Ao_dB	73.21			
ITI_NEW:LAB11_Part3:1	Bandwidth	15.31k			
ITI_NEW:LAB11_Part3:1	fu	69.56M			
ITI_NEW:LAB11_Part3:1	GBW	70.01M			
ITI_NEW:LAB11_Part3:1	Ao_phase				
ITI_NEW:LAB11_Part3:1	Phase margin	83.9			

Hand analysis

1. Gain

$$A_V = g_{m10}((r_{o13}(1 + g_{m13}r_{o15}))//((r_{o12}(1 + g_{m12}r_{o5})))$$
$$A_V = 74.2dB$$

2. Bandwidth

$$Bandwidth = \frac{1}{2\pi RC_L}$$
$$C_L = 500fF$$
$$\text{R}=(r_{o13}(1 + g_{m13}r_{o15}))//((r_{o12}(1 + g_{m12}r_{o5})$$
$$Bandwidth = 14.94KHz$$

3. Fu

since the Fully-Differential Folded Cascode OTA has another pole at high frequency we can use the approximation of Fu=GBW

$$Fu = Bandwidth \times Gain$$

Fu=74.8MHz

4. GBW

GBW=$Bandwidth \times Gain$

GBW=74.8MHz

5. Phase margin

$$Phase\ margin = 180 - \tan^{-1}(\frac{UGF}{Dominant\ pole}) - \tan^{-1}(\frac{UGF}{Non - dominant\ pole})$$

$$UGF = 69.56MHz$$

$$Dominant\ pole = 15.31KHz$$

$$Non - dominant\ pole \approx 600MHz$$

(The value of the non-dominant pole was estimated from the Bode plot as the frequency point where the magnitude response begins to decrease again, following the initial roll-off caused by the dominant pole)

$$Phase\ margin = 83.4°$$

PART 4: Open-Loop OTA Simulation (Actual CMFB)

CMFB design

Since it is required to have the total current consumption of the CMFB to be half the current consumption of the Input pair + cascode in the OTA

Then the total current consumption of the CMFB = $30\mu A$

We will divide the total current consumption to make every branch have equal current in it so each branch must have $6\mu A$

M_0 , M_1, M_2, M_9, M_{12}

$$W_{current\ source\ (OTA)} \rightarrow I_{current\ source\ (OTA)}$$

$$W \rightarrow I$$

$$10.51\mu \times 3 \rightarrow 15\mu$$

$$W \rightarrow 6\mu$$

$$W = 12.612\mu$$

L=600n

M_7

$$W_{tail\ (OTA)} \rightarrow I_{tail\ (OTA)}$$

$$W \rightarrow I$$

$$4.16\mu \times 2 \rightarrow 30\mu$$

$$W \rightarrow 12\mu$$

$$W = 3.328\mu$$

L=600n

$M_{10}, M_{11}, M_6, M_8, M_{13}$

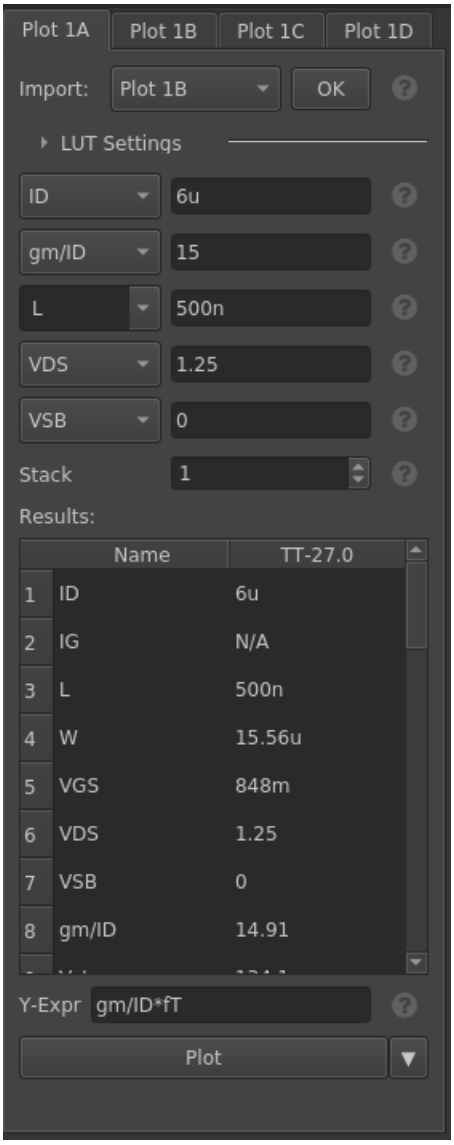
$I_D = 6\mu$

$\frac{g_m}{I_D}$=15

L=500n

$V_{ds} = 1.25V$

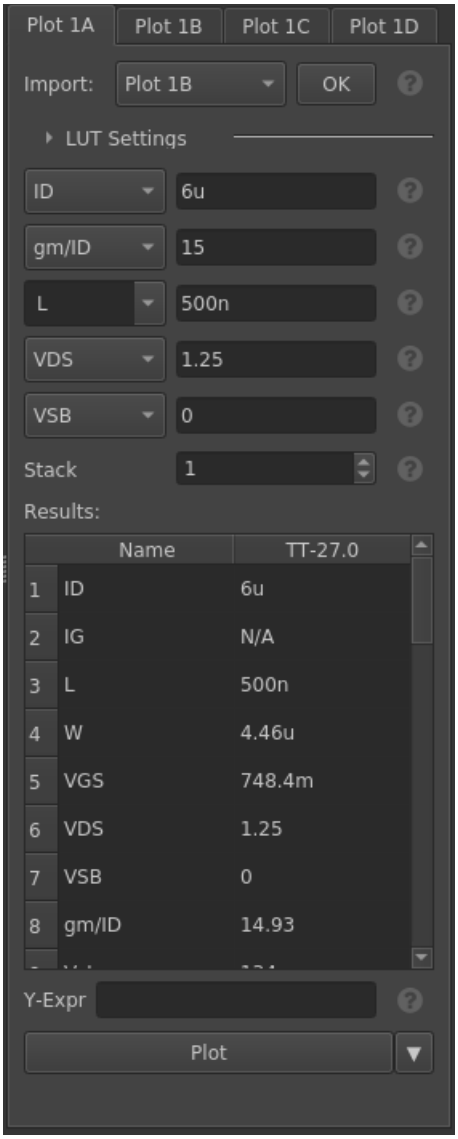
PMOS



$$W = 15.56\mu$$

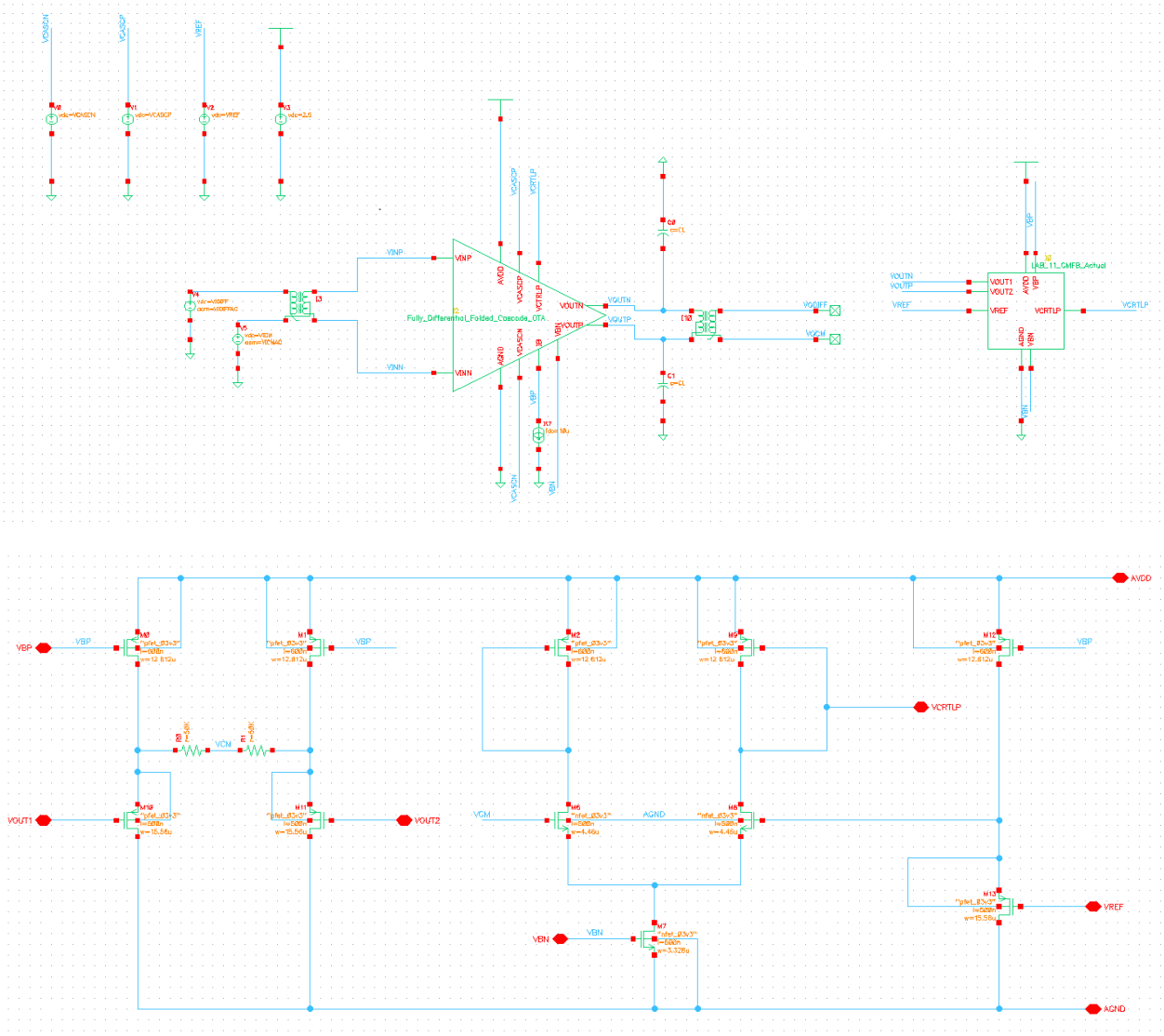
$$L = 500n$$

NMOS



$$W = 4.46\mu$$

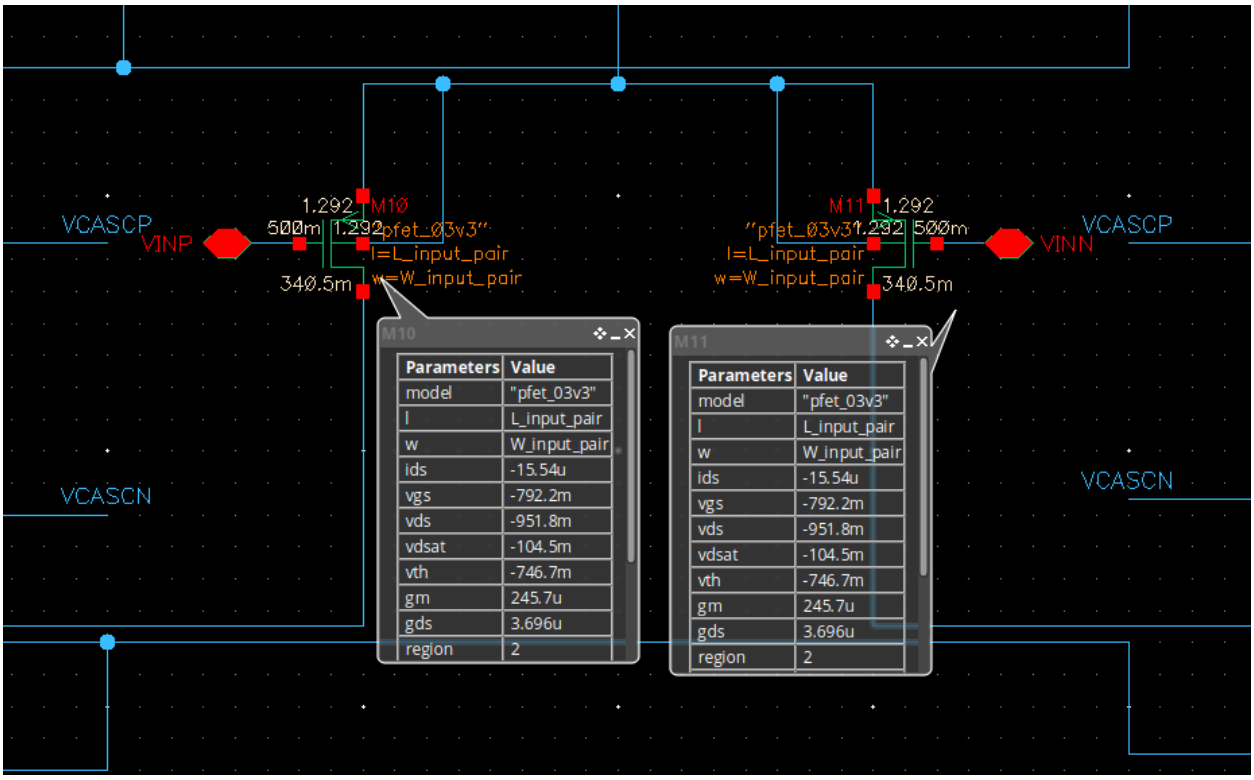
$$L = 500n$$


VCASCN
VCASCP
VREF
VINP
VINN
VOUTN
VOUTP
VCRTLP
VCMFF
VCMI
Fully_Differential_Folded_Cascode_OTA
LAB_11_CMFB_Actual
AVDD
AGND
VBP
VBN
VCM
VOUT1
VOUT2
R0
R1
C0
C1
L0

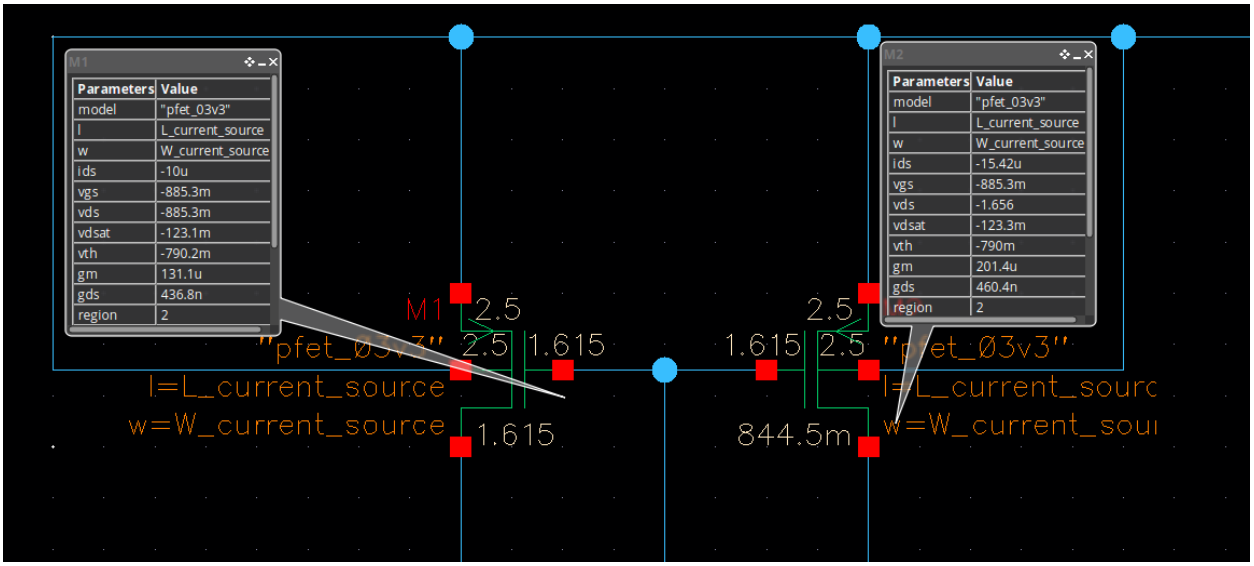
DC OP

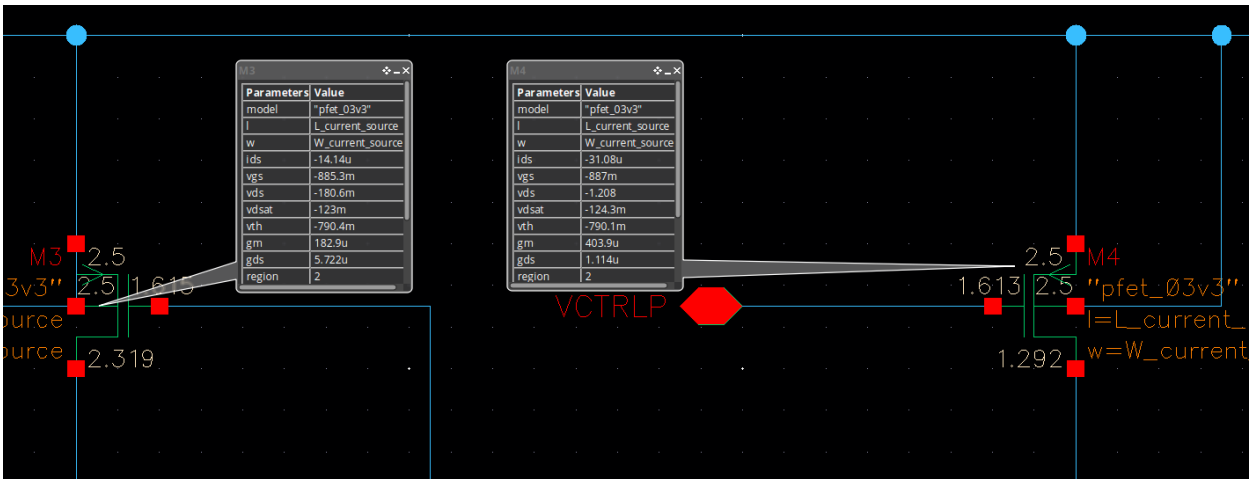
OTA

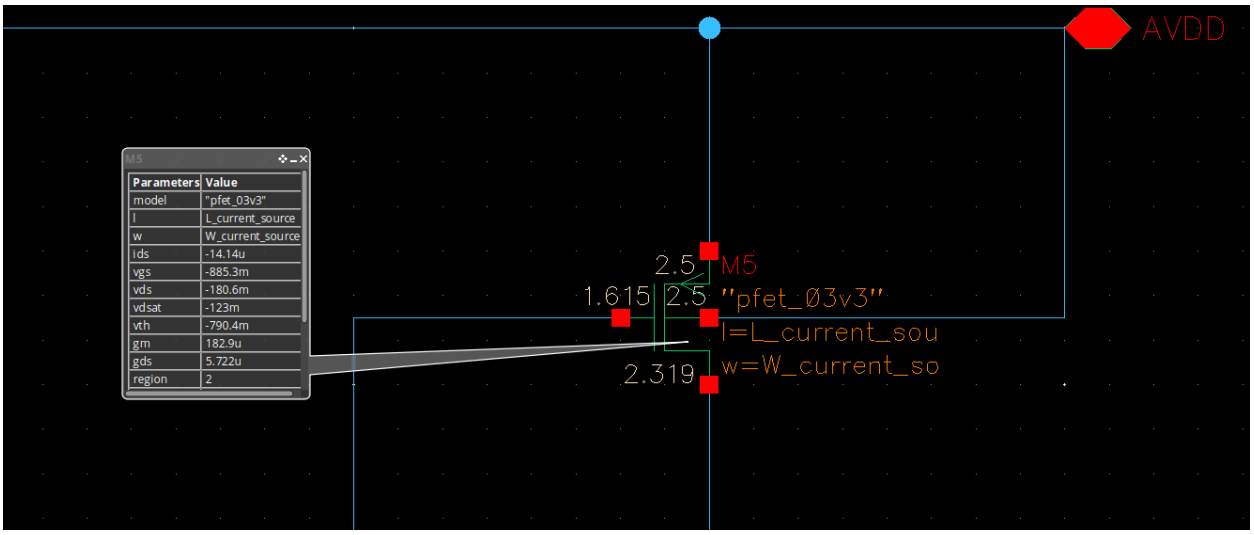
Input pair



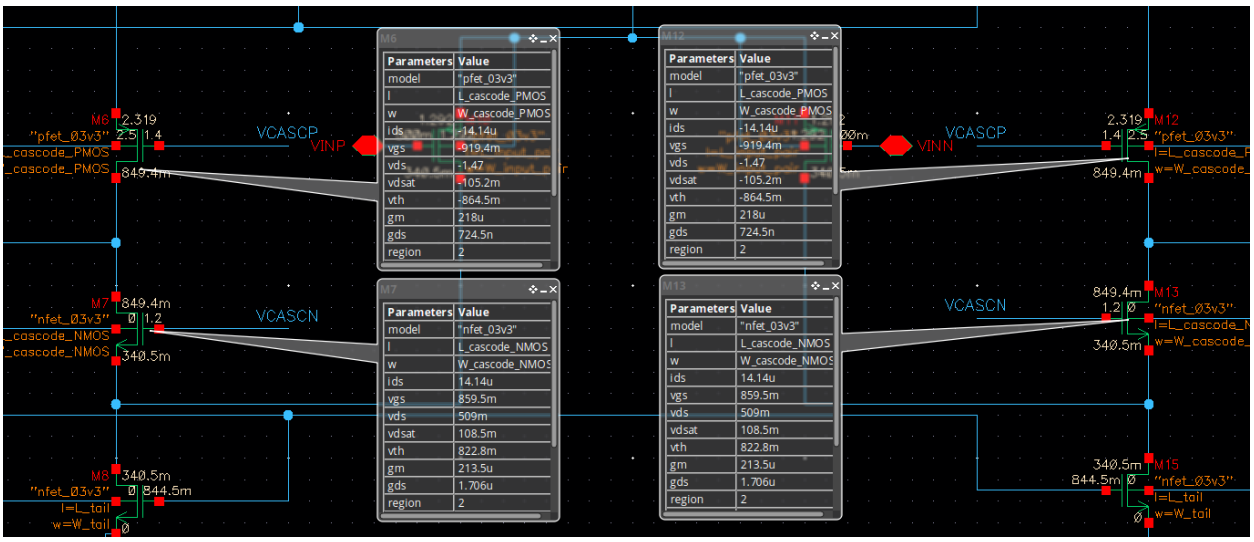
Current source



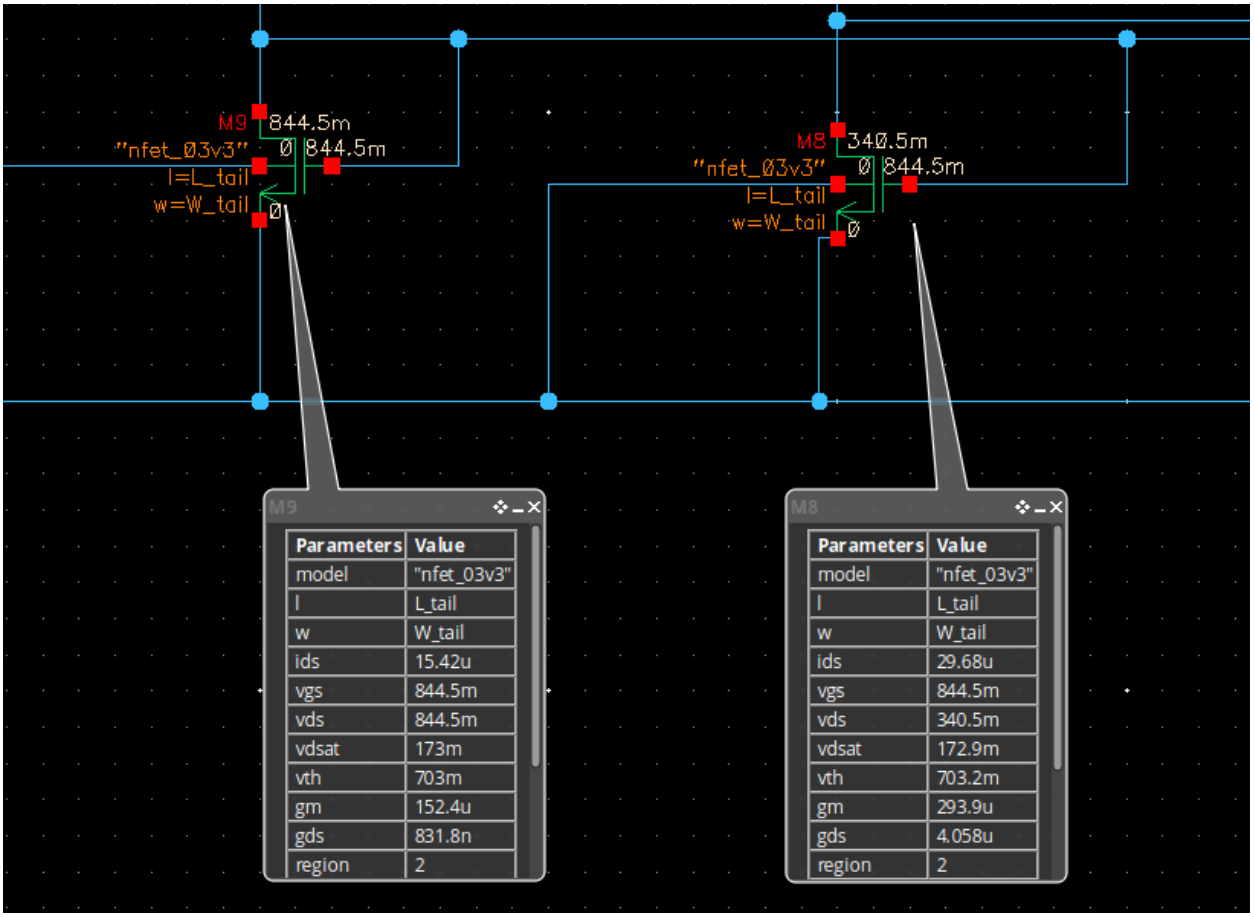

M3
2.5
2.319
VCTRLP
2.5
M4
1.613
2.5
"pfet_Ø3v3"
1.292
w=W_current

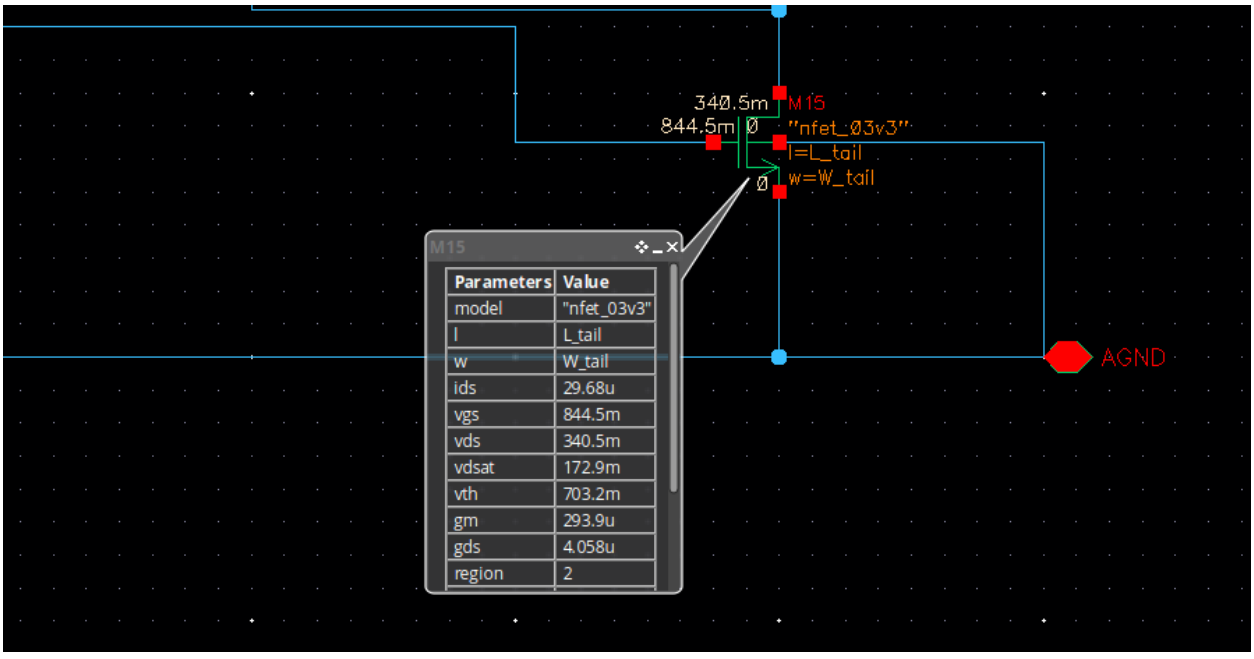

AVDD
2.5
M5
1.615
2.5
"pfet_Ø3v3"
2.319
w=W_current_so

Cascode

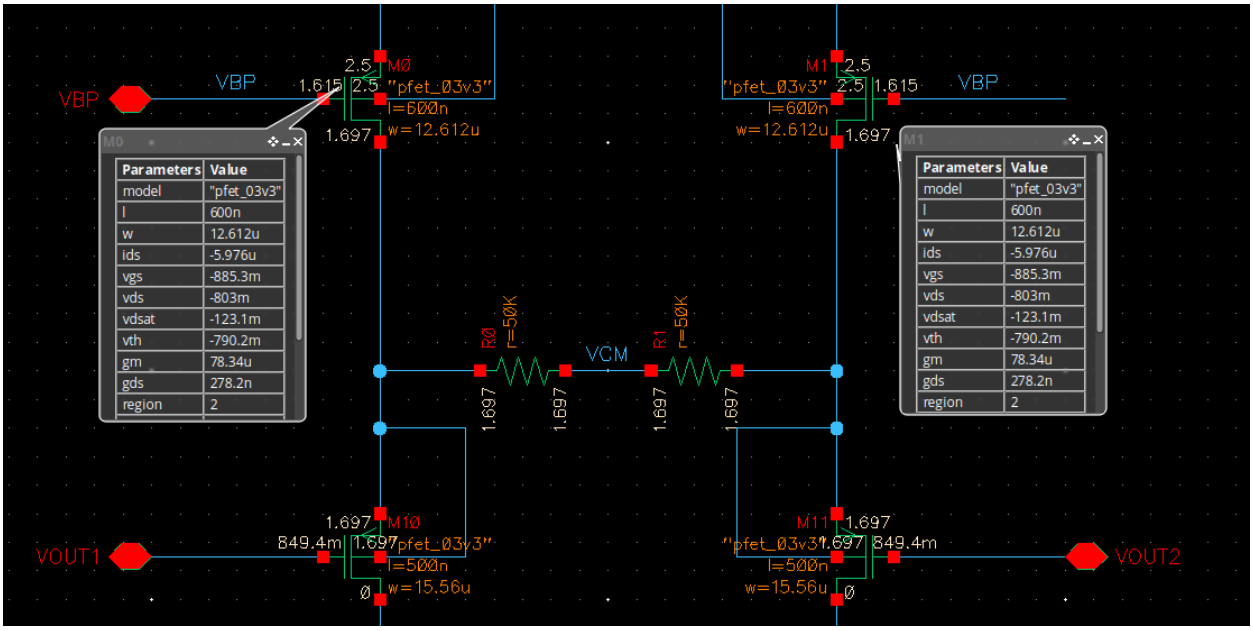

M6
2.319
"pfet_Ø3v3"
2.5
1.4
849.4m
VCASCP
VINP
M12
VINN
M7
849.4m
"nfet_Ø3v3"
VCASCN
340.5m
M13
M8
340.5m
"nfet_Ø3v3"
844.5m
M15
"nfet_Ø3v3"
w=W_tail

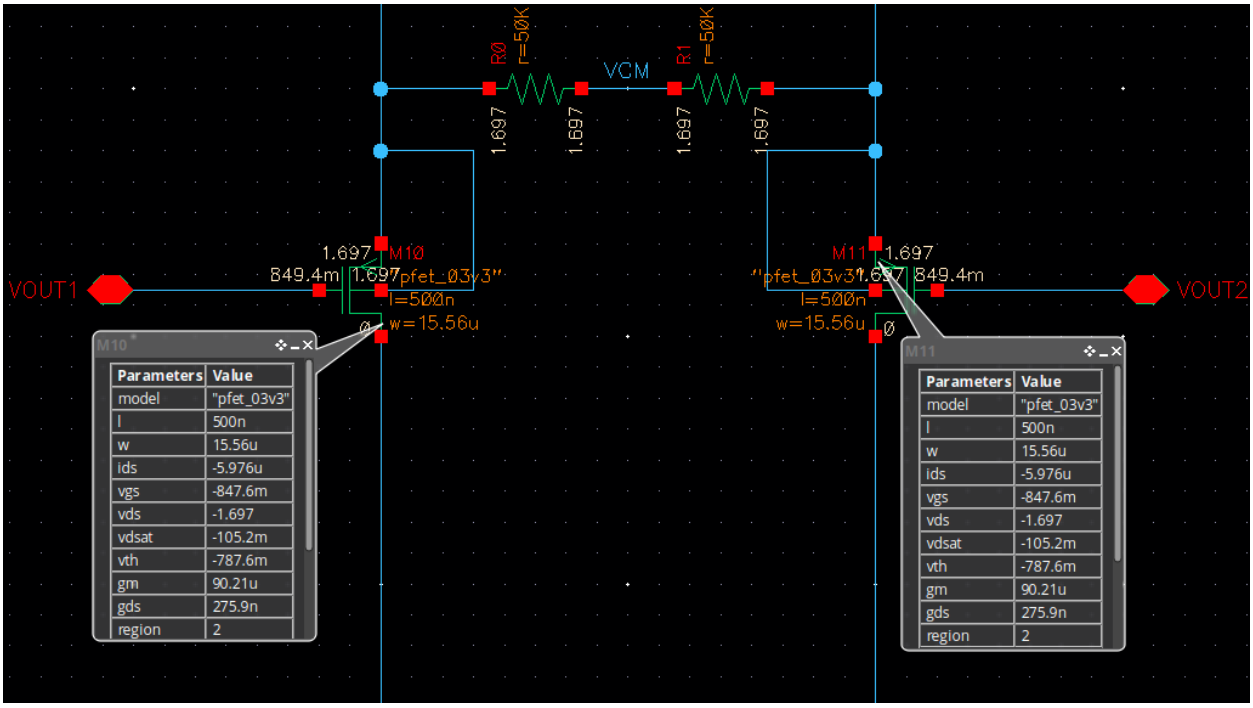
Tail

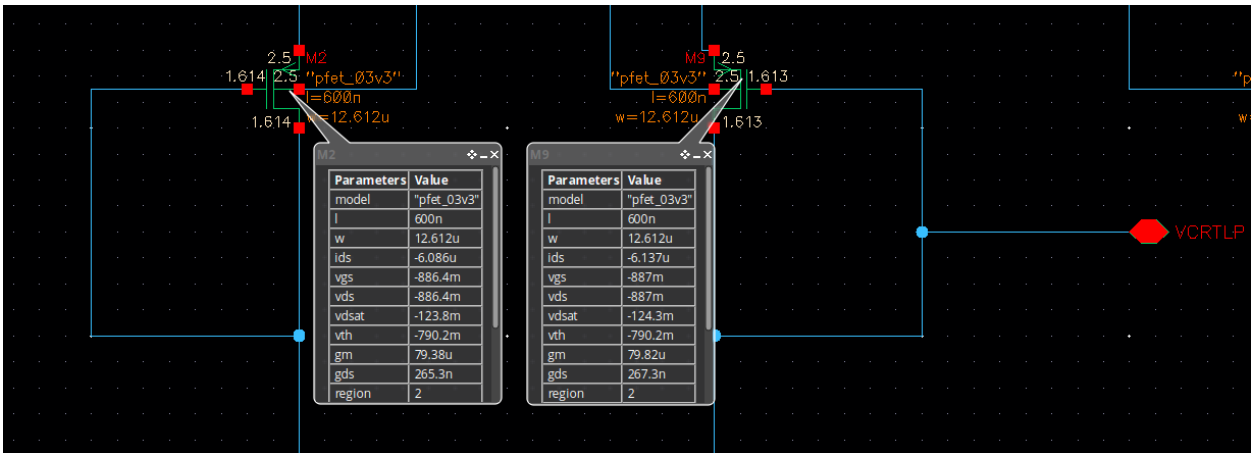

M9
844.5m
"nfet_03v3"
Ø
844.5m
l=L_tail
w=W_tail
Ø
M8
340.5m
"nfet_03v3"
Ø
844.5m
l=L_tail
w=W_tail
Ø
M9
Parameters Value
model "nfet_03v3"
l L_tail
w W_tail
ids 15.42u
vgs 844.5m
vds 844.5m
vdsat 173m
vth 703m
gm 152.4u
gds 831.8n
region 2
M8
Parameters Value
model "nfet_03v3"
l L_tail
w W_tail
ids 29.68u
vgs 844.5m
vds 340.5m
vdsat 172.9m
vth 703.2m
gm 293.9u
gds 4.058u
region 2

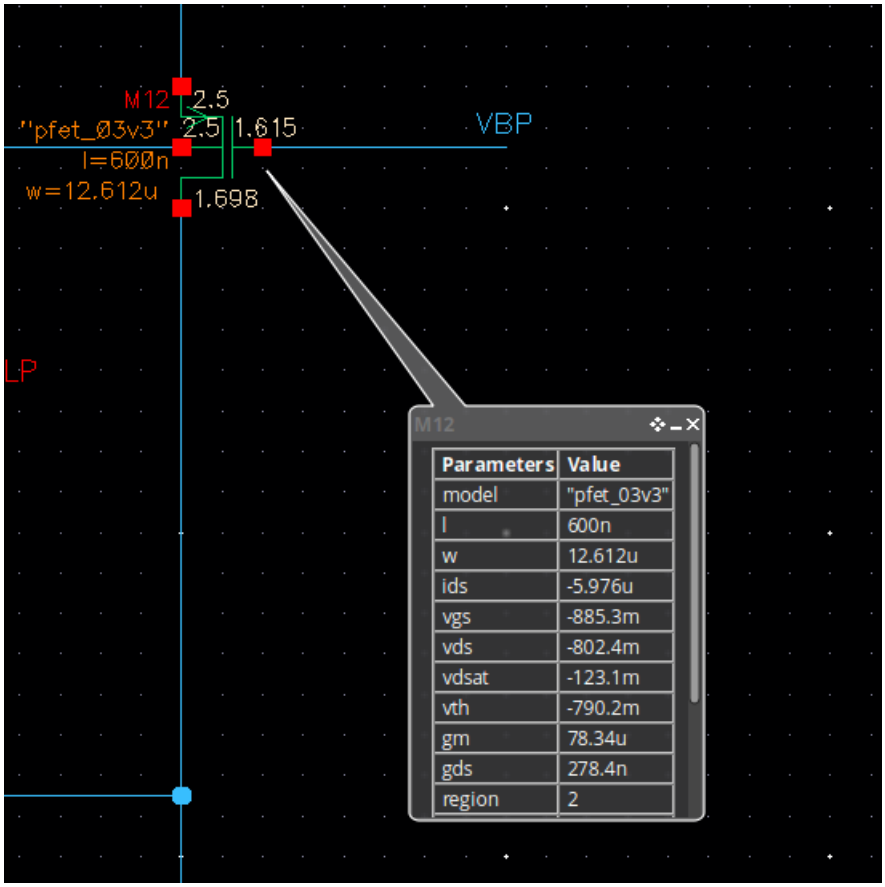

340.5m
844.5m
M15
Ø
"nfet_03v3"
l=L_tail
w=W_tail
Ø
AGND
M15
Parameters Value
model "nfet_03v3"
l L_tail
w W_tail
ids 29.68u
vgs 844.5m
vds 340.5m
vdsat 172.9m
vth 703.2m
gm 293.9u
gds 4.058u
region 2

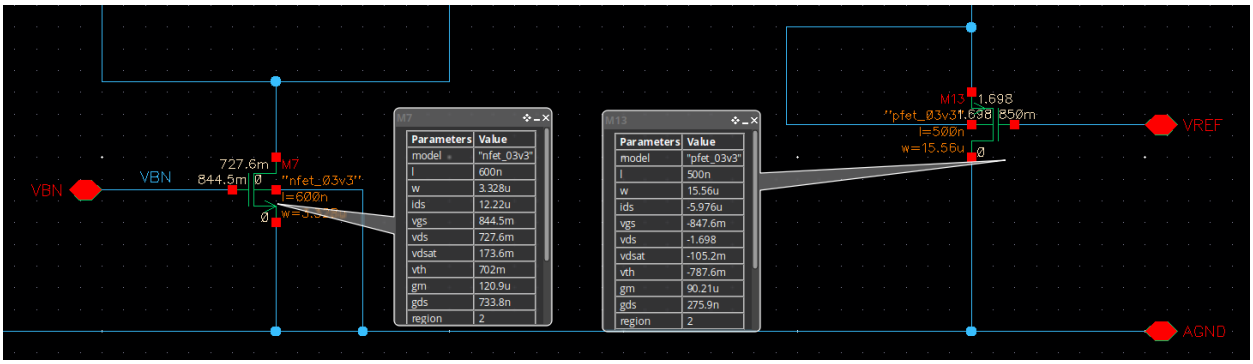
CMFB

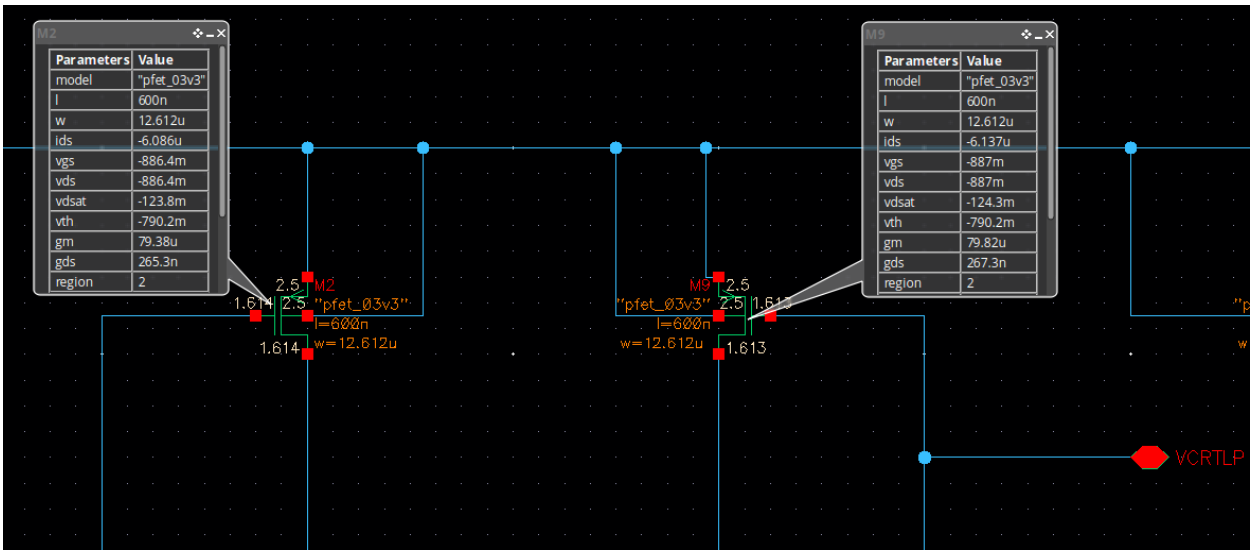

VBP
VBP
2.5
M0
1.615
2.5
"pfet_03v3"
l=600n
1.697
w=12.612u
M1
2.5
"pfet_03v3"
2.5
1.615
VBP
l=600n
w=12.612u
1.697
M0
Parameters
Value
model
"pfet_03v3"
l
600n
w
12.612u
ids
-5.976u
vgs
-885.3m
vds
-803m
vdsat
-123.1m
vth
-790.2m
gm
78.34u
gds
278.2n
region
2
M1
Parameters
Value
model
"pfet_03v3"
l
600n
w
12.612u
ids
-5.976u
vgs
-885.3m
vds
-803m
vdsat
-123.1m
vth
-790.2m
gm
78.34u
gds
278.2n
region
2
R0
r=50K
VCM
R1
r=50K
1.697
1.697
1.697
1.697
VOUT1
1.697
M10
849.4m
1.697
"pfet_03v3"
l=500n
w=15.56u
M11
1.697
"pfet_03v3"
1.697
849.4m
l=500n
w=15.56u
VOUT2


R0
r=50K
VCM
R1
r=50K
1.697
1.697
1.697
1.697
VOUT1
1.697
M10
849.4m
1.697
"pfet_03v3"
l=500n
w=15.56u
M11
1.697
"pfet_03v3"
1.697
849.4m
l=500n
w=15.56u
VOUT2
M10
Parameters
Value
model
"pfet_03v3"
l
500n
w
15.56u
ids
-5.976u
vgs
-847.6m
vds
-1.697
vdsat
-105.2m
vth
-787.6m
gm
90.21u
gds
275.9n
region
2
M11
Parameters
Value
model
"pfet_03v3"
l
500n
w
15.56u
ids
-5.976u
vgs
-847.6m
vds
-1.697
vdsat
-105.2m
vth
-787.6m
gm
90.21u
gds
275.9n
region
2


2.5
M2
1.614
2.5
"pfet_03v3"
l=600n
1.614
w=12.612u
M9
2.5
"pfet_03v3"
2.5
1.613
l=600n
w=12.612u
1.613
VCRTLP
M2
Parameters
Value
model
"pfet_03v3"
l
600n
w
12.612u
ids
-6.086u
vgs
-886.4m
vds
-886.4m
vdsat
-123.8m
vth
-790.2m
gm
79.38u
gds
265.3n
region
2
M9
Parameters
Value
model
"pfet_03v3"
l
600n
w
12.612u
ids
-6.137u
vgs
-887m
vds
-887m
vdsat
-124.3m
vth
-790.2m
gm
79.82u
gds
267.3n
region
2


M12
2.5
"pfet_03v3"
2.5
1.615
VBP
l=600n
w=12.612u
1.698
LP
M12
Parameters
Value
model
"pfet_03v3"
l
600n
w
12.612u
ids
-5.976u
vgs
-885.3m
vds
-802.4m
vdsat
-123.1m
vth
-790.2m
gm
78.34u
gds
278.4n
region
2





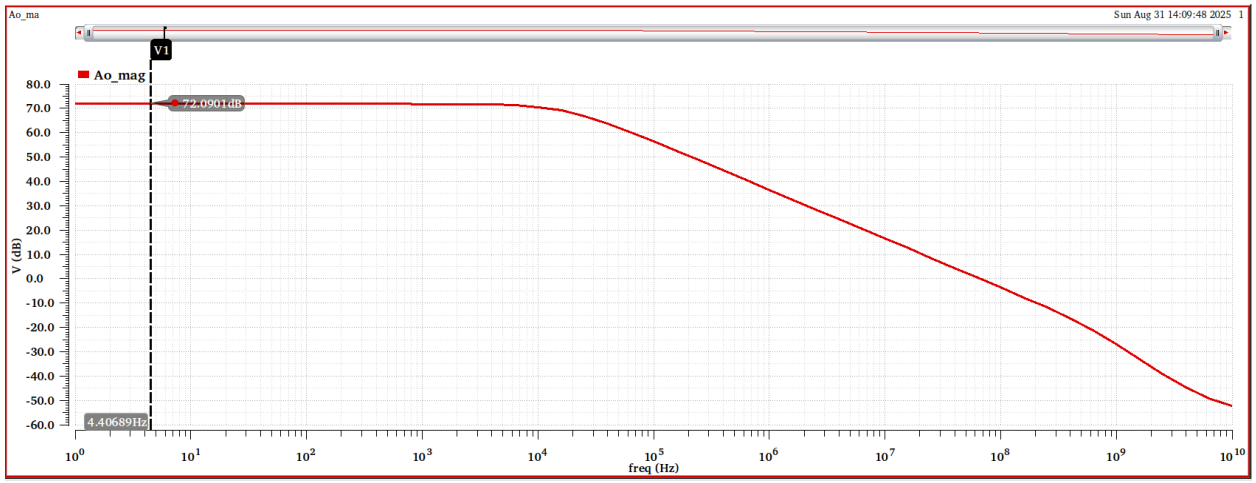
- The common mode level at the output of the OTA is 849.4mV which is nearly equal to V_{ref}
- $\frac{VOUT}{VIN} = \frac{1.698-1.697}{1.614-1.613}$

$$\frac{VOUT}{VIN} = 1$$

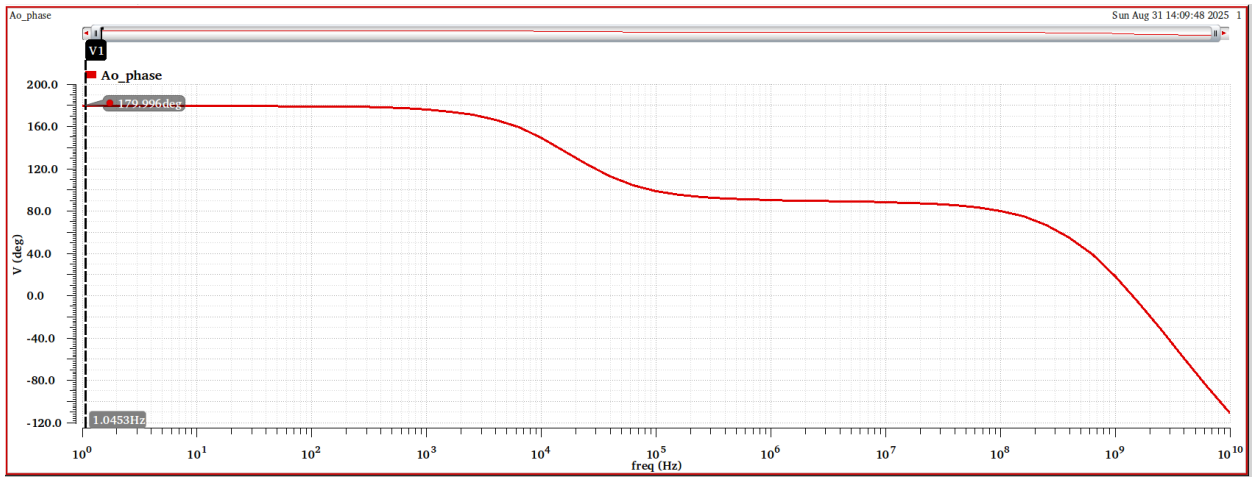
the value of $\frac{VOUT}{VIN}$=1 because the differential amplifier act as a buffer so its gain=1

Diff small signal ccs

Diff gain in dB



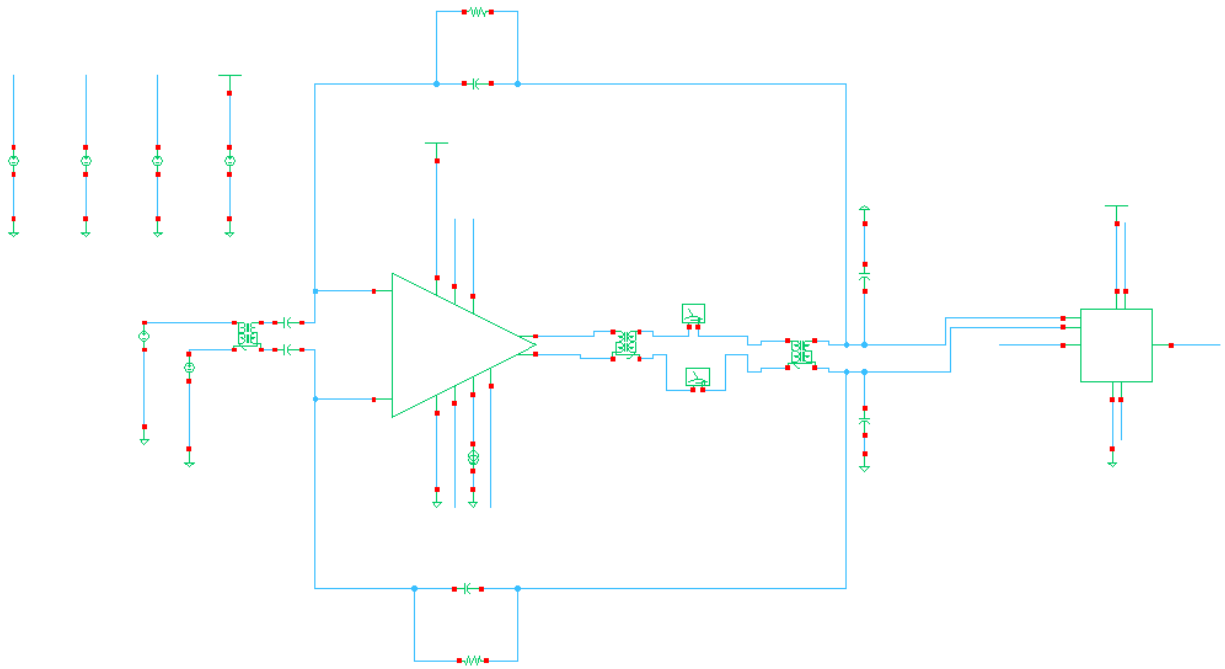
Diff gain phase



DC gain, BW, GBW, UGF, and PM

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_NEW:LAB11_Part4:1	Ao	4.023k			
ITI_NEW:LAB11_Part4:1	Bandwidth	17.23k			
ITI_NEW:LAB11_Part4:1	Ao_dB	72.09			
ITI_NEW:LAB11_Part4:1	fu	71.05M			
ITI_NEW:LAB11_Part4:1	GBW	69.32M			
ITI_NEW:LAB11_Part4:1	Ao_mag				
ITI_NEW:LAB11_Part4:1	Ao_phase				
ITI_NEW:LAB11_Part4:1	Phase margin	83.81			

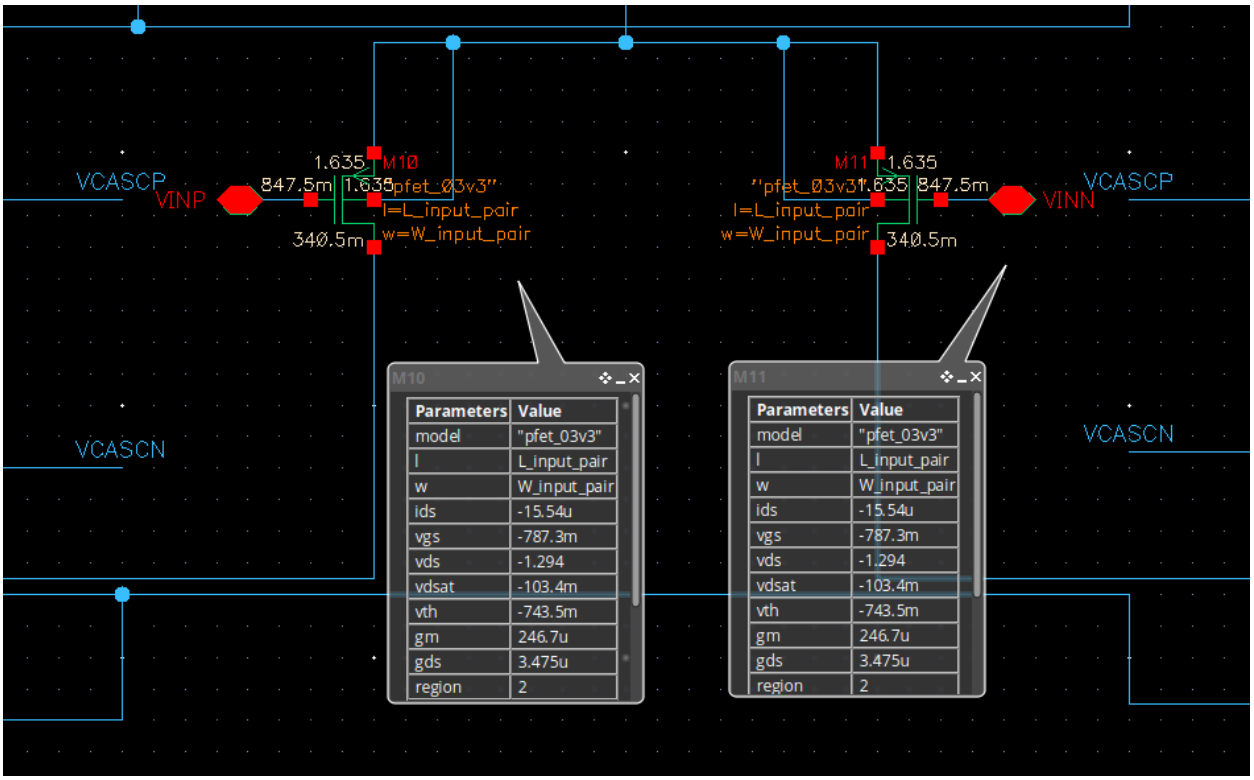
PART 5: Closed Loop Simulation (AC and STB Analysis)



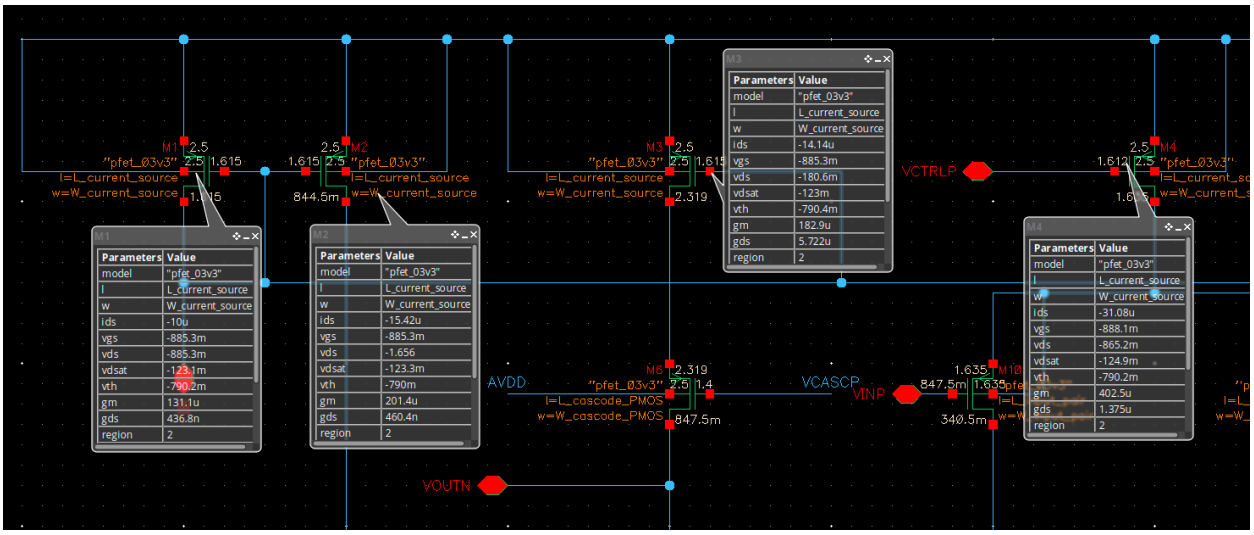
DC OP

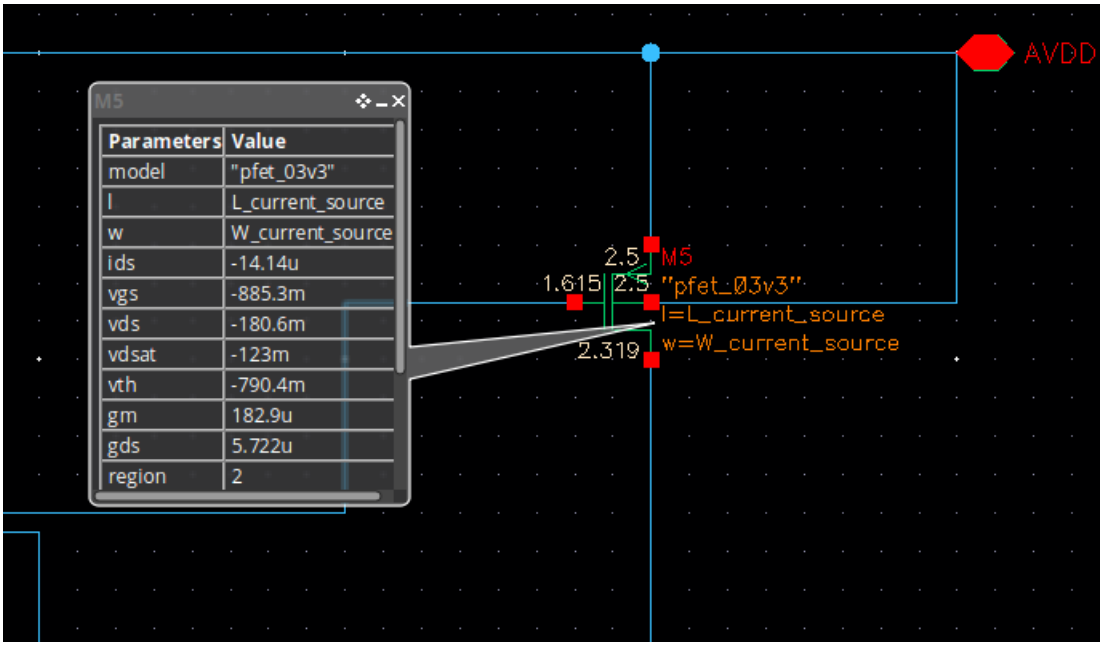
OTA

Input pair

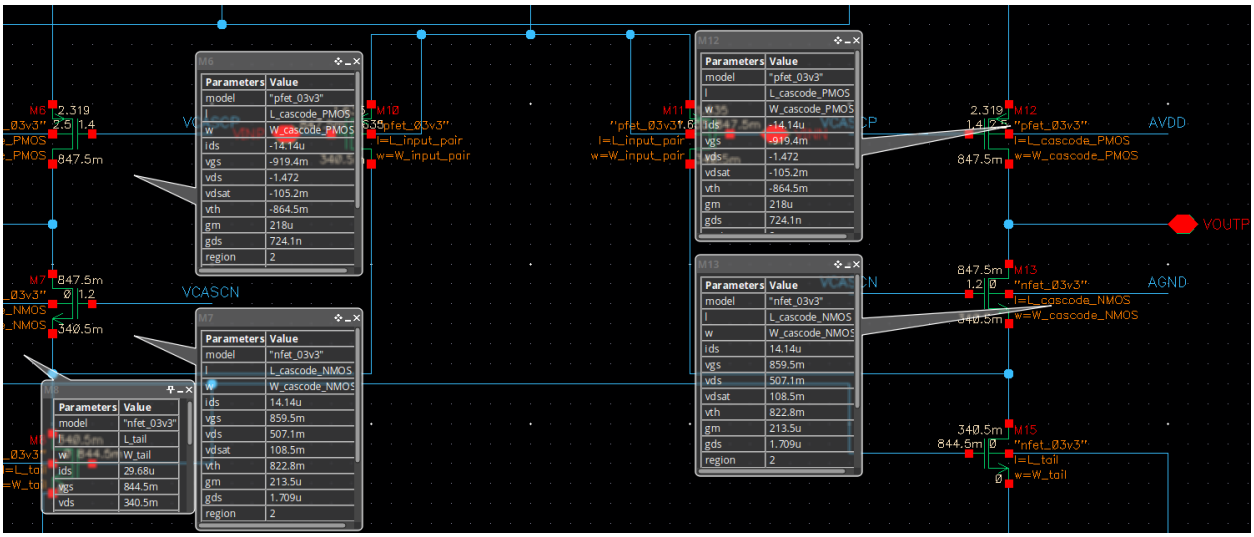


Current source

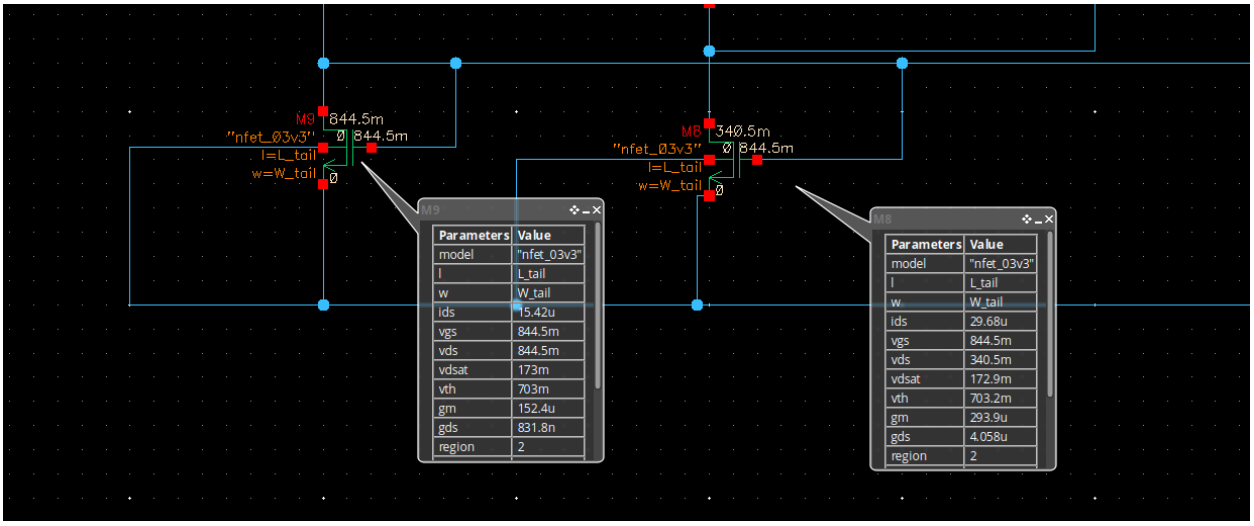


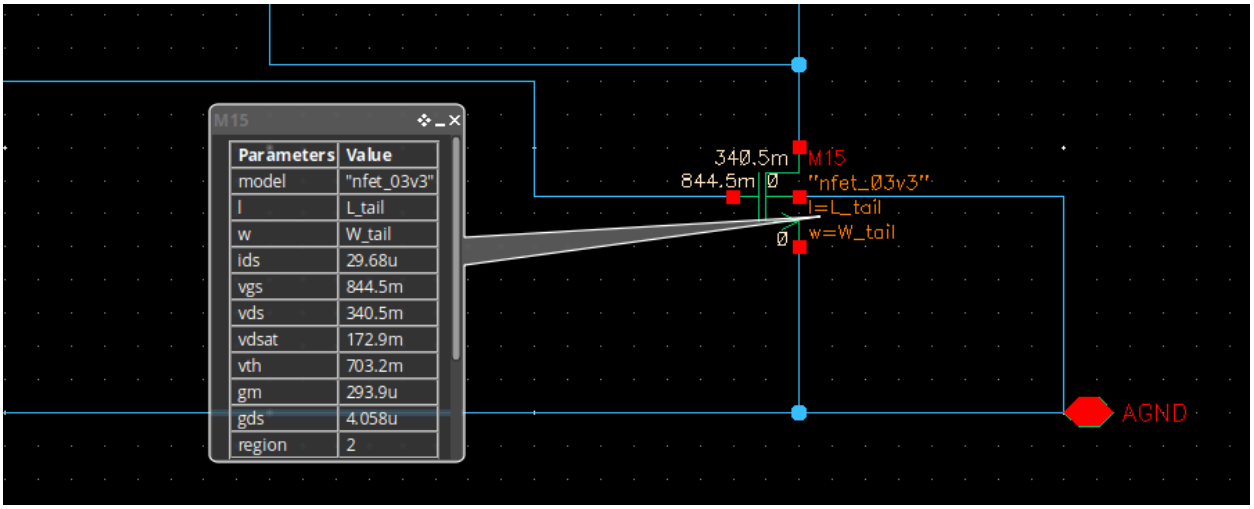

AVDD
M5
Parameters Value
model "pfet_03v3"
l L_current_source
w W_current_source
ids -14.14u
vgs -885.3m
vds -180.6m
vdsat -123m
vth -790.4m
gm 182.9u
gds 5.722u
region 2
2.5
1.615
2.5
M5
"pfet_03v3"
l=L_current_source
2.319
w=W_current_source

Cascode

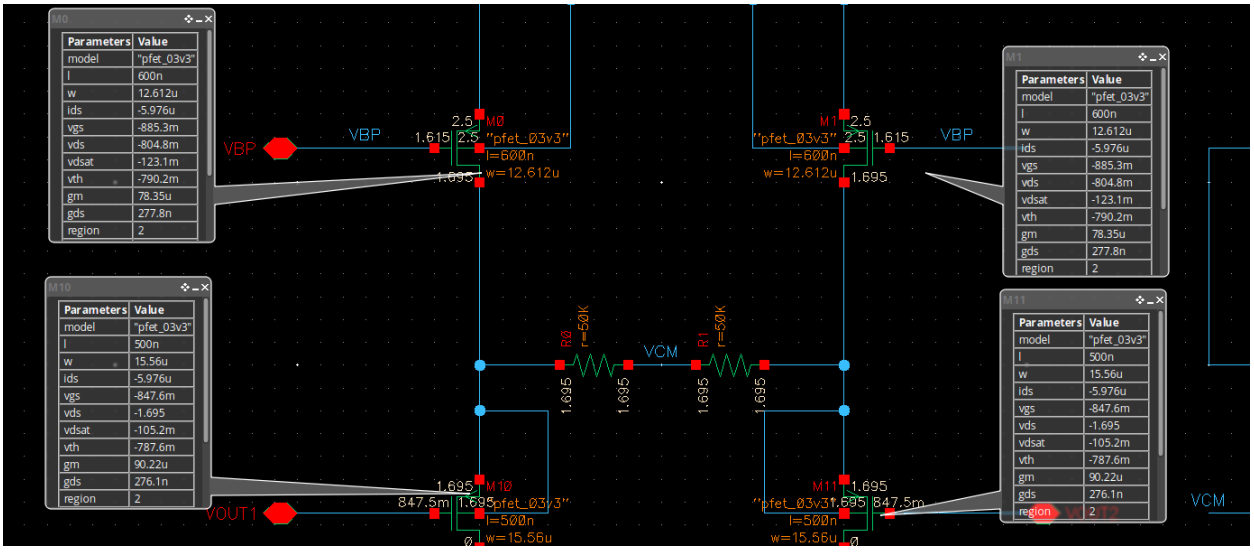

M6
Parameters Value
model "pfet_03v3"
l L_cascode_PMOS
w W_cascode_PMOS
ids -14.14u
vgs -919.4m
vds -1.472
vdsat -105.2m
vth -864.5m
gm 218u
gds 724.1n
region 2
M12
Parameters Value
model "pfet_03v3"
l L_cascode_PMOS
w W_cascode_PMOS
ids -14.14u
vgs -919.4m
vds -1.472
vdsat -105.2m
vth -864.5m
gm 218u
gds 724.1n
M13
Parameters Value
model "nfet_03v3"
l L_cascode_NMOS
w W_cascode_NMOS
ids 14.14u
vgs 859.5m
vds 507.1m
vdsat 108.5m
vth 822.8m
gm 213.5u
gds 1.709u
region 2
M7
Parameters Value
model "nfet_03v3"
l L_cascode_NMOS
w W_cascode_NMOS
ids 14.14u
vgs 859.5m
vds 507.1m
vdsat 108.5m
vth 822.8m
gm 213.5u
gds 1.709u
region 2
M8
Parameters Value
model "nfet_03v3"
l L_tail
w W_tail
ids 29.68u
vgs 844.5m
vds 340.5m
VCASCN
AVDD
AGND
VOUTP

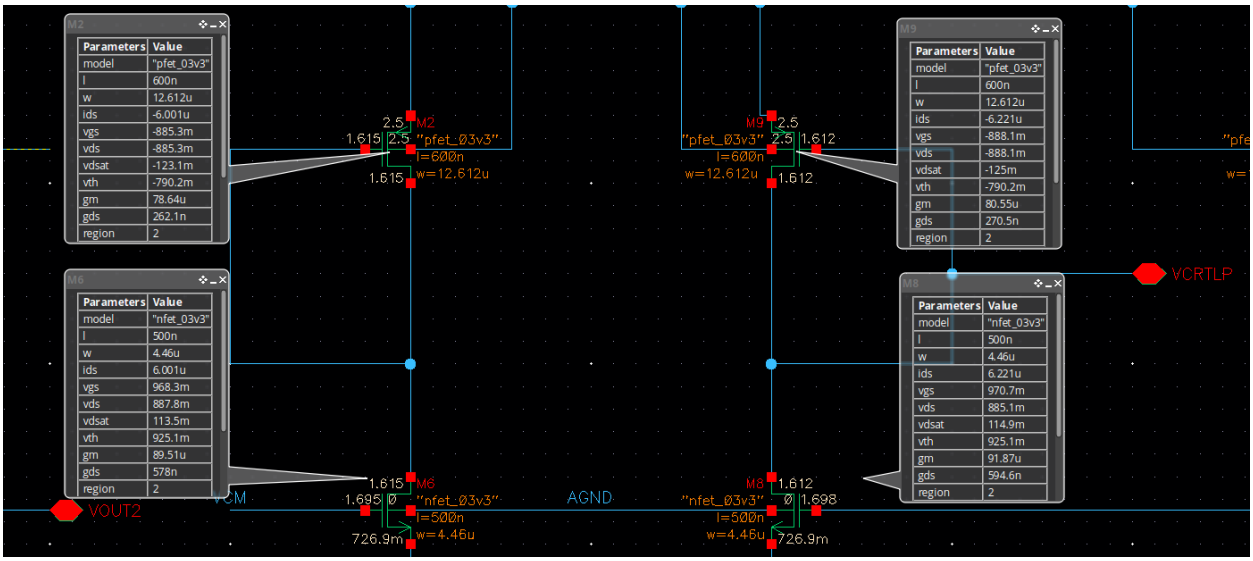
Tail

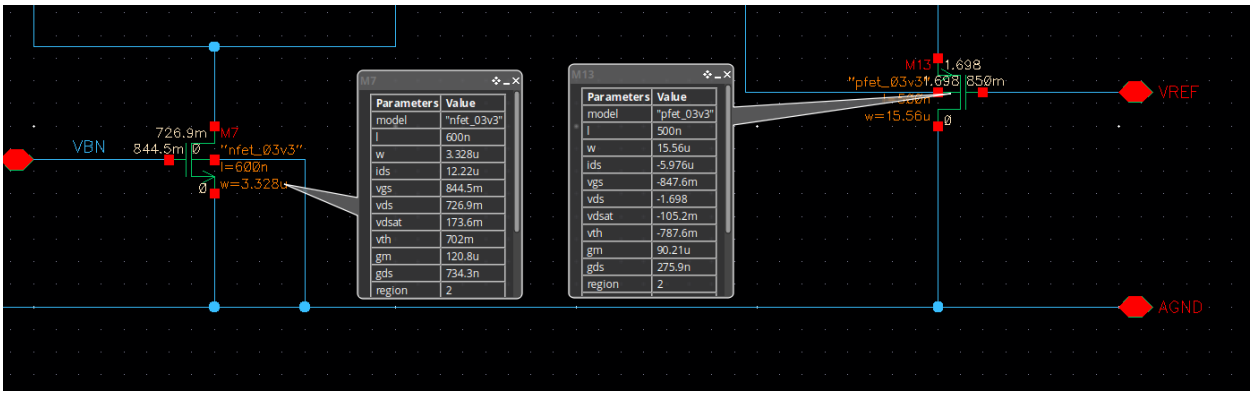

M9
844.5m
"nfet_03v3"
Ø
844.5m
l=L_tail
w=W_tail
Ø
M8
340.5m
"nfet_03v3"
Ø
844.5m
l=L_tail
w=W_tail
Ø
M9
Parameters Value
model "nfet_03v3"
l L_tail
w W_tail
ids 15.42u
vgs 844.5m
vds 844.5m
vdsat 173m
vth 703m
gm 152.4u
gds 831.8n
region 2
M8
Parameters Value
model "nfet_03v3"
l L_tail
w W_tail
ids 29.68u
vgs 844.5m
vds 340.5m
vdsat 172.9m
vth 703.2m
gm 293.9u
gds 4.058u
region 2

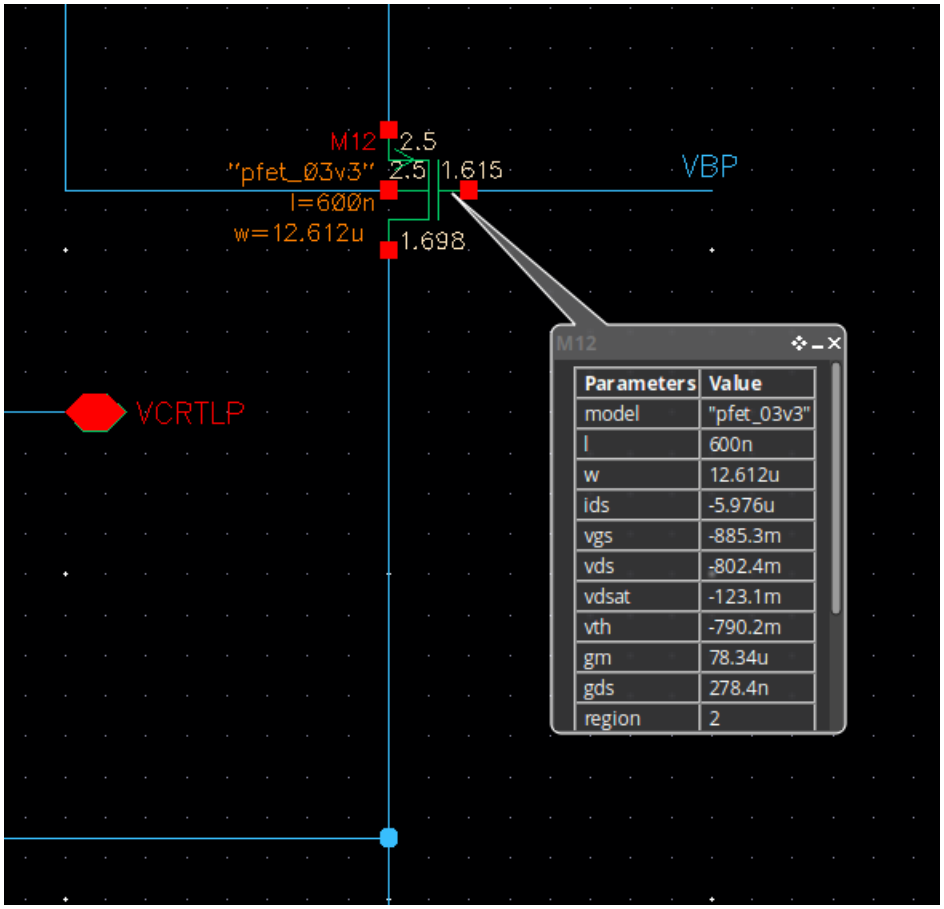

M15
Parameters Value
model "nfet_03v3"
l L_tail
w W_tail
ids 29.68u
vgs 844.5m
vds 340.5m
vdsat 172.9m
vth 703.2m
gm 293.9u
gds 4.058u
region 2
340.5m
M15
844.5m
Ø
"nfet_03v3"
l=L_tail
Ø
w=W_tail
AGND

CMFB


M0
Parameters Value
model "pfet_03v3"
l 600n
w 12.612u
ids -5.976u
vgs -885.3m
vds -804.8m
vdsat -123.1m
vth -790.2m
gm 78.35u
gds 277.8n
region 2
VBP
VBP
2.5
M0
1.615
2.5
"pfet_03v3"
l=600n
1.695
w=12.612u
M1
2.5
"pfet_03v3"
2.5
1.615
VBP
l=600n
w=12.612u
1.695
M1
Parameters Value
model "pfet_03v3"
l 600n
w 12.612u
ids -5.976u
vgs -885.3m
vds -804.8m
vdsat -123.1m
vth -790.2m
gm 78.35u
gds 277.8n
region 2
M10
Parameters Value
model "pfet_03v3"
l 500n
w 15.56u
ids -5.976u
vgs -847.6m
vds -1.695
vdsat -105.2m
vth -787.6m
gm 90.22u
gds 276.1n
region 2
R0
r=50K
VCM
R1
r=50K
1.695
1.695
1.695
1.695
M11
Parameters Value
model "pfet_03v3"
l 500n
w 15.56u
ids -5.976u
vgs -847.6m
vds -1.695
vdsat -105.2m
vth -787.6m
gm 90.22u
gds 276.1n
region 2
VOUT1
1.695
M10
847.5m
1.695
"pfet_03v3"
l=500n
Ø
w=15.56u
M11
1.695
"pfet_03v3"
1.695
847.5m
l=500n
w=15.56u
Ø
VCM

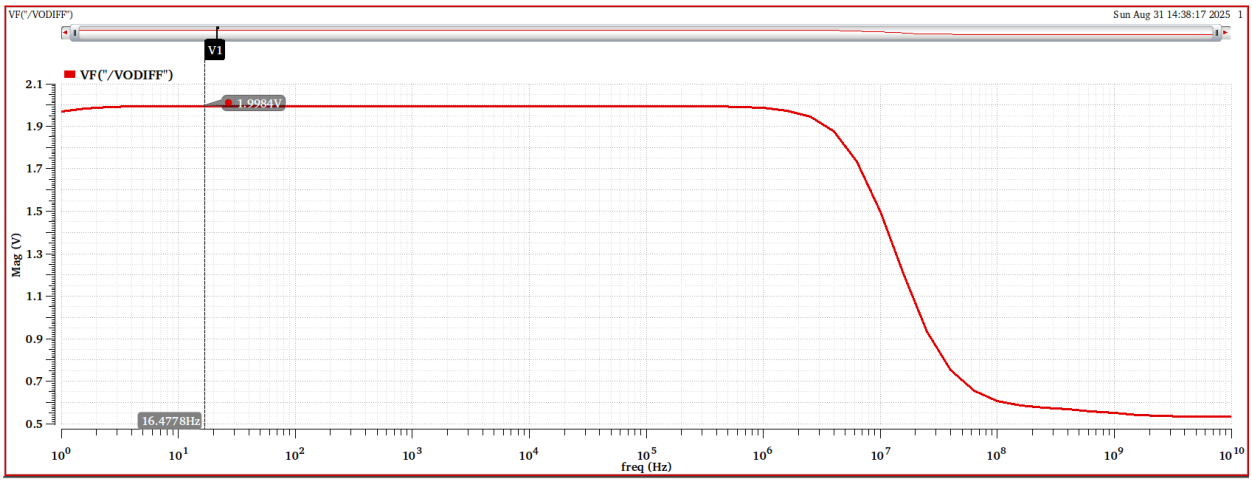

M2
Parameters Value
model "pfet_03v3"
l 600n
w 12.612u
ids -6.001u
vgs -885.3m
vds -885.3m
vdsat -123.1m
vth -790.2m
gm 78.64u
gds 262.1n
region 2
2.5 M2
1.615 2.5 "pfet_03v3"
l=600n
1.615 w=12.612u
M9
Parameters Value
model "pfet_03v3"
l 600n
w 12.612u
ids -6.221u
vgs -888.1m
vds -888.1m
vdsat -125m
vth -790.2m
gm 80.55u
gds 270.5n
region 2
M9 2.5
"pfet_03v3" 2.5 1.612
l=600n
w=12.612u 1.612
VCRTLP
M6
Parameters Value
model "nfet_03v3"
l 500n
w 4.46u
ids 6.001u
vgs 968.3m
vds 887.8m
vdsat 113.5m
vth 925.1m
gm 89.51u
gds 578n
region 2
M8
Parameters Value
model "nfet_03v3"
l 500n
w 4.46u
ids 6.221u
vgs 970.7m
vds 885.1m
vdsat 114.9m
vth 925.1m
gm 91.87u
gds 594.6n
region 2
VOUT2
VCM
1.615 M6
1.695 Ø "nfet_03v3"
l=500n
726.9m w=4.46u
AGND
M8 1.612
"nfet_03v3" Ø 1.698
l=500n
w=4.46u 726.9m


M7
Parameters Value
model "nfet_03v3"
l 600n
w 3.328u
ids 12.22u
vgs 844.5m
vds 726.9m
vdsat 173.6m
vth 702m
gm 120.8u
gds 734.3n
region 2
M13
Parameters Value
model "pfet_03v3"
l 500n
w 15.56u
ids -5.976u
vgs -847.6m
vds -1.698
vdsat -105.2m
vth -787.6m
gm 90.21u
gds 275.9n
region 2
VBN
726.9m M7
844.5m Ø "nfet_03v3"
l=600n
Ø w=3.328u
M13 1.698
"pfet_03v3" 1.698 850m
w=15.56u Ø
VREF
AGND



The common mode voltage at both the input and output of the OTA is 847.5 mV, which is nearly equal to V_{ref}. The output common mode level is directly set by the CMFB circuit, while the input is forced to the same potential through the DC feedback resistors R_f that provide a negative feedback path for the common mode signal. The input capacitances block any external DC component, ensuring that VICM = VOCM.

Differential closed-loop response

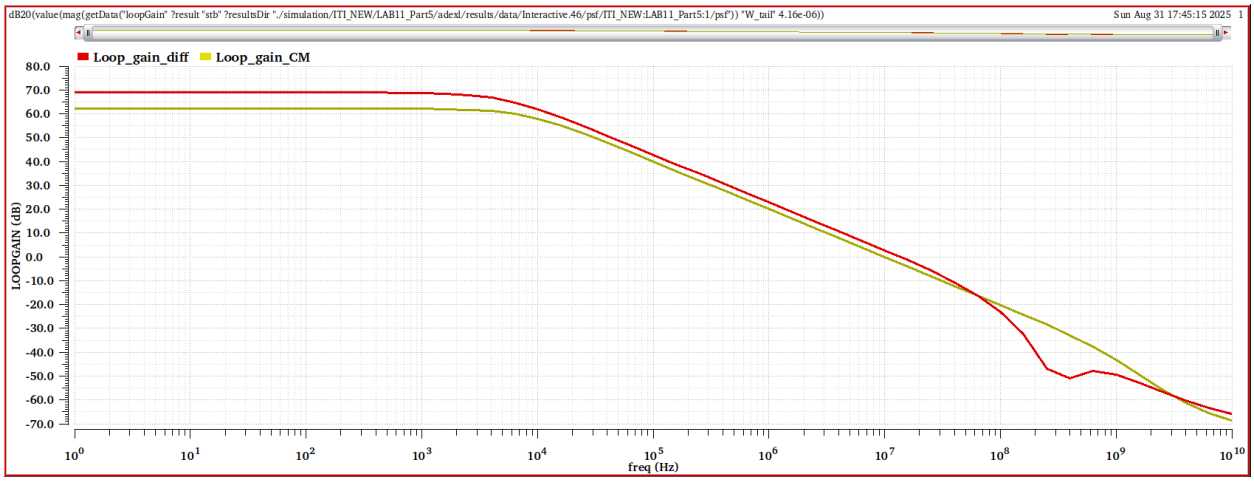


Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI_NEW:LAB11_Part5:1	Ao_magnitude				
ITI_NEW:LAB11_Part5:1	Ao_phase				
ITI_NEW:LAB11_Part5:1	Bandwidth	12.01M			

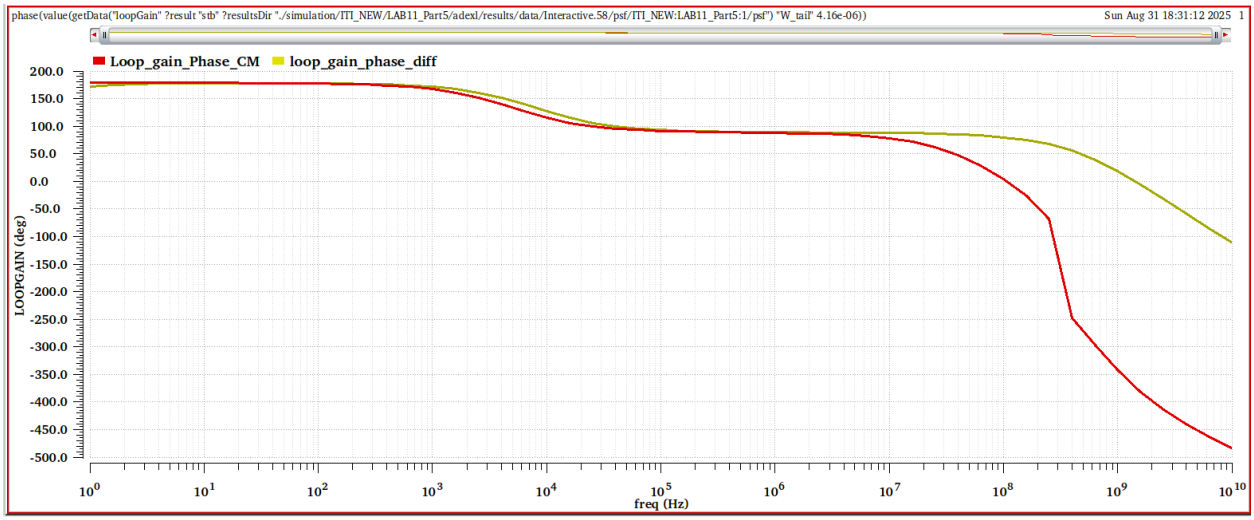
ITI_NEW:LAB11_Part5:1	Ao_dB				
ITI_NEW:LAB11_Part5:1	Ao_linea	1.998			
ITI_NEW:LAB11_Part5:1	fu	22.88M			
ITI_NEW:LAB11_Part5:1	Phase margin	84.09			

Differential and CMFB loops stability (STB analysis)

Loop gain overlaid



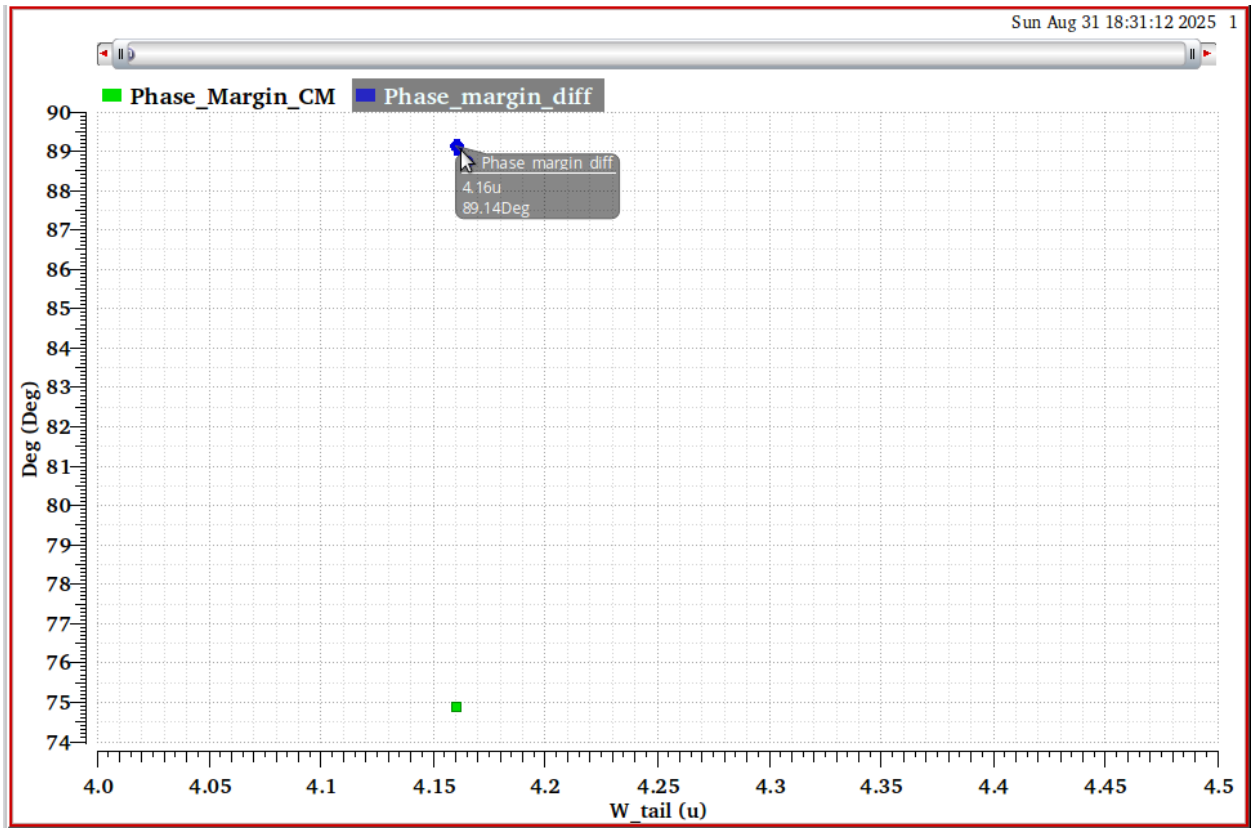
Loop gain phase overlaid



GBW and PM of both the DIFF and CM loops

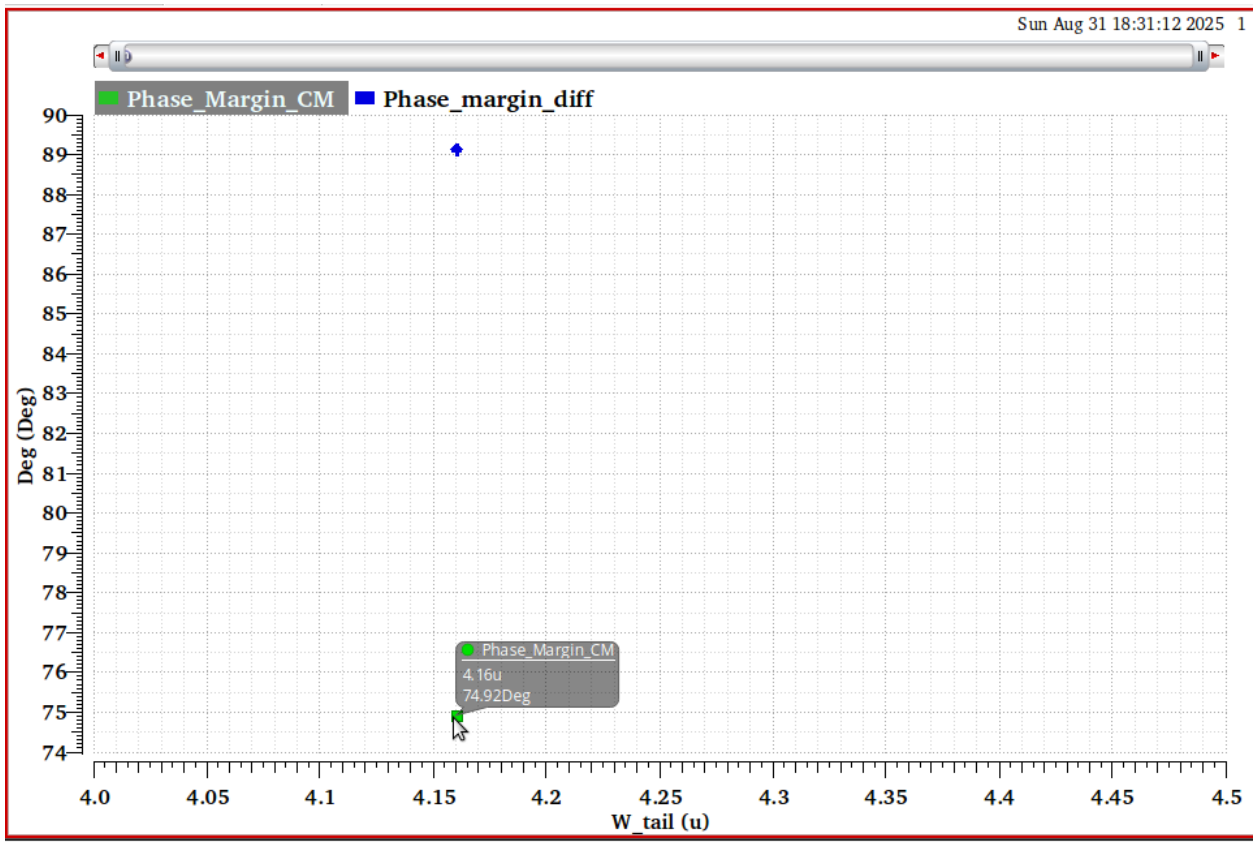
1. DIFF loop

ITI_NEW:LAB11_Part5:1	gainBwProd(mag(getData("lo...	10.31M			



2. CM loop

ITI_NEW:LAB11_Part5:1	gainBwProd(mag(getData("lo...	14.46M			



Comment:

The CM loop has extra non-dominant poles, those poles add phase lag near fu which makes the phase margin decreases

DC loop gain= open loop gain × β

Open loop gain=4575 , $\beta = \frac{1}{3}$

DC loop gain=63.66dB

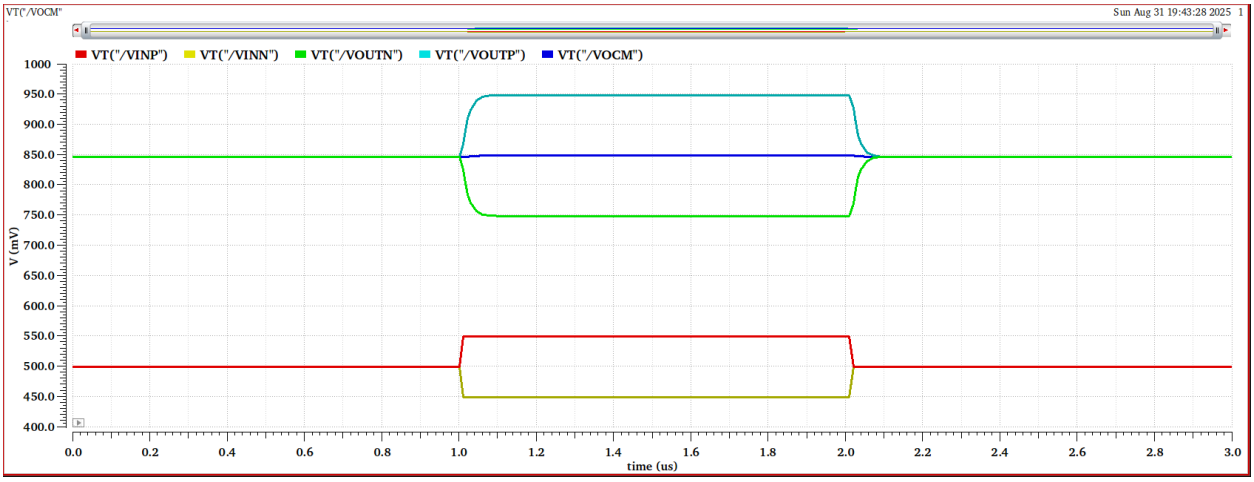
$parameter$	Open loop simulation value	Close loop simulation value
$DC\ loop\ gain$	63.66 dB	64 dB
GBW	69.32MHz	10.31MHz

Comment:

1. The DC loop gain is higher in the closed-loop simulation compared to the open-loop case because the feedback network stabilizes the operating point, leading to more effective utilization of the amplifier's gain.
2. the GBW is much higher in the open-loop simulation compared to the closed-loop, since closing the loop trades bandwidth for stability and accurate gain.

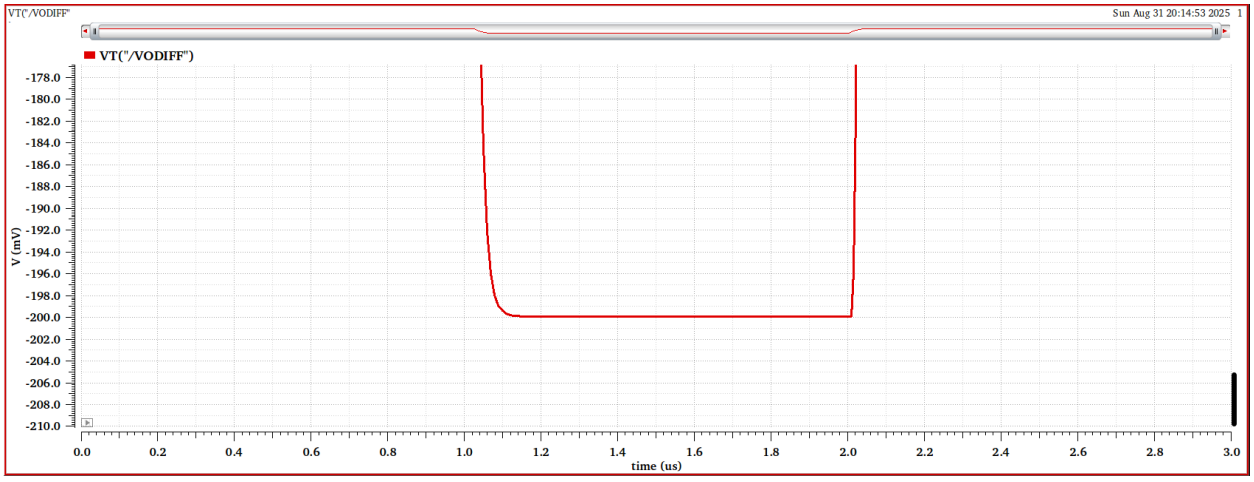
PART 6: Closed Loop Simulation (Transient Analysis)

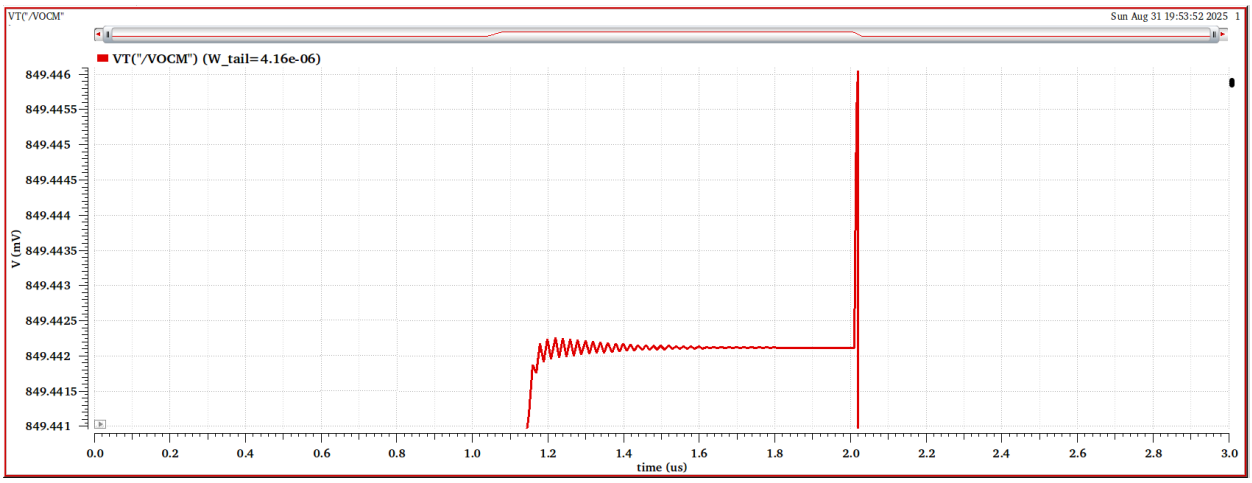
VINP, VINN, VOUTP, VOUTN, and VOCM



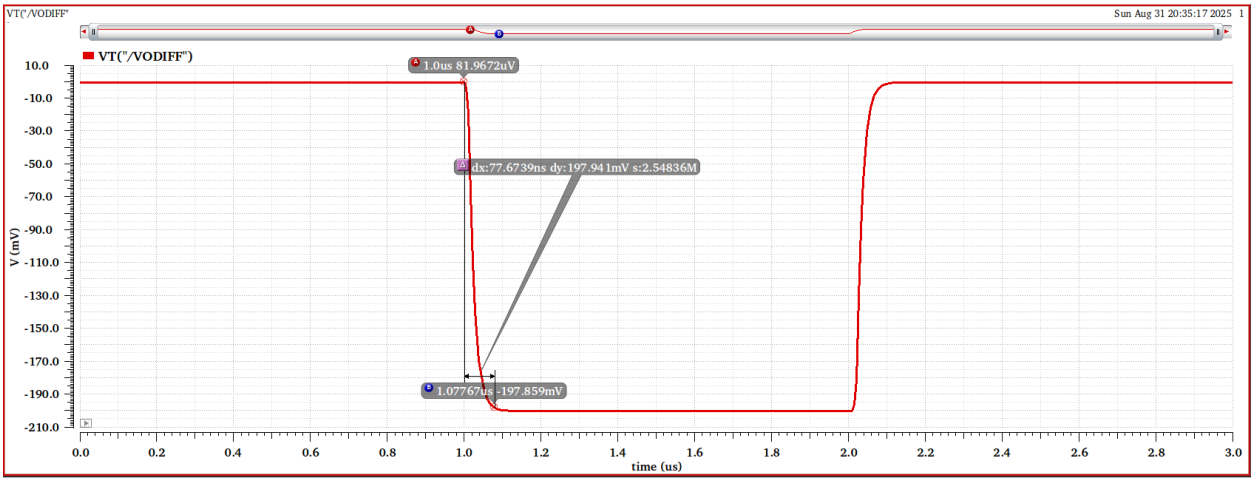
Comment:

The zoomed-in transient responses show noticeable ringing in the common mode output signal, whereas the differential output remains well-damped with no visible ringing. This difference arises because the CM loop typically has lower phase margin compared to the differential loop, making it more susceptible to underdamped behavior and oscillatory tendencies.





Settling time

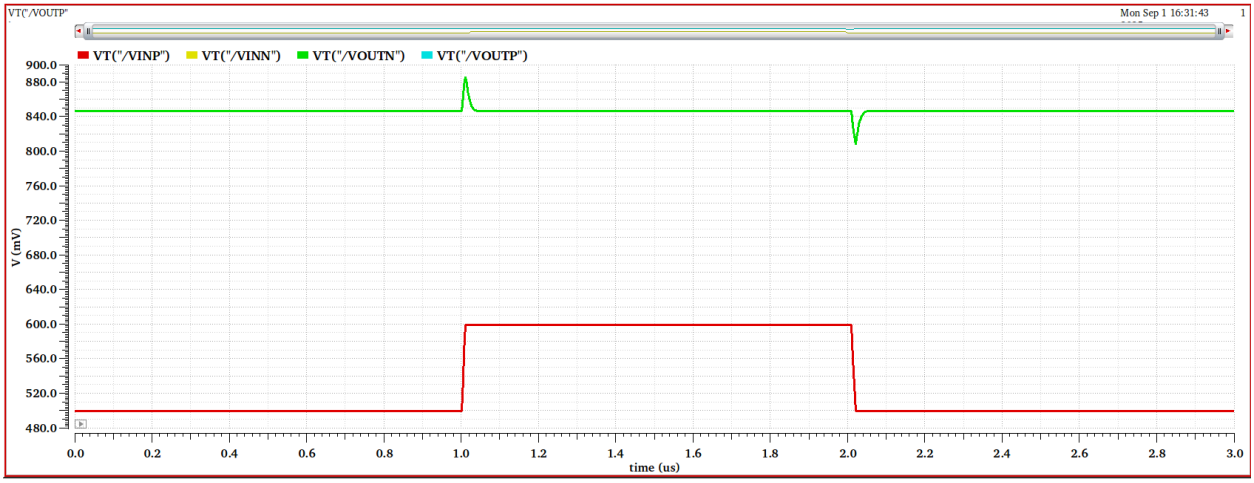


The value of the settling time is 78ns which is $\leq 100ns$ (spec is satisfied)

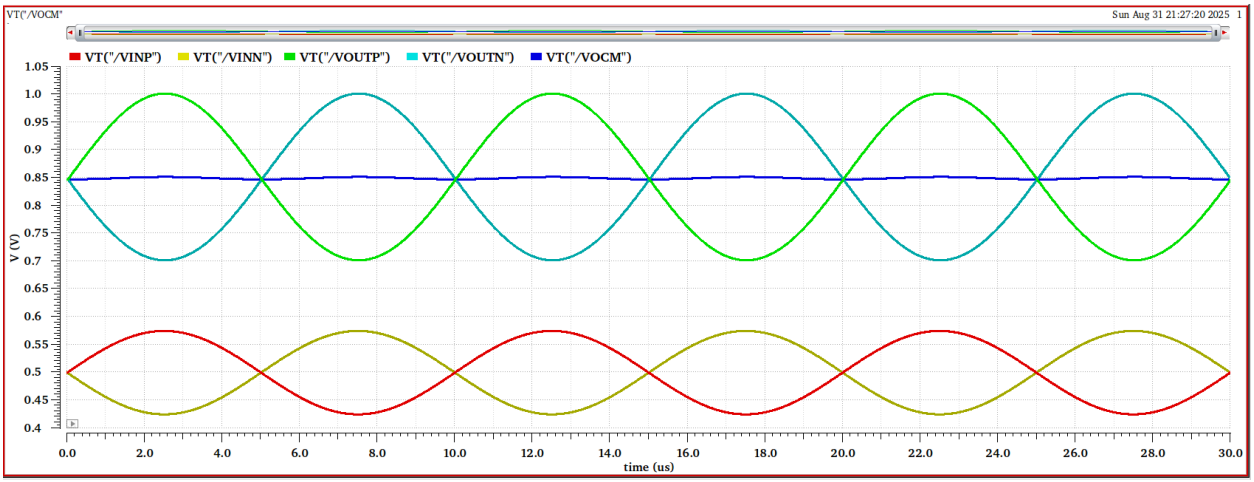
Differential and CMFB loops stability (transient analysis)

Comment:

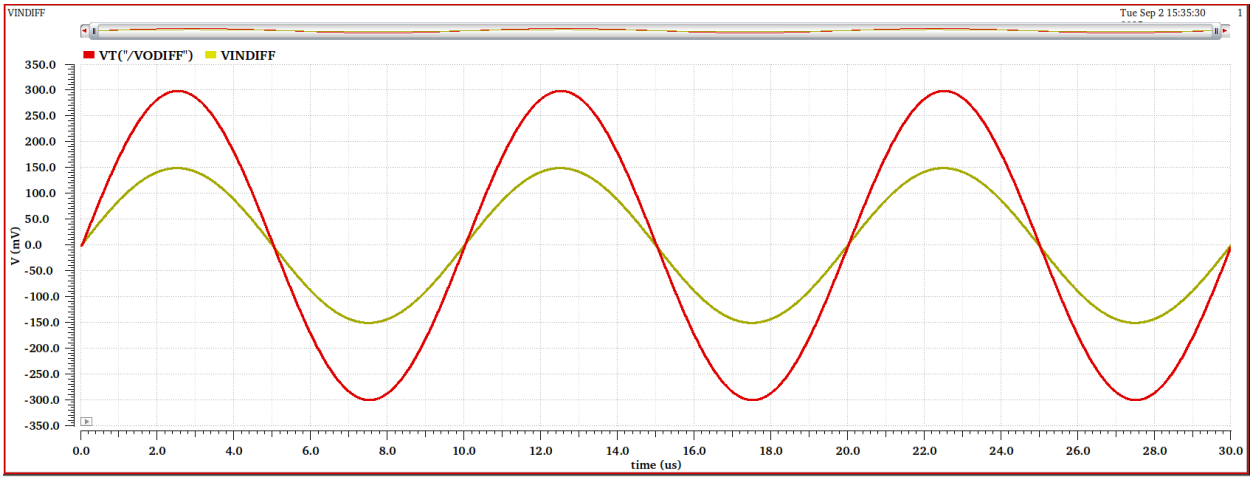
From the obtained graph, it is observed that the output voltage exhibits an overshoot. This occurs because the input common-mode level changes suddenly due to the applied voltage source, causing the output to respond with a sudden shift. The CMFB circuit then acts to restore the output to its nominal level, which results in the observed overshoot



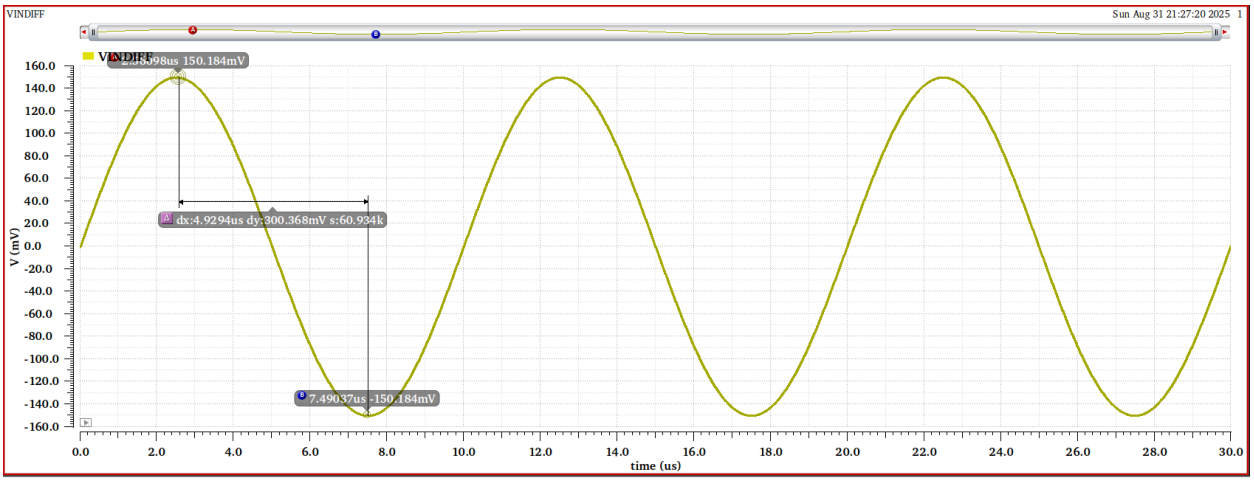
Output swing

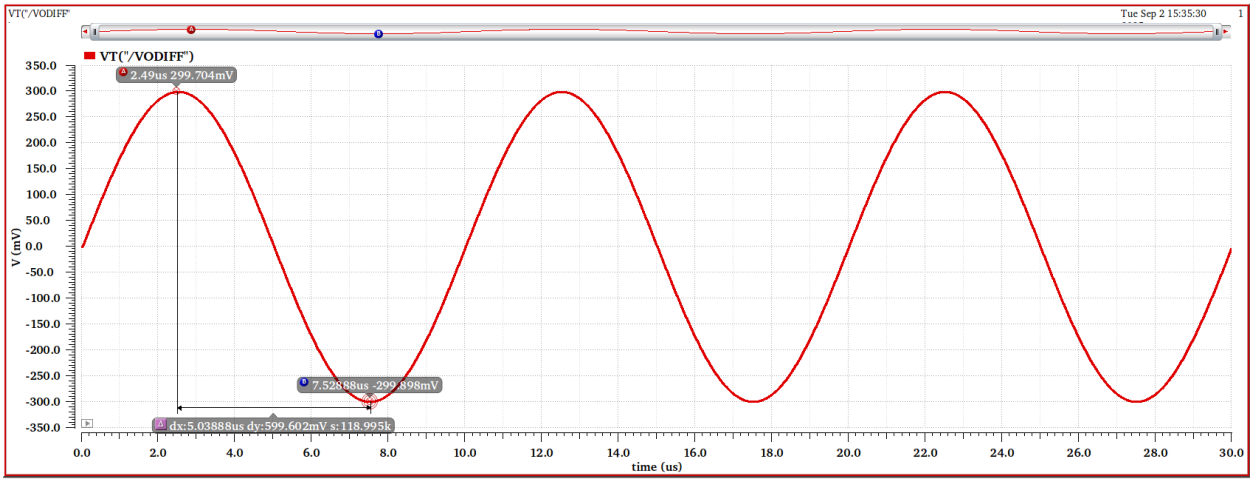


Vindiff and voutdiff overlaid



Peak to peak





Loop gain

$$Loop\ gain = \frac{peak - to - peak\ of\ VODIFF}{peak - to - peak\ of\ VIDIFF}$$

$$Loop\ gain = \frac{599.602}{300.368}$$

$$Loop\ gain = 1.9962$$