ITI

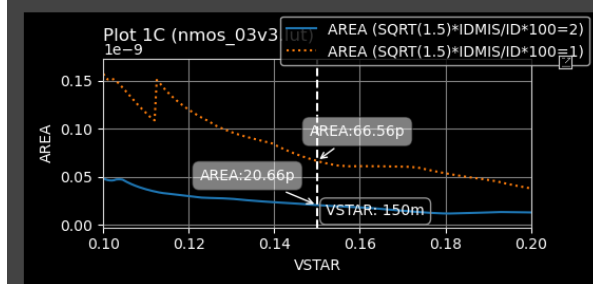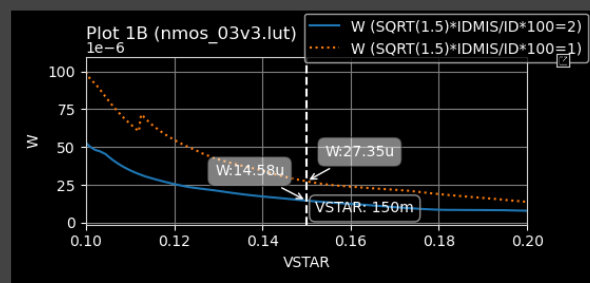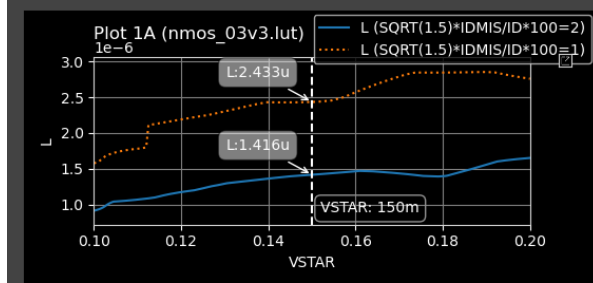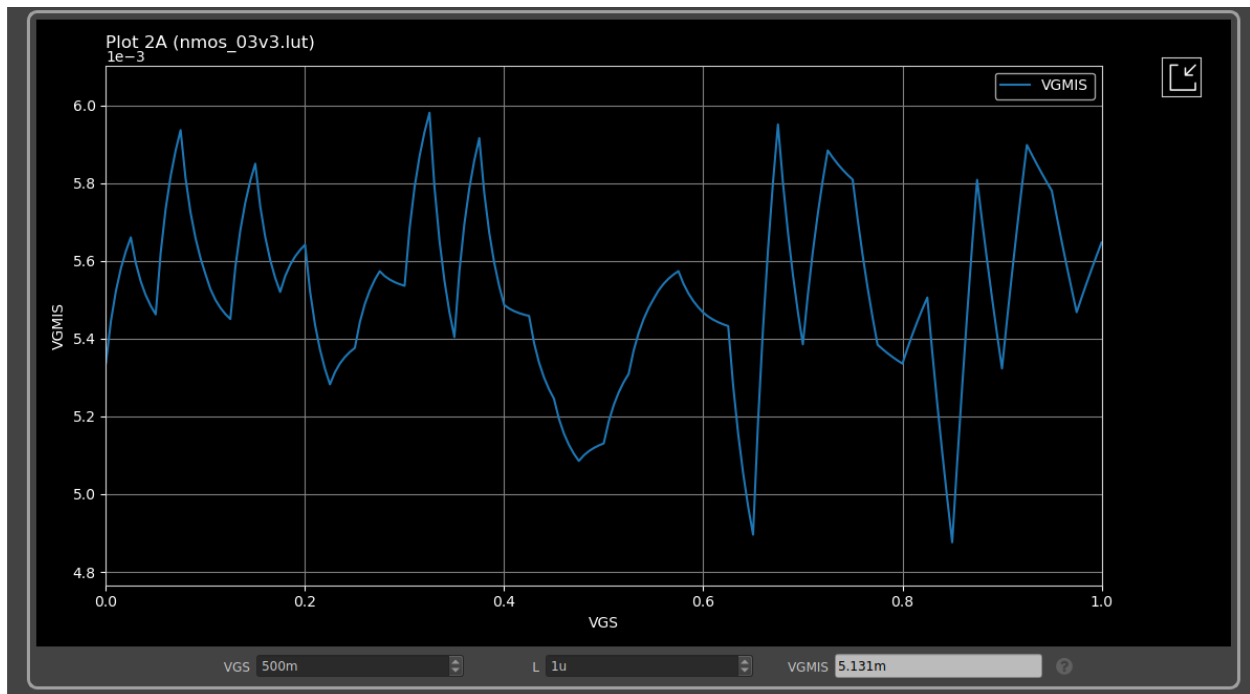LAB 5

Simple vs Wide Swing (Low Compliance)

Cascode Current Mirror

Contents

Part 1: Exploring Sizing Tradeoffs Using SA
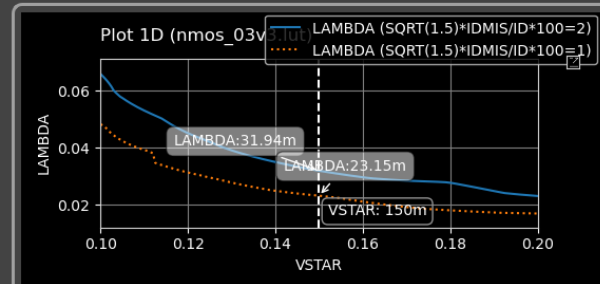
From the above graphs $W = 14.58\ \mu m$, $L = 1.416\ \mu m$

```
734 ********************************************************************************
735 * 3.3V NMOS Models
736 ********************************************************************************
737 *
738 .lib nmos_3p3_t
739
740
741 .subckt nmos_3p3_sab d g s b w=10u l=0.28u par=1 s_sab=0.48u d_sab=1.78u as=0 ad=0 ps=0 pd=0 nrd=0 nrs=0 dtemp=0 nf=1 sa=0 sb=0 sd=0 m=1
742
743 .param
744 + par_vth=0.007148
745 + par_k=0.007008
746 + par_l=1.5e-7
747 + par_w=-1e-7
748 + par_leff='l-par_l'
749 + par_weff='par*(w-par_w)'
750 + p_sqrtarea='sqrt((par_leff)*(par_weff))'
751
752 .param
753 + var_k='0.7071*par_k* 1e-06 / p_sqrtarea'
754 + mis_k=agauss(0,var_k,1)
755
756 .param
757 + var_vth='0.7071*par_vth* 1e-06 / p_sqrtarea'
758 + mis_vth=agauss(0,var_vth,1)
759
760 xr1 d d1 b nplus_u_m1 wr='w' lr='(d_sab==0) ? 1e-15 : d_sab'
761 xr2 s s1 b nplus_u_m1 wr='w' lr='(s_sab==0) ? 1e-15 : s_sab'
762
763
764 m0 d1 g s1 b nmos_3p3 w='w' l='l' as=as ad=ad ps=ps pd=pd nrd=nrd nrs=nrs nf=nf sa=sa sb=sb sd=sd
765 +delvto='mis_vth*sw_stat_mismatch'
766 .ends
767
768
769 .model  nmos_3p3.0  nmos
770 +level = 54
771 +lmin    = 2.8e-007
772 +lmax    = 5e-007
773 +wmin    = 2.2e-007
774 +wmax    = 5e-007
775 +version = 4.5
776 +binunit = 2
777 +paramchk= 1
```

$$L = 1\mu m \quad W = 1\mu m$$

$$L_{eff} = L - par_{leff} \quad L_{eff} = 8.5 \times 10^{-7}$$

$$W_{eff} = par(W - par_w) \quad W_{eff} = 1.1 \times 10^{-6}$$

$$p_{sqerarea} = \sqrt{par_{leff} \times par_{weff}}$$

$$p_{sqerarea} = 9.67 \times 10^{-7}$$

$$VGMIS = \frac{0.7071 \times par_{vth} \times 1 \times 10^{-6}}{p_{sqerarea}}$$

$$VGMIS = 5.23mV$$

Part 2: Current Mirror Simulation

Schematic

R_B calculation

Since $R_B = \frac{V_{DS3}}{I_B}$, $V_{DS3} = V^* + 50mV$, $V^* = 150mV$

$R_B = 20K\Omega$

From the graph the value of $R_B = 27.25K\Omega$

Comment: The simulated value of R_B is larger than the analytical value. This discrepancy is expected because the analytical calculation typically involves simplifying ,while In contrast, the simulation considers more accurate transistor models and mismatch effects, which often result in a higher R_B to meet the same performance targets.

| Transistor	Vds	Vdsat	Region
M1	0.9	0.7573	Saturation
M2	0.7573	0.1197	Saturation
M3	0.2	0.1209	Saturation
M4	0.1998	0.1209	Saturation
M5	0.7	0.1219	Saturation
M6	0.5595	0.1121	Saturation

DC Sweep ($Iout$ vs VOUT)
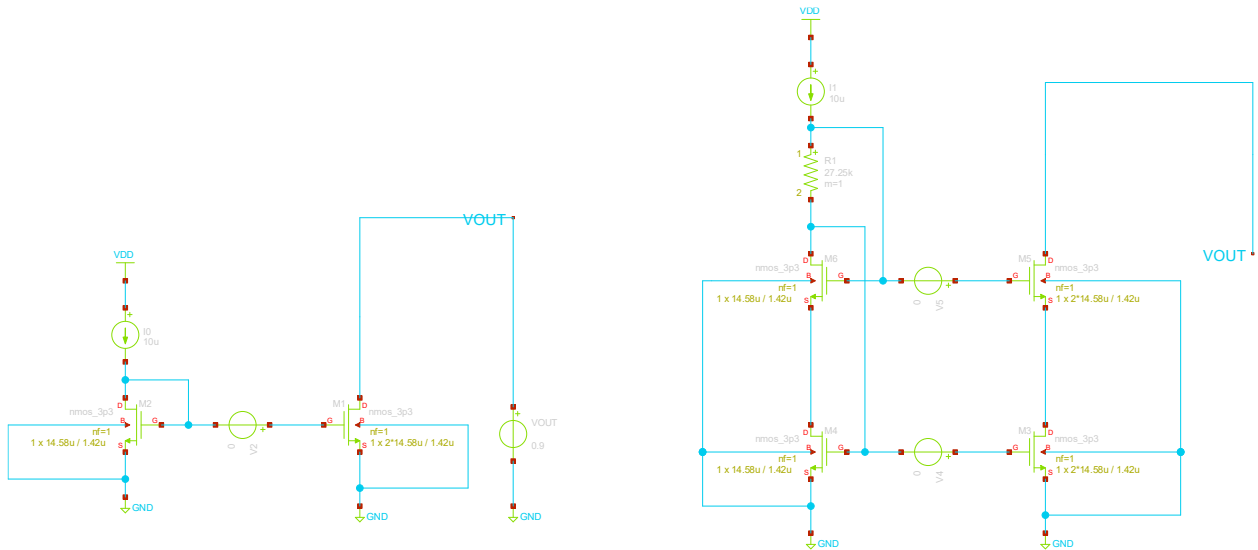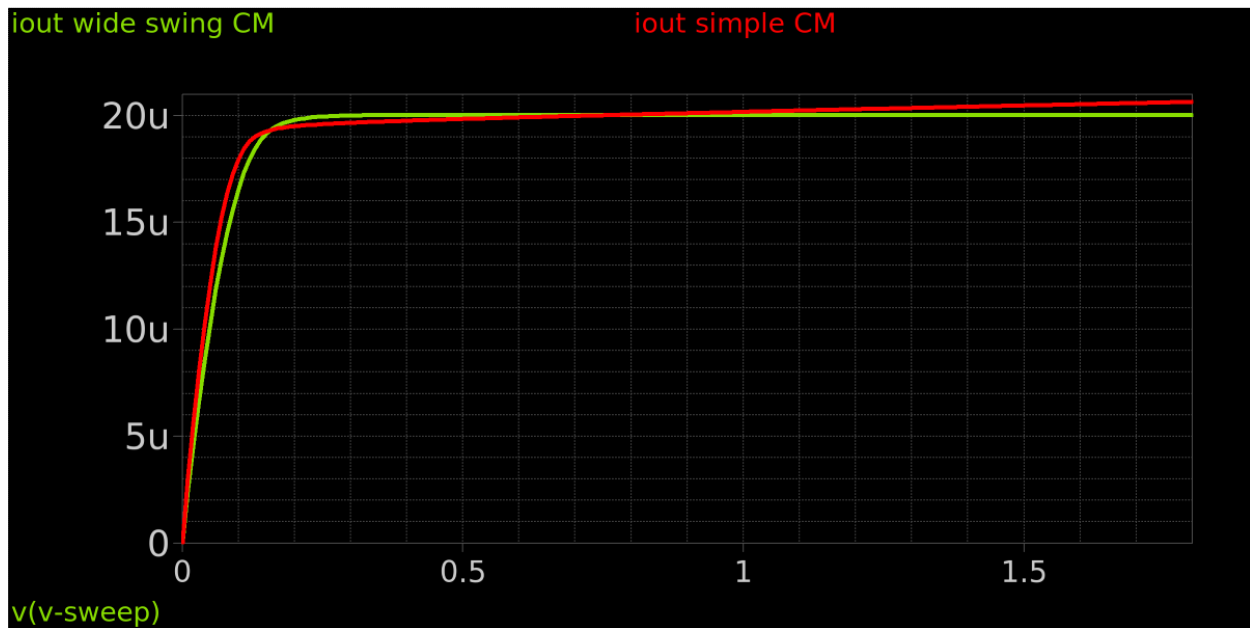
Comment:

When comparing the Iout vs. Vout characteristics of the simple current and the wide swing CM, we observe that in the simple CM, Iout continues to increase approximately linearly with Vout beyond a certain point. This indicates poor output resistance and weak current regulation.

In contrast, the wide swing CM shows that Iout becomes constant after a certain Vout, reflecting much better current regulation and higher output resistance. This behavior is due to the cascode structure maintaining the output transistor in saturation over a wider voltage range, thereby achieving improved output characteristics.
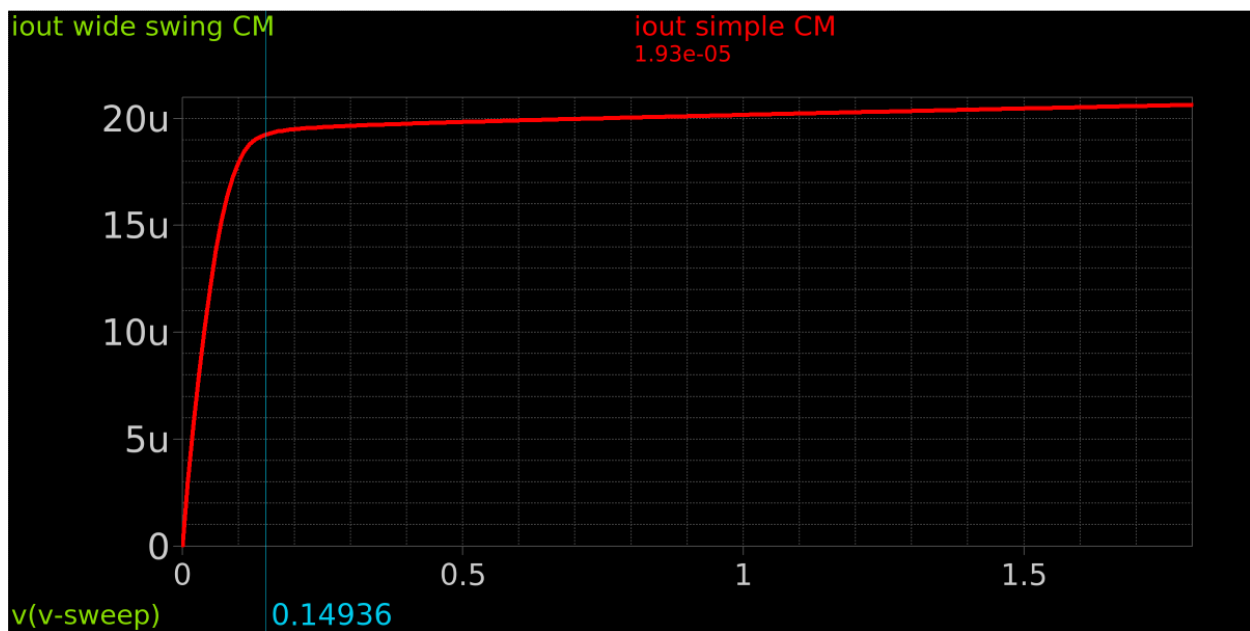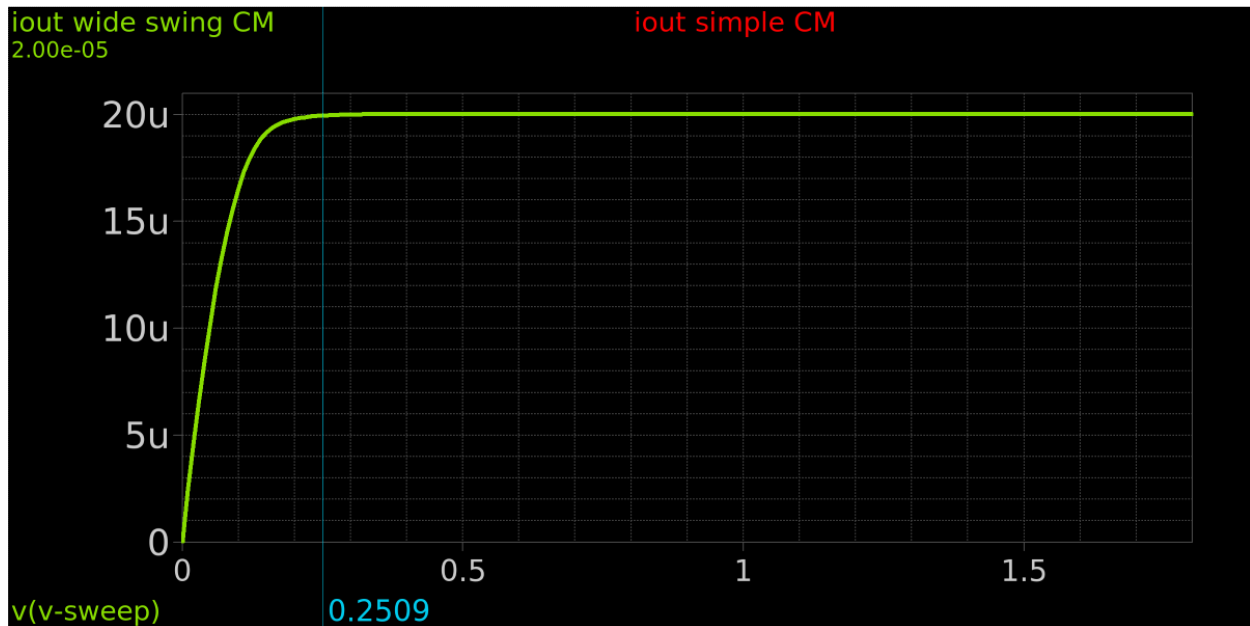
From the above 2 graphs,

$V_{compliance}(Simple\ CM)$=0.15V

$V_{compliance}(Wide\ swing\ CM)$= 0.251V

| 5.000000e-01 | 1.983372e-05 | 1.500000e+00 | 2.046570e-05 |

Figure 1 Iout at Vds=0.5V   *Figure 2 Iout at Vds=1.5V*
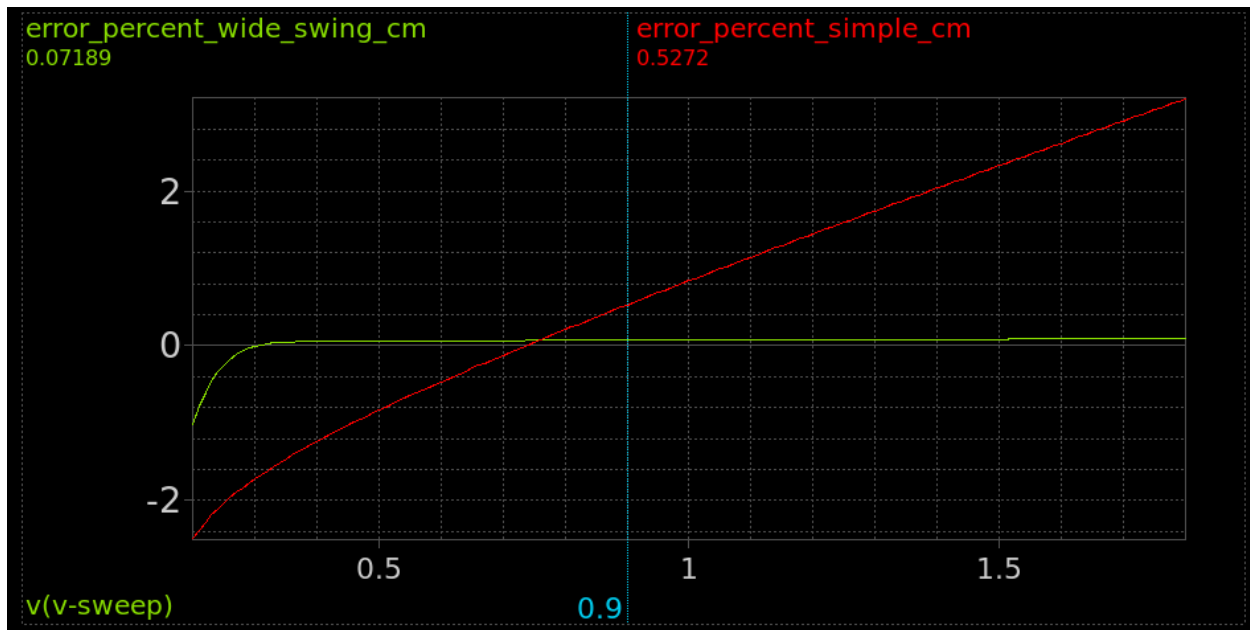
$$\Delta I = \frac{2.0465 - 1.9833}{2} \times 100$$

$$\Delta I = 3.16\%$$

| 7.400000e-01 | 2.000230e-05 |

*Figure 3 Vds at Iout=2IB*

$$I_{out} = 2\ I_B\ at\ Vout = 0.74V\ which\ is\ Vds\ of\ the\ transistor$$

Comment: The error percentage between IB and Iout is noticeably higher in the Simple Current Mirror, particularly at higher output voltages. This is primarily due to the limited output resistance and reduced compliance range, which causes Iout to deviate more significantly from the bias current as Vout increases.

In contrast, the Wide-Swing Current Mirror demonstrates significantly lower error percentages across a wider range of Vout. This improvement is due to its enhanced output impedance and increased output voltage swing capability, which allows it to better maintain Iout close to the bias current.
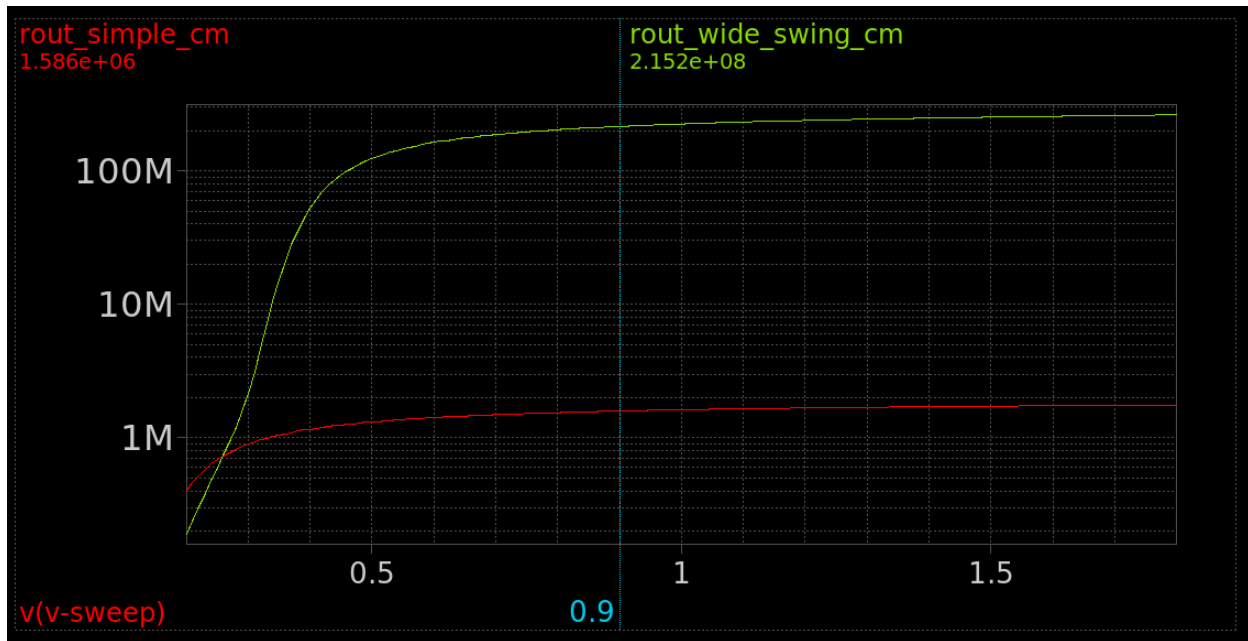
- Comment: The output resistance Rout of the Wide-Swing Current Mirror is significantly higher than that of the Simple Current Mirror. This is evident from the flatter Iout vs. Vout characteristic in the wide-swing design, indicating better current source behavior. In the Simple CM, Rout is limited by the intrinsic output resistance of a single MOSFET, resulting in a noticeable slope in the Iout vs. Vout curve. On the other hand, the Wide-Swing CM uses a cascode-like configuration that improves the output impedance by reducing the effect of Vout on the current. This leads to a more constant Iout, especially at higher Vout, and confirms that the wide-swing mirror offers superior performance in terms of output resistance.
- In both the simple and wide-swing current mirror topologies, Rout initially varies with Vout, but then becomes approximately constant beyond a certain Vout level. This behavior suggests that at lower output voltages, the transistors are transitioning between regions which affects output resistance. As Vout increases and the transistors settle into the saturation region, Rout stabilizes and becomes nearly independent of Vout.

Analytically Calculating the value of R_{out}

a) R_{out} of the simple current mirror

$$R_{out} = \frac{1}{g_{ds1}}, g_{ds1} = 6.305 \times 10^{-7}$$

$$R_{out} = 1.58M\Omega$$

b) R_{out} of the wide swing CM

$$R_{out} = r_{o5}(1 + (g_{m5} + g_{mb5})\, r_{o3}),$$

$$g_{ds5} = 6.578 \times 10^{-7}, g_{m5} = 2.694 \times 10^{-4}, g_{mb5} = 9.539 \times 10^{-5},$$

$$g_{ds3} = 2.6041 \times 10^{-6}$$

$$R_{out} = 2.145 \times 10^{8}\ \Omega$$

Mismatch

Calculating the value of the range of VMIS

VMIS will be swept from 0 to $\frac{\sqrt{1.5 \times 3.5 \times 10^{-3}}}{\sqrt{W \times L \times 10^{12}}}$, $W = 14.58\ \mu m$, $L = 1.416\ \mu m$
then VMIS will be swept from 0 to 942mV

1. Sweeping VMIS1 and making VMIS2=0

Monitoring the change of Iout of the simple CM

```
0.000000e+00     2.010544e-05  9.400000e-04     2.036020e-05
```

The percent of change in I $=\frac{I|0 - I|vgmis}{I|0} \times 100$

Change=1.25%

Monitoring the change of Iout of the wide swing CM

```
0.000000e+00     2.001438e-05  9.400000e-04     2.026462e-05
```

The percent of change in I $=\frac{I|0 - I|vgmis}{I|0} \times 100$

Change=1.25%

2. Sweeping VMIS2 and making VMIS1=0

Monitoring the change of Iout of the wide swing CM
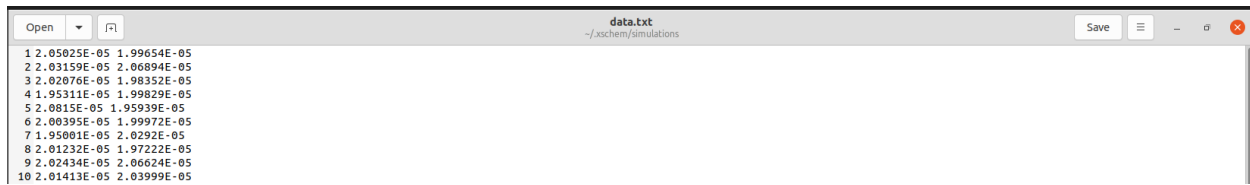
```
0.000000e+00      2.001438e-05    9.400000e-04      2.001616e-05
```

The percent of change in $I = \frac{I|0 - I|vgmis}{I|0} \times 100$

Change = 8.89×10^{-3} %

Monte Carlo (MC) Simulation

data.txt
~/.xschem/simulations

```
1 2.05025E-05 1.99654E-05
2 2.03159E-05 2.06894E-05
3 2.02076E-05 1.98352E-05
4 1.95311E-05 1.99829E-05
5 2.0815E-05 1.95939E-05
6 2.00395E-05 1.99972E-05
7 1.95001E-05 2.0292E-05
8 2.01232E-05 1.97222E-05
9 2.02434E-05 2.06624E-05
10 2.01413E-05 2.03999E-05
```

MATLAB code

```matlab
% Load the data from text file
data = load('data.txt');

% Separate the two columns
col1 = data(:,1);
col2 = data(:,2);

% BinWidth
binWidth = 5e-8;

% Compute mean and standard deviation
mean1 = mean(col1);
std1 = std(col1);
std_percent1 = (std1 / mean1) * 100;

mean2 = mean(col2);
std2 = std(col2);
std_percent2 = (std2 / mean2) * 100;

% Create histograms with Gaussian fits
figure;

subplot(2,1,1);
histogram(col1, 'BinWidth', binWidth, 'Normalization', 'pdf');
hold on;
x1 = linspace(min(col1), max(col1), 1000);
y1 = normpdf(x1, mean1, std1);
plot(x1, y1, 'r', 'LineWidth', 1.5);
title(sprintf('Iout of the simple CM (Std Dev = %.3f%%)', std_percent1));
xlabel('Value');
ylabel('Probability Density');
```

```
subplot(2,1,2);
histogram(col2, 'BinWidth', binwidth, 'Normalization', 'pdf');
hold on;
x2 = linspace(min(col2), max(col2), 1000);
y2 = normpdf(x2, mean2, std2);
plot(x2, y2, 'r', 'LineWidth', 1.5);
title(sprintf('Iout of the wide swing CM (Std Dev = %.3f%%)', std_percent2));
xlabel('Value');
ylabel('Probability Density');
```