

ITI
LAB09
Two-Stage Miller OTA

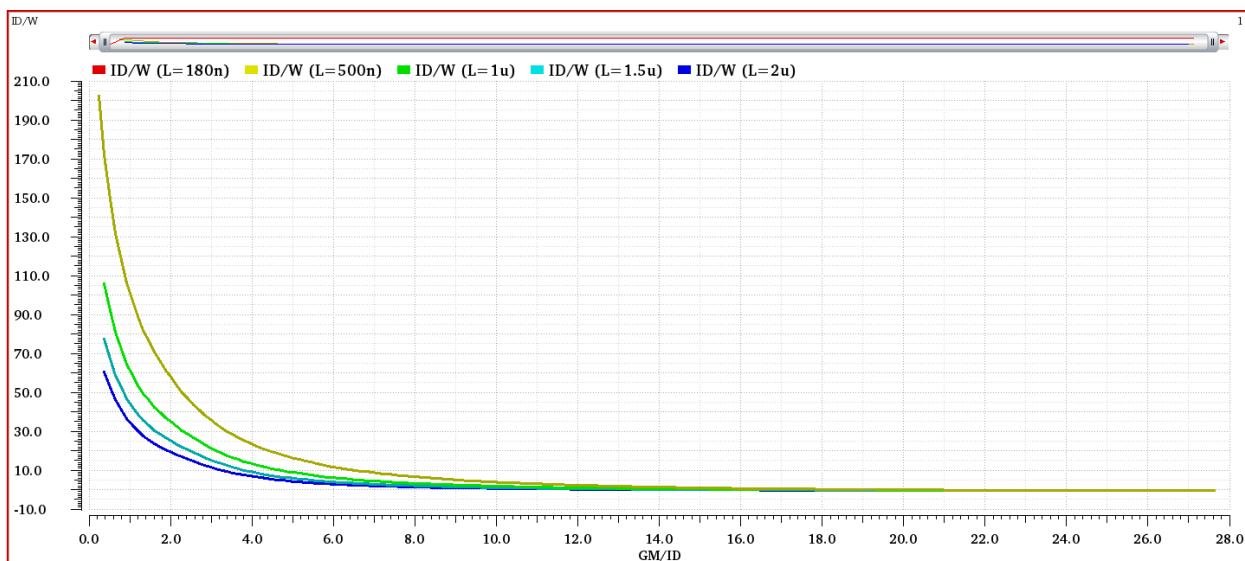
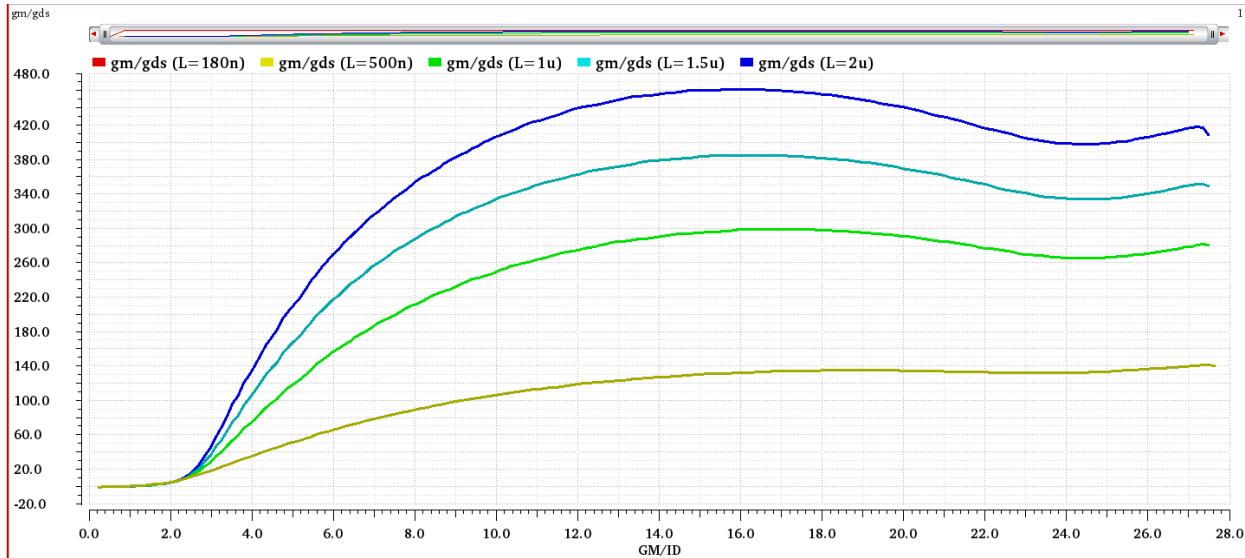
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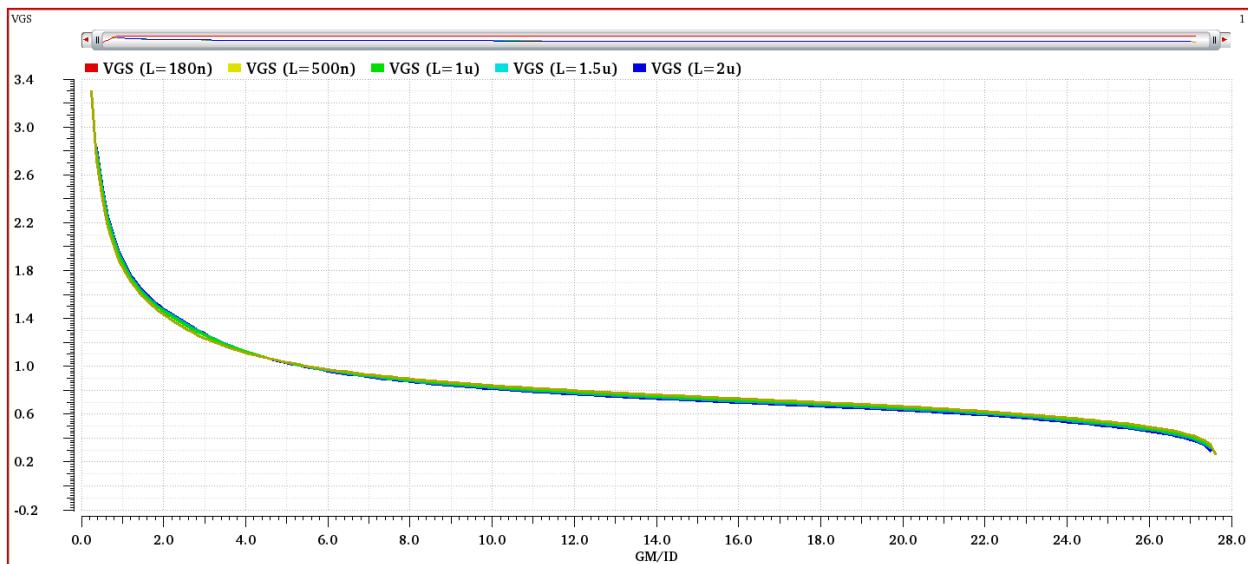
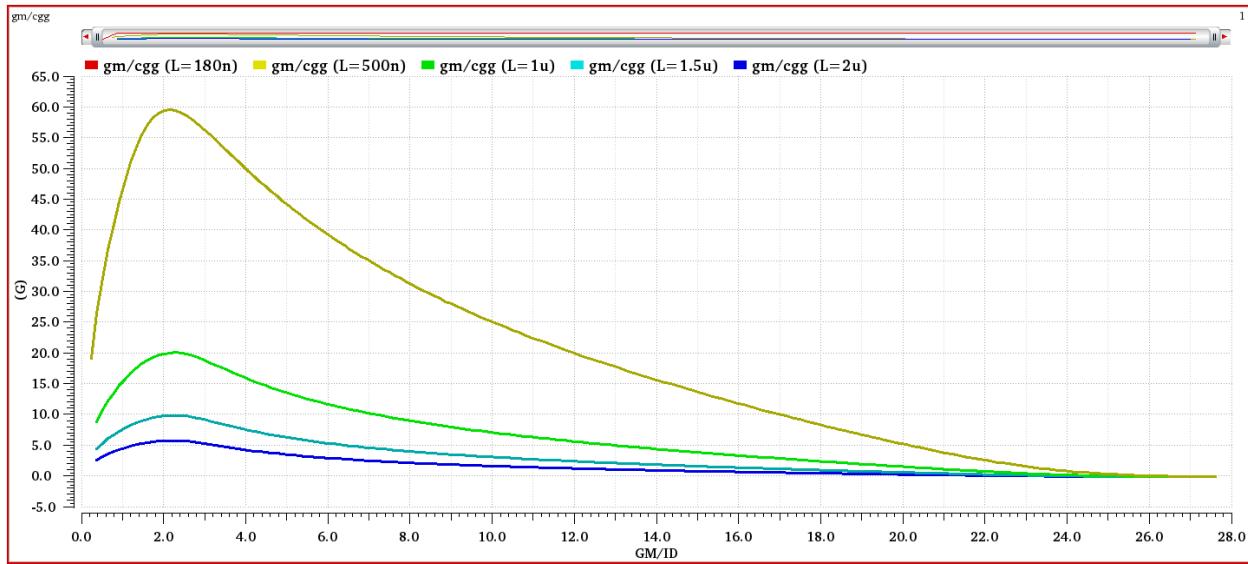
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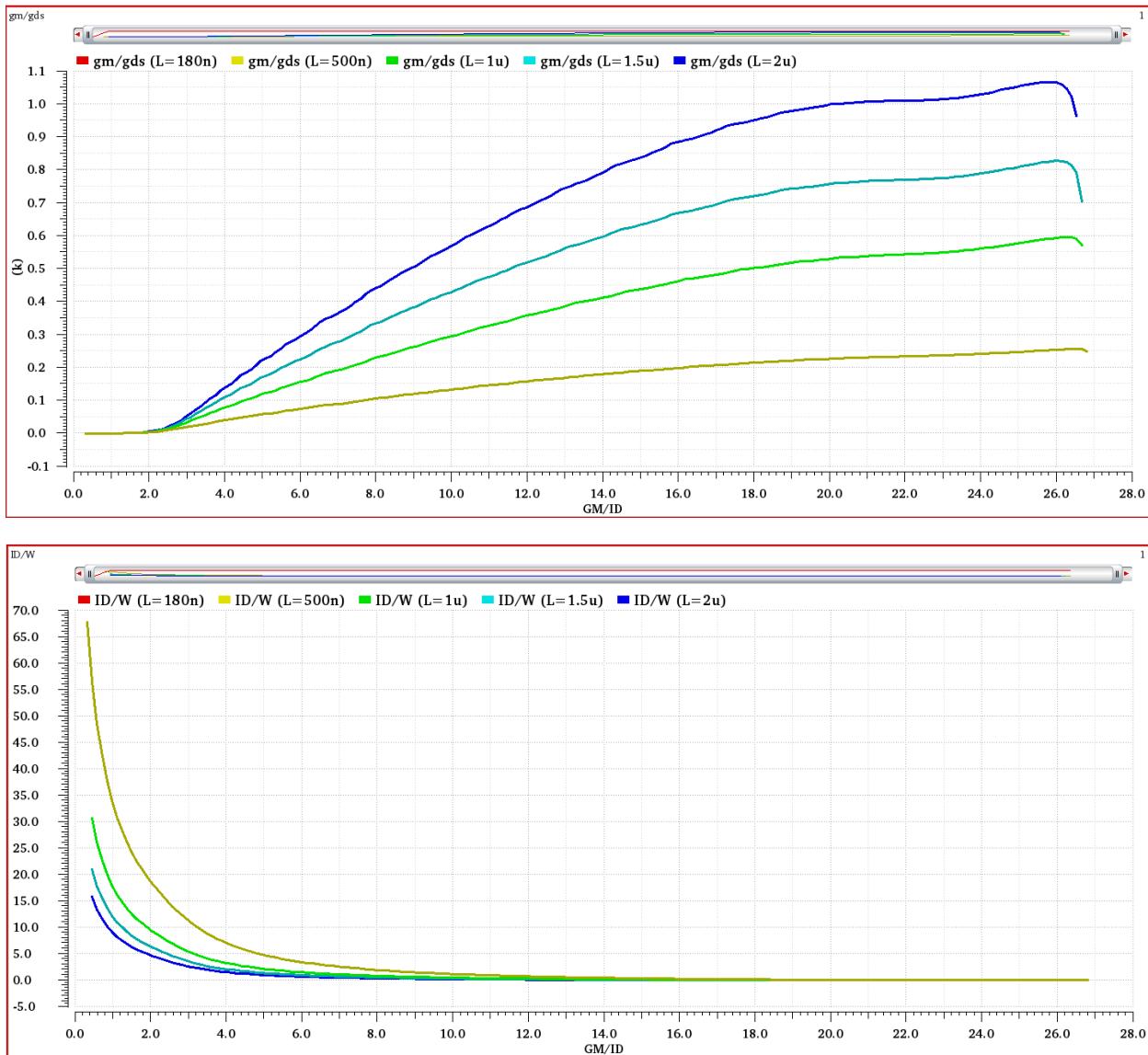
PART 1: gm/ID Design Charts

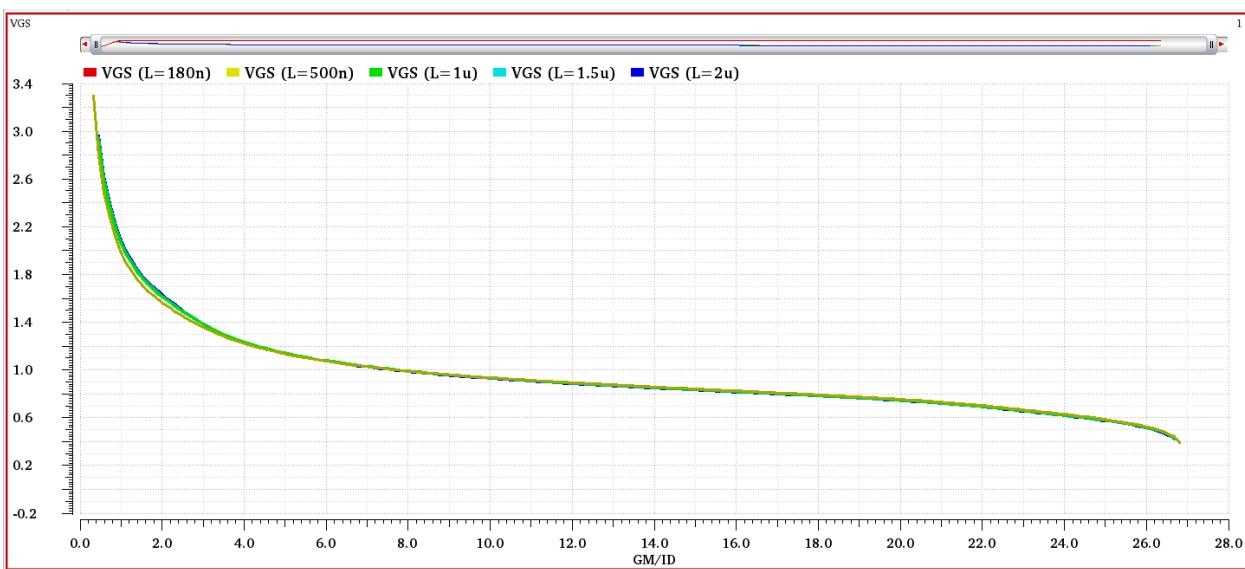
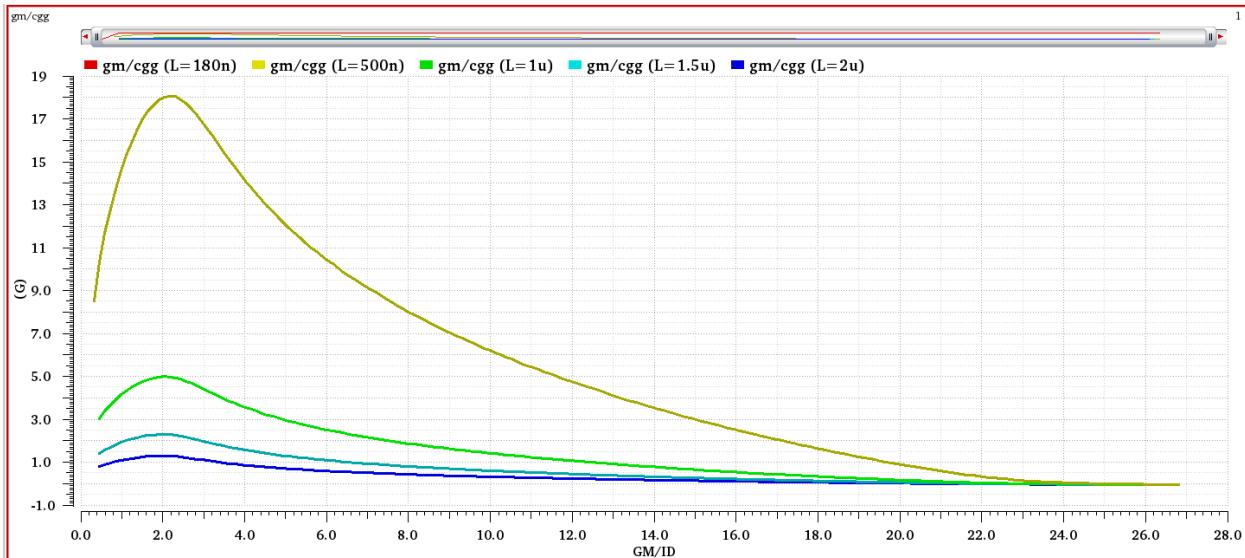
NMOS





PMOS





PART 2: OTA Design

Designing the input pair of the first stage

Since the CMRR high is 0.8 so we will use a PMOS input pair

it was asked to start with $C_C = 0.5 C_L$, $C_C = 2.5 \mu F$

$$t_{rise} = 70nS, t_{rise} = 2.2\tau, \tau = 31.8181nS$$

$$UGF = \frac{1}{2\pi\tau}, UGF \approx 5MHz, UGF = \frac{g_m}{2\pi C_{CC}}$$

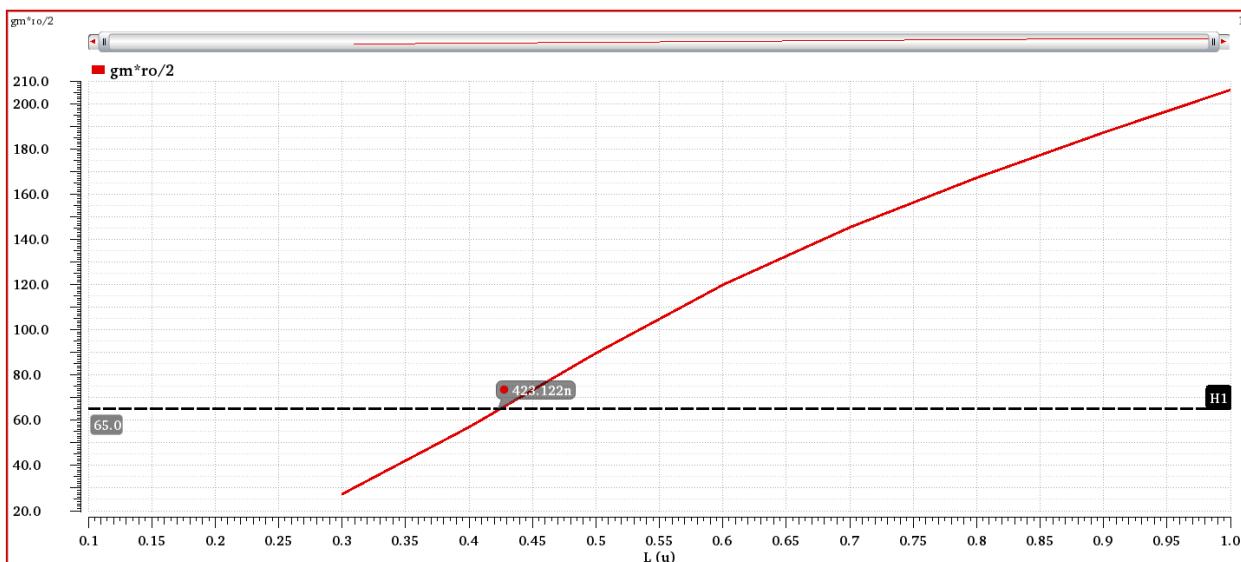
$$g_m = 78.6 \mu S$$

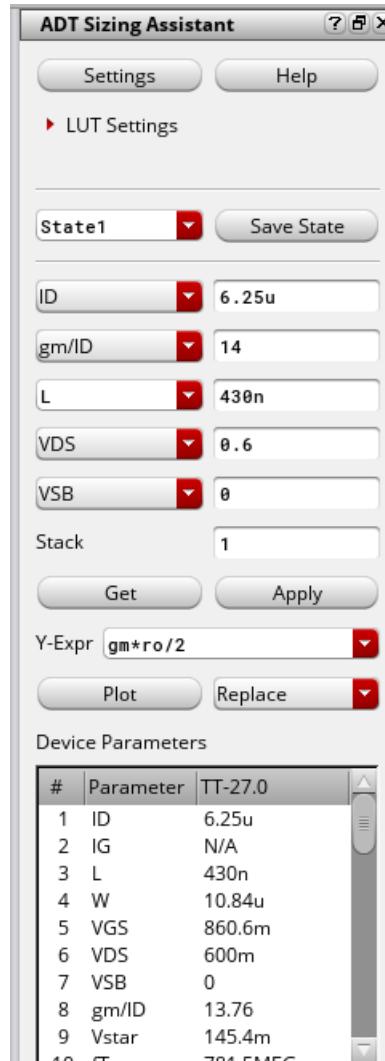
$$\text{Slew rate} = \frac{I_B}{C_{CC}}$$

$$I_B = 12.5 \mu A, I_D = 6.25 \mu A$$

$$\frac{g_m}{I_D} = 12.576V^{-1}, \text{ however we will use a margin for the } \frac{g_m}{I_D} \text{ to be 14}$$

Assume that the VDD is divided equally to each transistor so $V_{DS} = 0.6V$





However after using this dimension the gain of the first stage was 77dB which was above the required gain so we need to make a condition on the gds to make sure that the gain is within the required range

Since $g_m = 78.6\mu S$ and the gain of the first stage is

$0.5 g_m g_{ds}$

So $g_{ds} = 126.5 \Omega^{-1}$



Designing the tail current source

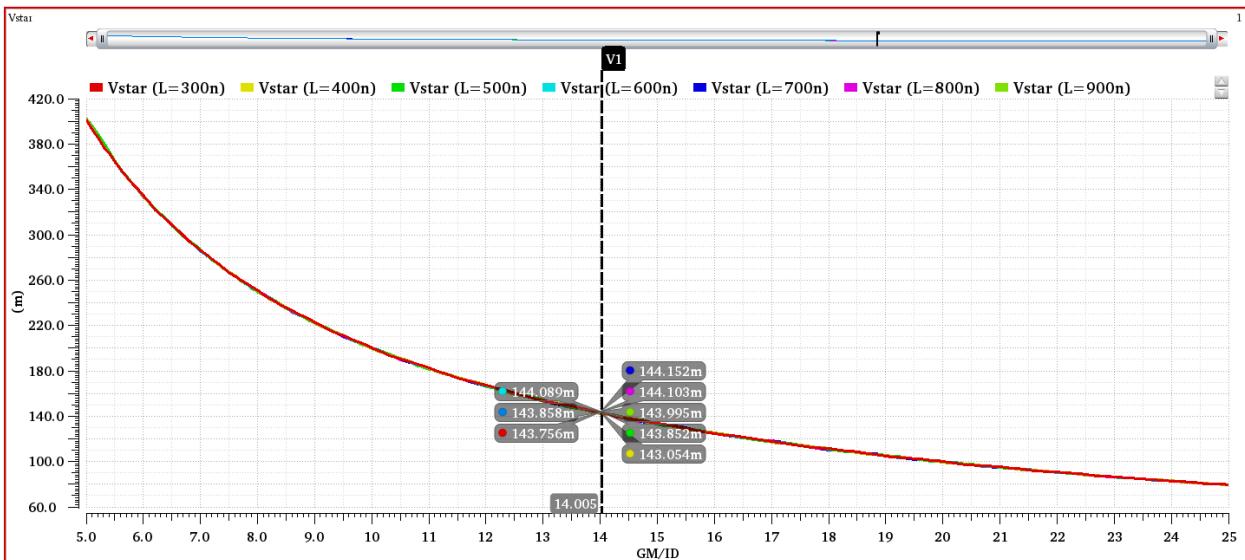
$$I_D = 12.5\mu A, V_{DS} = 0.6V$$

Assume the tail current source will have the same $\frac{g_m}{I_D}$ is the input pair

$$A_{Vcm} = -32dB, A_{Vcm} = \frac{1}{2 \times g_{mactive_load} \times \frac{1}{g_{dstail}}}$$

$$g_{mactive_load} = \frac{g_m}{I_D} \times I_D, I_D = 6.25\mu A, \frac{g_m}{I_D} = 10V^{-1}$$

$$g_{mactive_load} = 62.5\mu S$$



$$V^* = 0.14V$$

ADT Sizing Assistant

Settings Help

► LUT Settings

State1 Save State

ID: 12.5u
gm/ID: 14
gds: 2.49u
VDS: 0.6
VSB: 0
Stack: 1

Get Apply

Y-Expr: vgs-vth

Plot Replace

Device Parameters

#	Parameter	TT-27.0
1	ID	12.5u
2	IG	N/A
3	L	330n
4	W	15.34u
5	VGS	836.4m
6	VDS	600m
7	VSB	0
8	gm/ID	13.61
9	Vstar	146.9m

Designing the Transistor connected to IBIAS

Assuming the transistor connected to IBIAS is annotated with M1 and the tail current source is M2

Assuming all the current mirror transistors will have the same L

Assuming $\lambda = 0.1$

$$i_1 = 10\mu A$$

$$i_2 = 12.5\mu A$$

$$VDS_1 = 1.8V$$

$$VDS_2 = 0.6V$$

$$W_1 = W_2 \frac{(1+\lambda VDS_2) i_1}{(1+\lambda VDS_1) i_2}$$

$$W_1 \approx 11.1\mu m, L_1 = 330nm$$

Designing the Transistor connected above the second stage

Assuming the transistor connected to IBIAS is annotated with M1 and the Transistor connected above the second stage M2

Assuming all the current mirror transistors will have the same L

Assuming $\lambda = 0.1$

$$i_1 = 10\mu A$$

$$i_2 = 47.5\mu A$$

$$VDS_1 = 1.8V$$

$$VDS_2 = 0.9V$$

$$W_2 = W_1 \frac{(1+\lambda VDS_1) i_2}{(1+\lambda VDS_2) i_1}$$

$$W_2 \approx 57\mu m, L_2 = 330nm$$

However when I ran the dc op the value of VOUT was 1.1V which means that the value of the W needed tuning so I ran dc sweep on W to find the value of the W that will give VOUT=0.9V and it was $W_2 \approx 50.7\mu m$

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
5	ITI:LAB9:1	VOUT	882.1m			
Parameters: W_tail_mirror=50.5u						
6	ITI:LAB9:1	VOUT	888.7m			
Parameters: W_tail_mirror=50.6u						
7	ITI:LAB9:1	VOUT	895.3m			
Parameters: W_tail_mirror=50.7u						
8	ITI:LAB9:1	VOUT	901.8m			
Parameters: W_tail_mirror=50.8u						
9	ITI:LAB9:1	VOUT	908.4m			
Parameters: W_tail_mirror=50.9u						
10	ITI:LAB9:1	VOUT	914.9m			
Parameters: W_tail_mirror=51u						
11	ITI:LAB9:1	VOUT	921.4m			
Parameters: W_tail_mirror=51.1u						
12	ITI:LAB9:1	VOUT	927.9m			
Parameters: W_tail_mirror=51.2u						
13	ITI:LAB9:1	VOUT	934.4m			

Designing the active-load

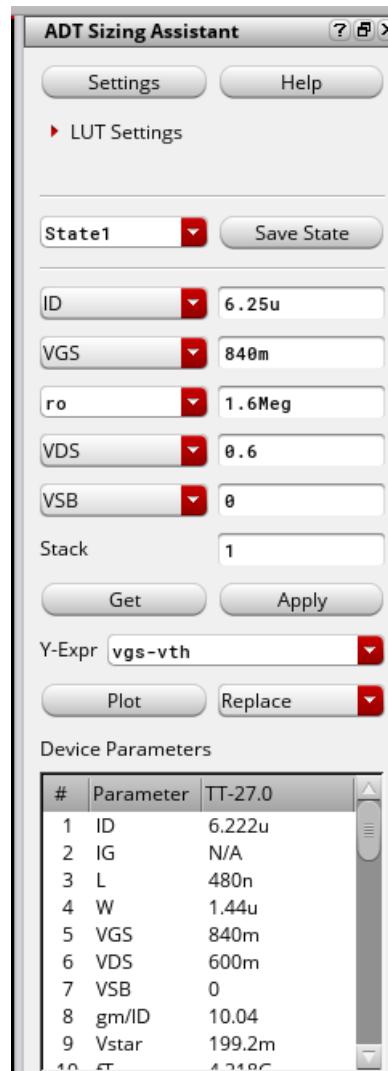
$$I_D = 6.25\mu A, V_{DS} = 0.6V$$

$$V_{gs} \geq V_{inCMmin} + V_{THinput_pair}, V_{THinput_pair} = 789mV$$

$$V_{gs} \geq 830mV$$

So we will take margin

$$V_{gs} = 840mV$$



Designing the second stage

$$I_D = 47.5\mu A$$

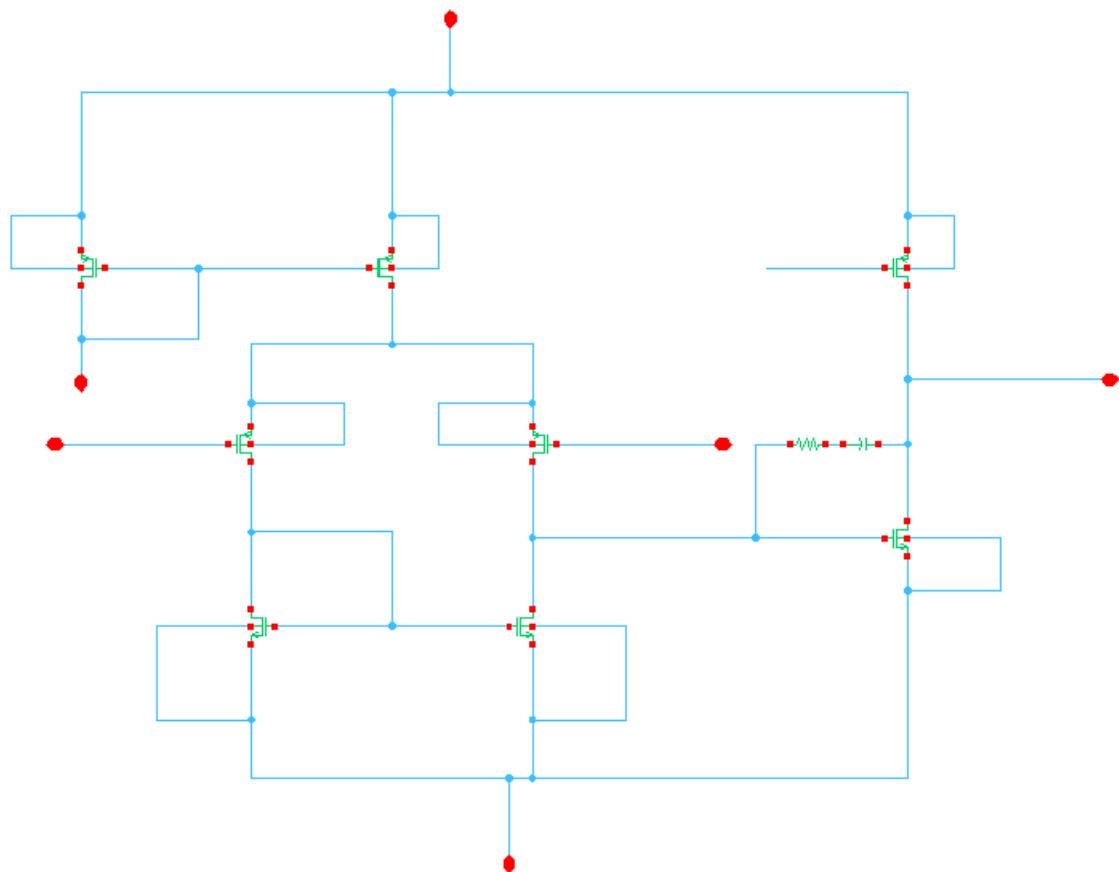
$$V_{DS} = 0.9V$$

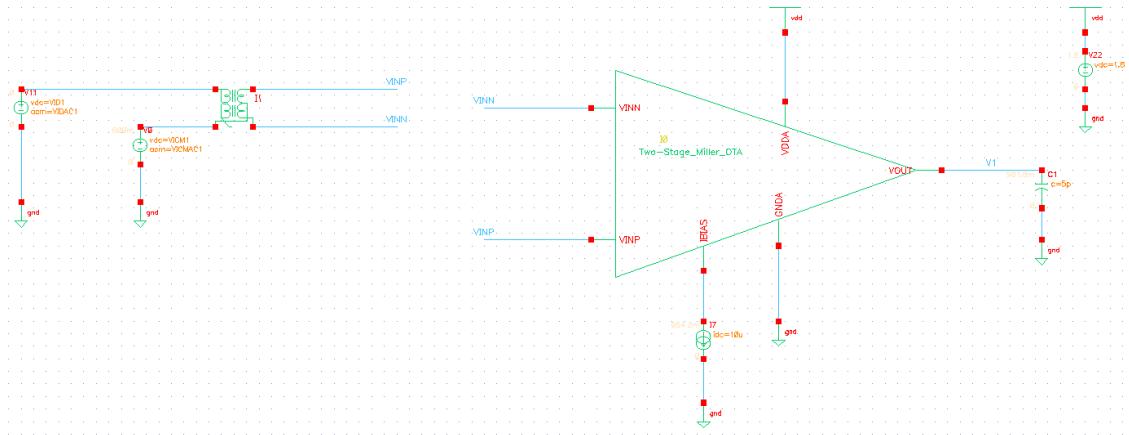
$$\frac{g_m}{g_{ds}} = 64$$



<i>Topology</i>	<i>W</i>	<i>L</i>
<i>First stage input pair</i>	$10.43\mu m$	$420nm$
<i>tail (above the first stage input pair)</i>	$15.34\mu m$	$330nm$
<i>tail (Connected to IBIAS)</i>	$11.1\mu m$	$330nm$
<i>tail (above the second stage)</i>	$50.7\mu m$	$330nm$
<i>Second stage</i>	$6.52\mu m$	$370nm$

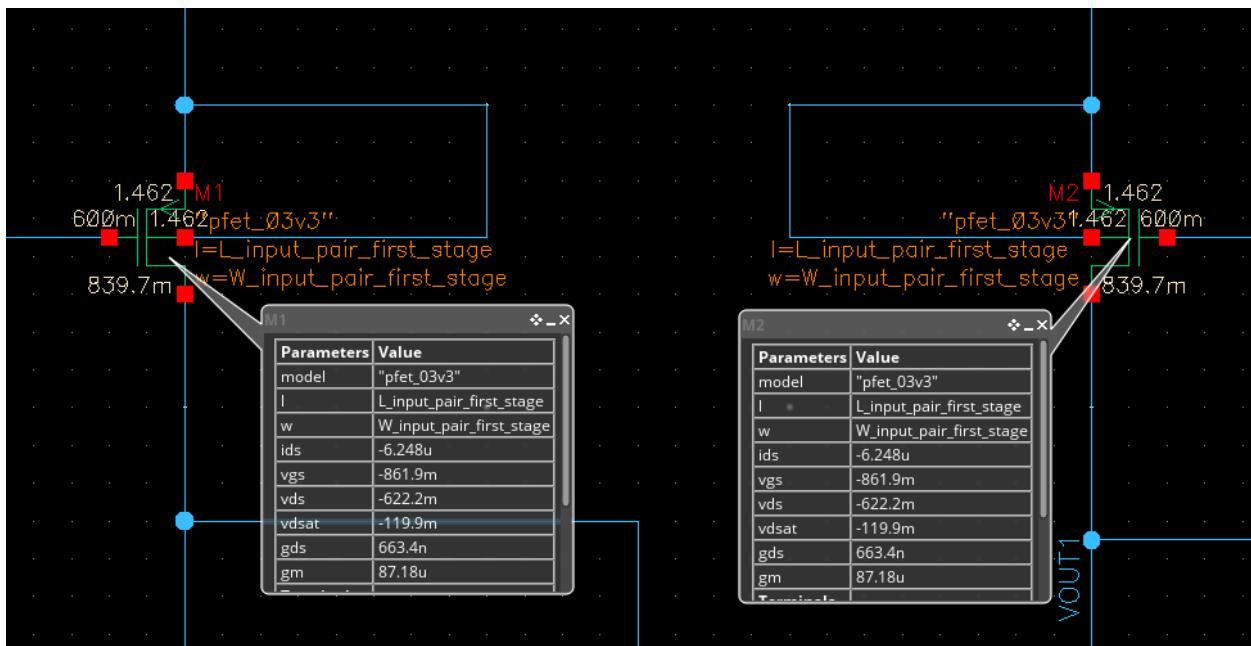
PART 3: Open-Loop OTA Simulation





DC op

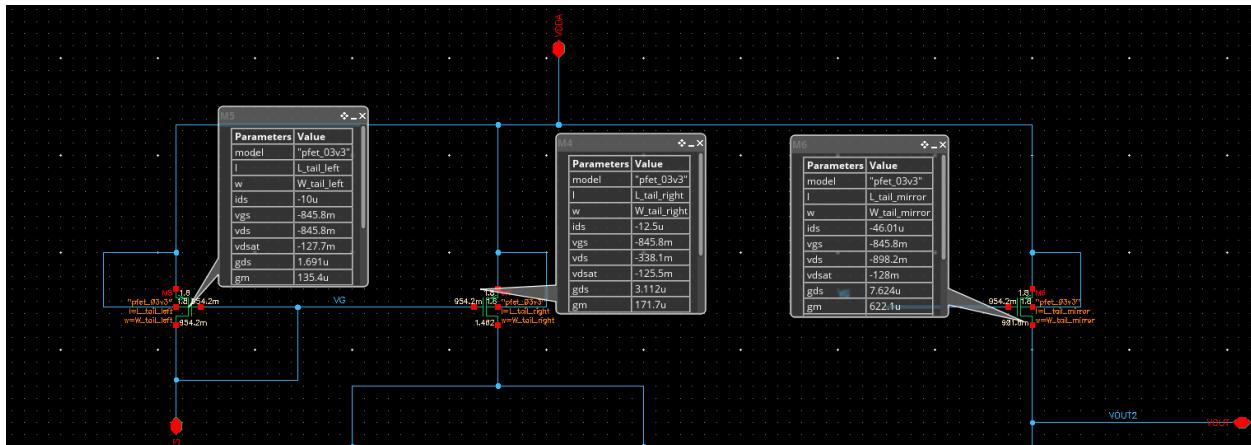
Input pair of the first stage



$$W_{input_pair_first_stage} = 10.4\mu m$$

$$L_{input_pair_first_stage} = 420nm$$

Tail current source



$$W_{tail_left} = 11.1\mu\text{m}$$

$$L_{tail_left} = 330\text{nm}$$

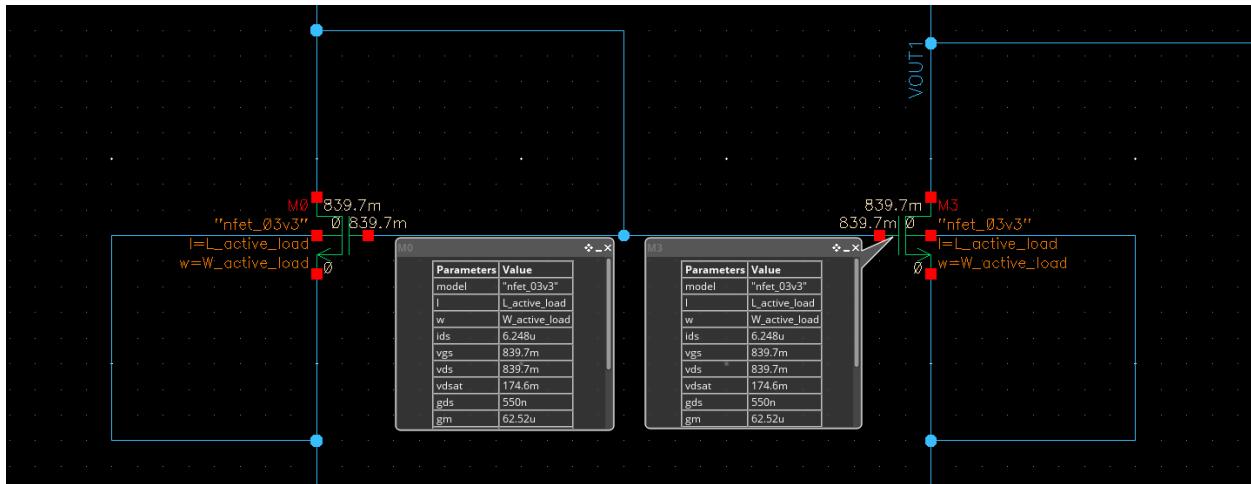
$$W_{tail_right} = 15.34\mu\text{m}$$

$$L_{tail_right} = 330\text{nm}$$

$$W_{tail_mirror} = 50.7\mu\text{m}$$

$$L_{tail_mirror} = 330\text{nm}$$

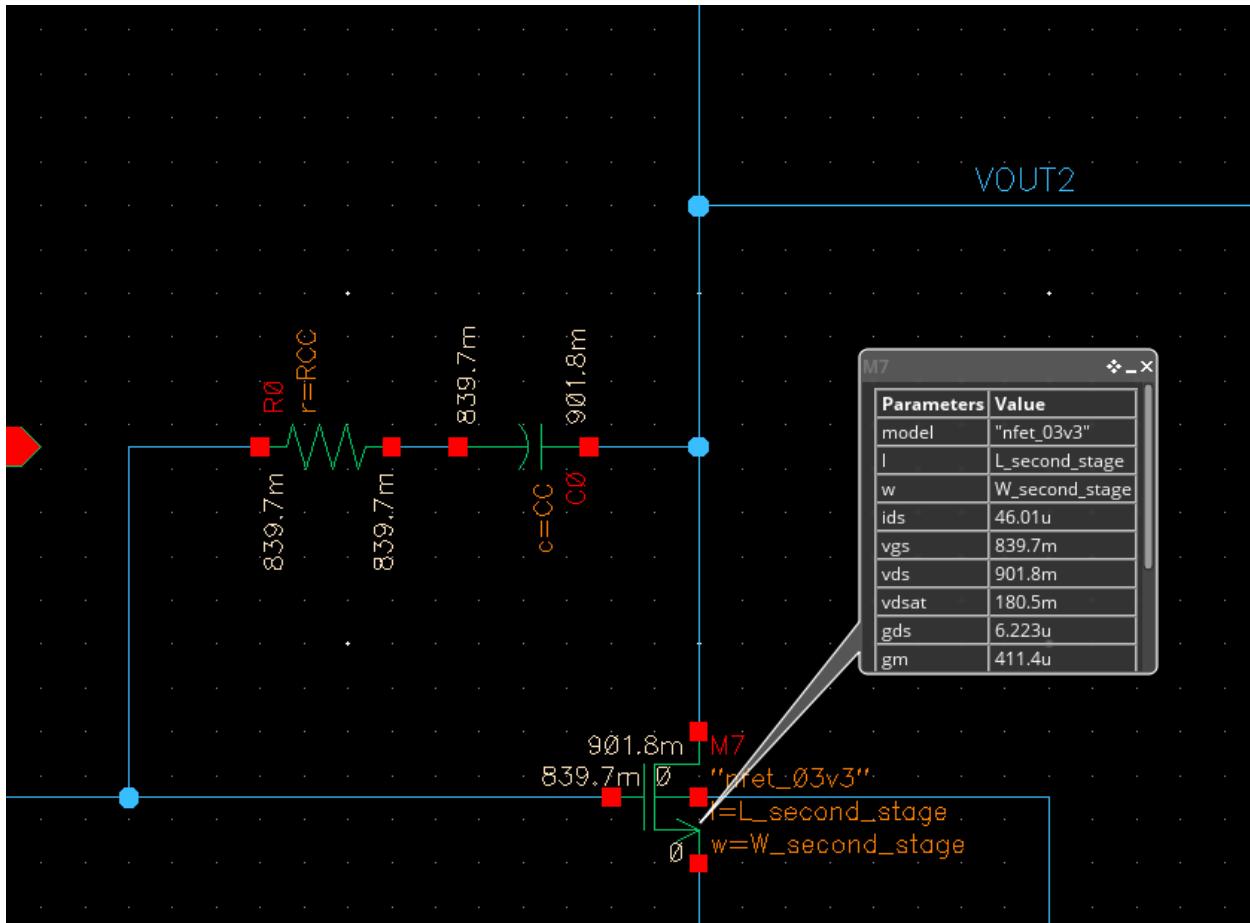
Active-load



$$W_{active_load} = 1.44\mu\text{m}$$

$$L_{active_load} = 480\text{nm}$$

Second stage

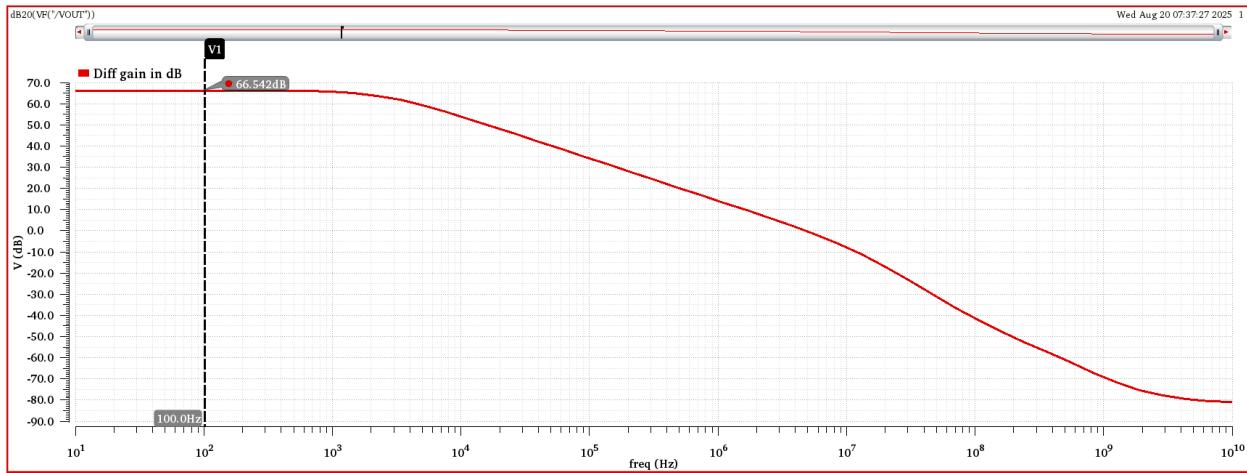


$$W_{second_stage} = 6.52\mu m$$

$$L_{second_stage} = 370nm$$

- The bias current splits equally between the transistors of the differential pair. Since both devices experience identical operating conditions, which makes also g_m exactly equal.
- The value of $V_{OUT2}=901.8mV$ as this is the value where the output swing is maximized.

Diff small signal ccs



Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI:LAB9:1	DC_gain_linear	2.125k			
ITI:LAB9:1	DC_gain_dB	66.55			
ITI:LAB9:1	Bandwidth	2.5k			
ITI:LAB9:1	Unity_gain_frequency	5.123M			
ITI:LAB9:1	GBW	5.314M			

Hand analysis

$$A_V = g_{m_{input_pair}}(r_o_{input_pair} // r_o_{active_load}) g_{m_{second_stage}}(r_o_{second_stage} // r_o_{tail})$$

$$A_V = 2126.34$$

$$A_V = 66.55 \text{ dB}$$

$$\text{Bandwidth} = \frac{1}{2\pi RC(1 + g_{m_{input_pair}})(r_o_{second_stage} // r_o_{tail})}$$

$$R = (r_o_{second_stage} // r_o_{tail}), C = C_C$$

$$\text{Bandwidth} = 2.5 \text{ KHz}$$

Unity gain frequency

$$UGF = \frac{g_{m_{input_pair}}}{2\pi C_{CC}}$$

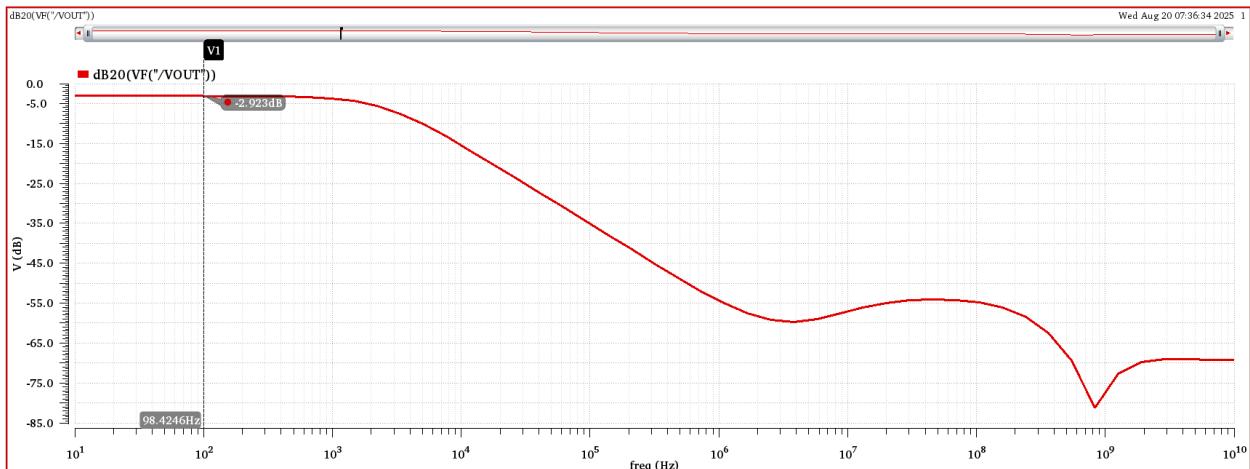
$$UGF = 5.55 \text{ MHz}$$

$$\text{GBW} = A_V \times \text{Bandwidth}$$

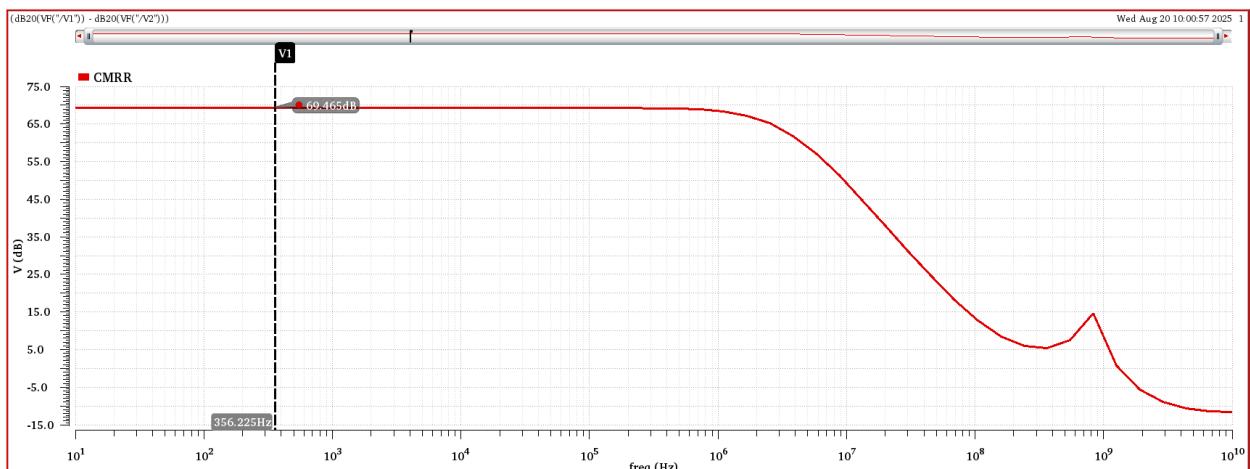
GBW=5.315MHz

parameter	Simulation value	Hand-analysis value
DC gain	66.55 dB	66.55 dB
Bandwidth	2.5KHz	2.5KHz
UGF	5.123MHz	5.55MHz
GBW	5.314MHz	5.315MHz

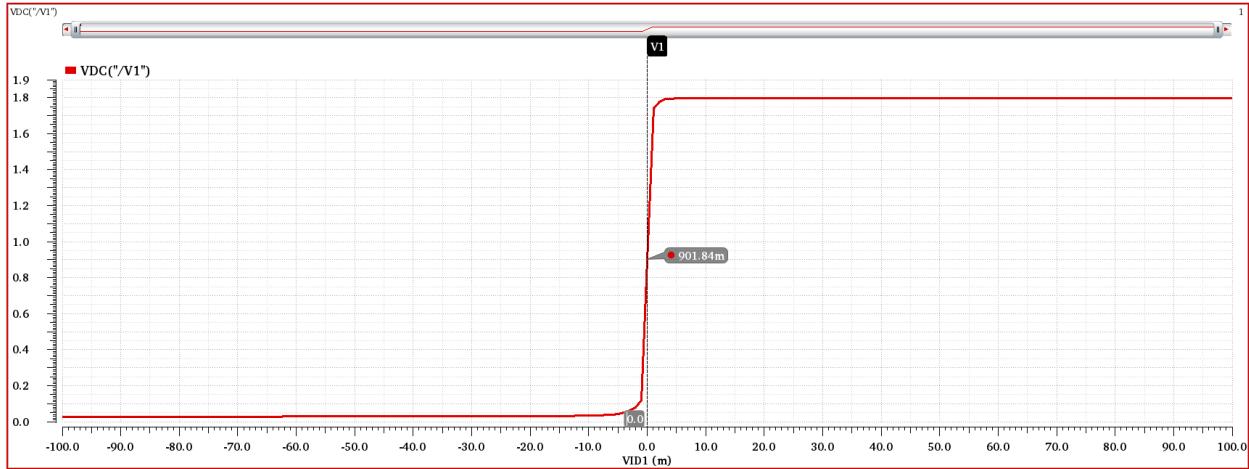
CM small signal ccs



CMRR(Optional)

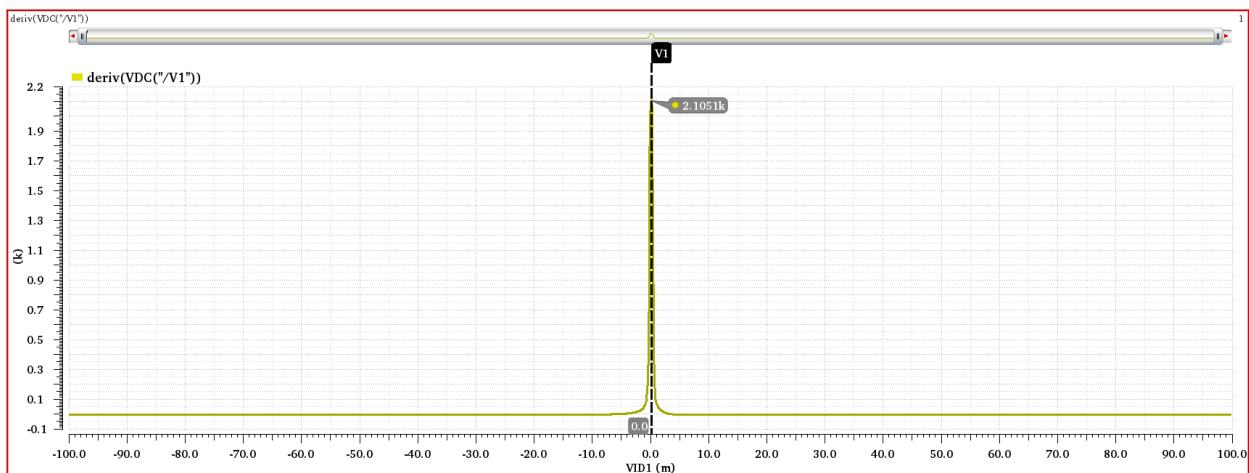


Diff large signal ccs (Optional)



Comment:

The value of $Vout$ at $VID=0$ is exactly equal to $VOUT2$ in the DC OP

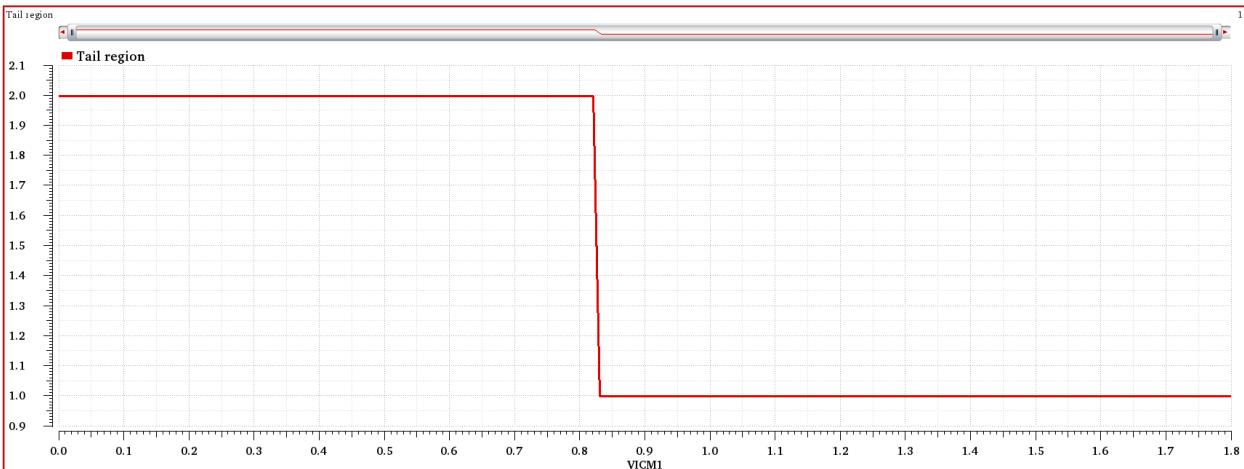
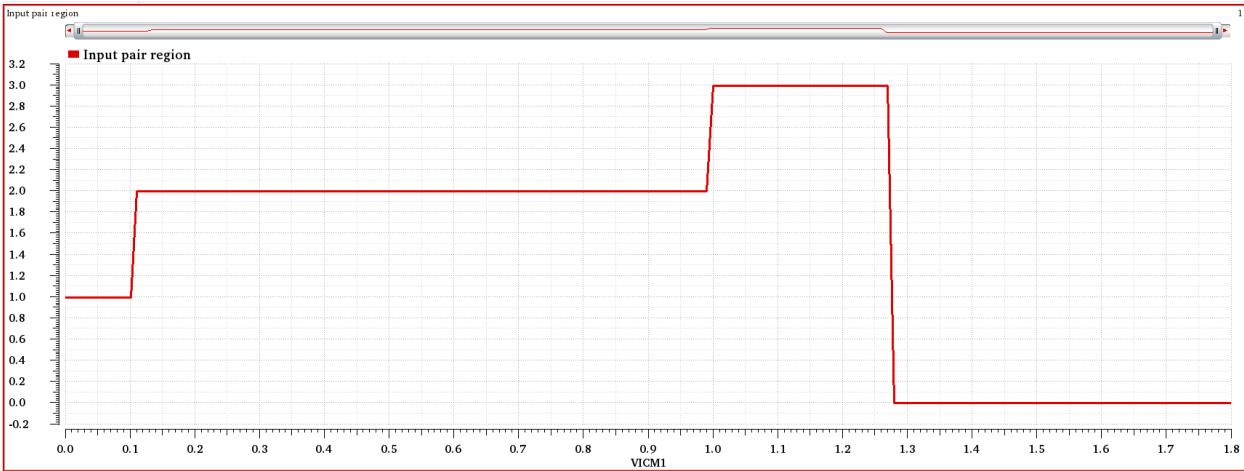


Comment:

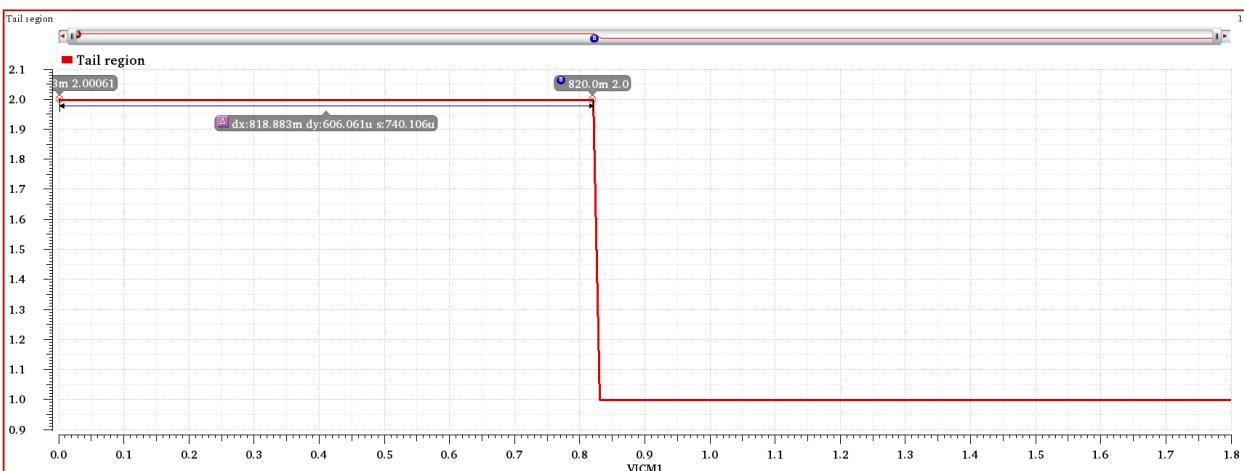
The DC gain extracted from the plot is nearly exactly similar to the value of the DC gain calculated in the DC OP

CM large signal ccs (region vs VICM)

Regions



CMIR



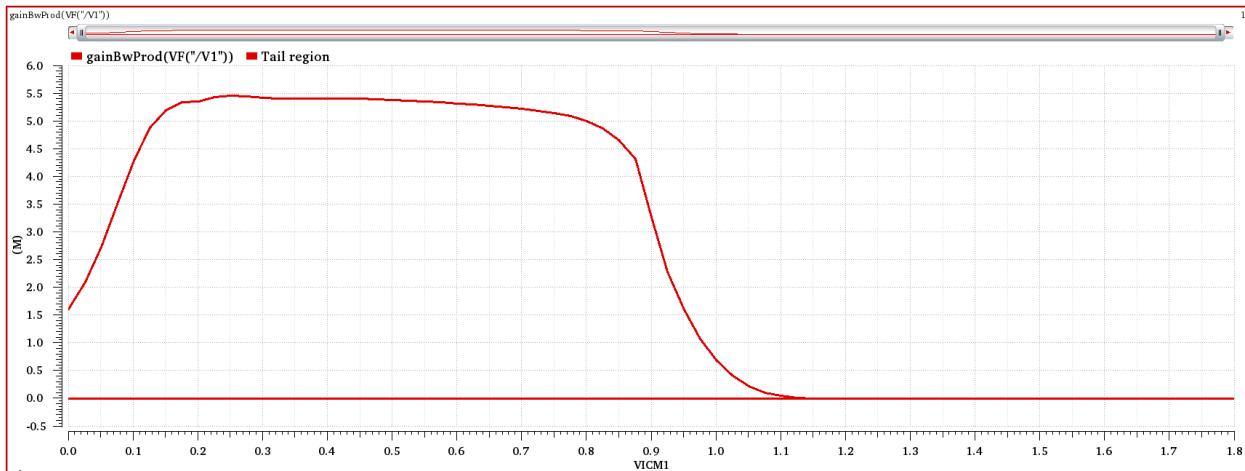
Hand analysis

$$V_{in_{max}} = VDD - V_{sg\ input_{pair}} - V_{dsat\ input\ pair}$$

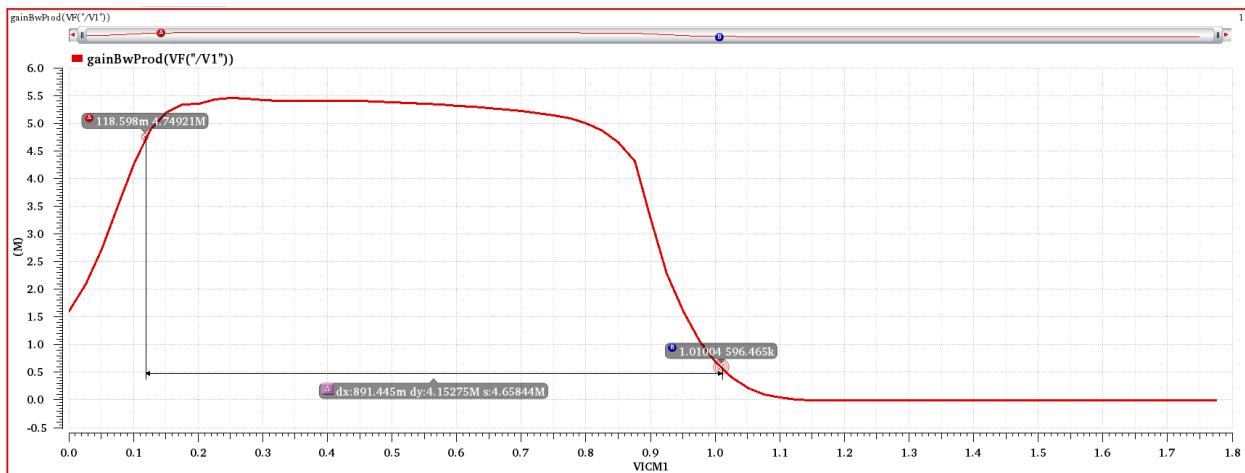
$$V_{in_{max}} = 1.8 - 0.8619 - 0.119$$

$$V_{in_{max}} = 0.8191V$$

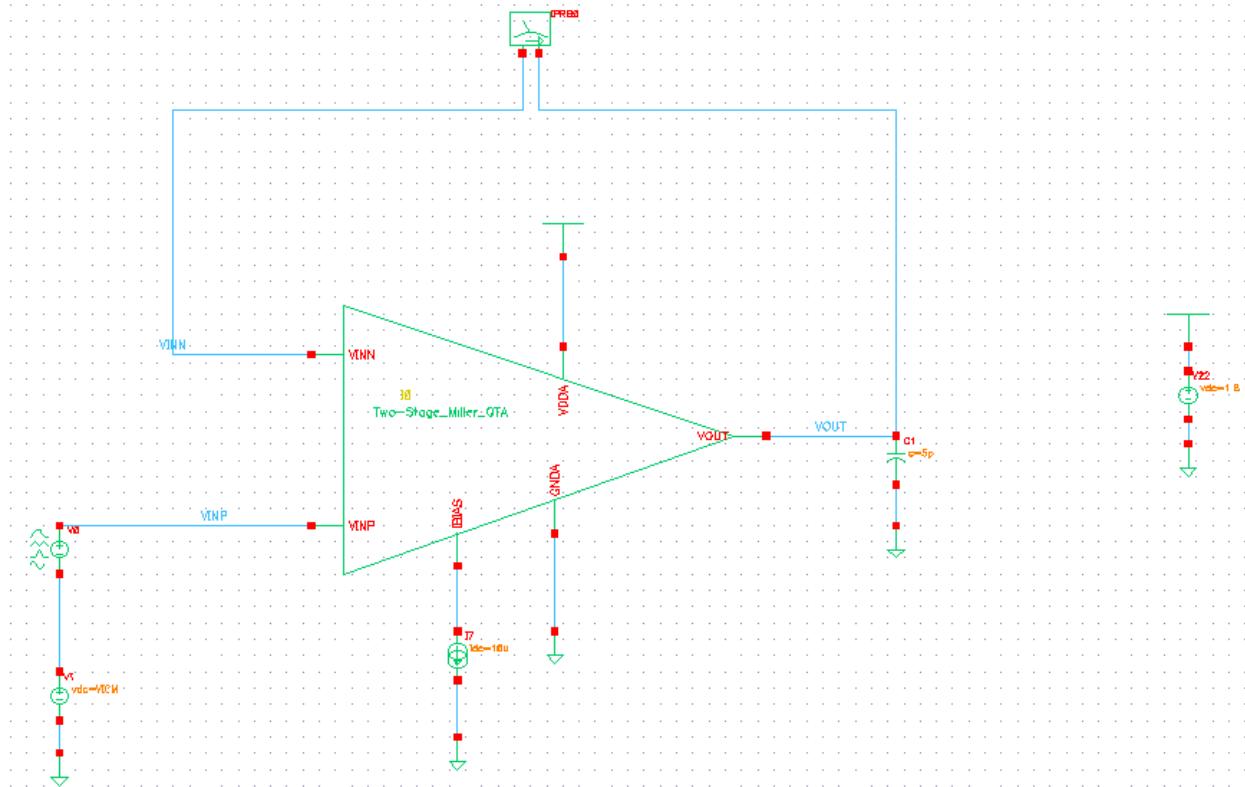
CM large signal ccs (GBW vs VICM) (Optional)



Input range calculated from the GBW graph

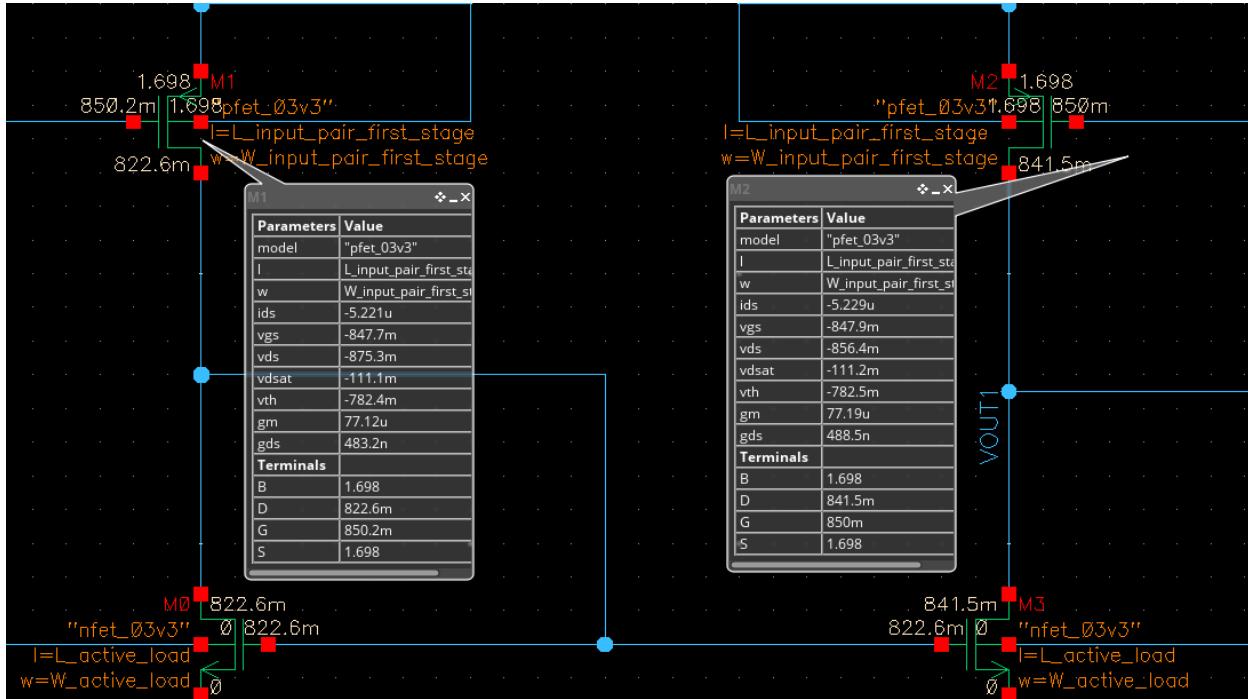


PART 4: Closed-Loop OTA Simulation

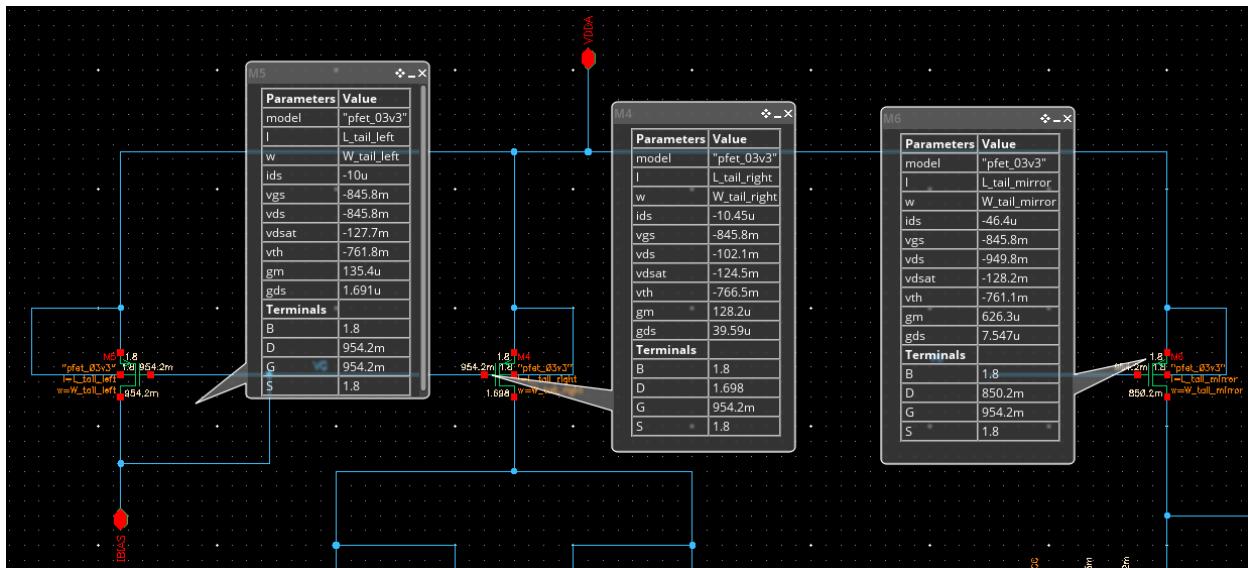


DC OP

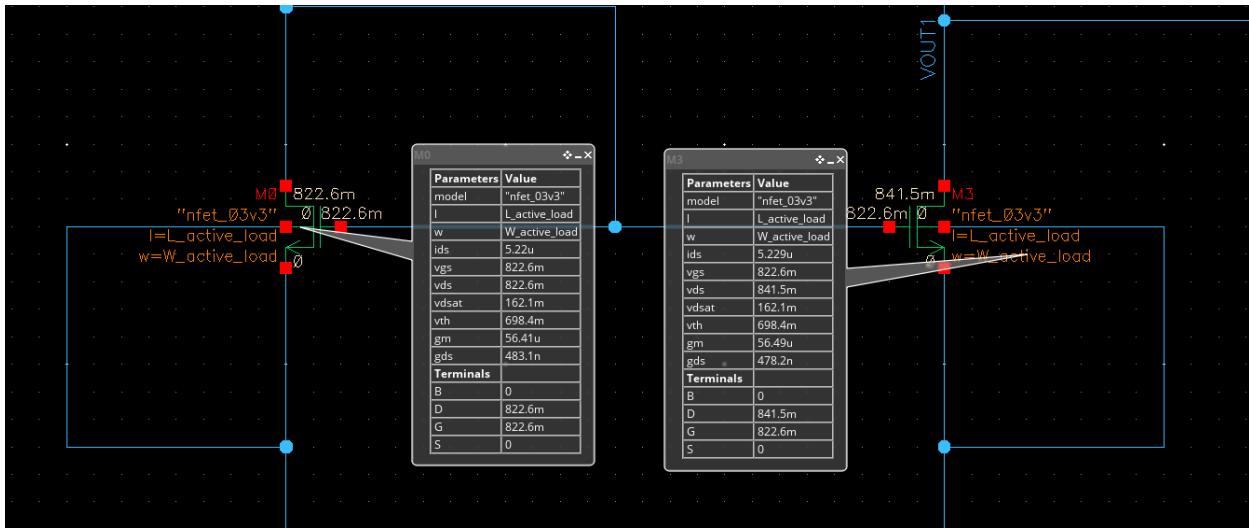
Input pair of the first stage



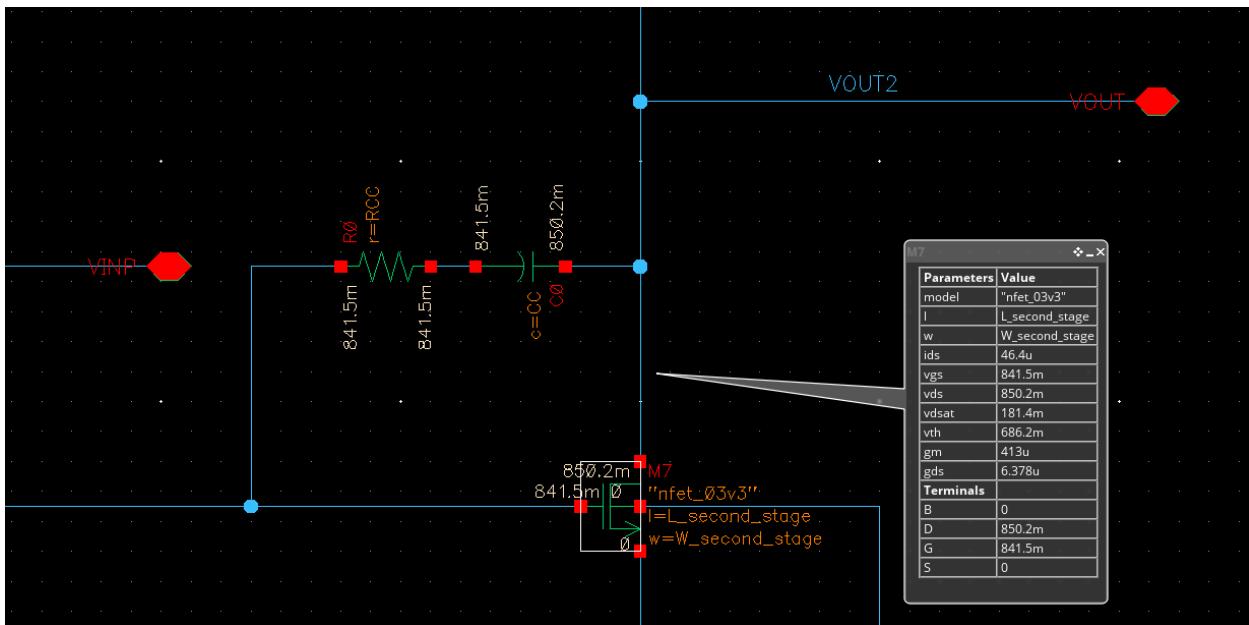
Tail current source



Active load



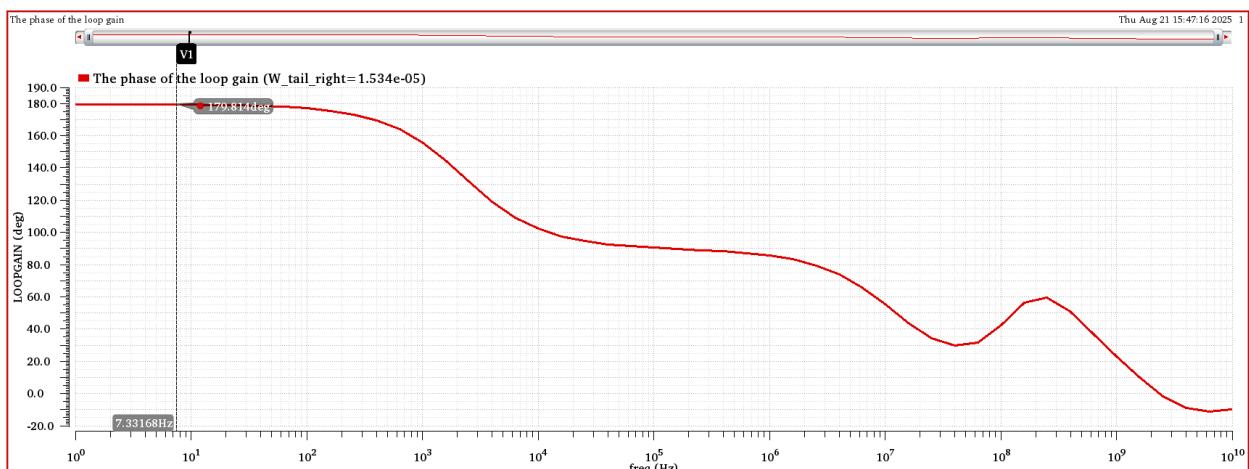
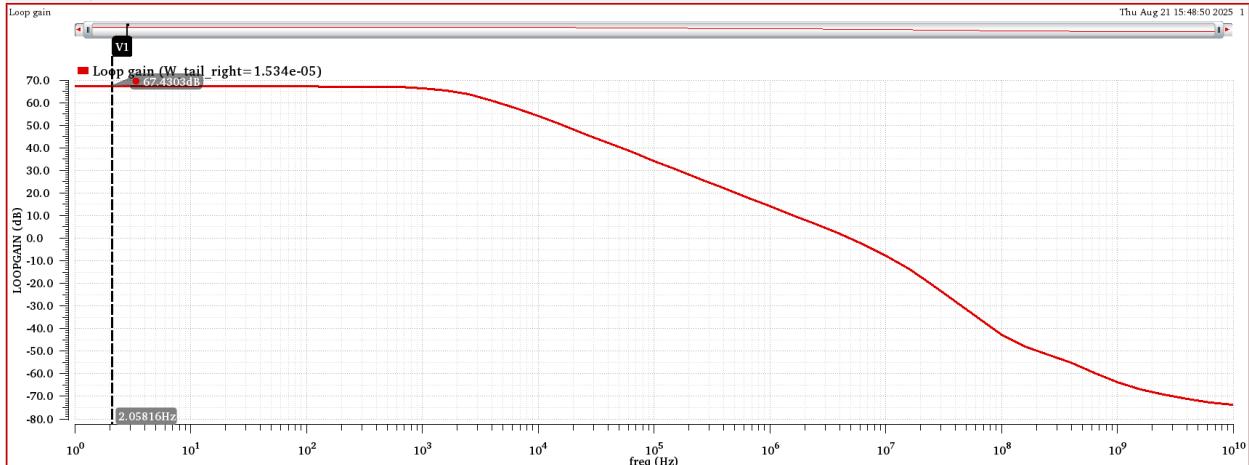
Second stage



- The DC output voltage of the first stage in the closed-loop configuration is not exactly equal to that observed in the open-loop simulation. In the closed-loop, the feedback action slightly adjusts the operating point of the input pair to enforce the feedback condition. This results in a small shift in the output DC voltage compared to the open-loop bias point, even though both remain close.

- The currents in the input differential pair are not exactly equal. This is because any small effect of feedback causes a slight imbalance in the tail current distribution. In closed-loop operation, the feedback drives one transistor to conduct slightly more than the other. As a result, the g_m values differ slightly

Loop gain



Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI:Closed_Loop_OTA_Simulation:1	DC_gain_dB	67.43			
ITI:Closed_Loop_OTA_Simulation:1	DC_gain_linear	2.352k			
ITI:Closed_Loop_OTA_Simulation:1	Unity gain	4.615M			
ITI:Closed_Loop_OTA_Simulation:1	Phase margin	73.18			
ITI:Closed_Loop_OTA_Simulation:1	Bandwidth	2.008k			
ITI:Closed_Loop_OTA_Simulation:1	GBW	4.724M			

Hand analysis

$$A_V = g_{m_{input_pair}}(r_o_{input_pair} // r_o_{active_load}) g_{m_{second_stage}}(r_o_{second_stage} // r_o_{tail})$$

$$A_V = 2378.726$$

$$A_V = 67.527 \text{ dB}$$

$$A_{CL} = \frac{A_{oL}}{1 + A_{oL}\beta}$$

$$A_{oL} = 2000$$

$$\beta = -7.49 \times 10^{-5}$$

$$Bandwidth = BW_{oL}(1 + A_{oL}\beta)$$

$$\text{Bandwidth} = 2125 \text{ Hz}$$

$$UGF_{CL} = UGF_{CL}(1 + A_{oL}\beta)$$

$$UGF = 4.356 \text{ MHz}$$

$$GBW_{CL} = GBW_{CL}(1 + A_{oL}\beta)$$

$$GBW = 4.5187 \text{ MHz}$$

$$\text{Phase margin} = 180 - \tan^{-1}\left(\frac{UGF}{\text{Dominant pole}}\right) - \tan^{-1}\left(\frac{UGF}{\text{Non-dominant pole}}\right)$$

$$\text{Dominant pole} = 2.008 \text{ kHz}$$

$$\text{Non-dominant pole} = 4 \times \omega_u$$

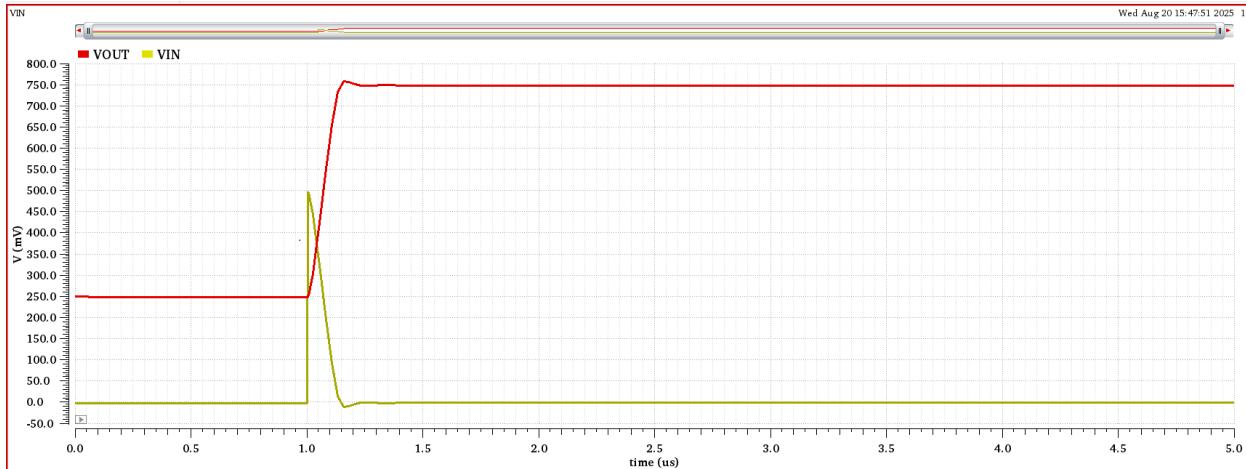
$$\text{Non-dominant pole} = 18.46 \text{ MHz}$$

$$\text{Phase margin} = 75.98^\circ$$

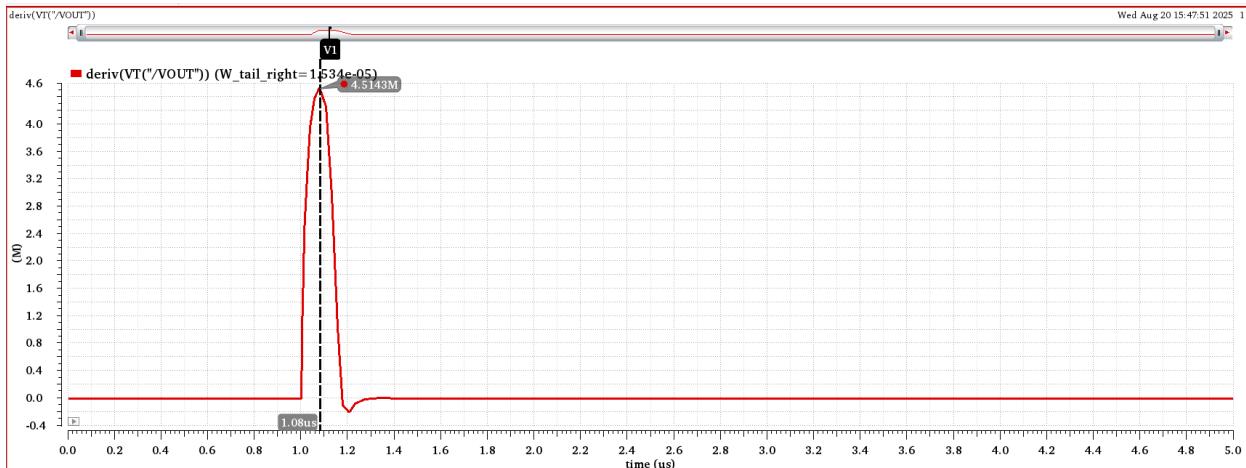
parameter	Simulation value	Hand-analysis value
DC gain	67.43 dB	67.527 dB
Bandwidth	2.008 kHz	2.125 kHz
UGF	4.615 MHz	4.5187 MHz
GBW	4.724 MHz	4.5187 MHz

Slew rate

VOUT and VIN overlaid



Slew rate



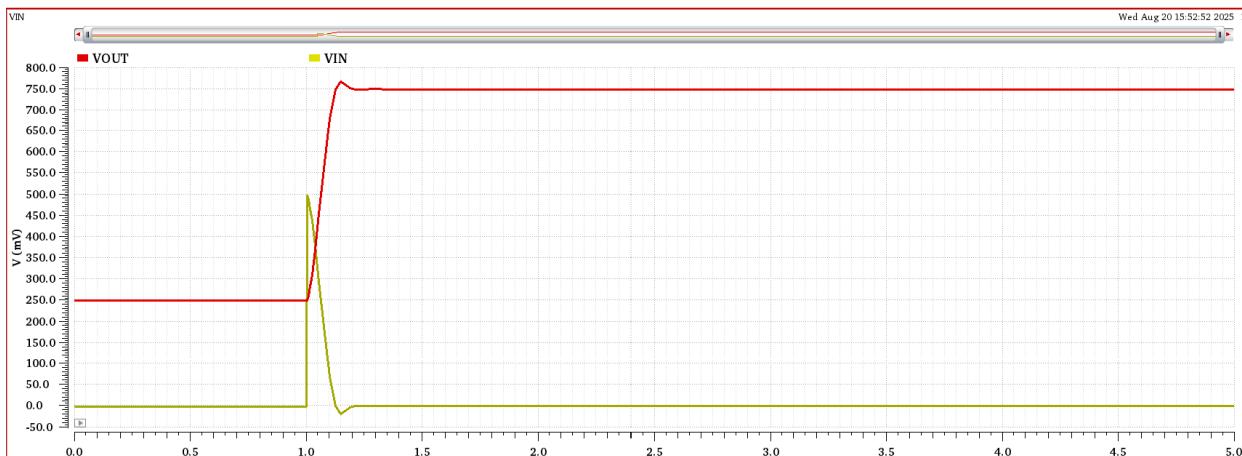
Comment: The value of the slew rate is below the required value which is 5M so this mean the value of the C_c needs tuning

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: CC=2p						
1	ITI:Closed_Loop_OTA_Simulation:1	ymax(deriv(VT("/VOUT")))	5.444M			
Parameters: CC=2.1p						
2	ITI:Closed_Loop_OTA_Simulation:1	ymax(deriv(VT("/VOUT")))	5.24M			
Parameters: CC=2.2p						
3	ITI:Closed_Loop_OTA_Simulation:1	ymax(deriv(VT("/VOUT")))	5.049M			
Parameters: CC=2.3p						
4	ITI:Closed_Loop_OTA_Simulation:1	ymax(deriv(VT("/VOUT")))	4.87M			
Parameters: CC=2.4p						
5	ITI:Closed_Loop_OTA_Simulation:1	ymax(deriv(VT("/VOUT")))	4.701M			
Parameters: CC=2.5p						
6	ITI:Closed_Loop_OTA_Simulation:1	ymax(deriv(VT("/VOUT")))	4.543M			

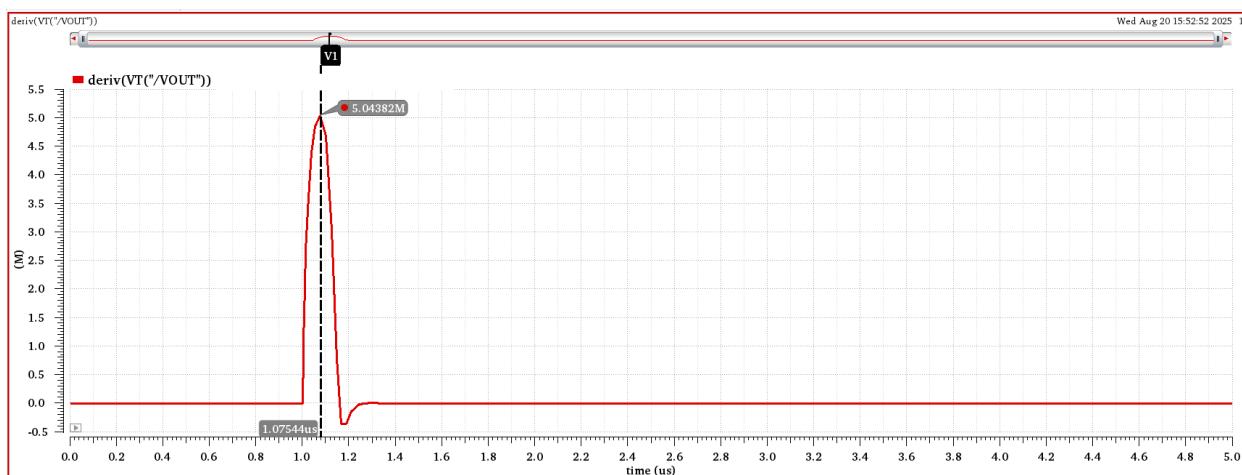
So the Value of the C_c after tuning is 2.2pF

Recalculating the above graphs after tuning

VOUT and VIN overlaid (after tuning)

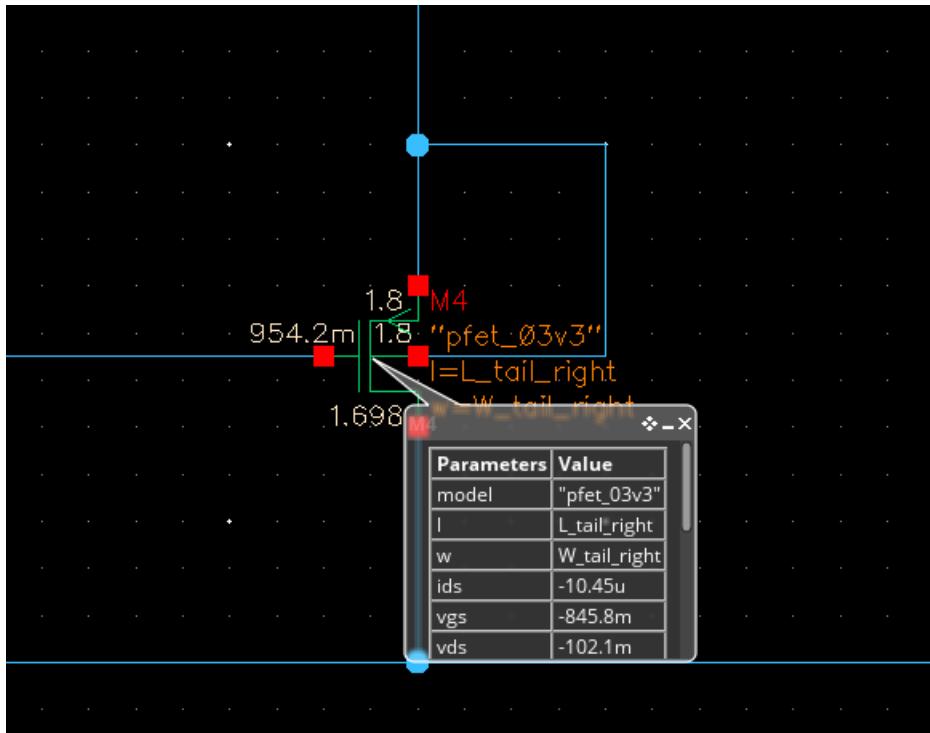


Slew rate (after tuning)



Hand analysis

$$\text{Slew rate} = \frac{I_B}{C_C}, C_c = 2.2\text{pF}$$



$$I_B = 10.45\mu A$$

$$\text{Slew rate} = 4.78 \text{ V}/\mu\text{s}$$

Double checking on the gain, fu, and GBW in addition to PM

Now I will double check on the gain, fu, and GBW in addition to PM to make sure that tuning the C_c doesn't make any of the requirements violated

Open-Loop OTA Simulation

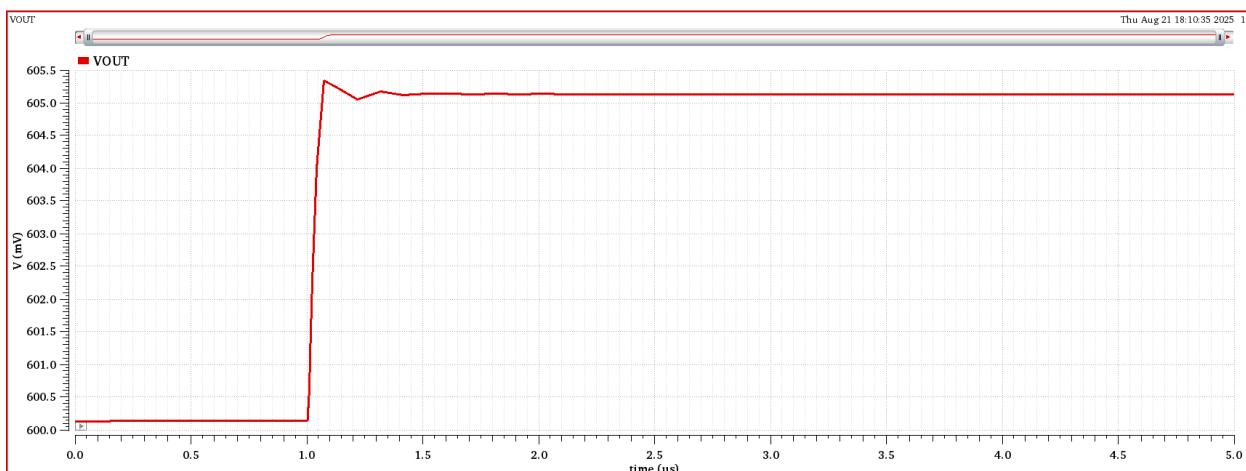
Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI:LAB9:1	DC_gain_linear	2.125k			
ITI:LAB9:1	DC_gain_dB	66.55			
ITI:LAB9:1	Bandwidth	2.834k			
ITI:LAB9:1	Unity_gain_frequency	5.596M			
ITI:LAB9:1	GBW	6.024M			

Closed-Loop OTA Simulation

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI:Closed_Loop_OTA_Simulation:1	DC_gain_dB	67.43			
ITI:Closed_Loop_OTA_Simulation:1	DC_gain_linear	2.352k			
ITI:Closed_Loop_OTA_Simulation:1	Unity gain	5.225M			
ITI:Closed_Loop_OTA_Simulation:1	Phase margin	71.14			
ITI:Closed_Loop_OTA_Simulation:1	Bandwidth	2.266k			
ITI:Closed_Loop_OTA_Simulation:1	GBW	5.33M			

Settling time

VOUT



Rise time

Test	Output	Nominal	Spec	Weight	Pass/Fail
ITI:Closed_Loop_OTA_Simulation:1	VOUT				
ITI:Closed_Loop_OTA_Simulation:1	Rise time	44.64n			

Comment:

From the graph it is noticed that there is a slight overshoot and damped oscillation, which indicates the presence of ringing. This occurs because the closed-loop system has a finite phase margin. The feedback loop does not completely suppress the second pole's effect, leading to ringing.

Comment:

The used rise-time is $t_{rise} = 2.2 \tau$ derived under the assumption of a first-order system, where the output response follows a single dominant pole. However, the two-stage Miller OTA is a second-order system. Due to the presence of the additional pole introduced by the Miller compensation, which means that the hand calculated rise time using the first order approximation tends to be slower than the simulated rise time.