

ITI
LAB09
Two-Stage Miller OTA

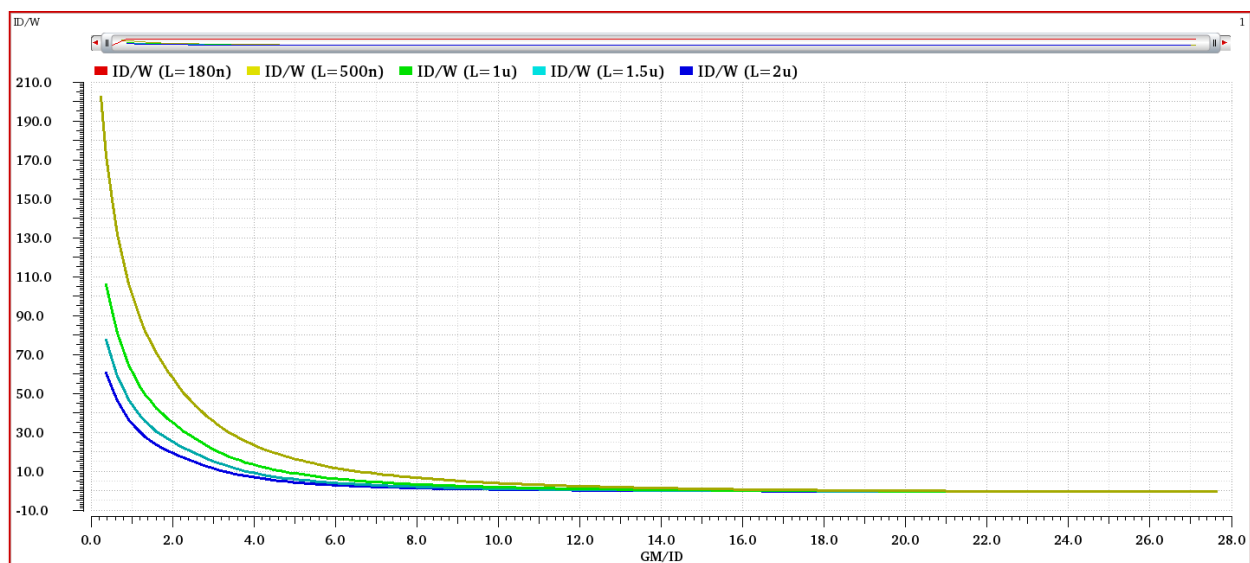
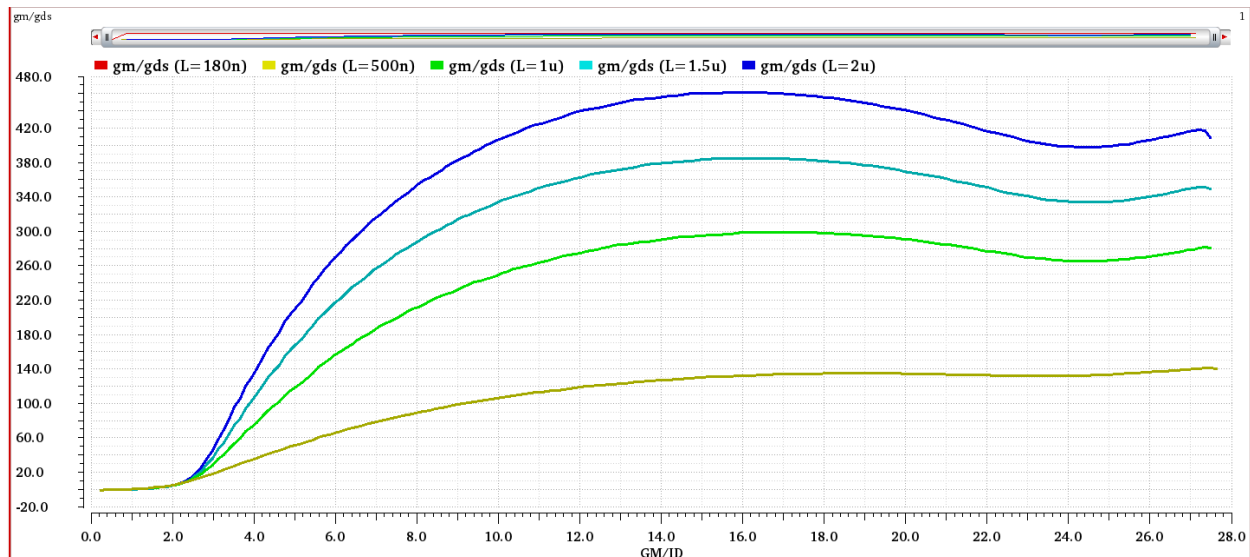
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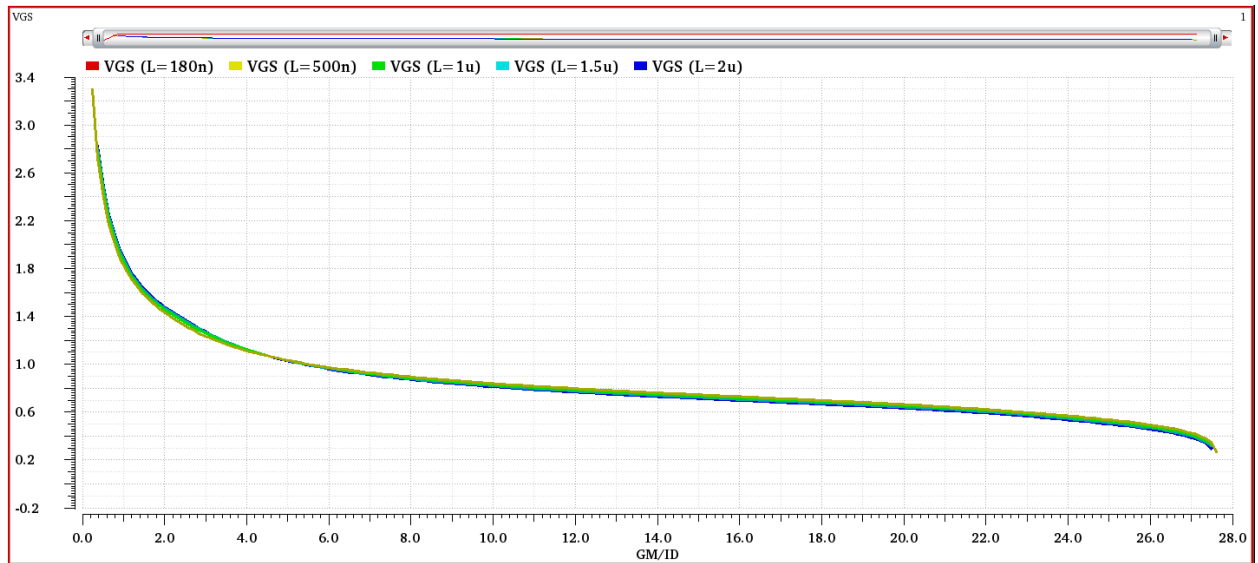
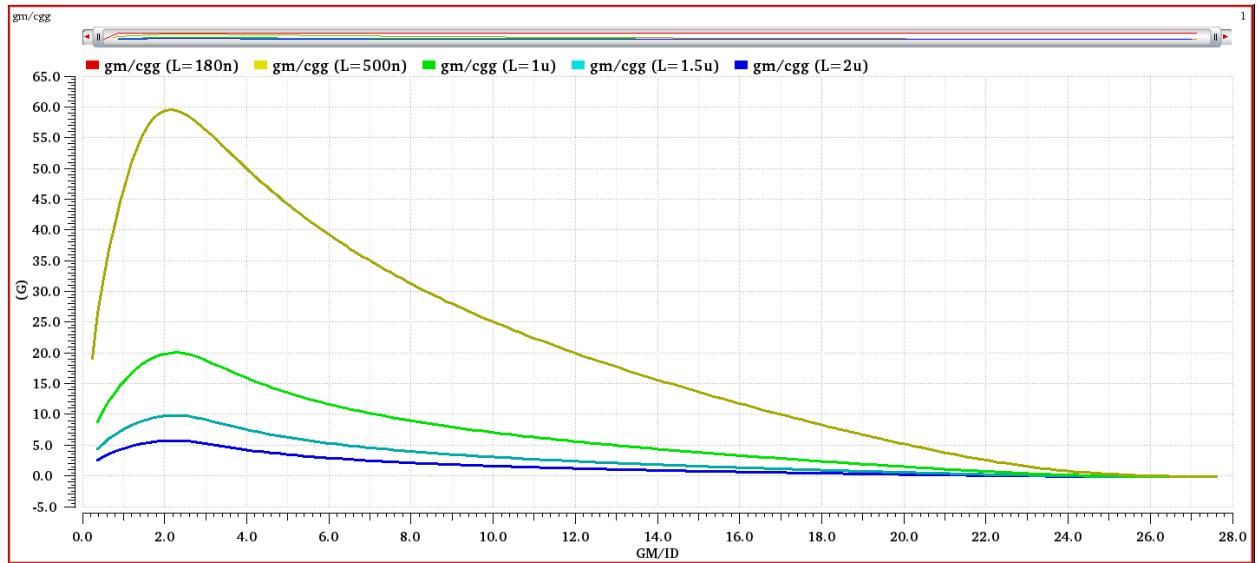
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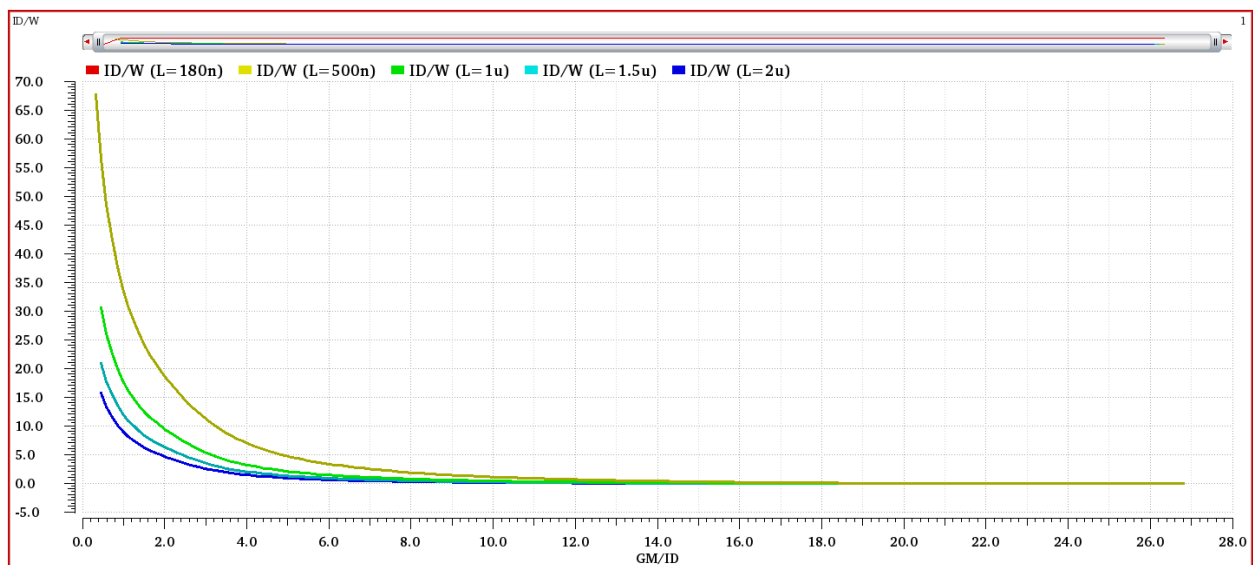
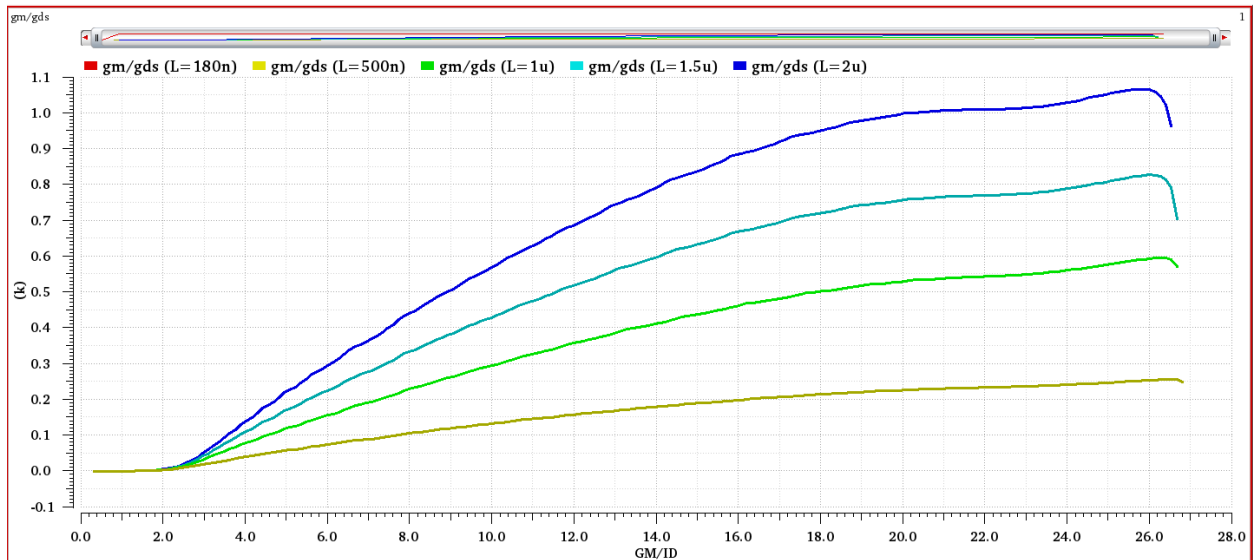
PART 1: gm/ID Design Charts

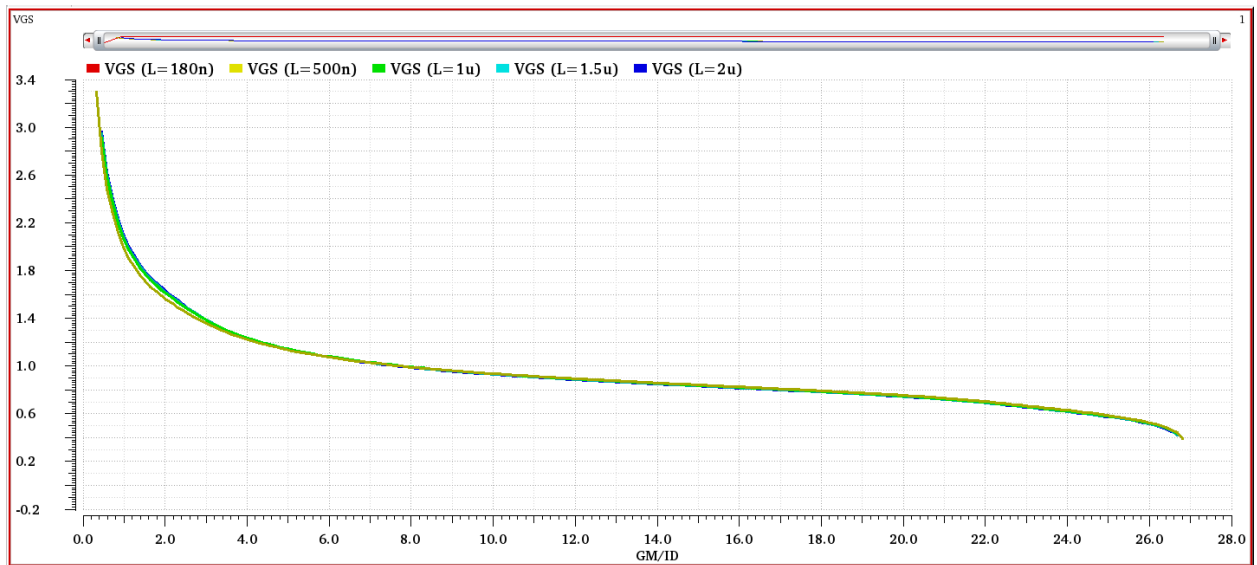
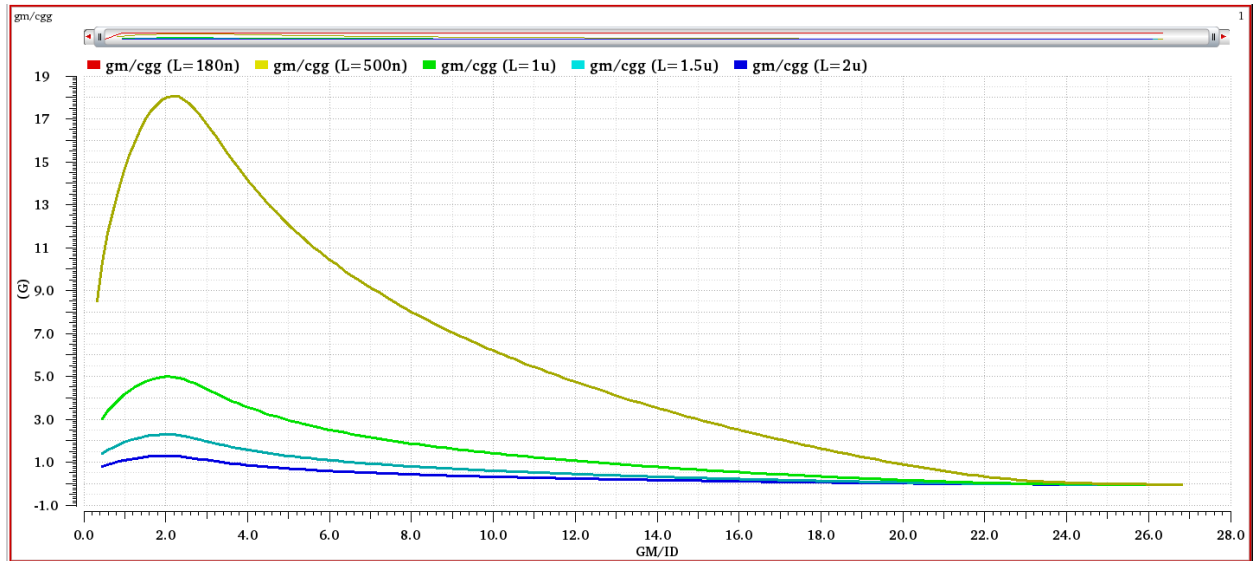
NMOS





PMOS





PART 2: OTA Design

Designing the input pair of the first stage

Since the CMIR high is 0.8 so we will use a PMOS input pair

it was asked to start with start with $C_C = 0.5 C_L$, $C_C = 2.5pF$

$$t_{rise} = 70nS, t_{rise} = 2.2\tau, \tau = 31.8181nS$$

$$UGF = \frac{1}{2\pi\tau}, UGF \approx 5MHz, UGF = \frac{g_m}{2\pi C_{CC}}$$

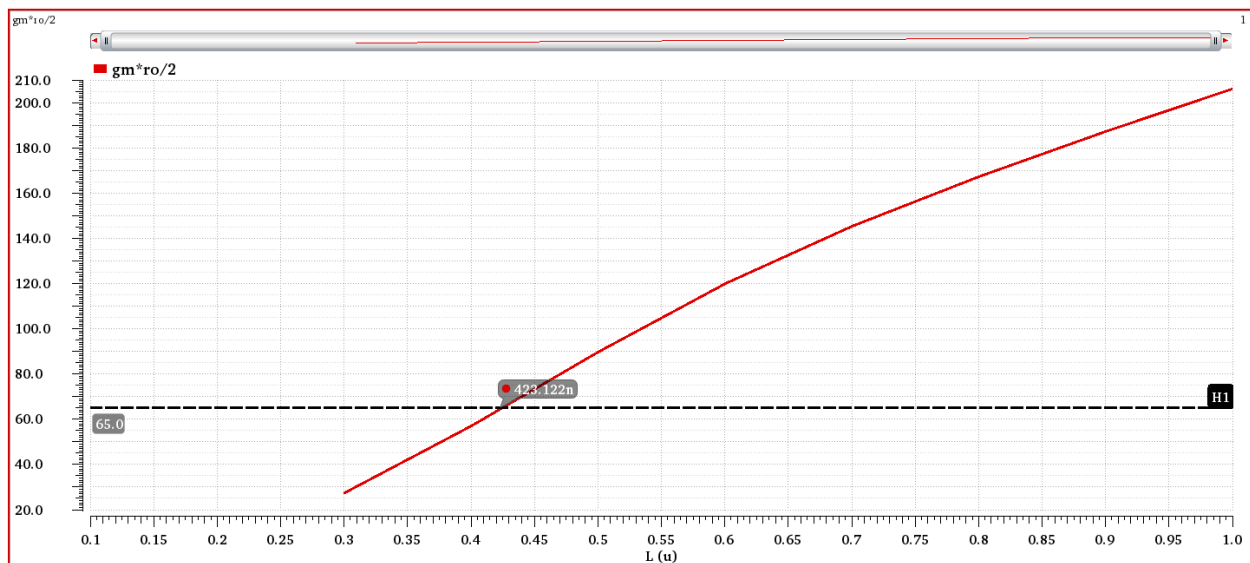
$$g_m = 78.6\mu S$$

$$Slew\ rate = \frac{I_B}{C_{CC}}$$

$$I_B = 12.5\mu A, I_D = 6.25\mu A$$

$$\frac{g_m}{I_D} = 12.576V^{-1}, \text{ however we will use a margin for the } \frac{g_m}{I_D} \text{ to be 14}$$

Assume that the VDD is divided equally to each transistor so $V_{DS} = 0.6V$



The screenshot shows the 'ADT Sizing Assistant' window. At the top, there are 'Settings' and 'Help' buttons. Below them is a 'LUT Settings' section with a 'State1' dropdown and a 'Save State' button. The main settings area includes input fields for 'ID' (6.25u), 'gm/ID' (14), 'L' (430n), 'VDS' (0.6), 'VSB' (0), and 'Stack' (1). There are 'Get' and 'Apply' buttons below these fields. The 'Y-Expr' field contains 'gm*ro/2' and has a 'Plot' button and a 'Replace' dropdown. At the bottom is a 'Device Parameters' table.

#	Parameter	TT-27.0
1	ID	6.25u
2	IG	N/A
3	L	430n
4	W	10.84u
5	VGS	860.6m
6	VDS	600m
7	VSB	0
8	gm/ID	13.76
9	Vstar	145.4m
10	ET	784.5MFC

However after using this dimension the gain of the first stage was 77dB which was above the required gain so we need to make a condition on the g_{ds} to make sure that the gain is within the required range

Since $g_m = 78.6\mu S$ and the gain of the first stage is

$$0.5 g_m g_{ds}$$

$$\text{So } g_{ds} = 126.5 \Omega^{-1}$$

The screenshot shows the 'ADT Sizing Assistant' window. At the top, there are 'Settings' and 'Help' buttons. Below them is a 'LUT Settings' section. A 'State1' dropdown menu is set to 'State1', with a 'Save State' button next to it. Below this, several input fields are shown, each with a dropdown arrow and a text box: 'ID' (6.25u), 'gm/ID' (14), 'gm/gds' (126.5), 'VDS' (0.6), 'VSB' (0), and 'Stack' (1). Below these are 'Get' and 'Apply' buttons. A 'Y-Expr' dropdown is set to '1/(id*ro)', with 'Plot' and 'Append' buttons below it. At the bottom, a 'Device Parameters' table is displayed.

#	Parameter	TT-27.0
1	ID	6.25u
2	IG	N/A
3	L	420n
4	W	10.43u
5	VGS	860m
6	VDS	600m
7	VSB	0
8	gm/ID	13.72
9	Vstar	145.8m

Designing the tail current source

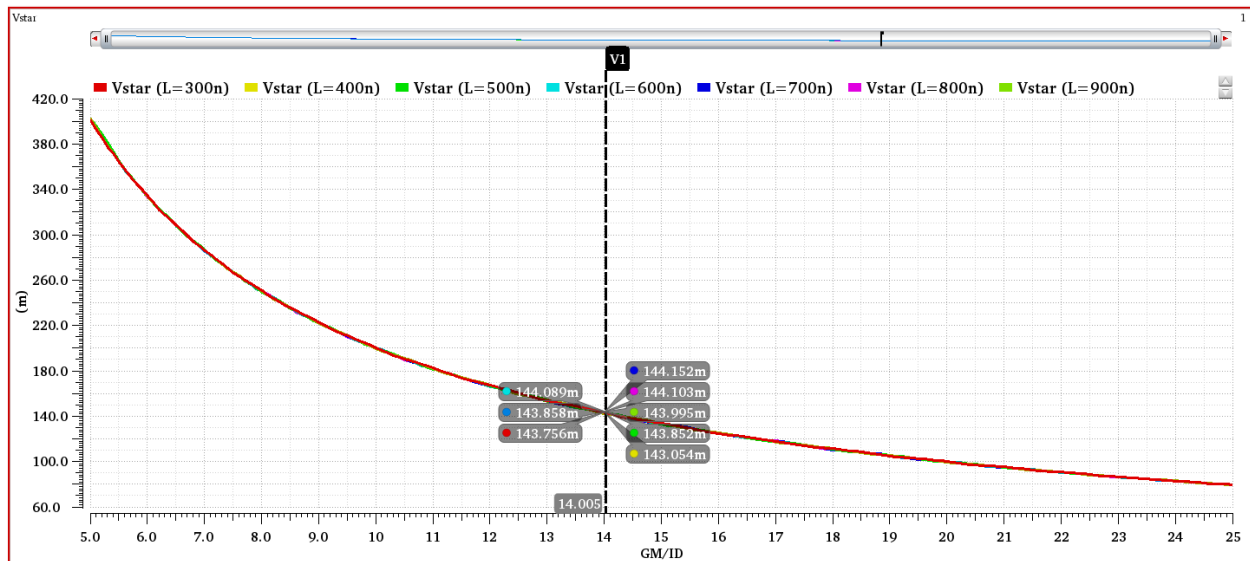
$$I_D = 12.5\mu A, V_{DS} = 0.6V$$

Assume the tail current source will have the same $\frac{g_m}{I_D}$ as the input pair

$$A_{Vcm} = -32dB, A_{Vcm} = \frac{1}{2 \times g_{m_{active_load}} \times \frac{1}{g_{ds_{tail}}}}$$

$$g_{m_{active_load}} = \frac{g_m}{I_D} \times I_D, I_D = 6.25\mu A, \frac{g_m}{I_D} = 10V^{-1}$$

$$g_{m_{active_load}} = 62.5\mu S$$



$$V^* = 0.14V$$

ADT Sizing Assistant
?
⛔
✕

Settings
Help

▶ LUT Settings

State1
Save State

ID
12.5u

gm/ID
14

gds
2.49u

VDS
0.6

VSB
0

Stack
1

Get
Apply

Y-Expr
vgs-vth

Plot
Replace

Device Parameters

#	Parameter	TT-27.0
1	ID	12.5u
2	IG	N/A
3	L	330n
4	W	15.34u
5	VGS	836.4m
6	VDS	600m
7	VSB	0
8	gm/ID	13.61
9	Vstar	146.9m

Designing the Transistor connected to IBIAS

Assuming the transistor connected to IBIAS is annotated with M1 and the tail current source is M2

Assuming all the current mirror transistors will have the same L

Assuming $\lambda = 0.1$

$$i_1 = 10\mu A$$

$$i_2 = 12.5\mu A$$

$$V_{DS_1} = 1.8V$$

$$V_{DS_2} = 0.6V$$

$$W_1 = W_2 \frac{(1+\lambda V_{DS_2})}{(1+\lambda V_{DS_1})} \frac{i_1}{i_2}$$

$$W_1 \approx 11.1\mu m, L_1 = 330nm$$

Designing the Transistor connected above the second stage

Assuming the transistor connected to IBIAS is annotated with M1 and the Transistor connected above the second stage M2

Assuming all the current mirror transistors will have the same L

Assuming $\lambda = 0.1$

$$i_1 = 10\mu A$$

$$i_2 = 47.5\mu A$$

$$V_{DS_1} = 1.8V$$

$$V_{DS_2} = 0.9V$$

$$W_2 = W_1 \frac{(1+\lambda V_{DS_1})}{(1+\lambda V_{DS_2})} \frac{i_2}{i_1}$$

$$W_2 \approx 57\mu m, L_2 = 330nm$$

However when i ran the dc op the value of VOUT was 1.1V which means that the value of the W needed tuning so I ran dc sweep on W to find the value of the W that will give VOUT=0.9V and it was $W_2 \approx 50.7\mu m$

Point ^	Test	Output	Nominal	Spec	Weight	Pass/Fail
5	ITI:LAB9:1	VOUT	882.1m			
Parameters: W_tail_mirror=50.5u						
6	ITI:LAB9:1	VOUT	888.7m			
Parameters: W_tail_mirror=50.6u						
7	ITI:LAB9:1	VOUT	895.3m			
Parameters: W_tail_mirror=50.7u						
8	ITI:LAB9:1	VOUT	901.8m			
Parameters: W_tail_mirror=50.8u						
9	ITI:LAB9:1	VOUT	908.4m			
Parameters: W_tail_mirror=50.9u						
10	ITI:LAB9:1	VOUT	914.9m			
Parameters: W_tail_mirror=51u						
11	ITI:LAB9:1	VOUT	921.4m			
Parameters: W_tail_mirror=51.1u						
12	ITI:LAB9:1	VOUT	927.9m			
Parameters: W_tail_mirror=51.2u						
13	ITI:LAB9:1	VOUT	934.4m			

Designing the active-load

$$I_D = 6.25\mu A, V_{DS} = 0.6V$$

$$V_{gs} \geq V_{inCM_{min}} + V_{TH_{input_pair}}, V_{TH_{input_pair}} = 789mV$$

$$V_{gs} \geq 830mV$$

So we will take margin

$$V_{gs} = 840mV$$

The screenshot shows the 'ADT Sizing Assistant' window. It has a 'Settings' button and a 'Help' button. Below them is a 'LUT Settings' section with a 'State1' dropdown and a 'Save State' button. The main settings area includes fields for 'ID' (6.25u), 'VGS' (840m), 'ro' (1.6Meg), 'VDS' (0.6), 'VSB' (0), and 'Stack' (1). There are 'Get' and 'Apply' buttons. Below these is a 'Y-Expr' field set to 'vgs-vth' and 'Plot' and 'Replace' buttons. At the bottom is a 'Device Parameters' table.

#	Parameter	TT-27.0
1	ID	6.222u
2	IG	N/A
3	L	480n
4	W	1.44u
5	VGS	840m
6	VDS	600m
7	VSB	0
8	gm/ID	10.04
9	Vstar	199.2m
10	ET	4.218C

Designing the second stage

$$I_D = 47.5\mu A$$

$$V_{DS} = 0.9V$$

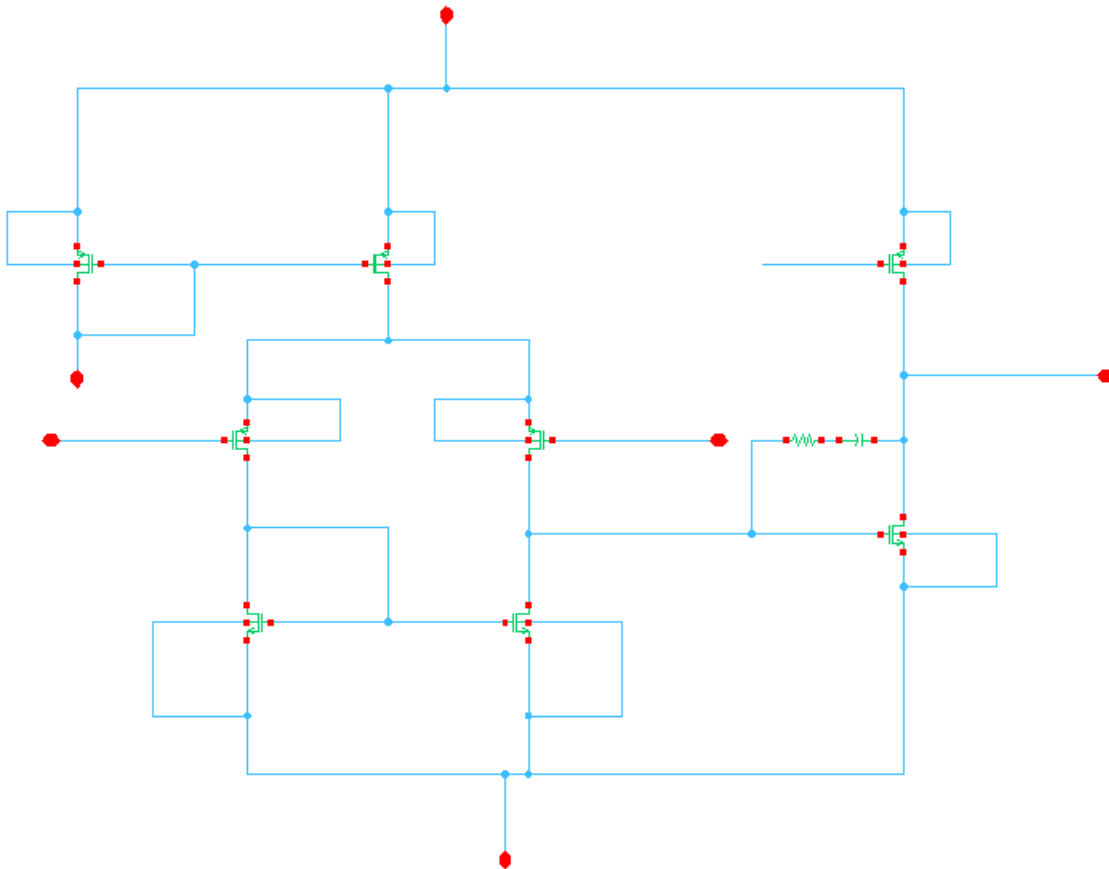
$$\frac{g_m}{g_{ds}} = 64$$

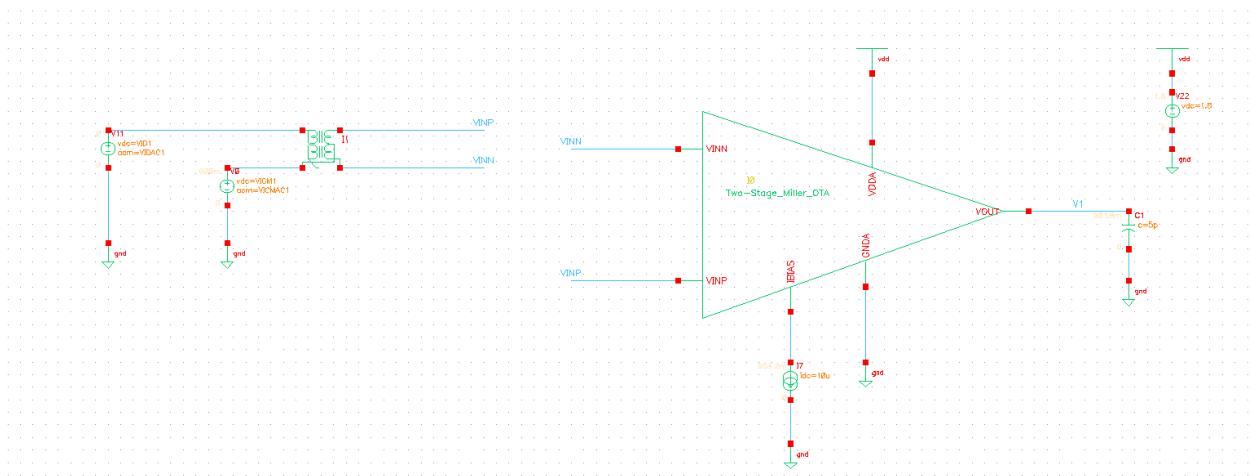
The screenshot shows the 'ADT Sizing Assistant' window. It has a 'Settings' button and a 'Help' button. Under 'LUT Settings', there is a 'State1' dropdown and a 'Save State' button. Below this, there are several input fields with dropdown menus: 'ID' (47.5u), 'VGS' (839.7m), 'gm/gds' (64), 'VDS' (0.9), and 'VSB' (0). There is also a 'Stack' input field with the value '1'. Below these are 'Get' and 'Apply' buttons. The 'Y-Expr' field contains '1/(id*ro)' and has a dropdown arrow. Below it are 'Plot' and 'Append' buttons. At the bottom, there is a 'Device Parameters' section with a table.

#	Parameter	TT-27.0
1	ID	46.69u
2	IG	N/A
3	L	370n
4	W	6.52u
5	VGS	839.7m
6	VDS	900m
7	VSB	0
8	gm/ID	8.842
9	Vstar	226.2m

<i>Topology</i>	<i>W</i>	<i>L</i>
<i>First stage input pair</i>	$10.43\mu m$	$420nm$
<i>tail (above the first stage input pair)</i>	$15.34\mu m$	$330nm$
<i>tail (Connected to IBIAS)</i>	$11.1\mu m$	$330nm$
<i>tail (above the second stage)</i>	$50.7\mu m$	$330nm$
<i>Second stage</i>	$6.52\mu m$	$370nm$

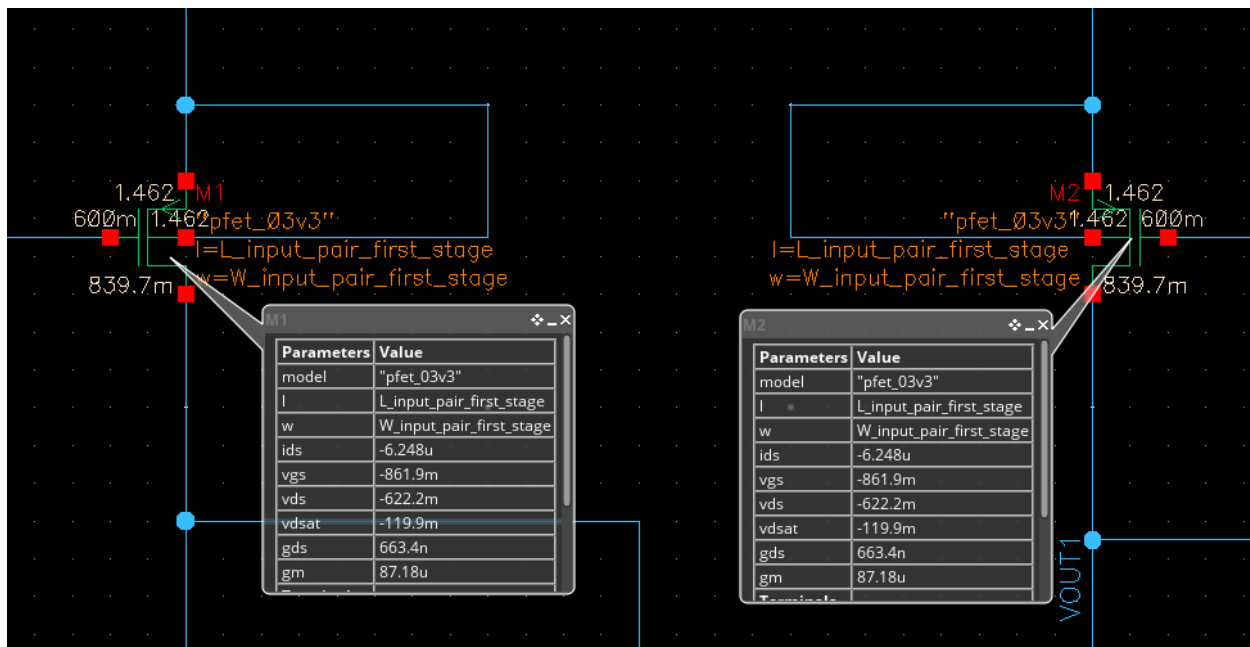
PART 3: Open-Loop OTA Simulation





DC op

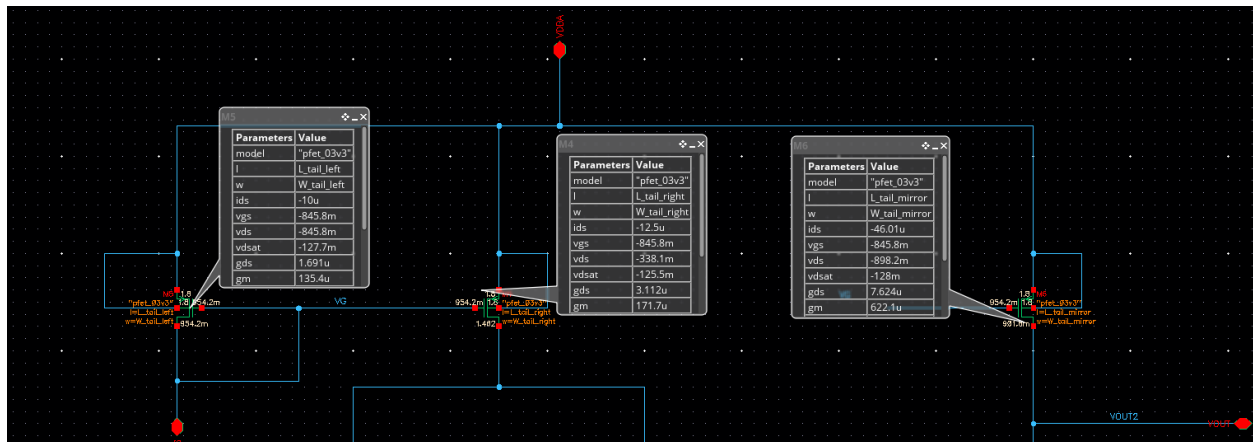
Input pair of the first stage



$$W_{input_pair_first_stage} = 10.4\mu m$$

$$L_{input_pair_first_stage} = 420nm$$

Tail current source



$$W_{tail_left} = 11.1\mu\text{m}$$

$$L_{tail_left} = 330\text{nm}$$

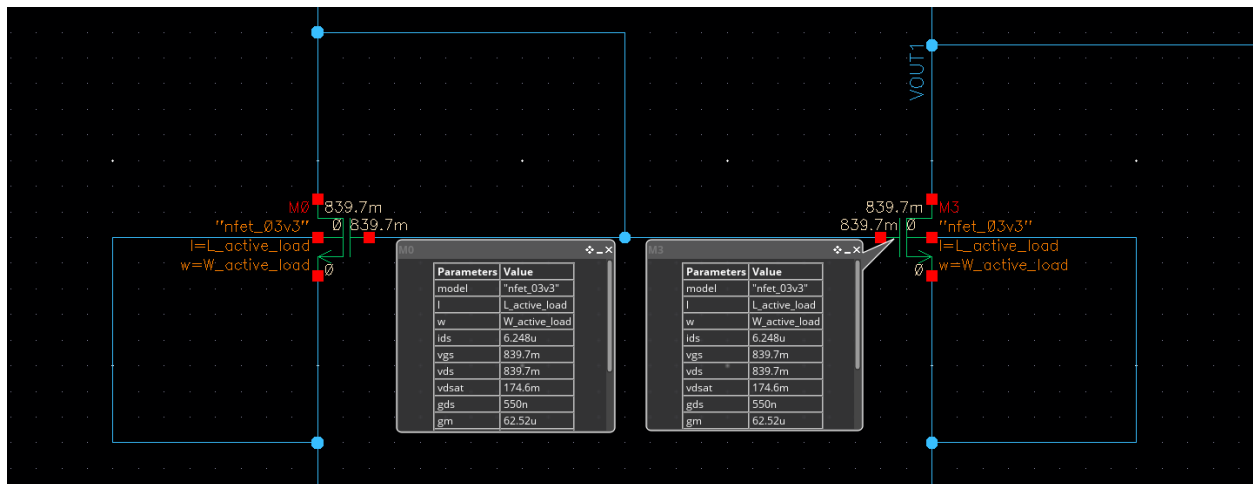
$$W_{tail_right} = 15.34\mu\text{m}$$

$$L_{tail_right} = 330\text{nm}$$

$$W_{tail_mirror} = 50.7\mu\text{m}$$

$$L_{tail_mirror} = 330\text{nm}$$

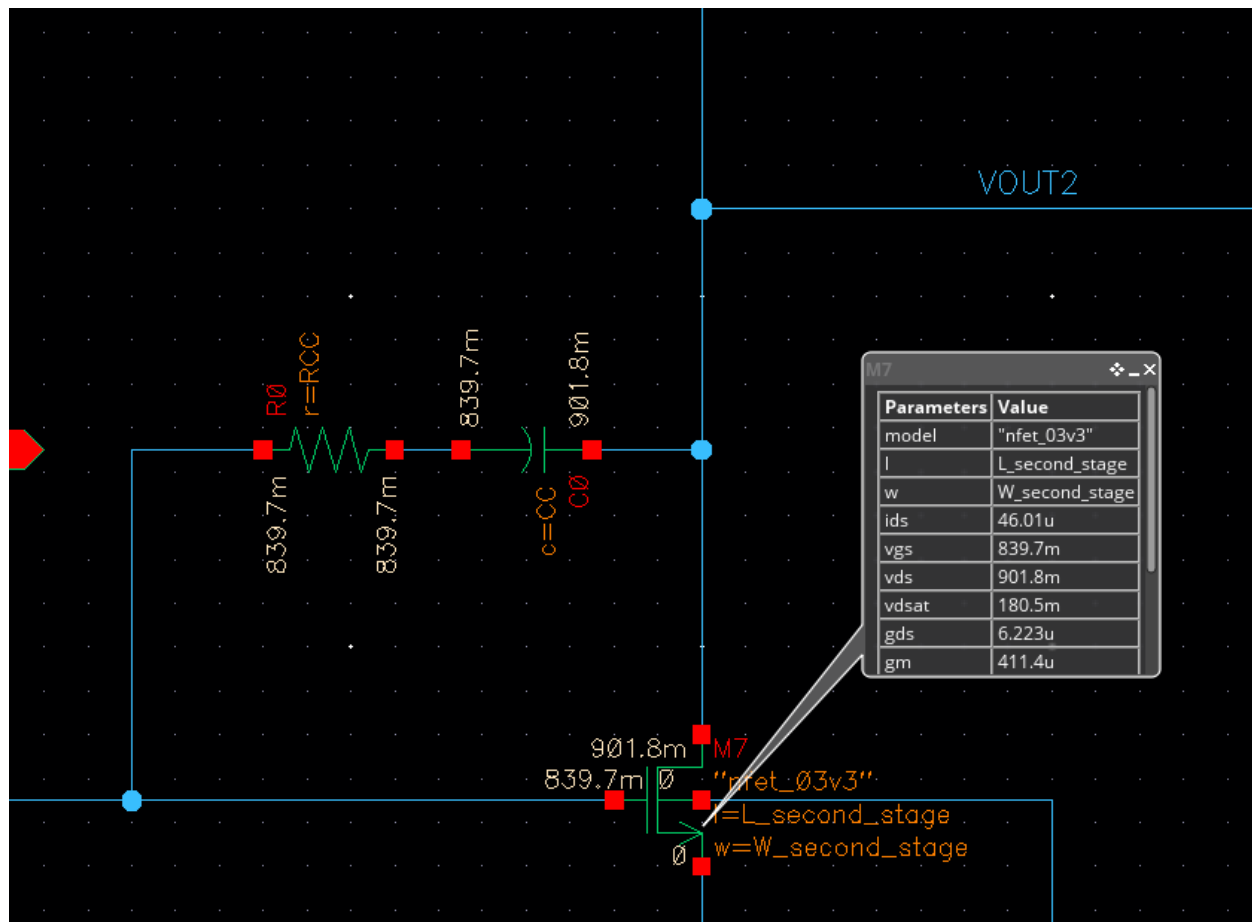
Active-load



$$W_{active_load} = 1.44\mu\text{m}$$

$$L_{active_load} = 480\text{nm}$$

Second stage

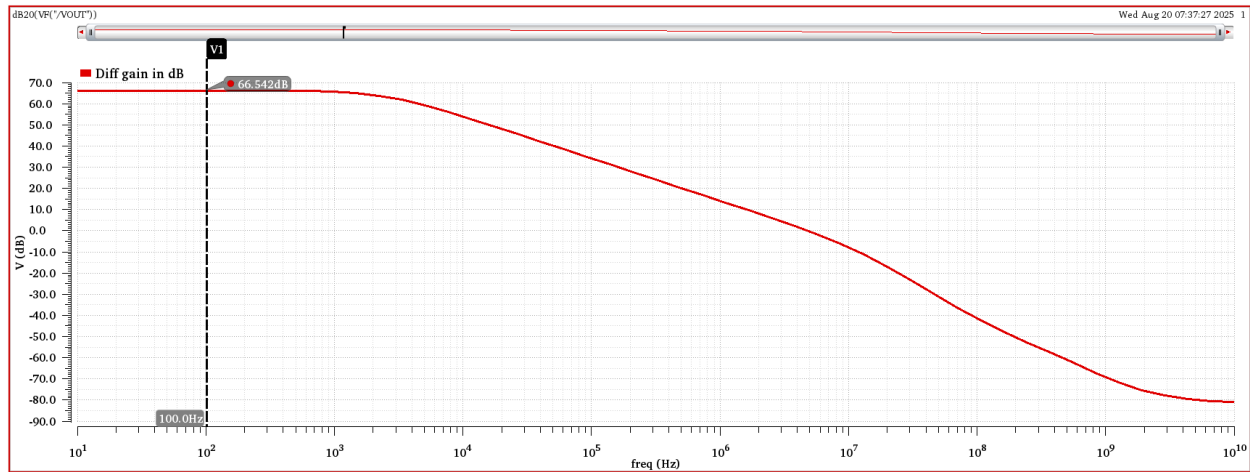


$$W_{second_stage} = 6.52\mu m$$

$$L_{second_stage} = 370nm$$

- The bias current splits equally between the transistors of the differential pair. Since both devices experience identical operating conditions, which makes also g_m exactly equal.
- The value of VOUT2=901.8mV as this is the value where the output swing is maximized.

Diff small signal ccs



Test	Output	Nominal	Spec	Weight	Pass/Fail
ITi:LAB9:1	DC_gain_linear	2.125k			
ITi:LAB9:1	DC_gain_dB	66.55			
ITi:LAB9:1	Bandwidth	2.5k			
ITi:LAB9:1	Unity_gain_frequency	5.123M			
ITi:LAB9:1	GBW	5.314M			

Hand analysis

$$A_V = g_{m_{input_pair}}(r_{o_{input_pair}} // r_{o_{active_load}}) g_{m_{second_stage}}(r_{o_{second_stage}} // r_{o_{tail}})$$

$$A_V = 2126.34$$

$$A_V = 66.55 \text{ dB}$$

$$Bandwidth = \frac{1}{2\pi RC(1 + g_{m_{input_pair}})(r_{o_{second_stage}} // r_{o_{tail}})}$$

$$R = (r_{o_{second_stage}} // r_{o_{tail}}), C = C_C$$

$$Bandwidth = 2.5 \text{ KHz}$$

$$\text{Unity gain frequency}$$

$$UGF = \frac{g_{m_{input_pair}}}{2\pi C_{CC}}$$

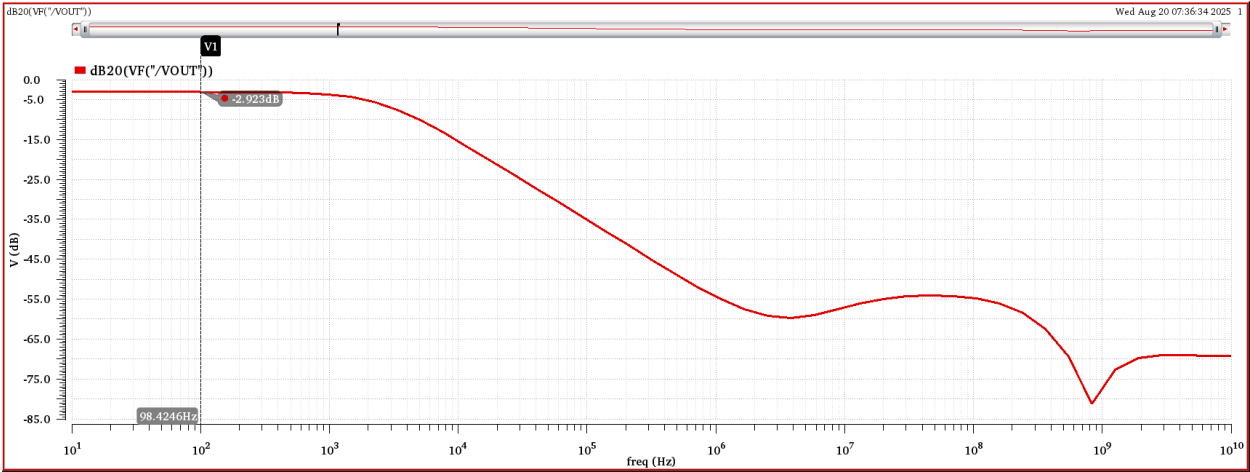
$$UGF = 5.55 \text{ MHz}$$

$$GBW = A_V \times Bandwidth$$

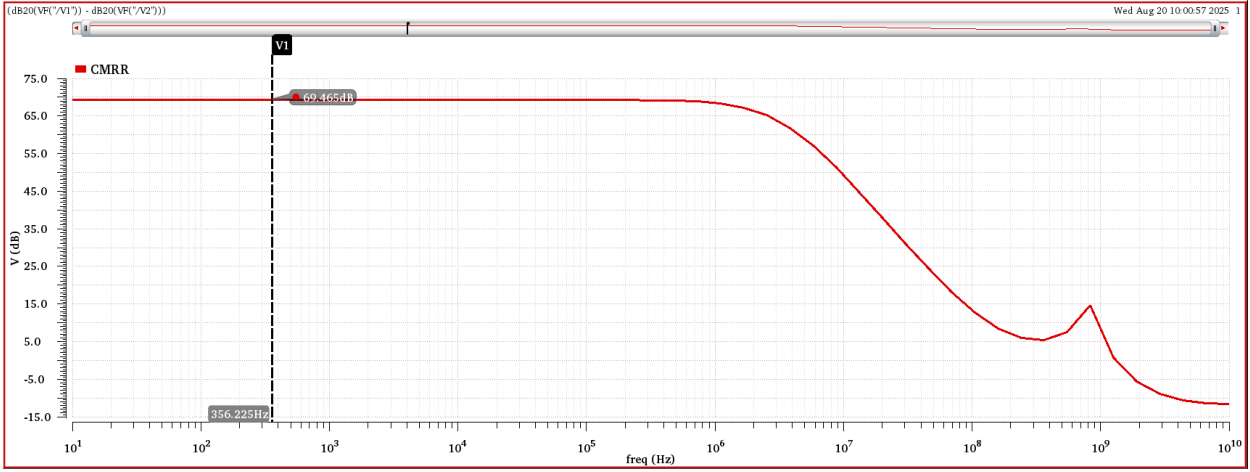
GBW=5.315MHz

<i>parameter</i>	Simulation value	Hand- analysis value
<i>DC gain</i>	66.55 dB	66.55 dB
<i>Bandwidth</i>	2.5KHz	2.5KHz
<i>UGF</i>	5.123MHz	5.55MHz
<i>GBW</i>	5.314MHz	5.315MHz

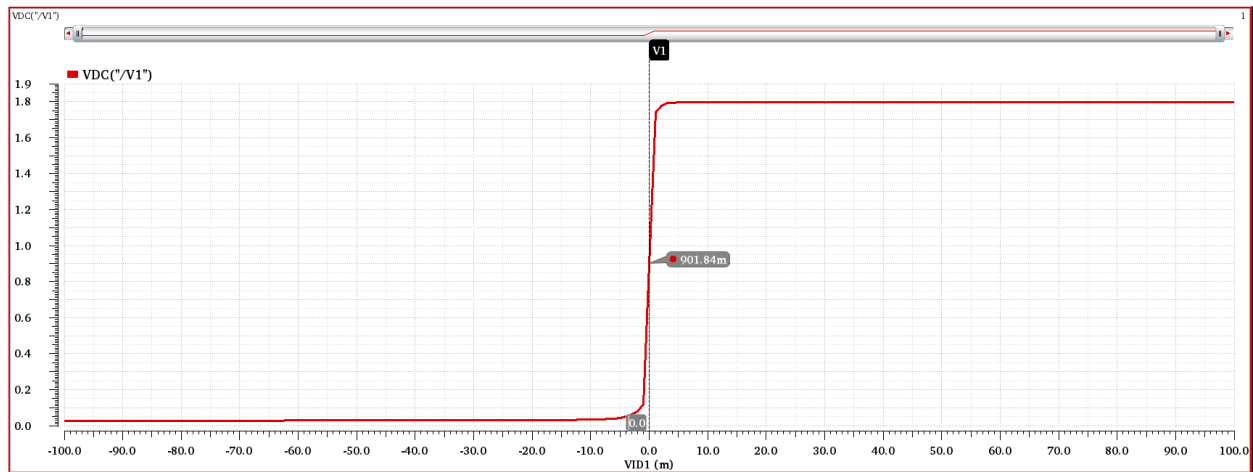
CM small signal ccs



CMRR(Optional)

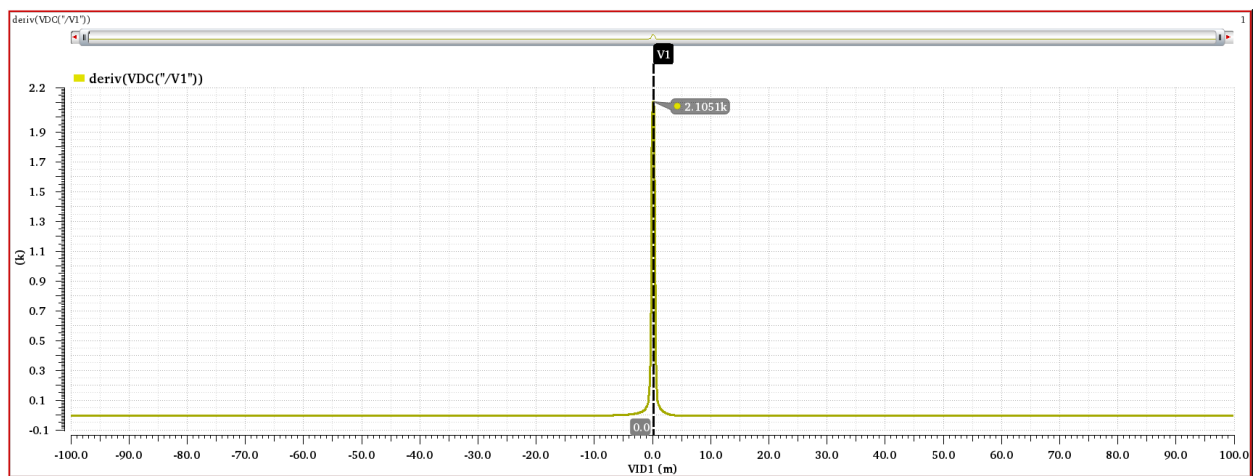


Diff large signal ccs (Optional)



Comment:

The value of V_{out} at $VID=0$ is exactly equal to V_{OUT2} in the DC OP

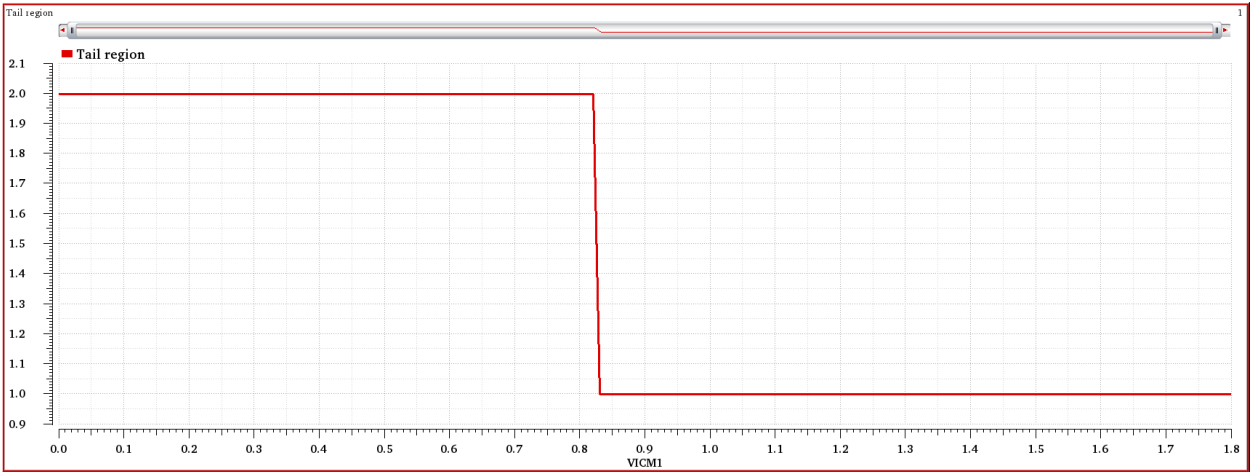
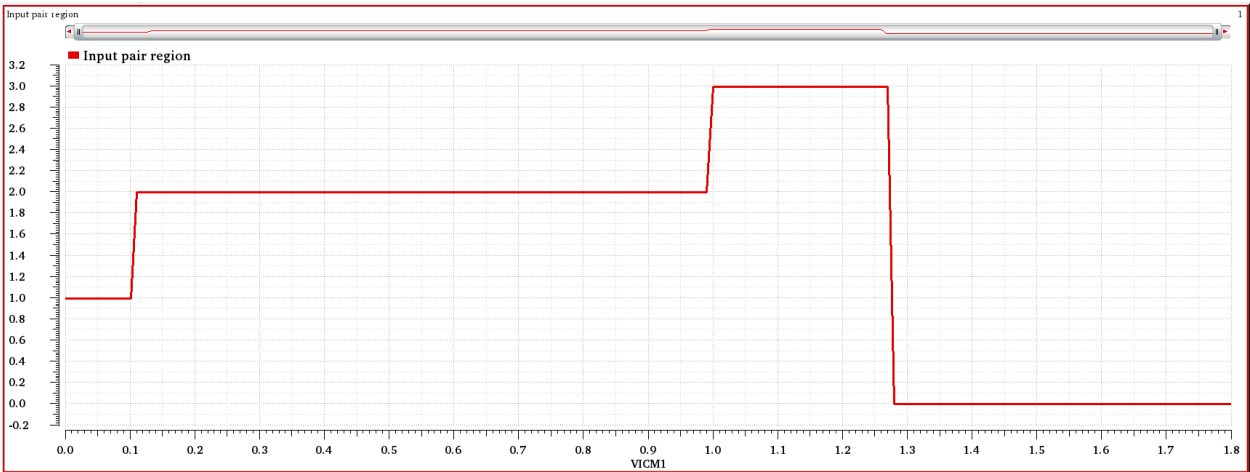


Comment:

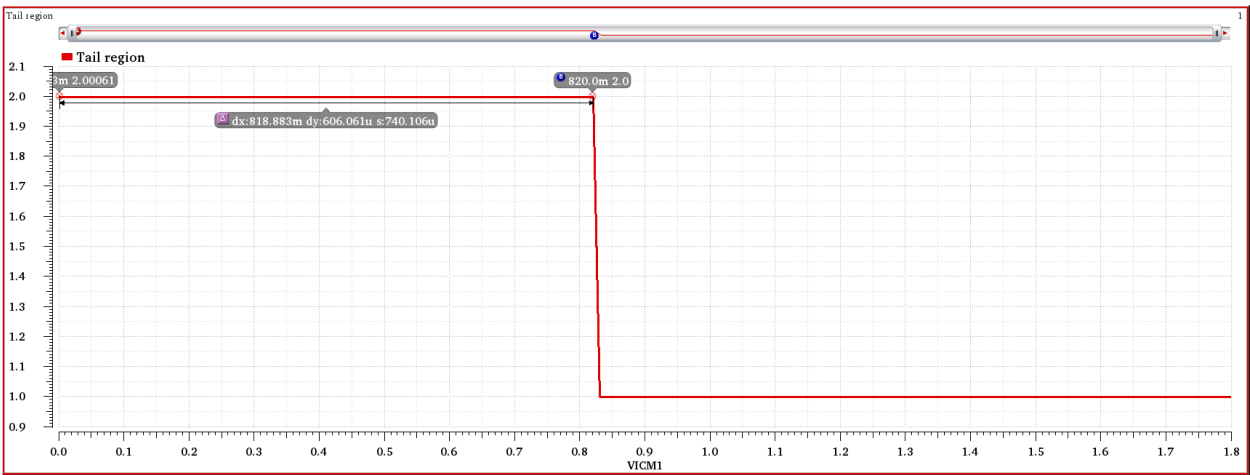
The DC gain extracted from the plot is nearly exactly similar to the value of the DC gain calculated in the DC OP

CM large signal ccs (region vs VICM)

Regions



CMIR



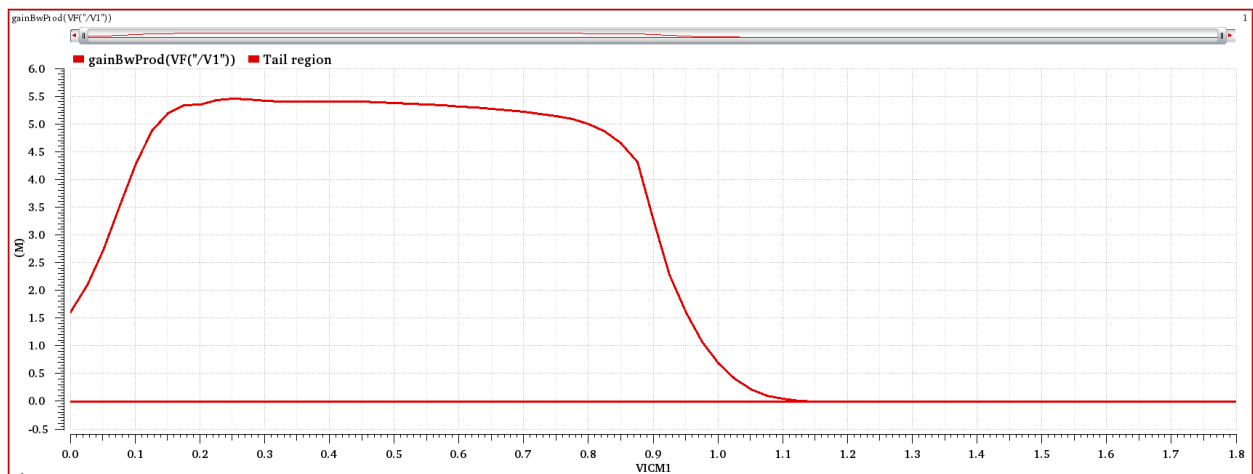
Hand analysis

$$V_{in_{max}} = V_{DD} - V_{sg_{input_{pair}}} - V_{dsat_{input_{pair}}}$$

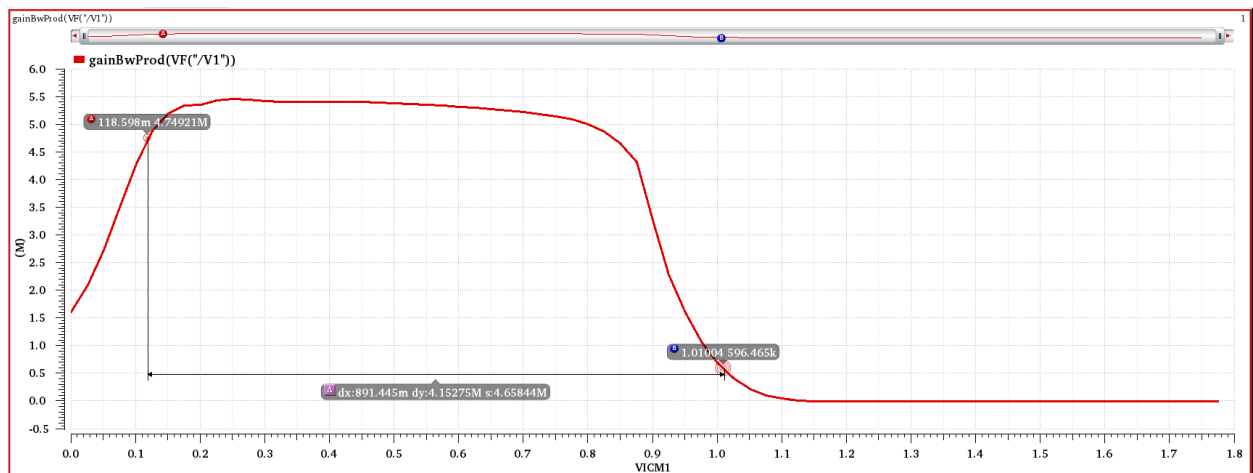
$$V_{in_{max}} = 1.8 - 0.8619 - 0.119$$

$$V_{in_{max}} = 0.8191V$$

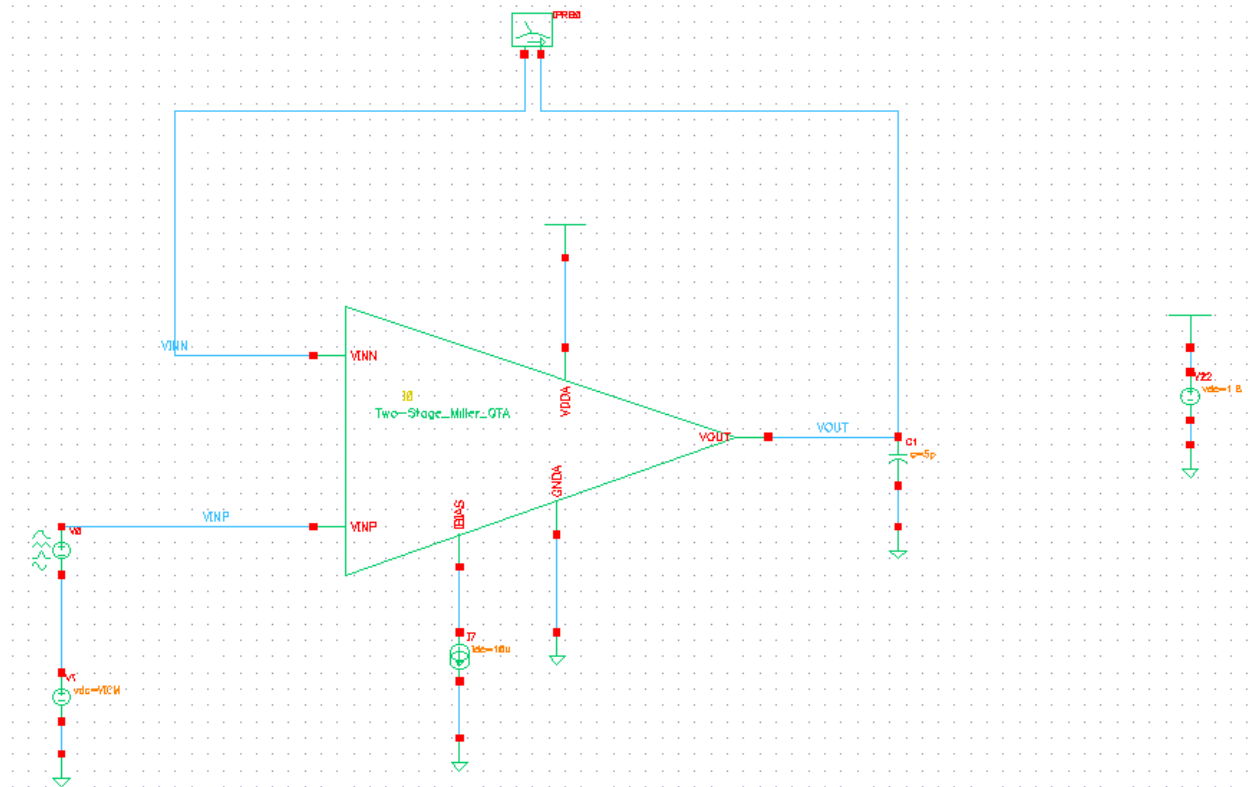
CM large signal ccs (GBW vs VICM) (Optional)



Input range calculated from the GBW graph

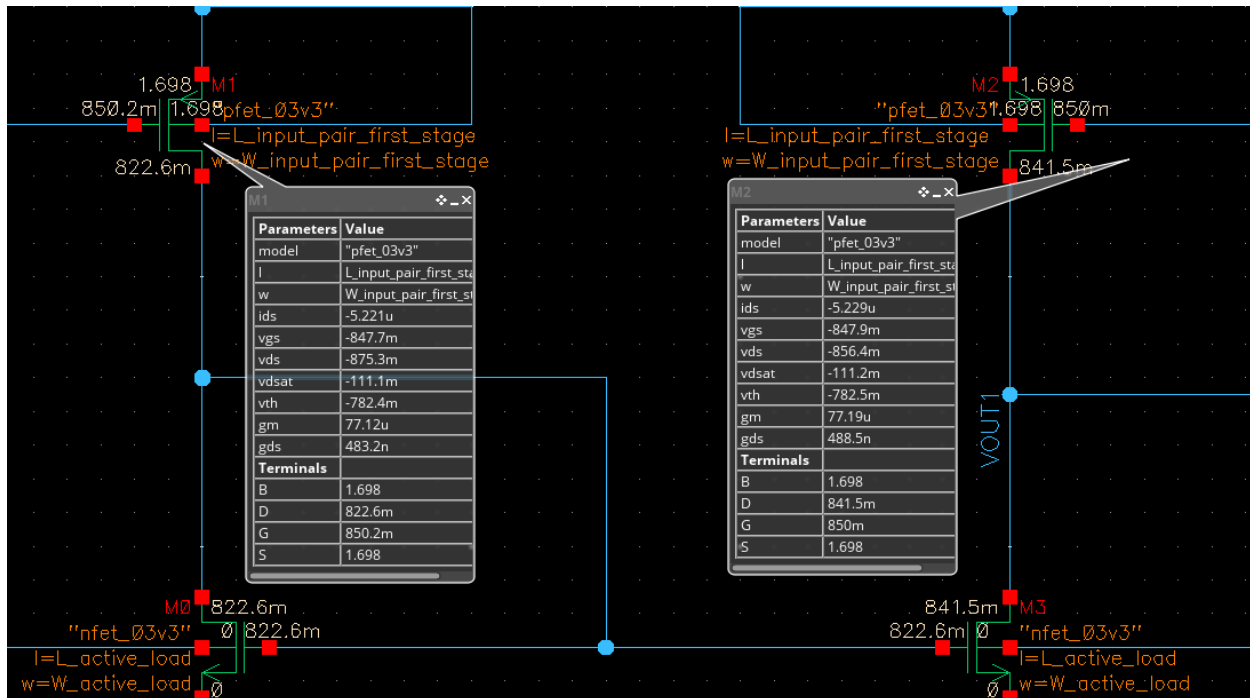


PART 4: Closed-Loop OTA Simulation

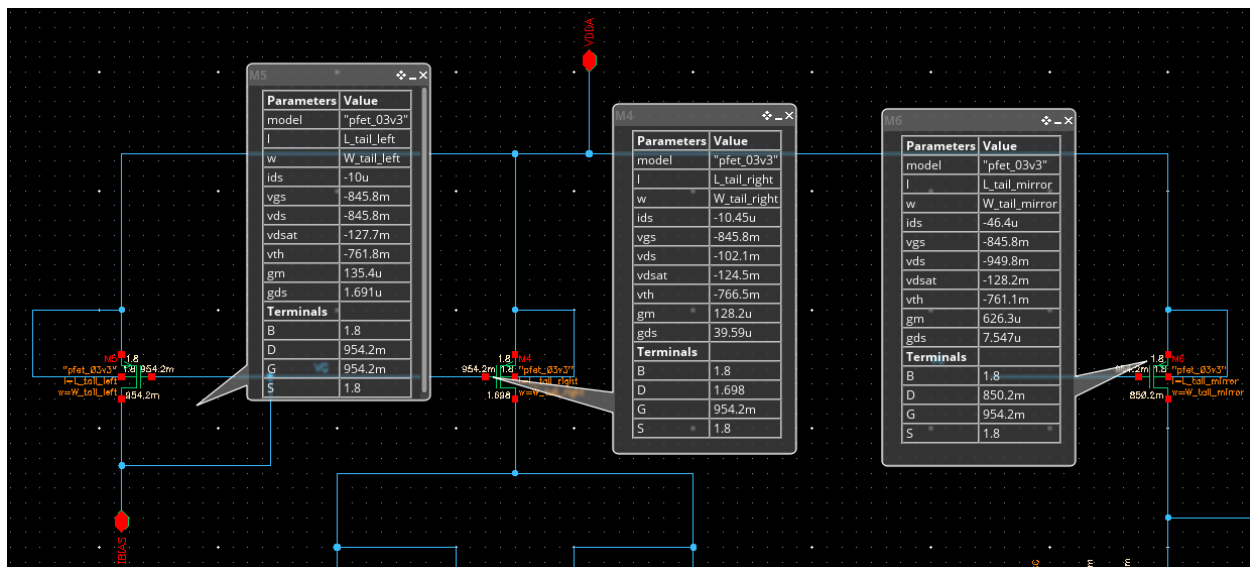


DC OP

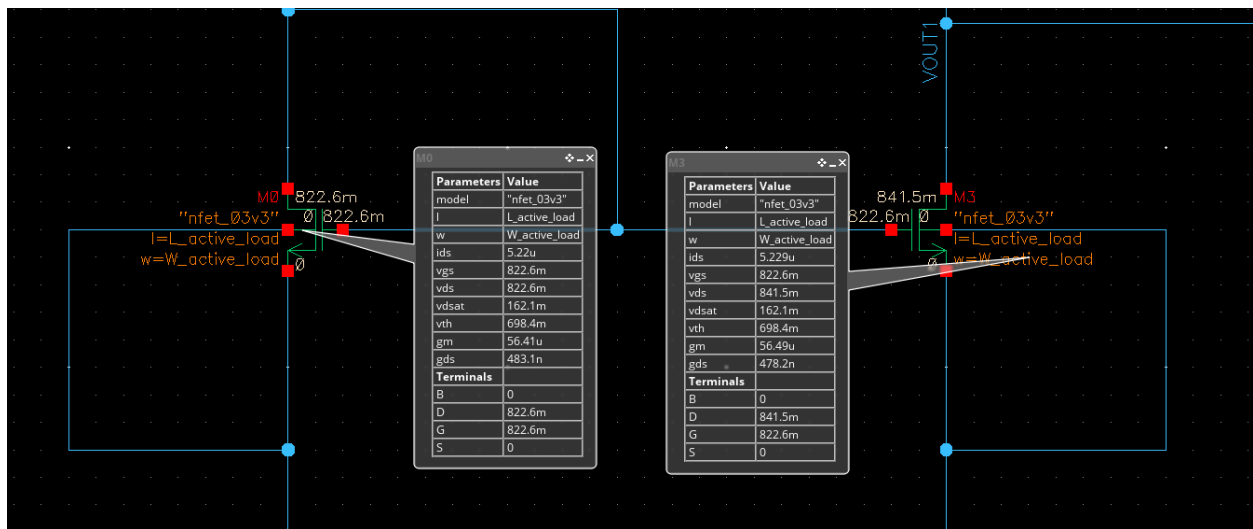
Input pair of the first stage



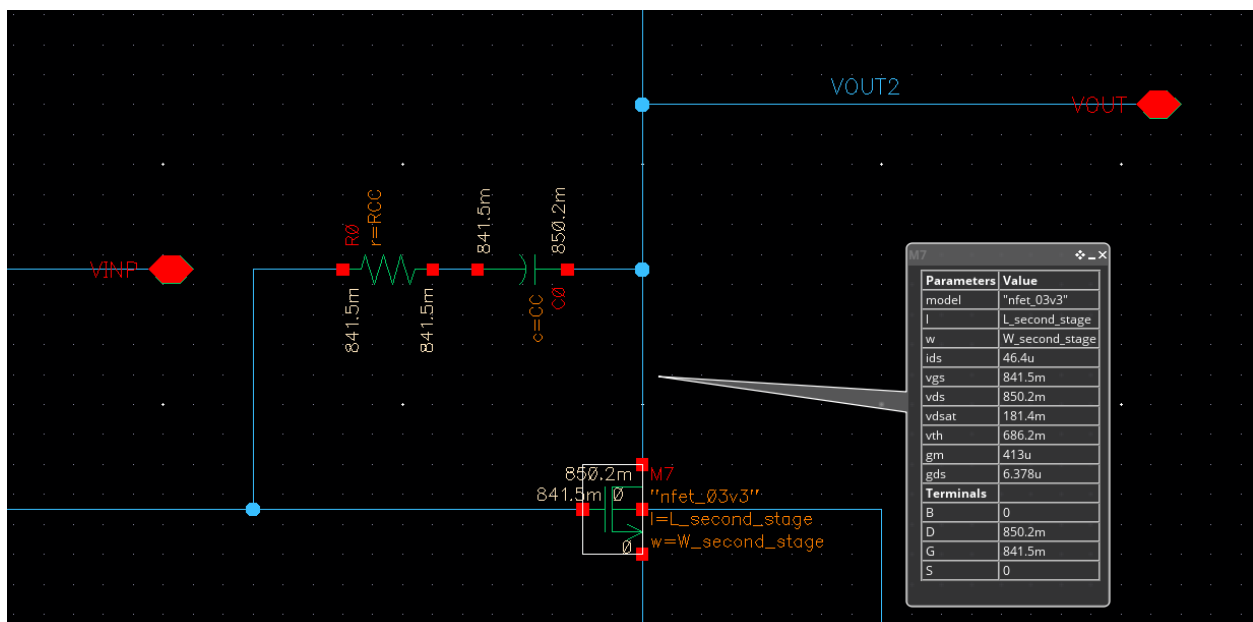
Tail current source



Active load



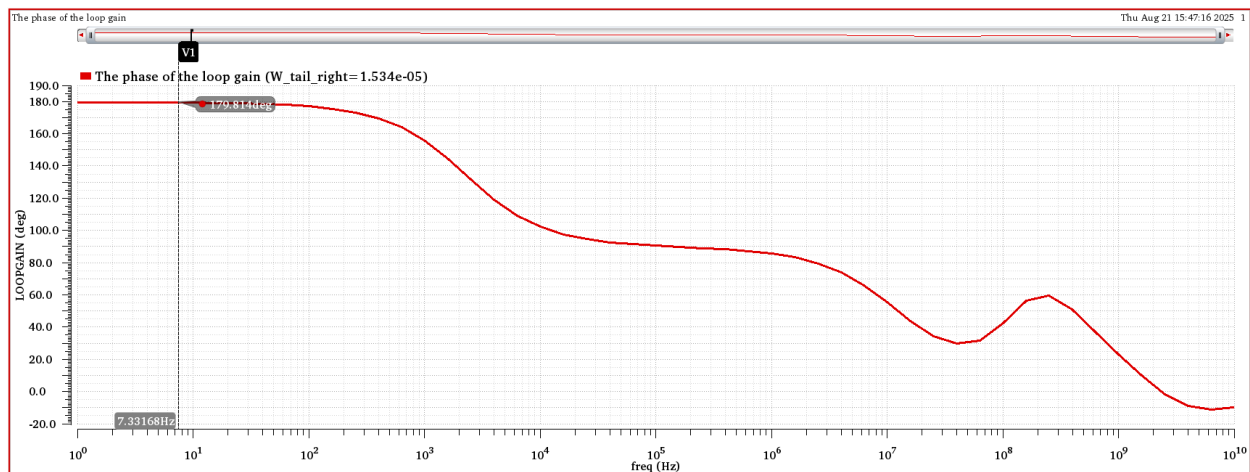
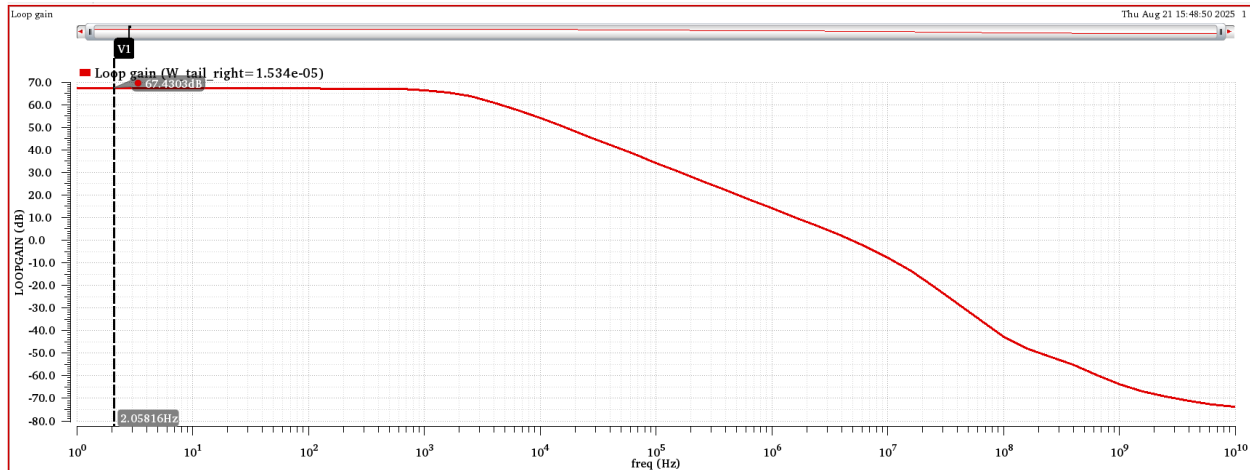
Second stage



- The DC output voltage of the first stage in the closed-loop configuration is not exactly equal to that observed in the open-loop simulation. In the closed-loop, the feedback action slightly adjusts the operating point of the input pair to enforce the feedback condition. This results in a small shift in the output DC voltage compared to the open-loop bias point, even though both remain close.

- The currents in the input differential pair are not exactly equal. This is because any small the effect of feedback causes a slight imbalance in the tail current distribution. In closed-loop operation, the feedback drives one transistor to conduct slightly more than the other. As a result, the g_m values differ slightly

Loop gain



Test	Output	Nominal	Spec	Weight	Pass/Fail
ITl:Closed_Loop_OTA_Simulation:1	DC_gain_dB	67.43			
ITl:Closed_Loop_OTA_Simulation:1	DC_gain_linear	2.352k			
ITl:Closed_Loop_OTA_Simulation:1	Unity gain	4.615M			
ITl:Closed_Loop_OTA_Simulation:1	Phase margin	73.18			
ITl:Closed_Loop_OTA_Simulation:1	Bandwidth	2.008k			
ITl:Closed_Loop_OTA_Simulation:1	GBW	4.724M			

Hand analysis

$$A_V = g_{m_{input_pair}}(r_{o_{input_pair}} // r_{o_{active_load}}) g_{m_{second_stage}}(r_{o_{second_stage}} // r_{o_{tail}})$$

$$A_V = 2378.726$$

$$A_V = 67.527 \text{ dB}$$

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

$$A_{OL} = 2000$$

$$\beta = -7.49 \times 10^{-5}$$

$$\text{Bandwidth} = BW_{OL}(1 + A_{OL}\beta)$$

$$\text{Bandwidth} = 2125 \text{ Hz}$$

$$UGF_{CL} = UGF_{CL}(1 + A_{OL}\beta)$$

$$UGF = 4.356 \text{ MHz}$$

$$GBW_{CL} = GBW_{CL}(1 + A_{OL}\beta)$$

$$GBW = 4.5187 \text{ MHz}$$

$$\text{Phase margin} = 180 - \tan^{-1}\left(\frac{UGF}{\text{Dominant pole}}\right) - \tan^{-1}\left(\frac{UGF}{\text{Non-dominant pole}}\right)$$

$$\text{Dominant pole} = 2.008 \text{ KHz}$$

$$\text{Non-dominant pole} = 4 \times \omega_u$$

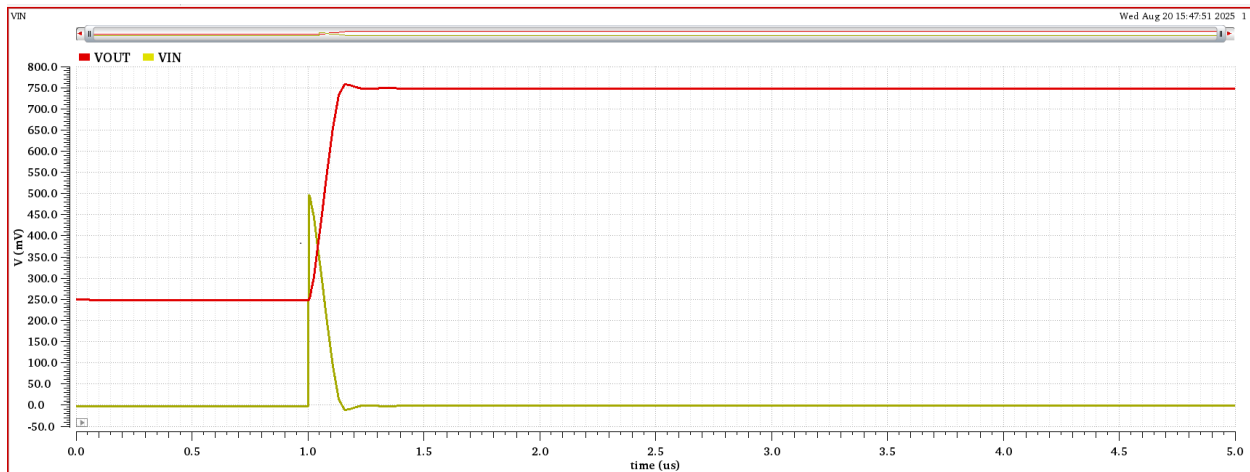
$$\text{Non-dominant pole} = 18.46 \text{ MHz}$$

$$\text{Phase margin} = 75.98^\circ$$

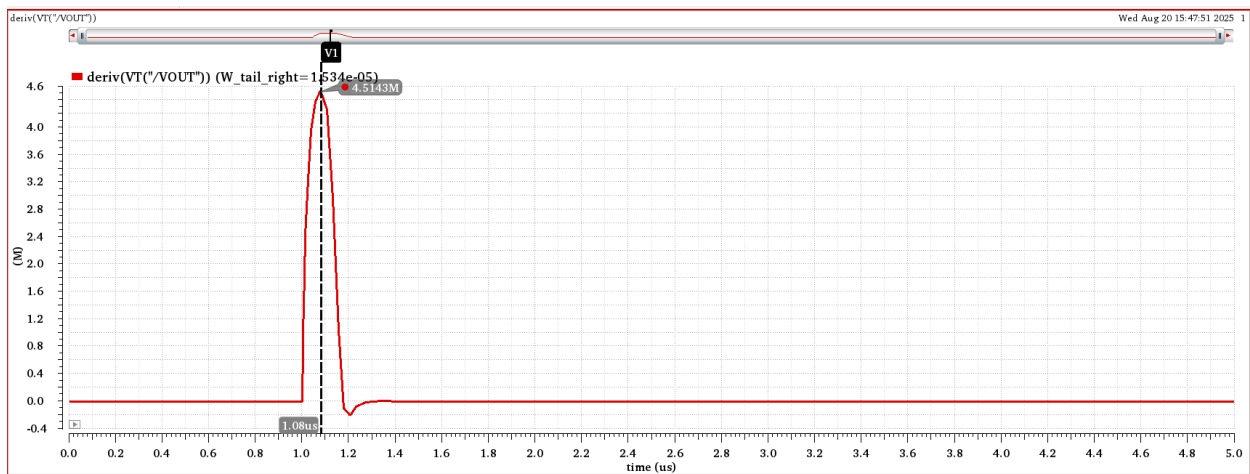
<i>parameter</i>	Simulation value	Hand- analysis value
<i>DC gain</i>	67.43 dB	67.527 dB
<i>Bandwidth</i>	2.008 KHz	2.125 KHz
<i>UGF</i>	4.615 MHz	4.5187 MHz
<i>GBW</i>	4.724 MHz	4.5187 MHz

Slew rate

VOUT and VIN overlaid



Slew rate



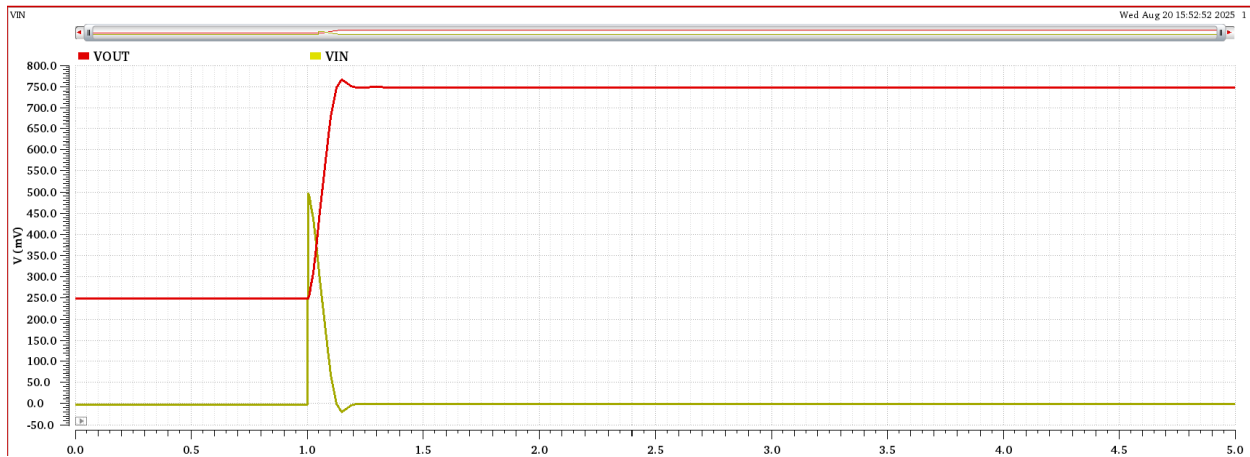
Comment: The value of the slew rate is below the required value which is 5M so this mean the value of the C_c needs tuning

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: CC=2p						
1	ITi:Closed_Loop_OTAsimulation:1	y _{max} (deriv(VT("/VOUT")))	5.444M			
Parameters: CC=2.1p						
2	ITi:Closed_Loop_OTAsimulation:1	y _{max} (deriv(VT("/VOUT")))	5.24M			
Parameters: CC=2.2p						
3	ITi:Closed_Loop_OTAsimulation:1	y _{max} (deriv(VT("/VOUT")))	5.049M			
Parameters: CC=2.3p						
4	ITi:Closed_Loop_OTAsimulation:1	y _{max} (deriv(VT("/VOUT")))	4.87M			
Parameters: CC=2.4p						
5	ITi:Closed_Loop_OTAsimulation:1	y _{max} (deriv(VT("/VOUT")))	4.701M			
Parameters: CC=2.5p						
6	ITi:Closed_Loop_OTAsimulation:1	y _{max} (deriv(VT("/VOUT")))	4.543M			

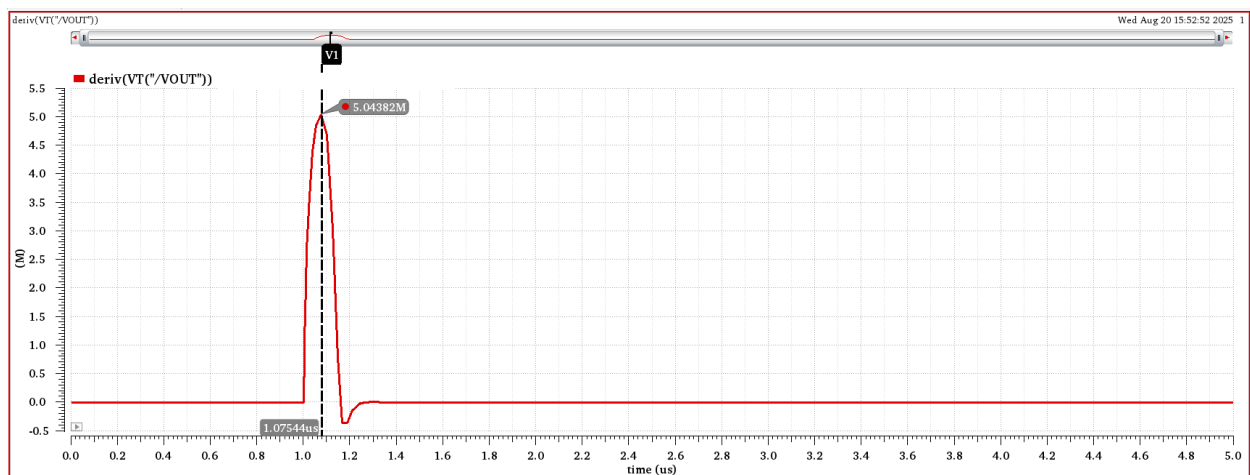
So the Value of the C_c after tuning is 2.2pF

Recalculating the above graphs after tuning

VOUT and VIN overlaid (after tuning)

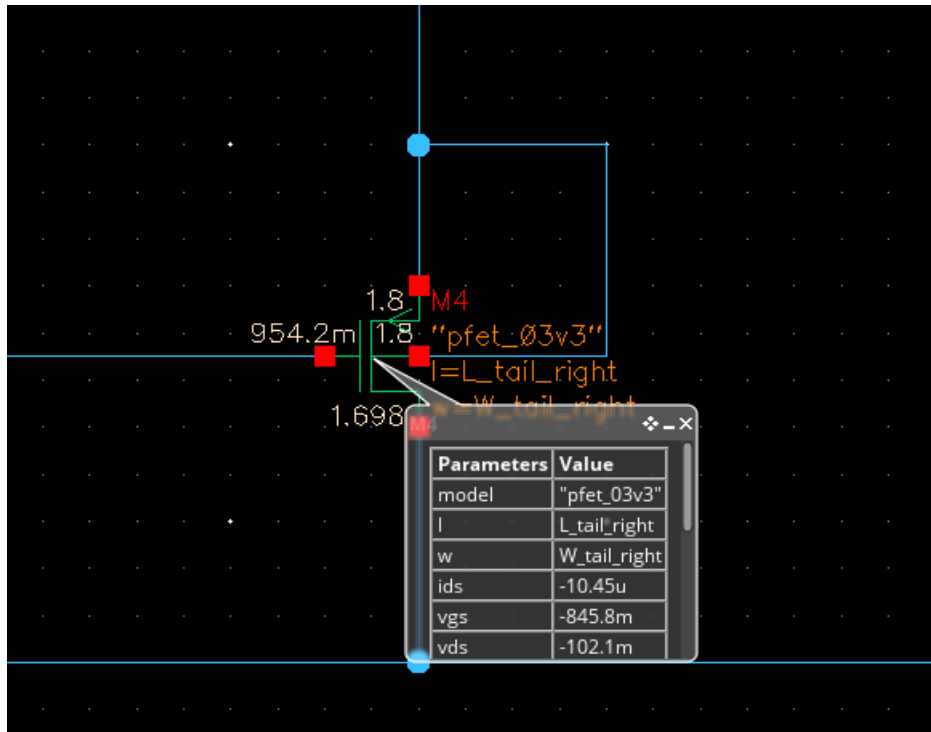


Slew rate (after tuning)



Hand analysis

$$\text{Slew rate} = \frac{I_B}{C_c}, C_c = 2.2\text{pF}$$



$$I_B = 10.45\mu A$$

$$\text{Slew rate} = 4.78 \text{ V}/\mu s$$

Double checking on the gain, fu, and GBW in addition to PM

Now I will double check on the gain, fu, and GBW in addition to PM to make sure that tuning the C_c doesn't make any of the requirements violated

Open-Loop OTA Simulation

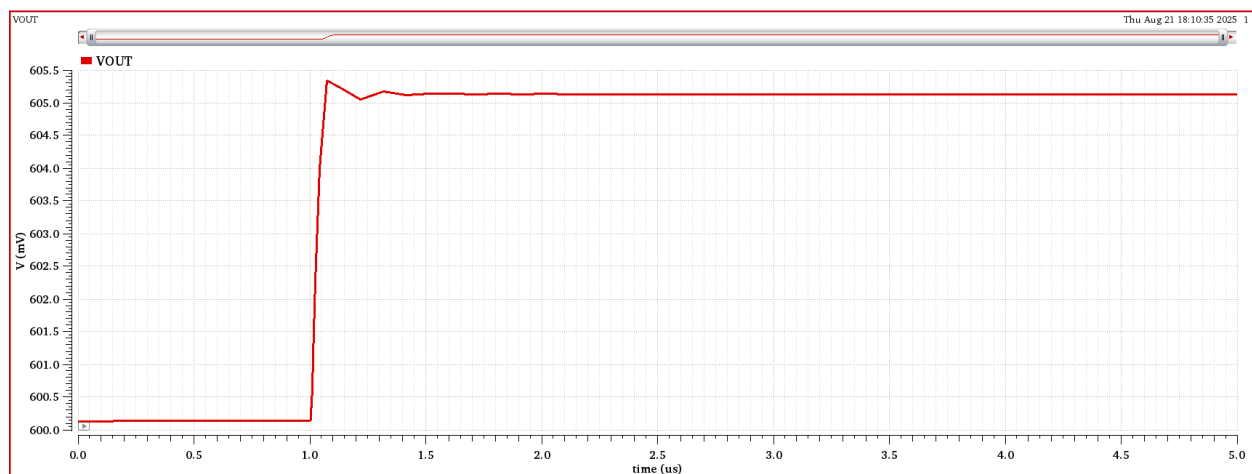
Test	Output	Nominal	Spec	Weight	Pass/Fail
ITi:LAB9:1	DC_gain_linear	2.125k			
ITi:LAB9:1	DC_gain_dB	66.55			
ITi:LAB9:1	Bandwidth	2.834k			
ITi:LAB9:1	Unity_gain_frequency	5.596M			
ITi:LAB9:1	GBW	6.024M			

Closed-Loop OTA Simulation

Test	Output	Nominal	Spec	Weight	Pass/Fail
IT1:Closed_Loop_OTAsimulation:1	DC_gain_dB	67.43			
IT1:Closed_Loop_OTAsimulation:1	DC_gain_linear	2.352k			
IT1:Closed_Loop_OTAsimulation:1	Unity gain	5.225M			
IT1:Closed_Loop_OTAsimulation:1	Phase margin	71.14			
IT1:Closed_Loop_OTAsimulation:1	Bandwidth	2.266k			
IT1:Closed_Loop_OTAsimulation:1	GBW	5.33M			

Settling time

VOUT



Rise time

Test	Output	Nominal	Spec	Weight	Pass/Fail
IT1:Closed_Loop_OTAsimulation:1	VOUT				
IT1:Closed_Loop_OTAsimulation:1	Rise time	44.64n			

Comment:

From the graph it is noticed that there is a slight overshoot and damped oscillation, which indicates the presence of ringing. This occurs because the closed-loop system has a finite phase margin. The feedback loop does not completely suppress the second pole's effect, leading to ringing.

Comment:

The used rise-time is $t_{rise} = 2.2 \tau$ derived under the assumption of a first-order system, where the output response follows a single dominant pole. However, the two-stage Miller OTA is a second-order system. Due to the presence of the additional pole introduced by the Miller compensation, which means that the hand calculated rise time using the first order approximation tends to be slower than the simulated rise time.