CPCS-211 Syllabus

Catalog Description

CPCS-211 Digital Logic Design
Credit: 3 (Theory: 3, Lab: 0, Practical: 1)
Prerequisite: CPIT-201
Classification: Department Required

This objective of this course is to provide an introduction to the fundamental concepts of digital logic design. Topics include number systems, binary codes, Boolean algebra, canonical and fundamental forms of Boolean functions, functions applications to digital circuits design, minimization of Boolean functions by Boolean algebra and Karnaugh maps, two -level and multi-level digital circuits, decoders, encoders, multiplexers, demultiplexers, latches, flip-flops, registers, counters, analysis and synthesis of synchronous sequential circuits. Additionally, this course includes a laboratory component in which students apply the design principles learned in lectures to the design of combinational circuits and synchronous sequential circuits.

Class Schedule

Meet 50 minutes 3 times/week or 80 minutes 2 times/week

Lab/Tutorial 90 minutes 1 times/week

Textbook

Marcovitz, Alan B., , "Introduction to logic design", McGraw-Hill; 3 edition (2009-01-09)

ISBN-13 9780073191645 **ISBN-10** 0073191647

Grade Distribution

Week	Assessment	Grade %
3	Quiz 1	1
4	Exam 1	15
5	Quiz 2	1
6	Homework Assignments	5
8	Quiz 3	1
12	Exam 2	15
13	Quiz 4	1
14	Project (Individual)	20
14	Quiz 5	1
16	Comprehensive Final Exam	40

Last Articulated

December 10, 2017

Relationship to Student Outcomes

a	b	c	d	e	f	g	h	i	j	k
x		x						x	x	

Course Learning Outcomes (CLO)

By completion of the course the students should be able to

1. Represent numeric data in various number systems and add/subtract numbers using signed magnitude 1's complement and 2's complement. (a)
2. Construct circuits for Boolean functions using various logic gates. (c)
3. Simplify Boolean functions using various Boolean Algebra rules. (a)
4. **Simplify Boolean functions of 2, 3, 4 and 5 variables using Karnaugh maps in Sum of Product and Product of Sum forms. (a)**
5. Design Iterative Combinational systems for adders and construct adder/substrator and comparator circuits using logic gates. (c)
6. **Construct various types of decoders, encoders, priority encoder, multiplexer and de-multiplexer using logic gates. (a)**
7. **Describe gate arrays like ROM, PLA, PAL, as well as design larger circuits using these gate arrays. (a)**
8. Design sequential systems, state tables, state diagrams, latches and various flip flop circuits and will learn leading edge triggered and trailing edge triggered flip flops. (a)
9. Derive characteristic tables, characteristic equations, state diagrams and timing diagrams for these flip flops. (c)
10. Analyze Moore model and Mealy model sequential circuits by constructing state tables and state diagrams. (j)
11. **Design sequential circuits using RS, D, T and JK- flip flops (c)**
12. Design Moore and Mealy model sequential circuits from state diagrams and state tables. (c)
13. **Design synchronous counters, 4-bit counters and up/down counters from state diagrams and truth tables, using various gates. (i)**
14. Design Asynchronous counters using various types of flip-flops. (i)
15. Derive state tables and state diagrams for various complex problems using Moore and Mealy models. (a)

Coordinator(s)

Dr. Mohamed Dahab, Associate Professor

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Topics Coverage Durations

Topics	Weeks
Introduction to Number Systems and Binary Codes	2
Introduction to Combinational Systems	2
The Karnaugh Maps	2
Designing Combinational Systems	1
Decoders and Encoders	2
Multiplexers, De-Multiplexers and Gate arrays	2
Analysis of Sequential Systems	2
Design of Sequential Systems	2