CPCS-214 Syllabus

Catalog Description

CPCS-214 Computer Organization and Architecture (I)
Credit: 3 (Theory: 3, Lab: 0, Practical: 1)
Prerequisite: CPCS-211
Classification: Department Required

The objective of this course is to explain how computers are designed and how they work. Students are introduced to modern computer principles using a typical processor. They learn how efficient memory systems are designed to work closely with the processor, and how input/output (I/O) systems bring the processor and memory together with a wide range of devices. The course emphasizes system-level issues and understanding program performance. Topics include instructions sets, assembly language, internal data representation, computer arithmetic, processor data path and control, memory hierarchy, I/O devices and interconnects, and an introduction to parallel processing.

Class Schedule

Lab/Tutorial 90 minutes 1 times/week

Meet 50 minutes 3 times/week or 80 minutes 2 times/week

Textbook

David A. Patterson, John L. Hennessy, , "Computer Organization and Design", Morgan Kaufmann;(2008-11-17)

ISBN-13 9780080922812 **ISBN-10** 0080922813

Grade Distribution

Week	Assessment	Grade %
3	Quiz 1	2.5
3	Graded Lab Work 1	2
4	Graded Lab Work 2	2
5	Graded Lab Work 3	2
5	Quiz 2	2.5
6	Graded Lab Work 4	2
7	Exam 1	15
8	Graded Lab Work 5	2
9	Quiz 3	2.5
11	Quiz 4	2.5
12	Exam 2	15
14	Lab Exam	15
16	Comprehensive Final Exam	35

Last Articulated

October 4, 2017

Relationship to Student Outcomes

a	b	c	d	e	f	g	h	i	j	k
x	x	x								

Course Learning Outcomes (CLO)

By completion of the course the students should be able to

1. Identify concpets related to computer technology and processors. (a)
2. **Compile C/Java programs into MIPS assembly language. (c)**
3. Trace the execution of a MIPS program and its data structures. (b)
4. Write assembly language program for certain programming oriented problem. (c)
5. **Represent integer and floating-point numbers into IEEE single and double precision formats. (a)**
6. Write MIPS codes for floating point operations. (b)
7. Identify the components and assess the CPU performance. (a)
8. **Trace the execution of instructions on a single cycle datapath design supported with control signals. (b)**
9. Explain performance issues of the single cycle datapath design and its trade-offs. (b)
10. **Explain the principles of pipelined execution. (a)**
11. Determine structural, data and control hazards in a MIPS codes. (b)
12. Compare memory technologies available for computing systems, and the basic principle behind a memory hierarchy. (a)
13. Explain the and issues involved with cache memory. (b)
14. **Explain the steps and issues involved with virtual memory. (b)**
15. Explain the different multiprocessors and parallel processing architecutures, and parallel decomposition (b)

Coordinator(s)

Dr. Abdullah Almenbri, Associate Professor

CPCS-214 Syllabus

Topics Coverage Durations

Topics	Weeks
Computer abstaction and technology	2
Performance	1
Instructions sets and assembly language	4
Arithmetic for computers	1
Basics of logic design	1
Processor	2
Pipelining	2
Memory hierarchy	1
Parallel processors	1