

Truth table :

x4	x3	x2	x1	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Code :

```
module    Lab1_assesment1  (x1,x2,x3,x4,f);

input x1,x2,x3,x4;
output    f;

assign  f= ( ( ~(x1 & x2) ^ ( ~x2 & x3)) & ( ~x3 & x4));

endmodule
```

Quartus II - C:/Users/Dell/Desktop/Spring_2022/CSE460/Lab/Lab 1/Lab1_assessment1/Lab1_assessment1 - [RTL Viewer]

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Lab1_assessment1.v

Page Title: Lab1_assessment1

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Project Navigator

Entity	Combinational ALUTs	ALMs
Stratix II: AUTO	1 (1)	1 (1)

Tasks

Flow: Compilation

Task

- Complete Design
- Analysis & Synthesis
 - Edit Settings
 - View Report
- Analysis & Elaboration
- Partition Merge
- Netlist Viewers
 - RTL Viewer
 - State Machine Viewer
 - Technology Map Viewer
- Design Assistant (Post-Mapping)

Message

Type: Processing (13)

System (11) Extra Info Info (13) Warning Critical Warning Error Suppressed Flag

Message: 0 of 26

Location:

For Help, press F1

RTL Viewer

Hierarchy List

- Lab1_assessment1
- Primitives
- Pins
- Nets

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Lab1_assessment1.v

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 14.8 ns

Pointer: 2.47 ns Interval: -12.33 ns Start: End:

Table:

Name	Value at 14.8 ns
f	A 0
x1	A 1
x2	A 0
x3	A 1
x4	A 0

Message

Type: Processing (9)

System (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16

Location:

For Help, press F1