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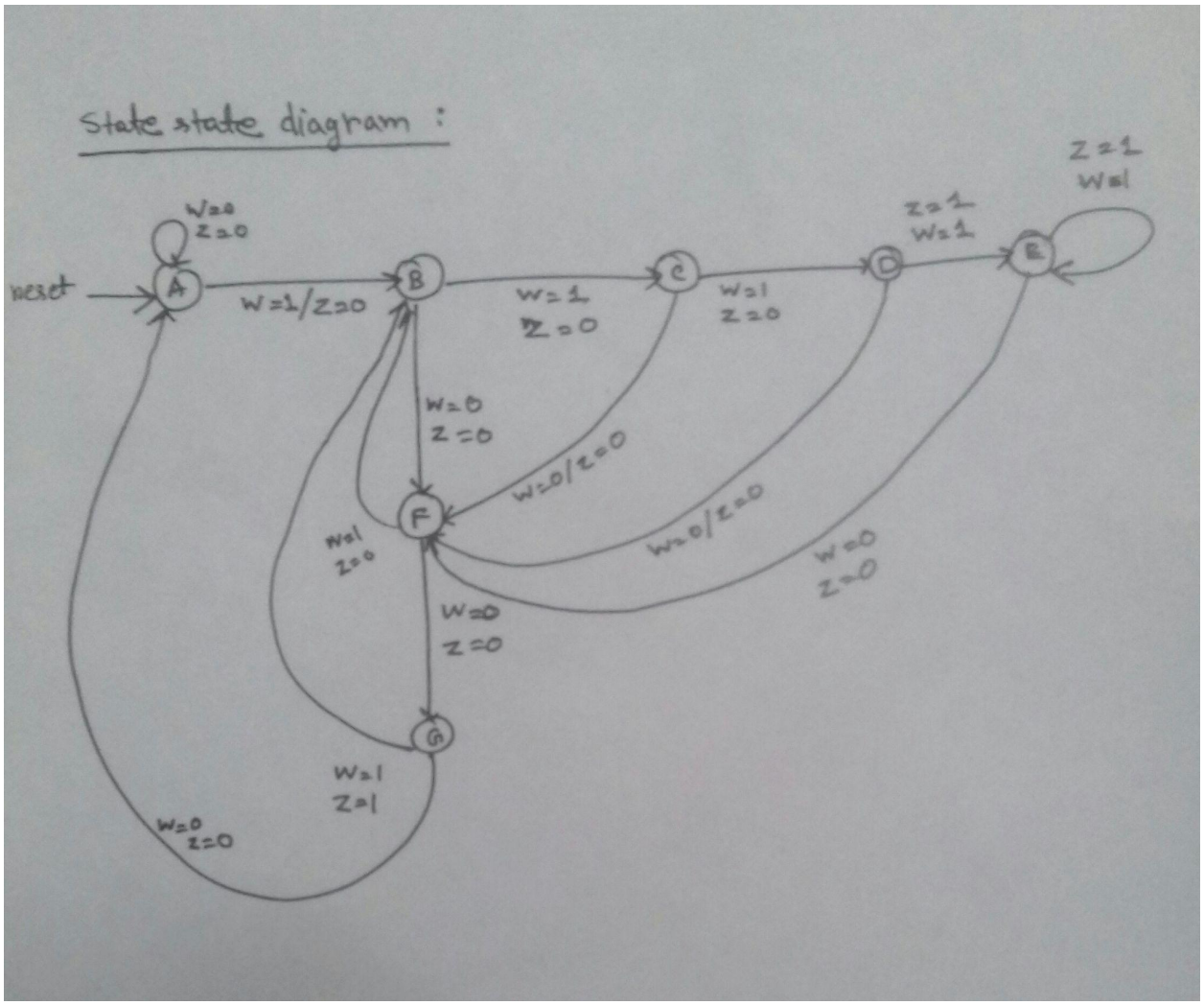
Section : 5
CSE460 Lab 3

Problem: Derive the state diagram of the Mealy version for the example FSM that is, the FSM will generate $z = 1$ at the instant the input values of w have the pattern 1111 or 1001. Overlapping of the input patterns are allowed.

Answer:

State diagram :



State table diagram :

Present state (y3 y2 y1)	Next state (Y3Y2Y1)		Output (Z)	
	w=0	w=1	w=0	w=1
A	A	B	0	0
B	F	C	0	0
C	F	D	0	0
D	F	E	0	1
E	F	E	0	1
F	G	B	0	0
G	A	B	0	1

State assignment table :

Present state (y3 y2 y1)	Next state Y3 Y2 Y1		Output (Z)	
	w=0	w=1	w=0	w=1
000	000	001	0	0
001	101	010	0	0
010	102	011	0	0
011	103	100	0	1
100	104	100	0	1
101	110	001	0	0
110	000	001	0	1

Verilog code :

```
module  exp3(z,w,clock,reset);

input clock, reset, w;
output reg z;
reg [2:0] y;
parameter [2:0] A = 0, B = 1, C = 2, D=3, E=4, F=5, G=6, S7=7;

always @(posedge clock, posedge reset)
      if (reset) y<=A;

      else

            case(y)
            A: if (w)
            begin
            z<=0;
            y<=B;
            end

            else
            begin
            z<=0;
            y<=A;
            end


            B: if (w)
            begin
            z<=0;
            y<=C;
            end

            else
            begin
            z<=0;
            y<=F;
            end


            C: if (w)
            begin
            z<=0;
            y<=D;
            end

            else
            begin
            z<=0;
            y<=F;
            end


            D: if (w)
            begin
```

```
            z<=1;
            y<=D;
            end

            else
            begin
            z<=0;
            y<=F;
            end


            E: if (w)
            begin
            z<=1;
            y<=E;
            end

            else
            begin
            z<=0;
            y<=F;
            end


            F: if (w)
            begin
            z<=0;
            y<=B;
            end

            else
            begin
            z<=0;
            y<=G;
            end


            G: if (w)
            begin
            z<=1;
            y<=B;
            end

            else
            begin
            z<=0;
            y<=A;
            end
            endcase

endmodule
```

Timing diagram :