

## CSE460 Lab Assignment 2

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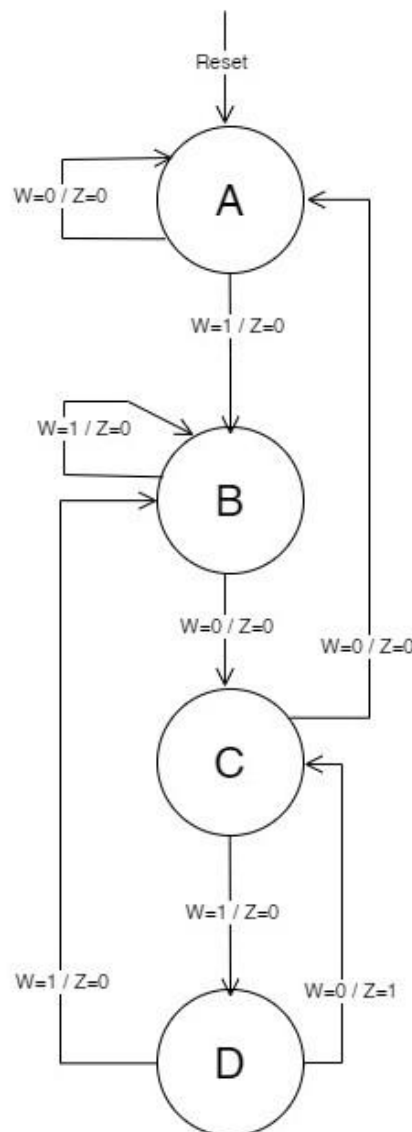
ID : 19301097

Section : 5

**Problem 1 :** An FSM has an input  $w$  and an output  $z$ . The machine has to generate  $z = 1$  when the following patterns in  $w$  are detected: 1010; otherwise,  $z = 0$ . The machine should reset when (Reset = 0).

**Answer :**

- Mealy type FSM will be used
- State diagram :



c. State-assigned table :

Present state (y2 y1)	Next state Y2 Y1		Output ( Z )	
	w=0	w=1	w=0	w=1
A (00)	A (00)	B (01)	0	0
B (01)	C (10)	B (01)	0	0
C (10)	A (00)	D (11)	0	0
D (11)	C (10)	B (01)	1	0

**Code :**

```

module probl_1(clock, reset, w, z, present_state,
next_state);

input clock, reset,w;

output reg z;
output reg [1:0] present_state, next_state;

parameter stateA= 2'b00,
stateB= 2'b01,
stateC= 2'b10,
stateD= 2'b11;

always@(posedge clock)
begin
    if(reset==1)
        begin
            present_state = stateA;
            next_state = stateA;
        end
    else
        begin
            present_state = next_state;
            case(present_state)

                // stateA
                stateA: if(w == 0)

                    begin
                        next_state = stateA;
                        z = 0;
                    end
            end
        end
    end
end

```

```

else if(w == 1)
begin
next_state = stateB;
z = 0;
end

// stateB
stateB: if(w == 0)

begin
next_state = stateC;
z = 0;
end

else if(w == 1)

begin
next_state = stateB;
z = 0;
end

// stateC
stateC: if(w == 0)

begin
next_state = stateA;
z = 0;
end

else if(w == 1)

begin
next_state = stateD;
z = 0;
end

// stateD
stateD: if(w == 0)

begin
next_state = stateC;
z = 1;
end

```

```

        else if(w == 1)

            begin
                next_state = stateB;
                z = 0;
            end

        endcase
    end
end
endmodule

```

### E.

as we are using mealy type FSM so, when we will get 1010 sequence then on that same clock cycle we will get  $z=1$  as output.

now, in the timing diagram from 0ns — 50ns the input was 0 so, we stay at state A(00). Then from 50ns — 100ns input was 1 and present state was B.

Next <sup>three</sup> clock cycle's positive edge ~~the~~ input was 0 1 0 sequentially. Which means we should get a high output for  $z$  in time frame 200ns — 250ns and the output  $z=1$  then.

From 250ns — 300ns  $z=0$  cause the input was 1 but from 300ns to 350ns the input was 0 so, the output  $z=1$  because of the overlapping sequence we get 1010 from 150ns — 350ns.

From the simulation I get,

clock	(0-50)ns $t_1$	(50-100)ns $t_2$	(100-150)ns $t_3$	(150-200)ns $t_4$	(200-250)ns $t_5$	(250-300)ns $t_6$	(300-350)ns $t_7$	(350-400)ns $t_8$	(400-450)ns $t_9$
w	0	1	0	1	0	1	0	0	0
z	0	0	0	0	1	0	1	0	0

In the simulation at (200-250)ns and at (300-350)ns the output is high

## Compilation report:

Quartus II - D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 2/prob1\_1/prob1\_1 - prob1\_1.v

File Edit View Project Assignments Processing Tools Window Help

Project Navigator: prob1\_1.v

Entity: Stratix II: AUTO

Tasks: Flow: Compilation

Task: Compile

Messages:

```

1 module prob1_1(clock, reset, w, z, present_state,
2 next_state);
3
4 input clock, reset,w;
5
6 output reg z;
7 output reg [1:0] present_state, next_state;
8
9 parameter stateA= 2'b00,
10 stateB= 2'b01,
11 stateC= 2'b10,
12 stateD= 2'b11;
13
14 always@(posedge clock)
15 begin
16 if(reset==1)
17 begin
18 present_state = stateA;
19 next_state = stateA;
20 end
21 else
22

```

Quartus II

Full Compilation was successful (6 warnings)

OK

Messages:

Type	Message
Info	Quartus II Assembler was successful. 0 errors, 0 warnings
Info	*****
Info	Running Quartus II Classic Timing Analyzer
Info	Command: quartus_tan --read_settings_files=off --write_settings_files=off prob1_1 -c prob1_1 --timing_analysis_only
Warning	Found pins functioning as undefined clocks and/or memory enables
Info	Clock "clock" Internal fmax is restricted to 500.0 MHz between source register "next_state[1]-reg0" and destination register "z-reg0"
Info	Info: tsu for register "z-reg0" (data pin = "w", clock pin = "clock") is 3.821 ns
Info	Info: too from clock "clock" to destination pin "present_state[1]" through register "present_state[1]-reg0" is 6.945 ns
Info	Info: th for register "z-reg0" (data pin = "reset", clock pin = "clock") is 0.306 ns
Info	Quartus II Classic Timing Analyzer was successful. 0 errors, 1 warning
Info	Quartus II Full Compilation was successful. 0 errors, 6 warnings

System (11) Processing (56) Extra Info Info (50) Warning (6) Critical Warning Error Suppressed (6) Flag

Message: 0 of 182

For Help, press F1

## Simulation report:

Quartus II - D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 2/prob1\_1/prob1\_1 - [Simulation Report - Simulation]

File Edit View Project Assignments Processing Tools Window Help

Project Navigator: prob1\_1.v

Entity: Stratix II: AUTO

Tasks: Flow: Compilation

Task: Compile

Messages:

```

1 module prob1_1(clock, reset, w, z, present_state,
2 next_state);
3
4 input clock, reset,w;
5
6 output reg z;
7 output reg [1:0] present_state, next_state;
8
9 parameter stateA= 2'b00,
10 stateB= 2'b01,
11 stateC= 2'b10,
12 stateD= 2'b11;
13
14 always@(posedge clock)
15 begin
16 if(reset==1)
17 begin
18 present_state = stateA;
19 next_state = stateA;
20 end
21 else
22

```

Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 20.65 ns

Pointer: 20.65 ns

Interval: 80.0 ns

Start: 0 ns

End: 960.0 ns

Waveform signals:

Name	Value at 20.65 ns
reset	A 0
clock	A 1
w	A 0
z	A 0
.te[0]	B 0
.te[1]	B 0
.te[0]	B 0
.te[1]	B 0

Quartus II

Simulator was successful (3 warnings)

OK

Messages:

Type	Message
Info	Running Quartus II Simulator
Info	Command: quartus_sim --read_settings_files=on --write_settings_files=off prob1_1 -c prob1_1
Info	Using vector source file "D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 2/prob1_1/prob1_1.v"
Info	Option to preserve fewer signal transitions to reduce memory requirements is enabled
Warning	Found clock-sensitive change during active clock edge at time 50.0 ns on register "[prob1_1]next_state[0]-reg0"
Warning	Found clock-sensitive change during active clock edge at time 100.0 ns on register "[prob1_1]next_state[1]-reg0"
Warning	Found clock-sensitive change during active clock edge at time 200.0 ns on register "[prob1_1]z-reg0"
Info	Simulation partitioned into 1 sub-simulations
Info	Simulation coverage is 94.12 %
Info	Number of transitions in simulation is 289
Info	Quartus II Simulator was successful. 0 errors, 3 warnings

System (9) Processing (12) Extra Info Info (9) Warning (3) Critical Warning Error Suppressed Flag

Message: 0 of 19

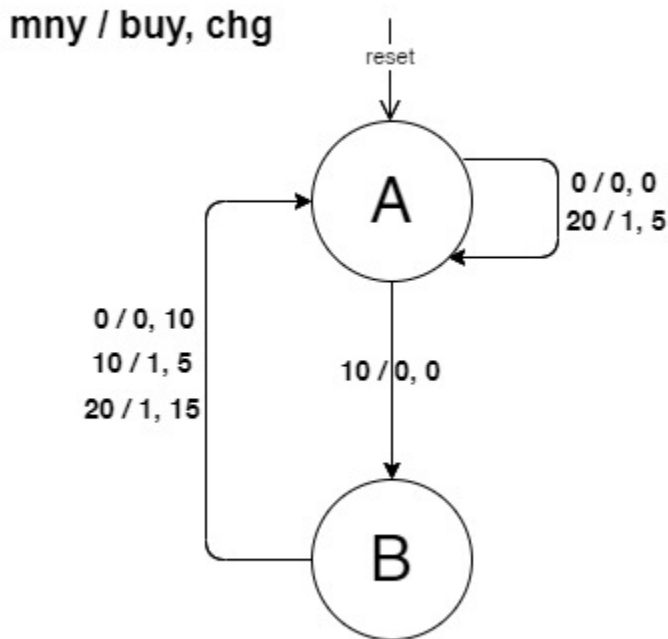
For Help, press F1

**Problem 2 :** You have to design a vending machine for a 15 Tk product. User's money, returned money by the machine, and product bought condition is represented as mny (2-bit input), chg (output), and buy (1-bit output).

The vending machine can only accept inputs: no money (mny = 00), Tk 10 (mny = 01), and Tk 20 (mny = 10). If no money is inserted into the machine, it will immediately return the user's money back. Once an acceptable input is more than or equal to 20 Tk, the machine immediately generates an output (buy=1), goes back to the initial state, and gives back the change (if required).

**Answer :**

**State diagram :**



The machine will produce 4 types of changes.

0tk, 5tk, 10tk, 15tk

As we have 4 changes so we need 2bit for chg output to represent all 4 changes.

0tk  $\rightarrow$  00

5tk  $\rightarrow$  01

10tk  $\rightarrow$  10

15tk  $\rightarrow$  11

clk	t <sub>1</sub>	t <sub>2</sub>	t <sub>3</sub>	t <sub>4</sub>	t <sub>5</sub>	t <sub>6</sub>	t <sub>7</sub>	t <sub>8</sub>	t <sub>9</sub>	t <sub>10</sub>
any	0	10	0	0	10	10	0	0	20	0
buy	0	0	0	0	0	1	0	0	1	0
chg	0	0	10	0	0	5	0	0	5	0

chg 0tk: at t<sub>3</sub> user didn't give any money so the change is 0tk

chg 5tk: at t<sub>9</sub> user gives 20tk so the buy=1 and change 5tk

chg 10tk: at t<sub>2</sub> user gives 10tk and t<sub>3</sub> <sup>user</sup> gave nothing so machine will return to state A and return is 10tk at t<sub>3</sub>

chg 15tk: this scenario isn't present in table but if user gives 10tk and then 20tk consecutively then user will get 15tk change



**A. State-assigned table :**

Present state (y)	Next state Y			Output					
				buy			chg		
	( mny2 mny1 )			( mny2 mny1 )			( mny2 mny1 )		
	<b>00</b> (0tk)	<b>01</b> (10tk)	<b>10</b> (20tk)	<b>00</b> (0tk)	<b>01</b> (10tk)	<b>10</b> (20tk)	<b>00</b> (0tk)	<b>01</b> (10tk)	<b>10</b> (20tk)
A (0)	A (0)	B (1)	A (0)	0	0	1	00 (0tk)	00 (0tk)	01 (5tk)
B (1)	A (0)	A (0)	A (0)	0	1	1	10 (10tk)	01 (5tk)	11 (15tk)

**Code :**

```
module exp2_2(clock, reset, mny, buy, present_state, next_state,
chg);
```

```
    input clock, reset;
    input [1:0] mny;
```

```
    output reg buy, present_state, next_state;
    output reg [1:0] chg;
```

```
    parameter      stateA= 0, //0tk/final state
                   stateB= 1, //10tk state
```

```
    n = 15, //price of my product
```

```
    R0= 2'b00, //0tk return
    R5= 2'b01, //5tk return
    R10= 2'b10, //10tk return
    R15= 2'b11; //15tk return
```

```
    always@(posedge clock)
    begin
```

```
        if(reset==1)
        begin
            present_state = stateA;
            next_state = stateA;
```

```
        end
```

```
        else
```

```
        begin
            present_state = next_state;
```

```
        case(present_state)
```

```
        stateA: if(mny == 2'b00) // 0 tk
            begin
```

```
                next_state = stateA;
                buy =0;
                chg = R0;
```

```
            end
```

```

else if(mny == 2'b01) // 10 tk
begin
    next_state = stateB;
    buy =0;
    chg = R0;
end
else if(mny == 2'b10) // 20 tk
begin
    next_state = stateA;
    buy =1;
    chg = R5;
end

stateB: if(mny == 2'b00) // 0 tk
begin
    next_state = stateA;
    buy =0;
    chg = R10;
end
else if(mny == 2'b01) // 10 tk
begin
    next_state = stateA;
    buy =1;
    chg = R5;
end
else if(mny == 2'b10) // 20 tk
begin
    next_state = stateA;
    buy =1;
    chg = R15;
end

endcase

end

endmodule

```

E.

In the simulation at time (300-350)ns the buy = 1 cause in the past two clock cycle the input was 10 + 10 = 20tk. The reason why in this time frame the change is 5tk.

Also in the (450-500)ns the output is buy = 1 cause the past clock cycles input is 20tk. The change is 5tk.

At (150-200)ns the buy = 0 and change is 10tk cause the past two clock cycle's input was 10tk.

### Compilation report:

Quartus II - D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 2/exp2\_2/exp2\_2 - exp2\_2.v

File Edit View Project Assignments Processing Tools Window Help

exp2\_2

Project Navigator

Entity

Stratix II: AUTO

exp2\_2

Tasks

Flow: Compilation

Task

Compile

Ana

Fite

Ass

Clas

exp2\_2

exp2\_2.v

```

1 module exp2_2(clock, reset, mny, buy, present_state, next_state, chg);
2
3   input clock, reset;
4   input [1:0] mny;
5
6   output reg buy, present_state, next_state;
7   output reg [1:0] chg;
8
9   parameter stateA= 0, //0tk/final state
10             stateB= 1, //10tk state
11
12             n = 15, //price of my product
13
14             R0= 2'b00, //0tk return
15             R5= 2'b01, //5tk return
16             R10= 2'b10, //10tk return
17             R15= 2'b11; //15tk return
18
19   always@(posedge clock)
20   begin
21     if(reset==1)

```

Quartus II

Full Compilation was successful (14 warnings)

OK

Message

Info: Quartus II Assembler was successful. 0 errors, 0 warnings

Info: Running Quartus II Classic Timing Analyzer

Info: Command: quartus\_ran --read\_settings\_files=off --write\_settings\_files=off exp2\_2 -c exp2\_2 --timing\_analysis\_only

Warning: Found pins functioning as undefined clocks and/or memory enables

Info: Clock "clock" Internal fmax is restricted to 500.0 MHz between source register "next\_state-reg0" and destination register "next\_state-reg0"

Info: tau for register "chg[0]-reg0" (data pin = "mny[0]", clock pin = "clock") is 3.529 ns

Info: tau from clock "clock" to destination pin "buy" through register "chg[0]-reg0" is 6.465 ns

Info: th for register "next\_state-reg0" (data pin = "mny[1]", clock pin = "clock") is -2.650 ns

Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 1 warning

Info: Quartus II Full Compilation was successful. 0 errors, 14 warnings

System (4) Processing (64) Extra Info Info (50) Warning (14) Critical Warning Error Suppressed (6) Flag

Message: 0 of 190

Location:

Ln 1, Col 13

Idle

For Help, press F1

## Simulation report:

