

CSE460 Lab Assignment 1

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Section : 5

Problem 1 : Design an 8 bit full adder using 1 bit full adder modules and add these two binary numbers: 8'b10110101 and 8'b10100111

Answer :

Code :

```
module problem1(S,Cout, A, B, Cin);

    input Cin;
    input [7:0]A,B;

    output [7:0]S;
    output Cout;
    wire Cout0, Cout1, Cout2, Cout3, Cout4, Cout5, Cout6;

    // A = 8'b10110101
    // B = 8'b10100111

    fulladd stage0 (S[0], Cout0, A[0], B[0], Cin);
    fulladd stage1 (S[1], Cout1, A[1], B[1], Cout0);
    fulladd stage2 (S[2], Cout2, A[2], B[2], Cout1);
    fulladd stage3 (S[3], Cout3, A[3], B[3], Cout2);
    fulladd stage4 (S[4], Cout4, A[4], B[4], Cout3);
    fulladd stage5 (S[5], Cout5, A[5], B[5], Cout4);
    fulladd stage6 (S[6], Cout6, A[6], B[6], Cout5);
    fulladd stage7 (S[7], Cout, A[7], B[7], Cout6);

endmodule

// This module implements a 1-bit full adder

module fulladd(sum, carryout, x, y, carryin);

    input x, y, carryin;
    output sum, carryout;

    assign sum = x ^ y ^ carryin;
    assign carryout = (x & y) | (carryin & (x ^ y));

endmodule
```

Compilation report :

Quartus II - D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 1/problem1/problem1 - problem1 - [Compilation Report - Flow Su]

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problem1

Project Navigator

Entity: Stratix II: AUTO

Combinational ALUTs: 12 (0)

ALMs: 6 (0)

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming file)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

Compilation Report - Flow Summary

Flow Summary

Flow Status: Successful - Sat Mar 05 19:44:47 2022

Quartus II Version: 8.1 Build 163 10/28/2008 SJ Web Edition

Revision Name: problem1

Top-level Entity Name: problem1

Family: Stratix II

Met timing requirements: Yes

Logic utilization: < 1 %

Combinational ALUTs: 12 / 12,480 (< 1 %)

Registered logic registers: 0 / 12,480 (0 %)

Registers: 0

Pins: 26 / 343 (8 %)

Pins: 0

Lock memory bits: 0 / 419,328 (0 %)

Lock 5-bit elements: 0 / 96 (0 %)

LUTs: 0 / 6 (0 %)

Total DLLs: 0 / 2 (0 %)

Device: EP2K10K10-3

Timing Models: Final

Quartus II

Full Compilation was successful (5 warnings)

OK

Messages

Type: Message

Info: Assembler is generating device programming files

Info: Quartus II Assembler was successful. 0 errors, 0 warnings

Info: Running Quartus II Classic Timing Analyzer

Info: Command: quartus --read_settings_files=off --write_settings_files=off problem1 -c problem1 --timing_analysis_only

Info: Longest tpd from source pin "A[1]" to destination pin "S[7]" is 12.028 ns

Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings

Info: Quartus II Full Compilation was successful. 0 errors, 5 warnings

System (44) Processing (51) Extra Info Info (46) Warning (5) Critical Warning Error Suppressed (6) Flag /

Message: 0 of 141

Location:

For Help, press F1

Simulation report :

Quartus II - D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 1/problem1/problem1 - problem1 - [Simulation Report - Simulati]

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problem1

Project Navigator

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Tasks

Flow: Compilation

Task

- Compile Design
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Simulation Report - Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 16,274 ns

Pointer: 3.46 ns

Interval: -12.81 ns

Start: 0 ps

End: 0 ps

Value at 16.27 ns

Name: A [181]

Value: 0

Name: B [167]

Value: 0

Name: Cin

Value: 0

Name: Cout

Value: 1

Name: S

Value: 0

Name: S[7]

Value: 1

Name: S[6]

Value: 1

Name: S[5]

Value: 1

Name: S[4]

Value: 1

Name: S[3]

Value: 1

Name: S[2]

Value: 1

Name: S[1]

Value: 0

Name: S[0]

Value: 0

Messages

Type: Message

System (38) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag /

Message: 0 of 16

Location:

For Help, press F1

Brief description :

Problem-01

In the problem 1 we take two 8 bit binary numbers and add these two binary numbers. The full adder circuit is designed using 1 bit full adder modules.

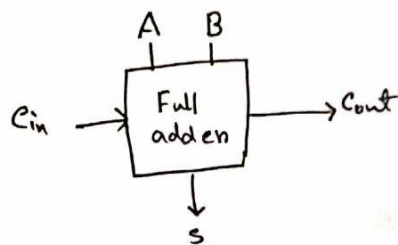


Figure: 1 bit full adder circuit.

A 1 bit full adder circuit takes 2 input each of them are 1 bit and takes another 1 bit binary number called C_{in} (carry in). Then the circuit adds these three binary numbers each of them are 1 bit. The output of these three 1 bit binary numbers is S and another output is the carry out (C_{out}).

The problem requires ^{two} 8 bit binary numbers and have to use 1 bit full adder module. So, we need 8 total 8 piece of 1 bit full adder circuit.

In the time diagram we see the addition result

$$\text{of } A = 10110101_{(2)} = 187_{(10)}$$

$$B = 10100111_{(2)} = 167_{(10)}$$

the circuit provides the output $\text{cout} = 1$

$$S = 01011100$$

So, the answer is 101011100

in the timing diagram: ~~XXXXXX~~

	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]
	1	0	1	1	0	1	0	1
								↓
B[7:0] →	1	0	1	0	0	1	1	1
								↓
2	0	1	0	1	1	1	0	0
↑	S[7]	S[6]	S[5]	S[4]	S[3]	S[2]	S[1]	S[0]
cout								

As the whole circuit performs addition bit by bit that's why
when $A[0] = 1$ and $B[0] = 1$ then $S[0] = 0$ and $\text{cout} = 1$

In time interval 0-80ns

$A[0] = 1$	$B[0] = 1$	$cout0 = 1$	$S[0] = 0$
$A[1] = 0$	$B[1] = 1$	$cout1 = 1$	$S[1] = 0$
$A[2] = 1$	$B[2] = 1$	$cout2 = 0$	$S[2] = 1$
$A[3] = 0$	$B[3] = 0$	$cout3 = 0$	$S[3] = 1$
$A[4] = 1$	$B[4] = 0$	$cout4 = 0$	$S[4] = 1$
$A[5] = 1$	$B[5] = 1$	$cout5 = 1$	$S[5] = 0$
$A[6] = 0$	$B[6] = 0$	$cout6 = 0$	$S[6] = 1$
$A[7] = 1$	$B[7] = 1$	$cout = 1$	$S[7] = 0$

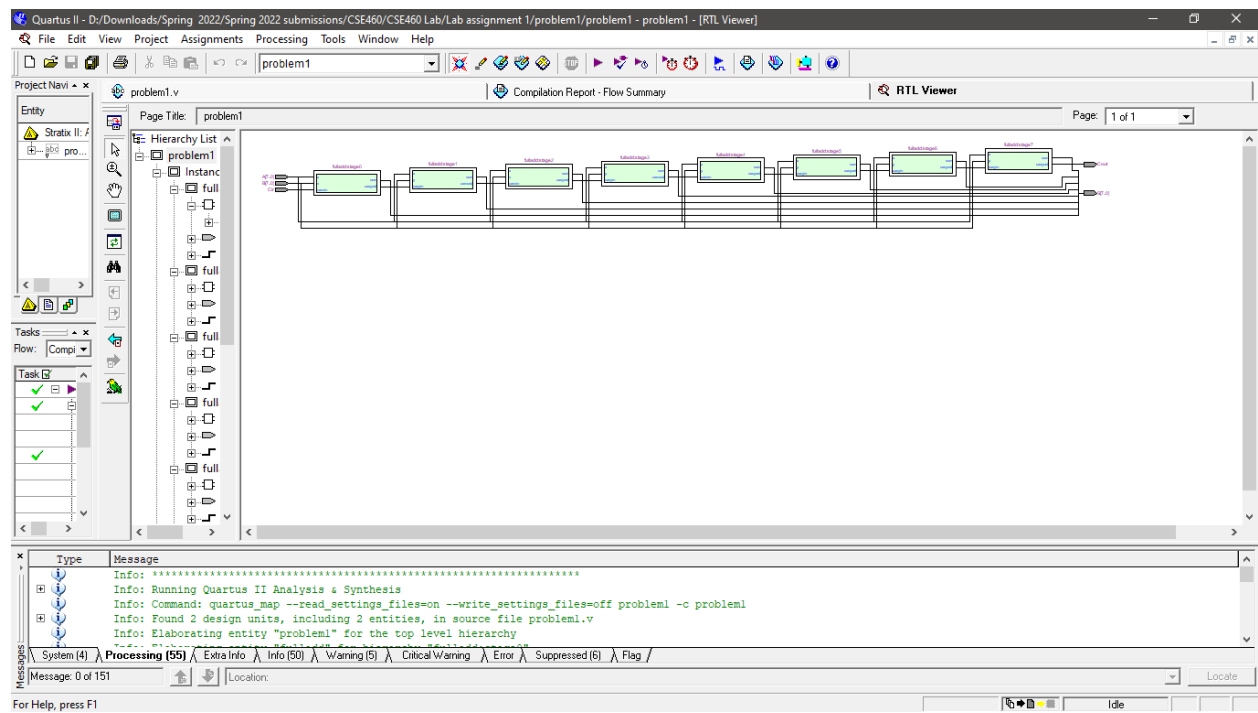
This ~~the~~ is the table representation of the time diagram.

When, $A[0] = 1$ and $B[0] = 1$ then the $S[0] = 0$ and the $cout0 = 1$, this $cout0 = 1$ will be the cin for $A[1]$ and $B[1]$.

So in the timing diagram from 0-80ns the $S[0] = 0$ or $S[0]$ is low. $S[1] = 0$, $S[2] = 1$, $S[3] = 1$, $S[4] = 1$, $S[5] = 0$, $S[6] = 1$, $S[7] = 0$ and $cout = 1$

This represents the binary numbers 101011100 which is the addition of $A = 8'b10110101$ and $B = 8'b10100111$

RTL schematic :



Problem 2: Design a 4 to 2 priority encoder ($0 > 1 > 3 > 2$) using Verilog HDL and verify using timing diagram.

Answer :

Code :

```
module problem2(w,y);

input [3:0]w;
output reg[1:0]y;

always @(w)
    casex (w)

        // priority 0>1>3>2

        4'bxxx1: y=0;
        4'bxx10: y=1;
        4'b1x00: y=3;
        4'b0100: y=2;

    endcase
endmodule
```


Compilation report :

Quartus II - D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 1/problem2/problem2 - problem2 - [Compilation Report - Flow Summary]

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problem2

Project Navigator

Entity	Combinational ALUTs	ALUTs
Stratix II: AUTO	5 (5)	3 (3)

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

Compilation Report - Flow Summary

Flow Status: Successful - Sat Mar 05 19:49:22 2022

Quartus II Version: 8.1 Build 153 10/28/2008 SJ Web Edition

Revision Name: problem2

Top-level Entity Name: problem2

Family: Stratix II

Met timing requirements: Yes

Logic utilization: < 1 %

Combinational ALUTs: 5 / 12,480 (< 1 %)

0 / 12,480 (0 %)

0

6 / 343 (2 %)

0

0 / 419,328 (0 %)

0 / 96 (0 %)

0 / 6 (0 %)

0 / 2 (0 %)

Device: EP2K10K10-3

Timing Models: Final

Quartus II

Full Compilation was successful (16 warnings)

OK

Messages

Type Message

- Warning: Found pins functioning as undefined clocks and/or memory enables
- Warning: Found 1 node(s) in clock paths which may be acting as ripple and/or gated clocks -- node(s) analyzed as buffer(s) resulting in clock skew
- Info: tsu for register "y[0]<clatch" (data pin = "w[3]", clock pin = "w[2]") is 3.196 ns
- Info: too from clock "w[3]" to destination pin "y[0]" through register "y[0]<clatch" is 9.358 ns
- Info: th for register "y[0]<clatch" (data pin = "w[0]", clock pin = "w[3]") is -0.692 ns
- Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 5 warnings
- Info: Quartus II Full Compilation was successful. 0 errors, 16 warnings

System (2) Processing (62) Extra Info Info (50) Warning (12) Critical Warning Error Suppressed (6) Flag

Message: 0 of 167

Location:

For Help, press F1

Simulation report :

Quartus II - D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 1/problem2/problem2 - problem2 - [Simulation Report - Simulation Waveforms]

File Edit View Project Assignments Processing Tools Window Help

problem2

Project Navigator

Entity	Combinational ALUTs	ALUTs
Stratix II: AUTO	5 (5)	3 (3)

Tasks

Flow: Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate programming files)
- Classic Timing Analysis
- EDA Netlist Writer
- Program Device (Open Programmer)

Simulation Report - Simulation Waveforms

Simulation mode: Functional

Master Time Bar: 16.975 ns

Pointer: 31.97 ns

Interval: 15.0 ns

Start: End:

Name Value

0 ps 10.0 ns 20.0 ns 30.0 ns 40.0 ns 50.0 ns 60.0 ns

0 w[3] A[6]

1 w[2] A[1]

2 w[1] A[1]

3 w[0] A[1]

4 y[1] A[0]

5 y[0] A[1]

6 y[1] A[0]

7 y[0] A[1]

Messages

Type Message

- Info: Command: quartus_sim --read_settings_files=on --write_settings_files=off problem2 -c problem2
- Info: Using vector source file "D:/Downloads/Spring 2022/Spring 2022 submissions/CSE460/CSE460 Lab/Lab assignment 1/problem2/problem2.vwf"
- Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
- Info: Simulation partitioned into 1 sub-simulations

System (13) Processing (9) Extra Info Info (9) Warning Critical Warning Error Suppressed Flag

Message: 0 of 16

Location:

For Help, press F1

Brief description :

Problem - 2

In this problem the priority of the encoder is $0 > 1 > 3 > 2$

which means when $w_0 = 1$ then we won't care about other w values. Same goes for when $w_1 = 1$ then w_0 have to be 0 and then we don't care about other w values and output would be 1

As it's a ^{to 2} 4 bit priority encoder so, we will take 4 bit input and will generate 2 bit output.

The priority is $0 > 1 > 3 > 2 \therefore w_0 > w_1 > w_3 > w_2$

which means,

w_3	w_2	w_1	w_0	
x	x	x	1	$\rightarrow y = 00$
x	x	1	0	$\rightarrow y = 01$
1	x	0	0	$\rightarrow y = 11$
0	1	0	0	$\rightarrow y = 10$

Let's
~~now if we~~ observe a scenario when, multiple input bits
are high.

Time range: 30ns to 32.5ns

$$w[3] = 1$$

$$w[2] = 1$$

$$w[1] = 0$$

$$w[0] = 0$$

in this scenario $w[0] = 0$

So, output wouldn't be 0 cause $w[0]$ position is
occupied by 0

Now, we will look for the next priority ~~in the~~ which
is $w[1]$ and here $w[1] = 0$ That's why we
have to look for next priority which is 3.

Now, $w[3] = 1$ so, we will show output = 0 = 11

Because the previous priority positions $w[0]$ and $w[2]$
are 0.

Most important thing is here $w[2] = 1$ but we
didn't care about that position. Because ~~port~~ 2
has the lower priority than 3. That's why we didn't

look at the position $w[2]$ cause we got a 1 in $w[3]$
position which has a higher priority than $w[2]$

So, the input : 1100

output : $y = 11$

This input shows that $w[3]$ has higher priority ^{than $w[2]$} the
reason why ^{though} $w[2] = 1$ but the output came from $w[3]$
which is $y = 3$

RTL schematic :

