COMSATS University Islamabad, Lahore Campus

Assignment 3 – FALL 2024

Course Title:	Computer Organization & Architecture				Course Code:	CPE 343	Credit Hours: 4(3,1)
Course Instructor:	Dr. Muhammad Naeem Awais				Program Name:	BCE	
Semester:	5th	Batch:	FA22	Section: A, B	Date Given:	5th December, 2024	
Submission Date:	**10th December, 2024**				**Maximum Marks:**	**30**	
Name:					**Registration Number:**		

Important Instructions / Guidelines:

- Draw neat schematics wherever needed
- Do your own work, PLAGARISM will be graded as ZERO
- **No late submission**.

Question 1: **[CLO4-PLO3-C3]** **[15 Marks]**

In a 5-stage pipelined MIPS architecture with branch decision in the 4th stage, ***discover*** different hazards found in the given sequence of code and propose solutions to eliminate these hazards:

```
1. LW   $s1, 5($s4)
2. AND  $s3, $s1, $s2
3. SUB  $s3, $s4, $s6
4. ADD  $s4, $s2, $s3
5. BEQ  $s8, $s9, 44
6. SW   $s7, 7($s1)
7. OR   $t7, $t4, $t5
8. AND  $t6, $t3, $t4
```

Fill the table.

Instruction Number	Hazard Type	Resource/Register Name	Hazard Source Instruction	Hazard Affected Instruction	Proposed Solution

Question 2: **[CLO4-PLO3-C3]** **[15 Marks]**

A multicycle floating-point (FP) pipelined MIPS architecture is equipped with the following functional units with the given latencies:

Functional Units	No. of Functional Units	Latency (cycles in EXE stage)
Integer	1	1
FP-Add	1	4
FP-Mul	1	6
FP-Div	1	10

Compute the total number of clock cycles to complete the execution of the following sequence of FP instructions:

```
L.D          F0, 0(R1)
L.D          F2, 0(R2)
ADD.D        F6, F0, F2
MULT.D       F8, F6, F2
DIV.D        F10,F8, F6
S.D          F10, 0(R1)
```

Demonstrate the hazards free execution of these instructions versus clock cycles by introducing the stalls where necessary and show the potential hazards with arrows.