COMSATS University Islamabad, Lahore Campus

Assignment 4 – FALL 2024

Course Title:	Computer Organization & Architecture				Course Code:	CPE 343	Credit Hours: 4(3,1)
Course Instructor:	Dr. Muhammad Naeem Awais				Program Name:	BCE	
Semester:	5th	Batch:	FA22	Section: A, B	Date Given:	20th December, 2024	
Submission Date:	**24th December, 2024**				**Maximum Marks:**	**20**	
Name:					**Registration Number:**		

Important Instructions / Guidelines:

- Draw neat schematics wherever needed
- Do your own work, PLAGARISM will be graded as ZERO
- **No late submission**.

Question 1: **[CLO4-PLO3-C3]** **[20 Marks]**

Set associate caches are implemented for a high-performance in memory hierarchy to processors. Below is a list of 32-bit memory address reference, given as word addresses:

25, 170, 222, 103, 60, 106, 63, 113, 101,123, 150, 11, 56, 70, 88, 90, 43

a) ***Compute*** the final cache contents for an 8-way set associative cache with 4 word blocks and a total size of 128 blocks?
b) Use LRU replacement. For each reference identify the index bits, the tag bits, the block offset bits, and if it is a hit or a miss.
c) Draw a block diagram of the mentioned cache.
d) ***Compute*** the miss penalty and average memory access time of this cache if the above mentioned cache takes 150 ns to return the first word of a block and 10 ns for each subsequent word. Assume this cache has hit rate of 80 % and has hit latency of 5 ns.