Solution

# COMSATS University Islamabad, Lahore Campus

## Assignment 3 – FALL 2024

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|---|---|---|---|---|---|---|---|
| Course Title: | Computer Organization & Architecture | | | | Course Code: | CPE 343 | Credit Hours: 4(3,1) |
| Course Instructor: | Dr. Muhammad Naeem Awais | | | | Program Name: | BCE | |
| Semester: | 5th | Batch: | FA22 | Section: | A, B | Date Given: | 5th December, 2024 |
| **Submission Date:** | **10th December, 2024** | | | | **Maximum Marks:** | | **30** |
| **Name:** | | | | | **Registration Number:** | | |

**Important Instructions / Guidelines:**

- Draw neat schematics wherever needed
- Do your own work. PLAGARISM will be graded as ZERO
- **No late submission.**

**Question 1:** **[CLO4-PLO3-C3]** **[15 Marks]**

In a 5-stage pipelined MIPS architecture with branch decision in the 4th stage, ***discover*** different hazards found in the given sequence of code and propose solutions to eliminate these hazards:

```
1. LW   $s1, 5($s4)
2. AND  $s3, $s1, $s2
3. SUB  $s3, $s4, $s6
4. ADD  $s4, $s2, $s3
5. BEQ  $s8, $s9, 44
6. SW   $s7, 7($s1)
7. OR   $t7, $t4, $t5
8. AND  $t6, $t3, $t4
```

Fill the table.

| Instruction Number | Hazard Type | Resource/Register Name | Hazard Source Instruction | Hazard Affected Instruction | Proposed Solution |
|---|---|---|---|---|---|
| 2 | RAW | S1 | 1 | 2 | Stall & Data Forwarding (DF) |
| 3 | WAW | S3 | 2 | 3 | Register renaming (RR) |
| 4 | WAR | S4 | 3 | 4 | " |
| 4 | RAW | S3 | 2,3 | 4 | Stall & DF |
| 6,7,8 | Control Hazard | | 5 | 6,7,8 | Move conditional decision H/W to 2nd stage |
| 6 | WAW | S1 | 1 | 6 | RR |
| 6 | WAR | S1 | 2 | 6 | RR |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |

**Question 2:** [CLO4-PLO3-C3] [15 Marks]

A multicycle floating-point (FP) pipelined MIPS architecture is equipped with the following functional units with the given latencies:

| Functional Units | No. of Functional Units | Latency (cycles in EXE stage) |
|---|---|---|
| Integer | 1 | 1 |
| FP-Add | 1 | 4 |
| FP-Mul | 1 | 6 |
| FP-Div | 1 | 10 |

```
LD      F0, 0(R1)
LD      F2, 0(R2)
ADD.D   F6, F0, F2
MULT.D  F8, F6, F2
DIV.D   F10, F8, F6
S.D     F10, 0(R1)
```

| CC | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LD F0,0(R1) | IF | ID | Exe | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | MS | | | | | | | | | | | | | | | | | | | |
| LD F2,0(R2) | | IF | ID | Exe | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | MS | | | | | | | | | | | | | | | | | | |
| ADD.D F6,F0,F2 | | | IF | ID | ⬡ | A1 | A2 | A3 | A4 | A5 | M8 | MS | | | | | | | | | | | | | | | | | | | |
| MULT.D F8,F6,F2 | | | | IF | ⬡ | ID | ⬡ | ⬡ | ⬡ | ⬡ | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | MS | | | | | | | | | | | | |
| DIV.D F10,F8,F6 | | | | | IF | ⬡ | ⬡ | ⬡ | ⬡ | ID | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | M8 | MS |
| S.D F10,0(R1) | | | | | | | | | | IF | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ID | Exe | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | ⬡ | M4 | MS |

Required total number of clock cycles = 31 cc