Memory Interfacing with 8088 Microprocessor

Fundamentals

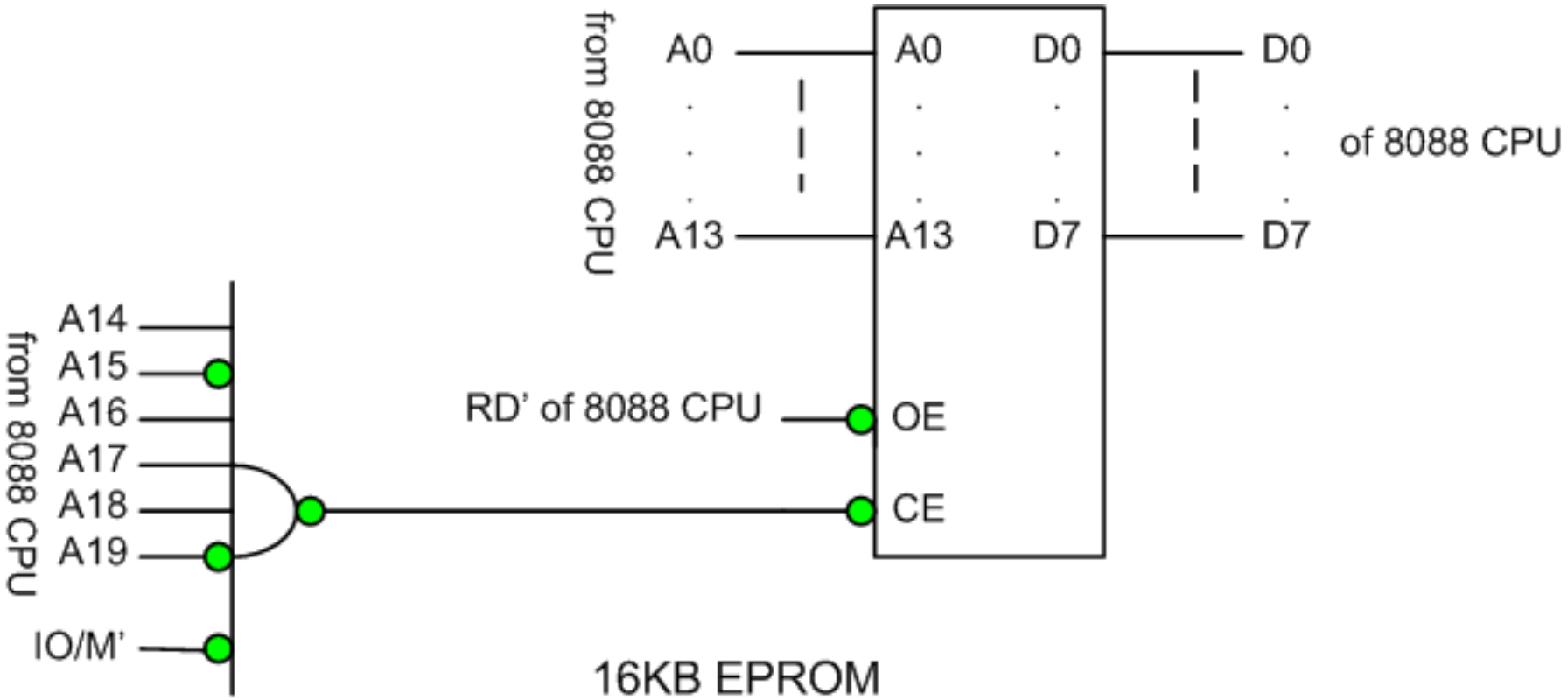
- Address decoding
- Glue logic
- Type of memory (RAM or ROM)
- Memory map
- Labelling the schematic
- Reverse engineering the schematic (determining memory map, memory size and type of memory etc.)

Interfacing Read-Only Memory

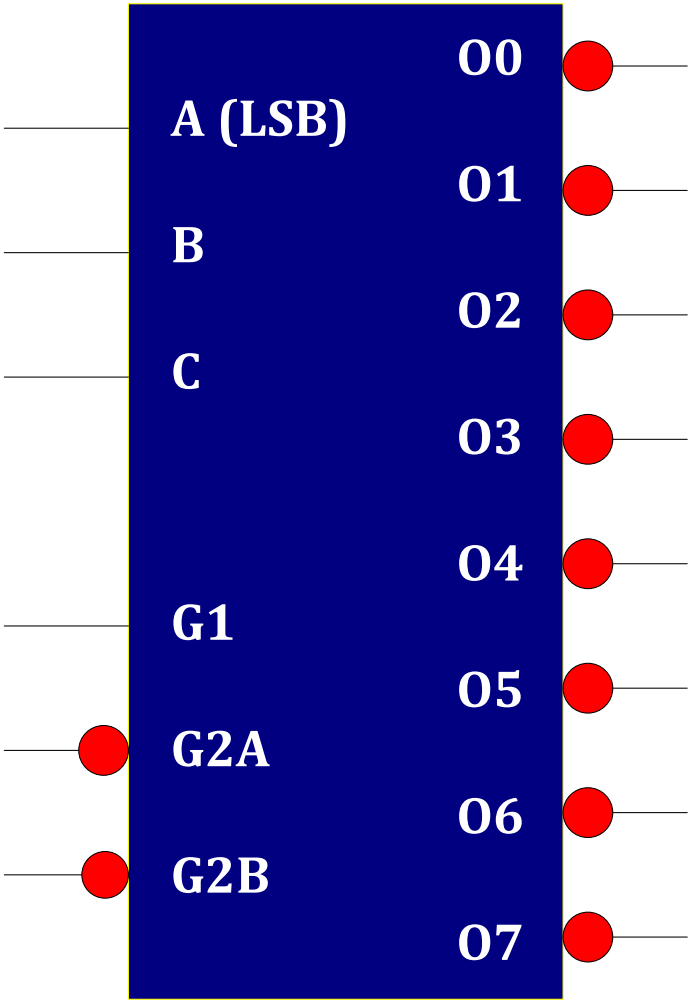
Some facts to know

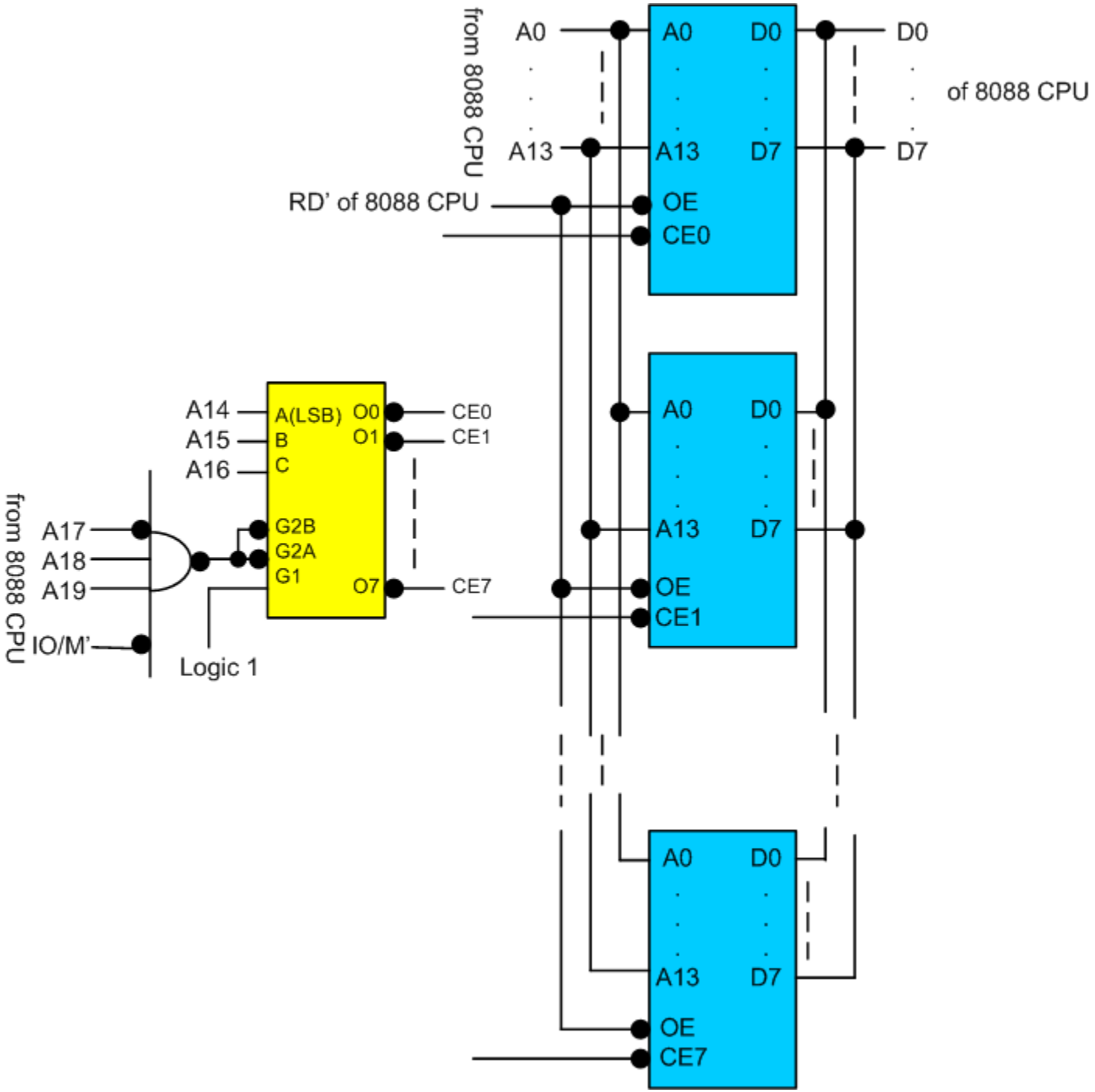
- In 8086 and 8088 CPUs, CS is FFFFH and IP is 0000H upon reset.
- So FFFF0H location must be found in ROM and should contain the first instruction
- As ROM cannot be written to, so WE pin is not available on ROM chips.

Interfacing a single ROM chip



74LS138 3x8 Complementary Decoder




from 8088 CPU
A0
A13
RD' of 8088 CPU
A0
D0
A13
D7
OE
CE0
D0
D7
of 8088 CPU
A14
A15
A16
A(LSB)
B
C
G2B
G2A
G1
O0
O1
O7
CE0
CE1
CE7
from 8088 CPU
A17
A18
A19
IO/M'
Logic 1
A0
D0
A13
D7
OE
CE1
A0
D0
A13
D7
OE
CE7

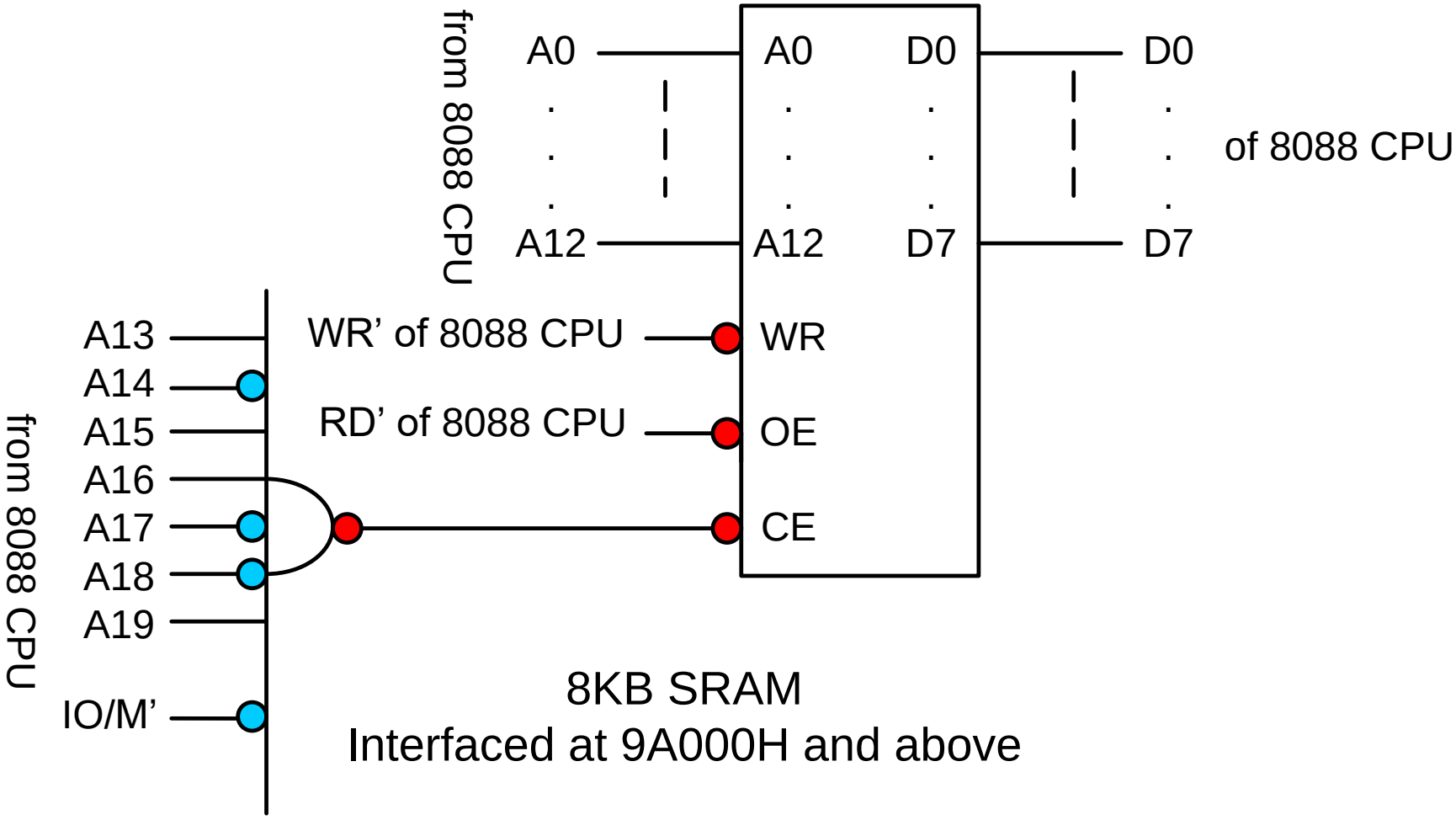
Interfacing Random Access Memory

Recall the SRAM

- Data Bus
- Address Bus
- Order of memory
- Control Bus or Control Lines

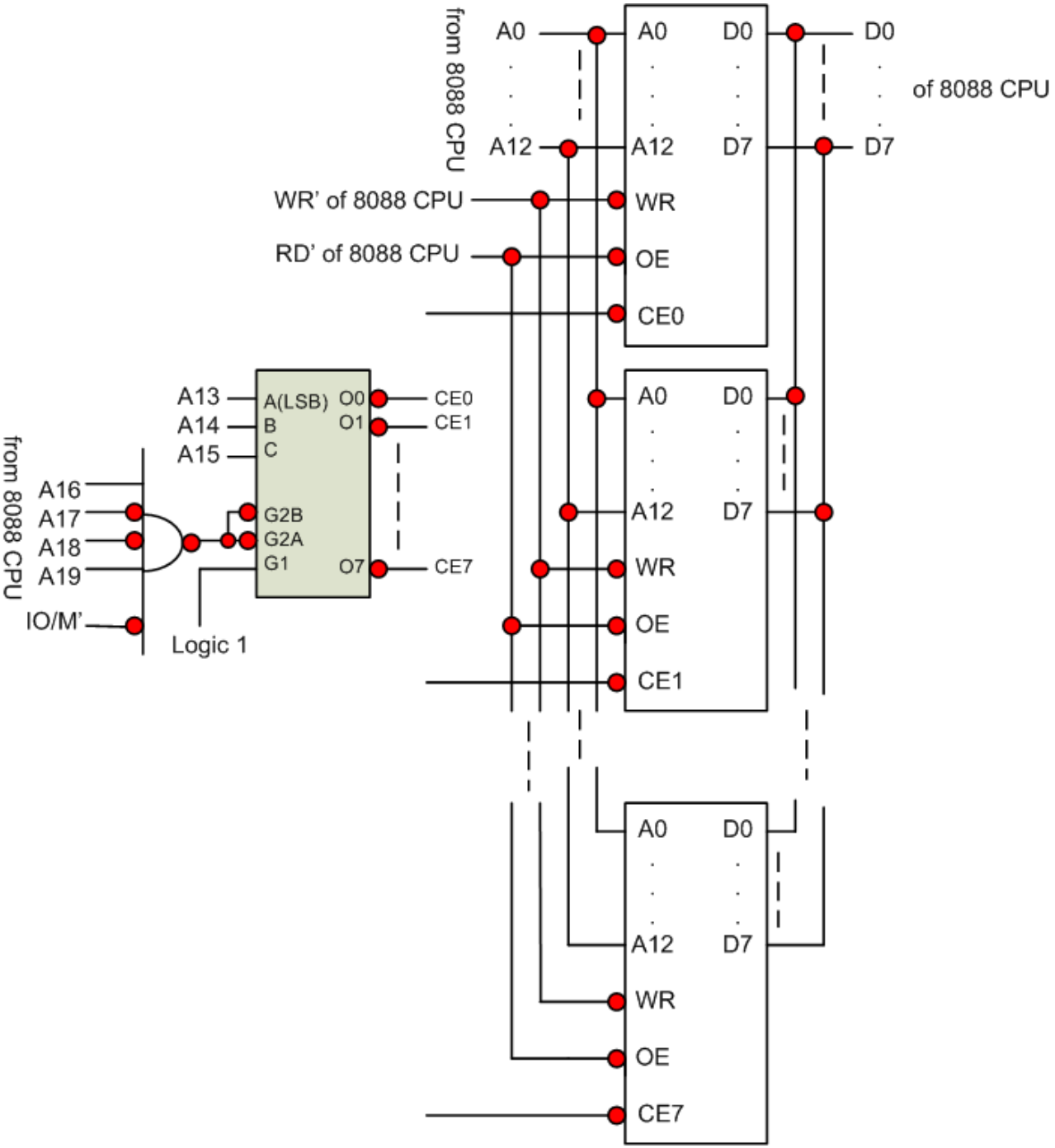
  (OE', WR', CS'(CE' or ME')
- Power lines (Vcc and GND)
- Tri-state or Z-state or High-impedance

Interfacing single SRAM chip



Truth Table of 74LS138

Inputs						Outputs							
Enable			Selection										
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{O0}$	$\overline{O1}$	$\overline{O2}$	$\overline{O3}$	$\overline{O4}$	$\overline{O5}$	$\overline{O6}$	$\overline{O7}$
X	X	1	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
0	X	X	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	1	1	0	1	1	1	1	1	1
1	0	0	0	1	0	1	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	0	0	1	1	1	1	0	1	1	1
1	0	0	1	0	1	1	1	1	1	1	0	1	1
1	0	0	1	1	0	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0


from 8088 CPU
A0
A12
A0
D0
A12
D7
WR
OE
CE0
D0
D7
of 8088 CPU
WR' of 8088 CPU
RD' of 8088 CPU
A13
A14
A15
A(LSB)
B
C
O0
O1
O7
CE0
CE1
CE7
G2B
G2A
G1
A16
A17
A18
A19
IO/M'
from 8088 CPU
Logic 1
A0
D0
A12
D7
WR
OE
CE1
A0
D0
A12
D7
WR
OE
CE7