COMSATS - Lancaster Dual Degree Programme

COMSATS Institute of Information Technology Lahore

Terminal–Spring 2016

Course Title:	Microprocessor Systems and Interfacing				Course Code:	EEE342	Credit Hours: 4(3,1)
Instructor:	Engr. Usman Rafique, Engr. Moazzam Ali Sahi				Programme:	B. Eng (Hons) TE, CE, EE	
Semester:	6th	Batch:	FA13, SP14	Section:	A	Date:	
Time Allowed:	180 Minutes				Maximum Marks:	100	
Student's Name:					Reg. No.	CIIT/DDP- /LHR	

Important Instructions / Guidelines:

- Answer all the questions on answer book in the same order as they are asked in question paper.
- Draw neat and clean figures wherever asked.
- Use of ***Calculator*** is NOT allowed.
- Cell phones are not allowed to keep with you even when they are switched off.
- Return the Question paper with the answer book

Question 1 20Marks

Interface 92KB EPROM and 48KB SRAM with 8088 CPU using at least one 64KB chip of EPROM and one 32KB chip of SRAM. Your design must use 74LS138 decoder in glue logic.
Memory map for total EPROM starts from 40000H and above and for SRAM, it starts from 60000H and above. For simplicity you may omit demultiplexing circuitry. You are required to provide:

a. Completely labelled single schematic diagram to interface EPROM and SRAM with CPU 12 Marks
b. Memory map for each memory chip 8 Marks

Question 2 20 Marks

a. Draw completely labelled schematics to interface a 4-pole stepper motor with 8088 CPU using 8255 PPI. Stepper motor is interfaced with PPI on Port A. 10 Marks
b. Write an 8086-88 assembly language program that rotates the stepper motor in part a by 45 degrees. Stepper motor's shaft rotation is scaled down by factor of 50. 10 Marks

Question 3 20 Marks

Interface 64KB SRAM with 8086 CPU using 8KB SRAM chips only. Memory map for total memory starts from 80000H and above. You are required to provide:

a. Completely labelled schematics of interfacing memory with CPU using "separate bank enable" approach 6 Marks
b. Completely labelled schematics of interfacing memory with CPU using "separate write strobe" approach 6 Marks
c. Memory map of each SRAM chip used in design 8 Marks

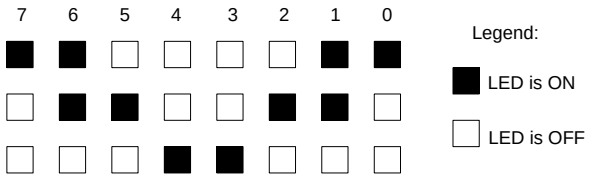
Question 4 20 Marks

Consider a magnetic disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1KB. The average seek time is 8ms, the track-to-track access time is 1.5ms, and the drive rotates at 3600rpm. Successive tracks in a cylinder can be read without head movement.

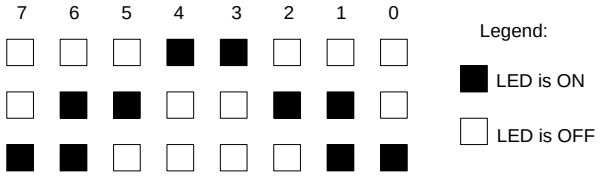
a. What is the disk capacity? 5 Marks
b. What is the average access time? Assume this file is stored in successive sectors and tracks of successive cylinders, starting at sector 0, track 0, of cylinder i. 5 Marks
c. Estimate the time required to transfer a 5MB file. 5 Marks
d. What is the burst transfer rate? 5 Marks

Question 5 20 Marks

You are required to design a digital system using 8088 CPU that involves push buttons and LEDs. Two push buttons, PB0 and PB1, are connected with bit0 and bit1 of an input port, respectively. Input port has port number 78H. Eight LEDs are connected with an output port having port number 80H. Your system must work as follows:
When PB0 is pressed, following pattern must be shown on eight LEDs only once



When PB1 is pressed, following pattern must be shown on eight LEDs only once



You are required to provide:

a. LEDs connection schematics with output port 5 Marks
b. Pushbuttons connection schematics with input port 5 Marks
c. An 8088 assembly language program, with as many minimum instructions as possible, that fulfils the system's requirement 10 Marks

END OF PAPER

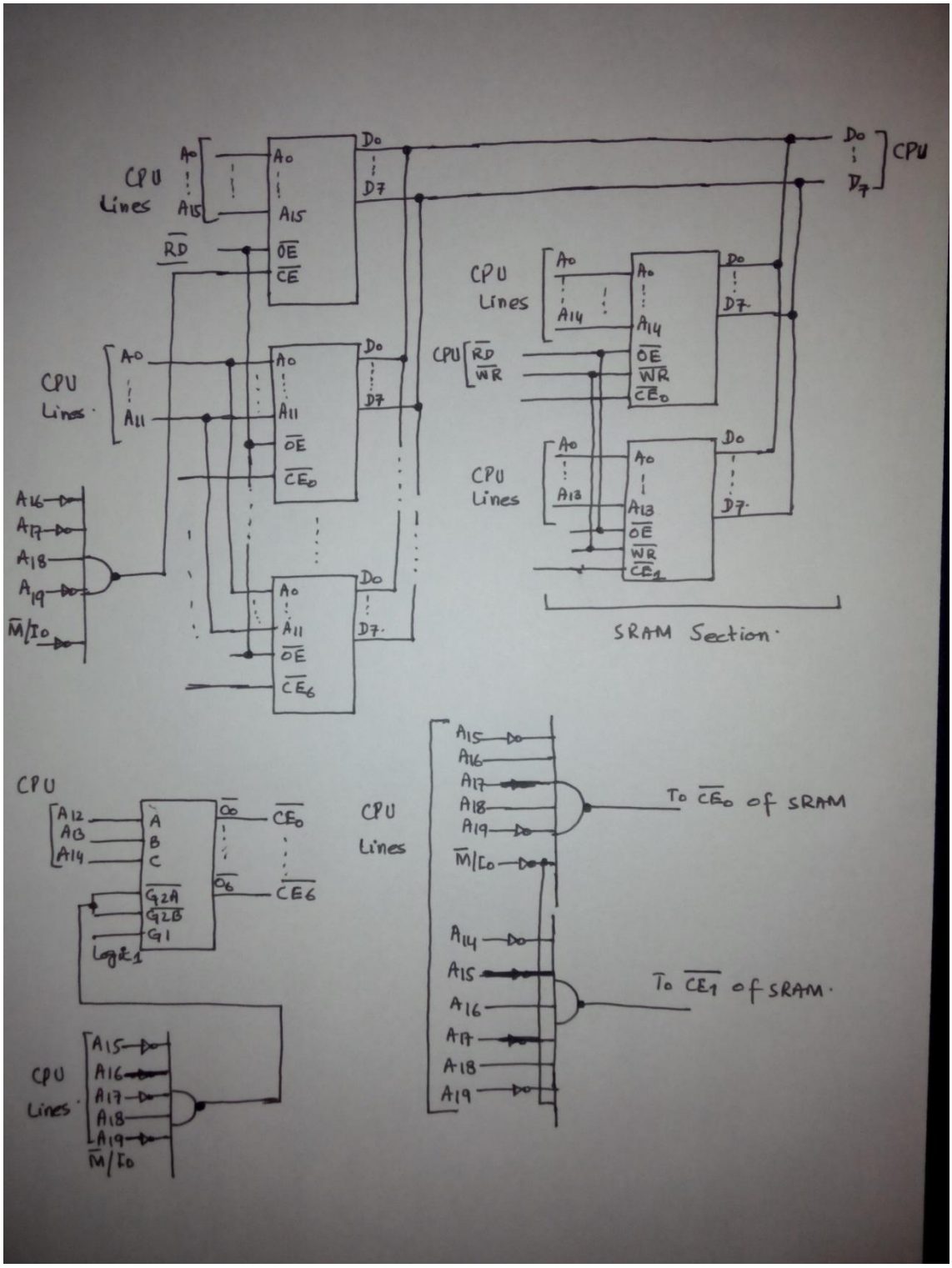
Solution Key

Question 1 20 Marks

Interface 92KB EPROM and 48KB SRAM with 8088 CPU using at least one 64KB chip of EPROM and one 32KB chip of SRAM. Your design must use 74LS138 decoder in glue logic.

Memory map for total EPROM starts from 40000H and above and for SRAM, it starts from 60000H and above. For simplicity you may omit demultiplexing circuitry. You are required to provide:

a. Completely labelled single schematic diagram to interface EPROM and SRAM with CPU 12 Marks

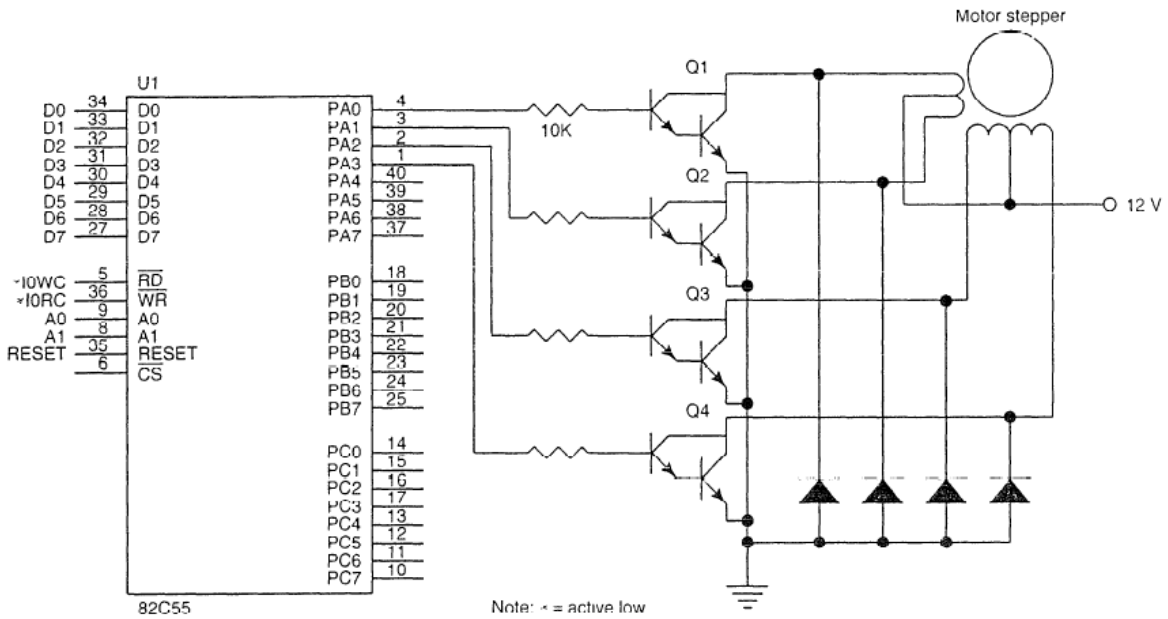


b. Memory map for each memory chip 8 Marks

SRAM:
SRAM (64KB): 40000H to 4FFFFH
SRAM0: 50000H to 50FFFH
SRAM1: 51000H to 51FFFH
SRAM2: 52000H to 52FFFH
SRAM3: 53000H to 53FFFH
SRAM4: 54000H to 54FFFH
SRAM5: 55000H to 55FFFH
SRAM6: 56000H to 56FFFH
EPROM:
EPROM0: 60000H to 67FFFH
EPROM1: 68000H to 6CFFFH

Question 2 20 Marks

a. Draw completely labelled schematics to interface a 4-pole stepper motor with 8088 CPU using 8255 PPI. Stepper motor is interfaced with PPI on Port A. 10 Marks



b. Write an 8086-88 assembly language program that rotates the stepper motor in part a by 45 degrees. Stepper motor's shaft rotation is scaled down by factor of 50. 10 Marks

```
START:
        MOV   CX, 6
        MOV   AL, 9BH
        OUT   0AFH, AL
                                        2
ROTATE:
        MOV   AL, 0FH
        OUT   0ACH, AL                  2

        MOV   AL, 0EH
        OUT   0ACH, AL                  2
```

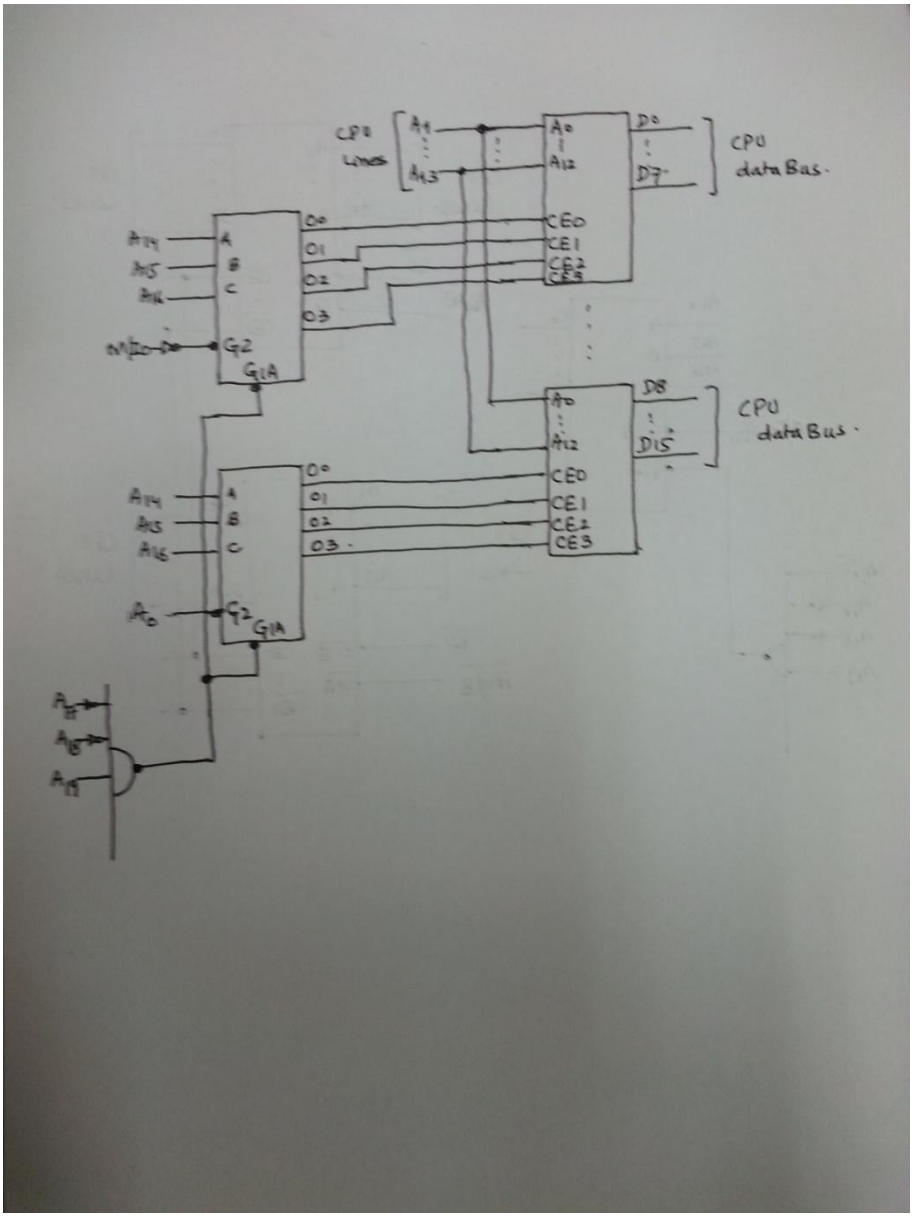
```
MOV   AL, 0CH
OUT   0ACH, AL                                  2


MOV   AL, 08H
OUT   0ACH, AL                                  2

JMP   ROTATE
HLT
```

Question 3 20 Marks

Interface 64KB SRAM with 8086 CPU using 8KB SRAM chips only. Memory map for total memory starts from 80000H and above. You are required to provide:

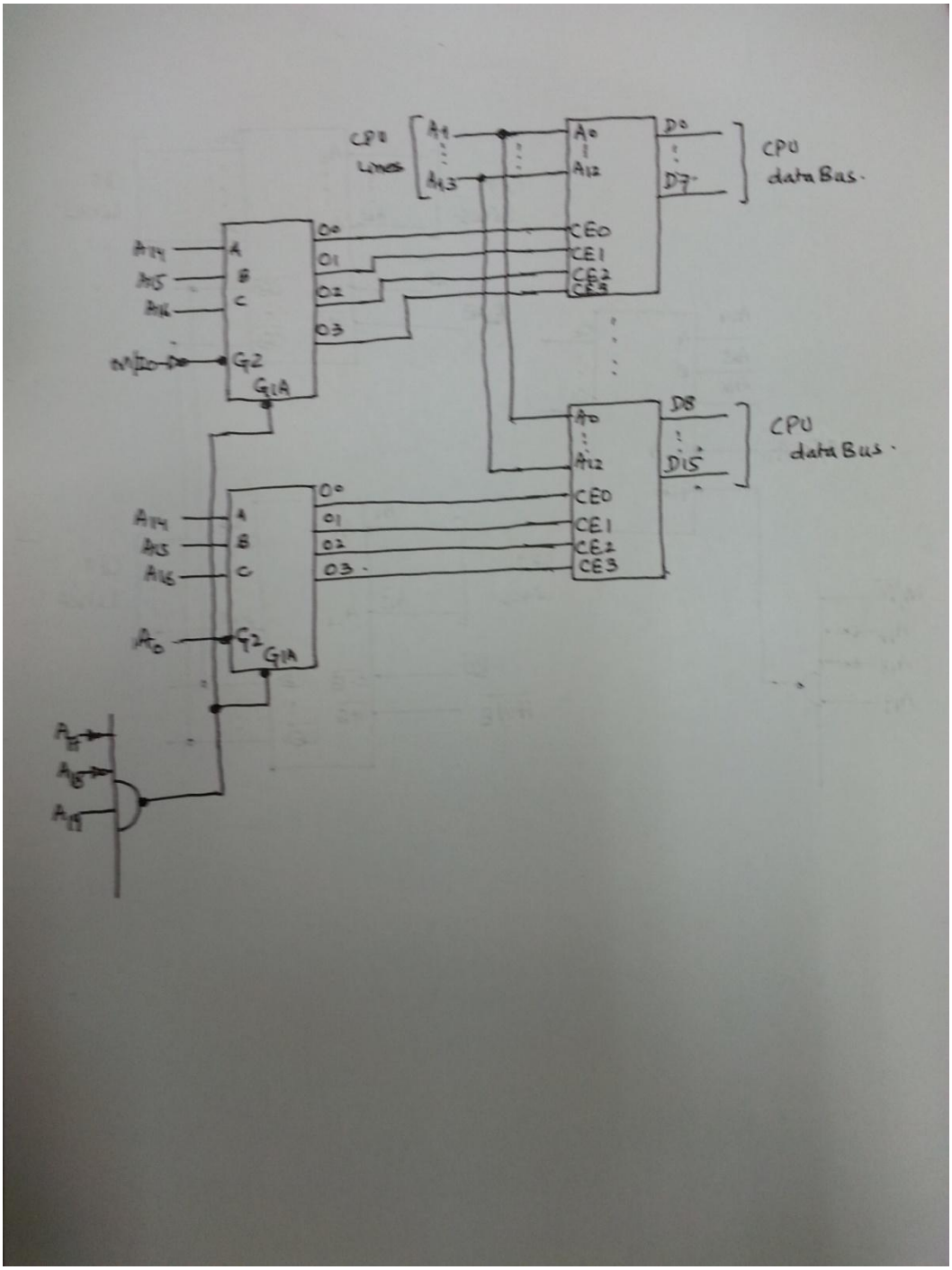
a. Completely labelled schematics of interfacing memory with CPU using "separate bank enable" approach

6 Marks



b. Completely labelled schematics of interfacing memory with CPU using “separate write strobe” approach

6 Marks



c. Memory map of each SRAM chip used in design 8 Marks

For lower bank:
80000H to 8FFFEH
For higher bank:
80001H to 8FFFFH

Question 4 20 Marks

a. Capacity = 8 × 512 × 64 × 1 KB = 256 MB

b. Rotational latency = rotation_time / 2 = 60 / (3600 × 2) = 8.3 ms.
Average access time = seek time + rotational latency = 16.3 ms

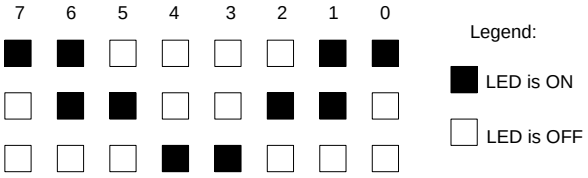
c. Each cylinder consists of 8 tracks × 64 sectors / track × 1 KB / sector = 512 KB, so 5 MB requires exactly 10 cylinders. The disk will need the seek time of 8 ms to find cylinder *i*, 8.3 ms on average to find sector 0, and 8 × (60 / 3.6) = 133.3 ms to read all 8 tracks on one cylinder. Then, the time needed to move to the next adjoining cylinder is 1.5 ms, which is the track-to-track access time. Assume a rotational latency before each track.

$$\text{Access Time} = 8 + 9 \times (8.3 + 133.3 + 1.5) + (8.3 + 133.3) = 1425.5 \text{ ms}$$

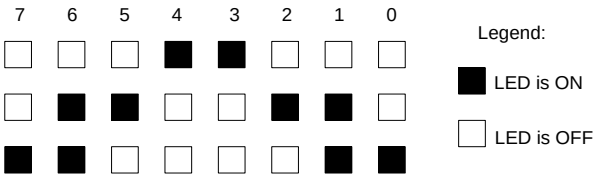
d. $$\text{Burst rate} = \frac{\text{revolutions}}{\text{second}} \times \frac{\text{sectors}}{\text{revolution}} \times \frac{\text{bytes}}{\text{secter}} = \frac{3600}{60} \times 64 \times 1\,\text{KB} = 3.84 \text{ MB/s}$$

Question 5 20 Marks

You are required to design a digital system using 8088 CPU that involves push buttons and LEDs. Two push buttons, PB0 and PB1, are connected with bit0 and bit1 of an input port, respectively. Input port has port number 78H. Eight LEDs are connected with an output port having port number 80H. Your system must work as follows:
When PB0 is pressed, following pattern must be shown on eight LEDs only once

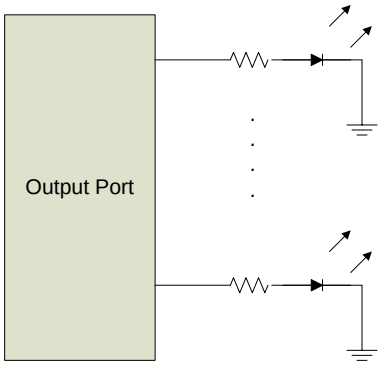


When PB1 is pressed, following pattern must be shown on eight LEDs only once

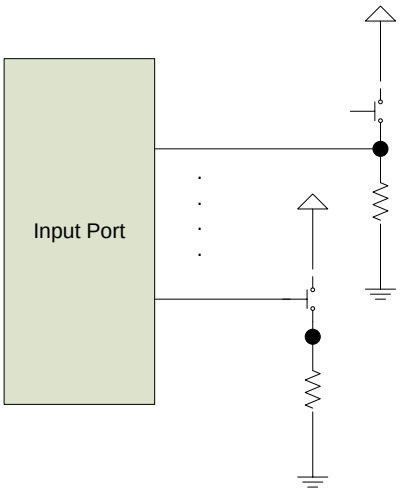


You are required to provide:

a. LEDs connection schematics with output port 5 Marks



b. Pushbuttons connection schematics with input port 5 Marks



c. An 8088 assembly language program, with as many minimum instructions as possible, that fulfils the system's requirement 10 Marks

```
START:
        IN    AL, 78H
        AND   AL, 01H
        CMP   AL, 1H
        JE    R1                                  2 marks
        IN    AL, 78H
        AND   AL, 02H
        CMP   AL, 2H                              2 marks
        JE    R2
        JMP   START                               2 marks
R1:
        MOV   AL, 0C3H
        OUT   80H, AL
        MOV   AL, 66H
        OUT   80H, AL
        MOV   AL, 18H
        OUT   80H, AL
        JMP   START                               2 marks
```

R2:

```
MOV   AL, 18H
OUT   80H, AL
MOV   AL, 66H
OUT   80H, AL
MOV   AL, 0C3H
OUT   80H, AL
JMP   START
HLT
```

2 marks