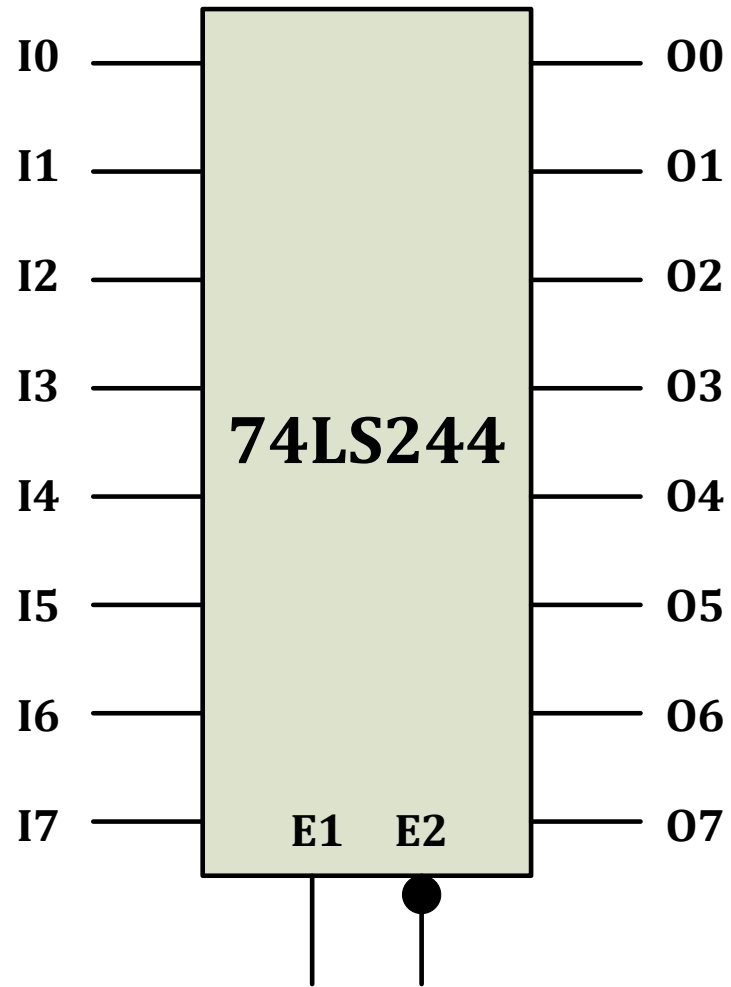# Ports Interfacing with 8088 CPU

IN and OUT Instructions, Input Ports, Output Ports, Address Decoding
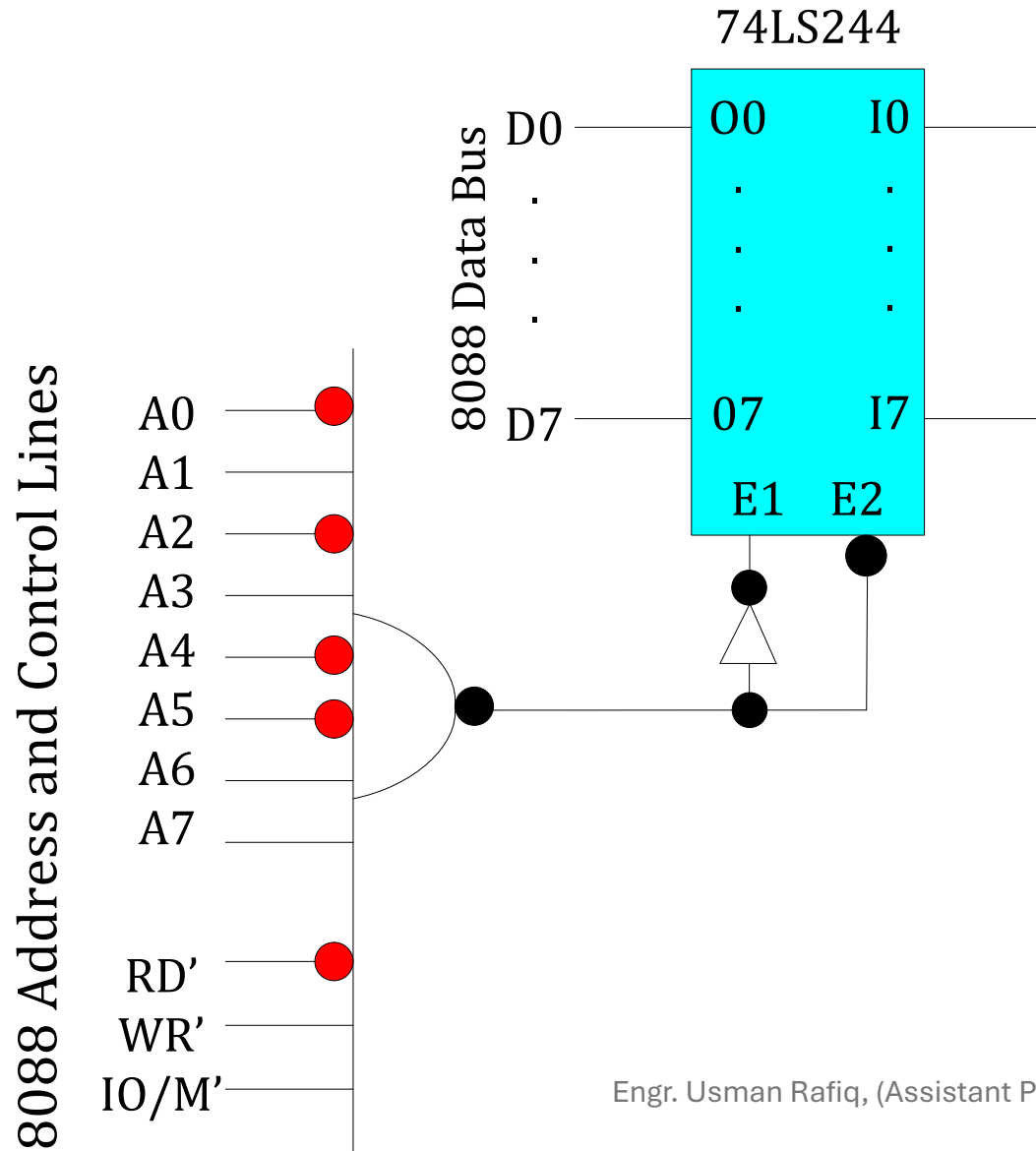
Fundamentals

➢ What is Port?

➢ Port number or Port ID

➢ IN instruction

➢ OUT instruction

➢ Registers involved in IN and OUT instructions

➢ Variable and Fixed port numbers

➢ Execution response of IN and OUT instructions (Status of address bus, data bus, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$)

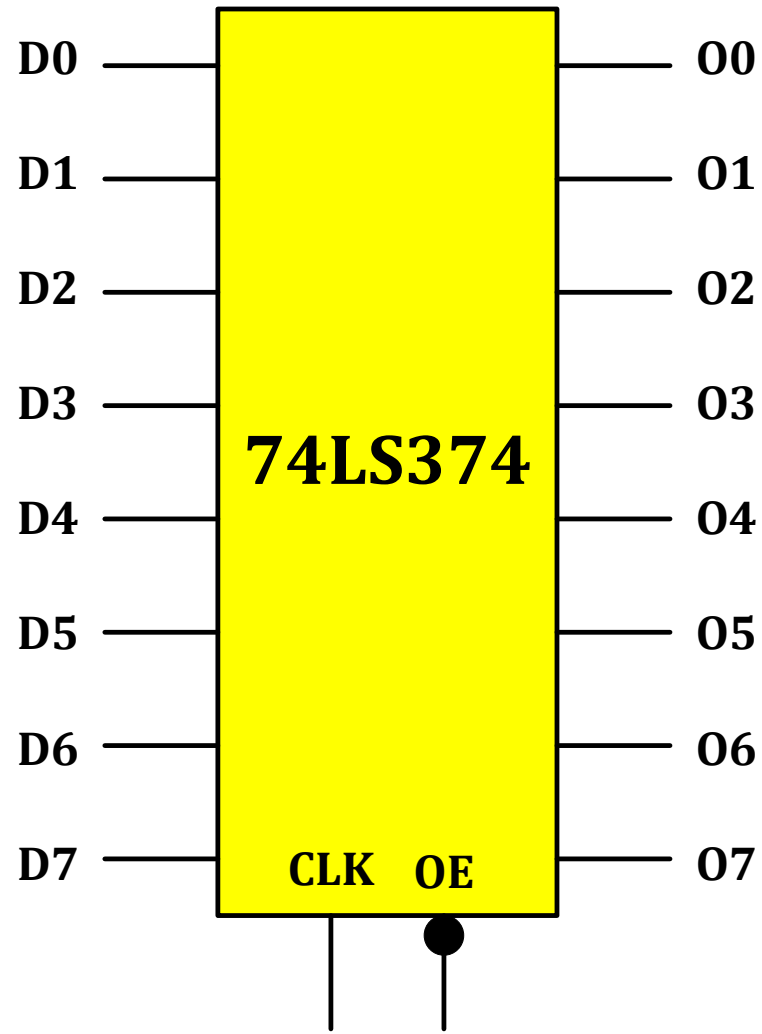Engr. Usman Rafiq, (Assistant Professor) CE Dept. CUI, Lahore Campus

2

74LS244 Tri-state buffer

Interfacing an Input Port

74LS244

8088 Data Bus

D0 — O0   I0

D7 — O7   I7

E1   E2

8088 Address and Control Lines

A0
A1
A2
A3
A4
A5
A6
A7

RD'
WR'
IO/M'

74LS374 8-bit parallel register

Interfacing an Output Port

74LS374

D0 — D0   O0

.   .   .

.   .   .

.   .   .

D7 — D7   07

CLK   OE

8088 Data Bus

8088 Address and Control Lines

A0
A1
A2
A3
A4
A5
A6
A7

RD'
WR'
IO/M'

Interfacing Bidirectional I/O Port
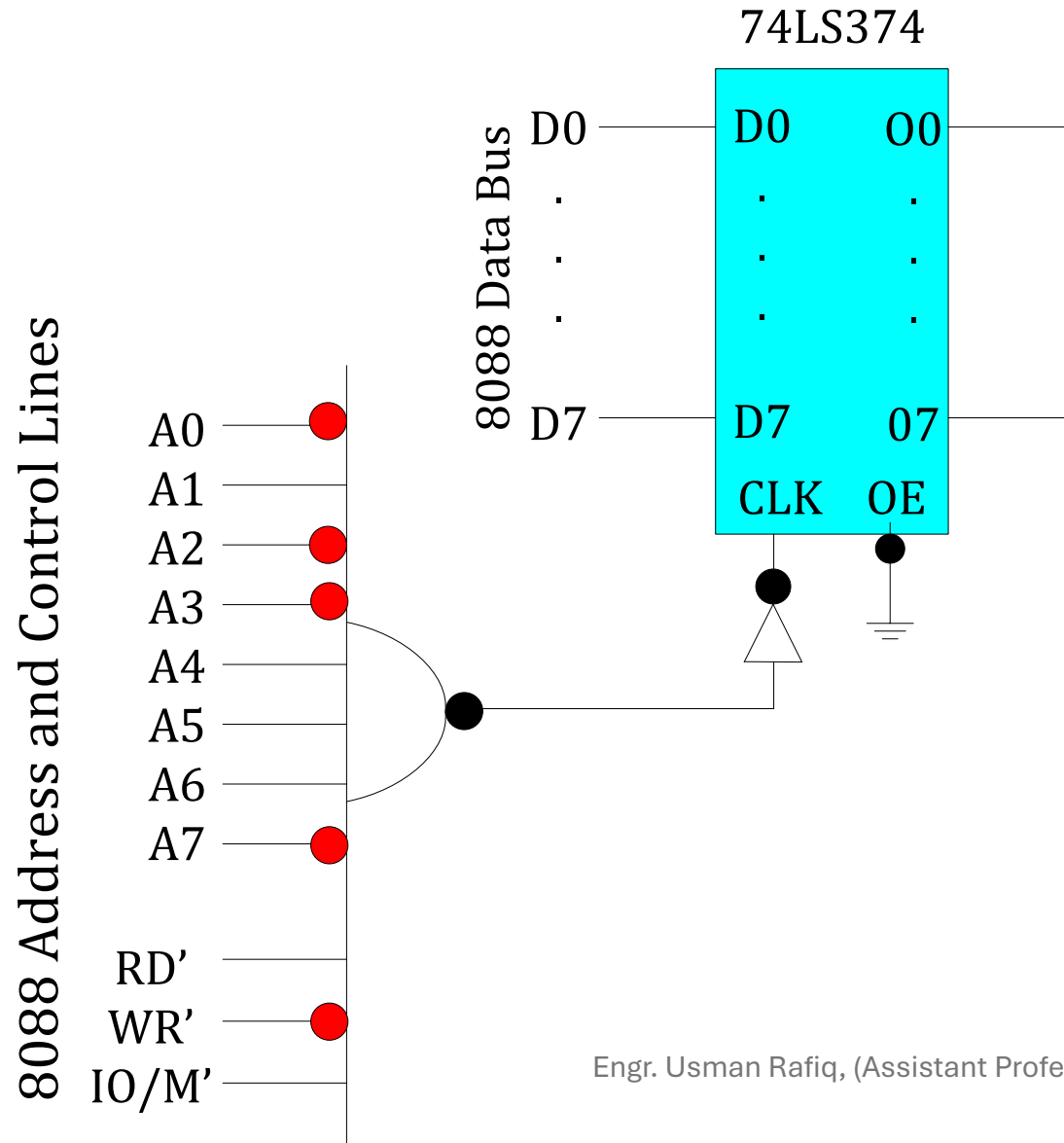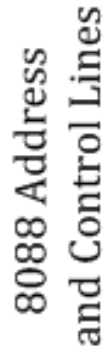
Memory-mapped I/O (Input Port)

74LS244

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8
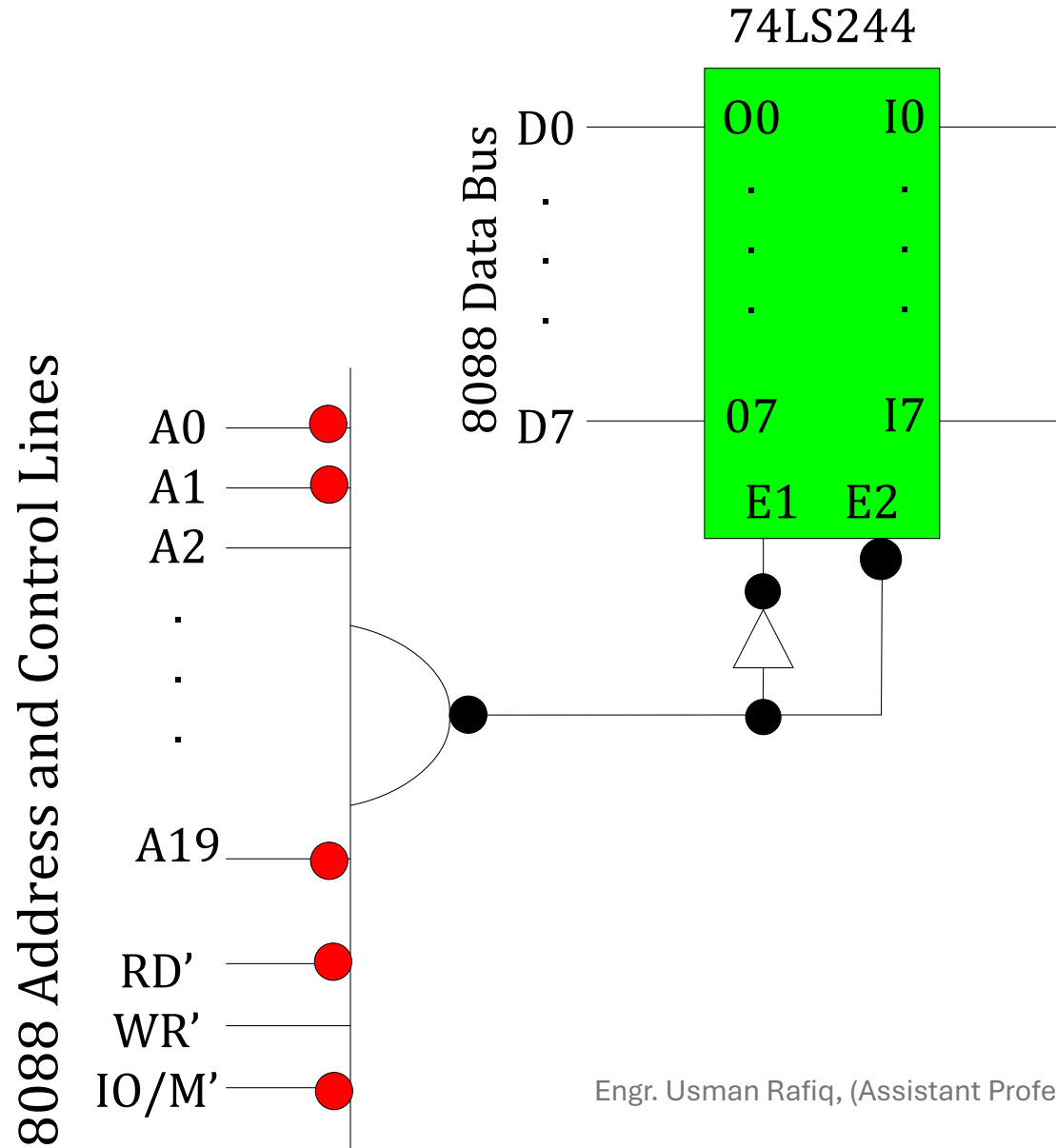
Memory-mapped I/O (Output Port)

74LS374

8088 Data Bus

D0 — D0   O0 —
.   .   .
.   .   .
.   .   .
D7 — D7   07 —

CLK   OE

8088 Address and Control Lines

A0
A1
A2
.
.
.
A19

RD'
WR'
IO/M'