Handouts on

Semiconductor Memory Devices

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Electronic memory circuits or solid-state memory circuits are semiconductors components that are designed to store digital information in form of binary data. These components are available in form of integrated circuits. Based on the data storage mechanism, memory circuits can be divided into two broader classes, the volatile and the non-volatile.

Volatile memory

The word volatile means 'invisible'. In the context of semiconductor memories, volatile memory is the one which loses its contents if electric power is removed from its circuit. On resuming electric power, older contents of this type of memory cannot be retrieved at all. Example of such memory is random access memory (RAM).

Non-volatile memory

These memories retain their stored contents even in the absence of electric power. Upon repowering up the device, stored contents can be retrieved. Examples of such memories are read-only memory (ROM) and flash memory.

RAM devices

RAM circuits can be classified in two major classes, static RAM and dynamic RAM. Static RAM (SRAM) is simpler to use in comparison to dynamic RAM (DRAM). SRAM is made with latches to store binary information (data) and is faster than DRAM in terms of accessing and storing data. However, SRAM is expensive than DRAM of the same storage capacity. DRAM is made of MOS

transistors that work as capacitors to store charge, which represent stored data. This charge leaks off with time hence causes data lost. In order to keep the data stored, DRAM circuits are continuously applied electric pulses that keep MOS capacitors charged hence data remain present in memory. This procedure is called 'refreshing'. Due to this continuous requirement of refreshing pulses, they are termed as 'dynamic'. SRAM does not require refreshing pulses hence called static in contrary.

ROM devices

ROM circuits do not contain latches or flip-flops to store information rather they use CMOS components to store data in them. Based on technology used to implement ROM circuits, they are classified as (i) PROM, (ii) EPROM and (iii) EEPROM.

PROM, abbreviation of 'programmable read-only memory', is a non-volatile memory circuit in which data is stored only once but can be read infinite times. Process of storing data in ROM is called 'programming' the ROM. PROM devices can be programmed using a special device called 'ROM programmer'. Once information has been written in PROM, it cannot be altered. If information is required to be changed, new PROM is to be used.

EPROM, abbreviation of 'erasable programmable read-only memory', is a type of ROM in which older data can be erased and new data can be programmed. EPROM integrated circuit contains a quartz window that exposes the semiconductor chip. Ultraviolet (UV) light is shown on this semiconductor chip through quartz window that erases the stored data and makes device ready to be programmed with new data. This procedure requires device to take out from the circuit board and place in EPROM eraser (device designed to delete EPROM contents) that shines UV on semiconductor chip of memory. Erasing EPROM takes several minutes. Hence it is a very time consuming process to erase older data and reprogramming the device with fresh data.

EEPROM, abbreviation of 'electrically erasable programmable read-only memory', is improved version of EPROM. As the name depicts, EEPROM can be erased and programmed using electric pulses. Hence EEPROMs do not require

removal from circuit boards for erasure. In addition to that, EEPROM can be erased in milliseconds as compared to EPROM that requires several minutes for erasure process. Once EEPROM is programmed, its contents can be read for infinite times.

Memory organization

Data are stored in a memory in discrete parts called 'cells'. In general, a cell stores one bit of binary data. How these cells are implemented, depends upon technology and architecture of memory circuit. These cells are arranged in memory circuit in form of a matrix that consists on rows and columns. Following figure shows arrangements of cells in certain memory circuit. This figure is valid for all three types of ROMs discussed above and for SRAM as well.

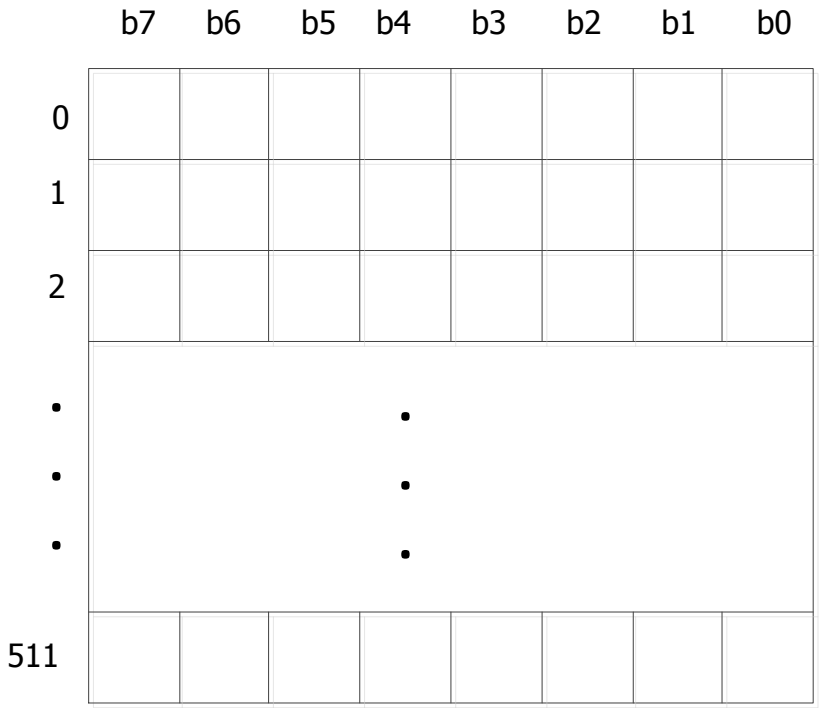

Fig. 1

Memory cells are arranged in 512 rows and 8 columns. Hence this memory contains 4096 cells and can store 4096 bits (4 Kb) of binary data. Each row is called a 'location' hence each location stores one byte of data. So it can be said

that this example memory device has 512 bytes (512 B) storage capacity. Number of each row is called address of that location. Hence for this memory, there are 512 unique addresses. Number of bits that can be stored at a single address is called data width of memory which is one byte in this case. In practice, data width is fixed for all the addresses in a memory circuit. Storage capacity for this exemplary memory device is written as 512x8 (called the order of memory), means it has 512 locations and each location is 8-bit wide.

As semiconductor memories are digital circuits, any kind of information that is to be transferred to or received from them is in binary. In order to access an individual location in memory, its corresponding address is required to be known. In this example memory device, 9 bits are required to generate total 512 addresses. Hence this memory device requires 9 'address lines' or in other words, 9-bit address bus, to access 512 locations uniquely.

8 lines are required in order to transfer 8 bits of data, stored in one location, to or from memory. These lines are called data lines or data bus. Hence this memory has 8-bit data bus. Similarly, a memory with2KB (2Kx8) capacity would have 11-bit address bus (11 address lines) and 8-bit data bus (8 data lines) etc. Memories may have 16-bit wide data bus in order to transfer 16 bits of data stored in one location.

Commercially available memory circuits

Semiconductor memories are assigned a unique alphanumeric code for their identification which is called its part number. Part number describes some fundamental information about type of memory and its storage capacity.

EPROM memory chips can be identified with part number that starts from 27. For example, a commercially available EPROM chip is 27C128. Here, 27 is the code for EPROM, C is for CMOS technology which is used to implement storage cells and 128 tells that it has 128 Kb of storage. Letter 'b' abbreviates bit(s) and letter 'B' abbreviates byte(s). This memory has 8-bit data bus, hence its order is 16Kx8 (16 KB = 128 Kb).

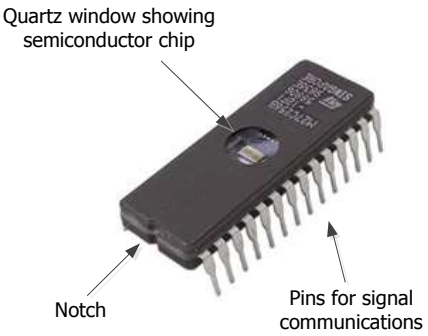

Fig. 2

As it has 16K locations, its address bus is 14-bit wide which is numbered from A_0 to A_{13}, such that A_0 is LSB and A_{13} is MSB. Its data lines are numbered from D_0 to D_7, such that D_0 is LSB and D_7 is MSB. Figure 2 shows a snapshot of EPROM IC.

Note that a memory device with part number 27C512 will be identified as EPROM with CMOS technology, 64Kx8 order and 64 KB storage capacity.

SRAMs are generally identified with code 61 or 62. For example, a commercially available SRAM is 61C16. It identifies that it is an SRAM (from code of 61), it is implemented using CMOS (from letter C) and its storage capacity is 16 Kb, ordered as 2Kx8 (2 KB).Following snapshot shows a RAM IC.

Fig. 3

Another part number is 62C256 which is 32 KB CMOS SRAM chip.

EEPROM memory chips are identified with code 28. For example, a commercially available device with part number 28C64 is an EEPROM with storage capacity of 64 Kb ordered as 8Kx8.

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An EEPROM IC is shown in following snapshot.

Fig. 4

Similarly, a 32 KB EEPROM will have part number 28C256.

Following table shows some common memory part numbers and their storage capacity.

Table 1

Memory Type	Part number	Storage capacity
EPROMs	27C16	2KB
	27C64	8KB
	27C128	16KB
	27C256	32KB
	27C512	64KB
SRAMs	61C16	2KB
	62C256	32KB
EEPROMs	28C16	2KB
	28C32	4KB
	28C256	32KB

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Note: All these memory chips have one-byte wide data bus.

Tri-state or High-impedance state

A digital circuit will be in tri-state or high-impedance state when no electrical information is exchanged between it and some other circuit attached to it. Strictly speaking with respect to memories, a memory will be tri-stated if it is "virtually absent" from the circuit. By virtually absent means, memory chip remains in the circuit but any kind of information exchange to or from it is aborted. In almost every memory chip or digital device, an input pin called 'chip select (CS)'or 'chip enable (CE)' is used to bring device in tri-state. When CS will be inactive, device will be in tri-state. Otherwise it will be performing its normal operation.

Writing data to SRAM

Data writing to SRAM requires a few steps that include address placement on its address bus, data placement on its data bus and activating write control signals. SRAM chip has three or four control lines that include a 'read' ($\overline{\text{RD}}$) line or output enable ($\overline{\text{OE}}$) line, a 'write enable' ($\overline{\text{WE}}$) line and one or two 'chip enable' ($\overline{\text{CE}}$) or 'chip select' ($\overline{\text{CS}}$) lines. $\overline{\text{RD}}$ or $\overline{\text{OE}}$ line, if activated, informs memory that a read operation (transferring data out of memory) is required to be performed. $\overline{\text{WE}}$ line, if activated, informs memory that a write operation (transferring data to the memory) is required to be performed. $\overline{\text{CS}}$ or $\overline{\text{CE}}$ line, if activated, allows any read and write operation. If $\overline{\text{CS}}$ or $\overline{\text{CE}}$ is inactive, all the lines on memory will be tri-stated and any read or write operation is aborted.

Consider pin-out of an SRAM chip given below.

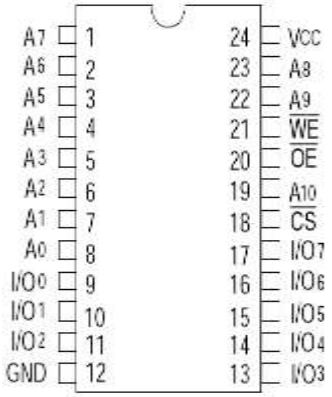

Fig.5

This memory has 11 address lines (A0 to A10) and 8 data lines (I/O0 to I/O7). In order to write in this memory, $\overline{CS}$ line is to be deactivated first by placing logic 1 on it. (Note that its symbol has a bar on it that required logic 0 for its activation). Now an 11-bit address is placed on address bus and data byte that is to be written at this address is placed on I/O lines. Then $\overline{WE}$ signal is activated (placing logic 0) and $\overline{OE}$signal is inactivated (placing logic 1). As final step, $\overline{CS}$ signal is activated that allows completing the write operation. After keeping $\overline{CS}$ active for a few nanoseconds, it is again inactivated so that another write operation can be performed following the same steps.

Reading from SRAM, EPROM and EEPROM

Reading from SRAM, EPROM or EEPROM follows identical procedure. Memory is first tri-stated by inactivating $\overline{CS}$ or $\overline{CE}$ line. Then address is placed on address bus, $\overline{OE}$ line is made active and $\overline{WE}$ line (in case of SRAM only) is made inactive. Activate $\overline{CS}$ or $\overline{CE}$ signal and memory will place stored data on its data bus that was saved in it at applied address.

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