Leading University

Department of Electrical and Electronics Engineering

Course Code: EEE - 4128
Course Title: VLSI-1(Lab)

Lab Report: 05
Design of CMOS inverter, 2 and 3 inputs CMOS NAND and NOR Gates Combinational Logic Circuits using DSCH2 software.

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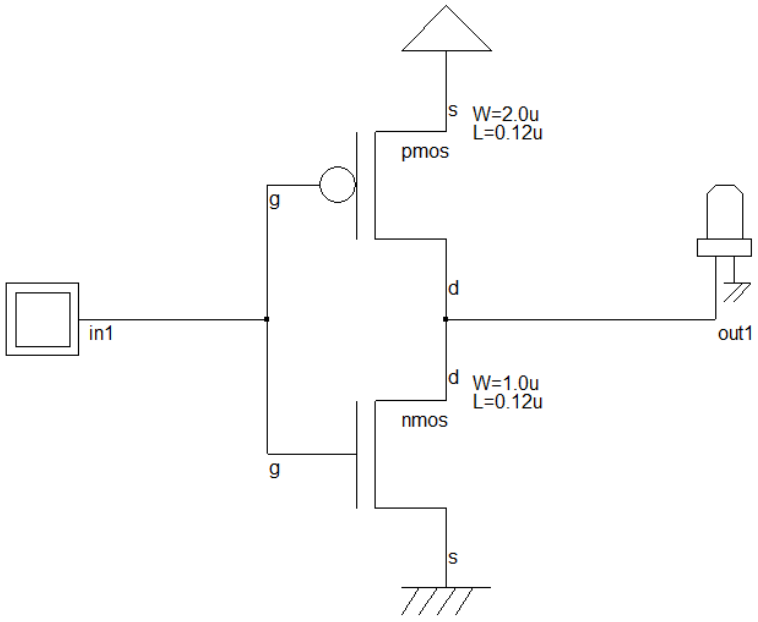
Experiment No.: 05

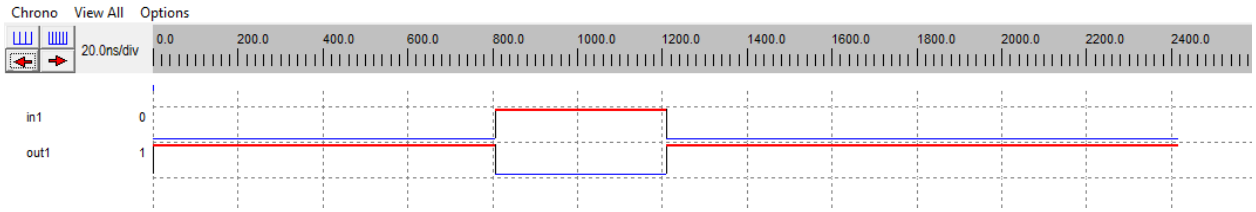
Title: Design of CMOS inverter, 2 and 3 inputs CMOS NAND and NOR Gates Combinational Logic Circuits using DSCH2 software.

Circuit Diagram and Simulations: All circuit diagrams and simulations have been completed in DSCH2 software.

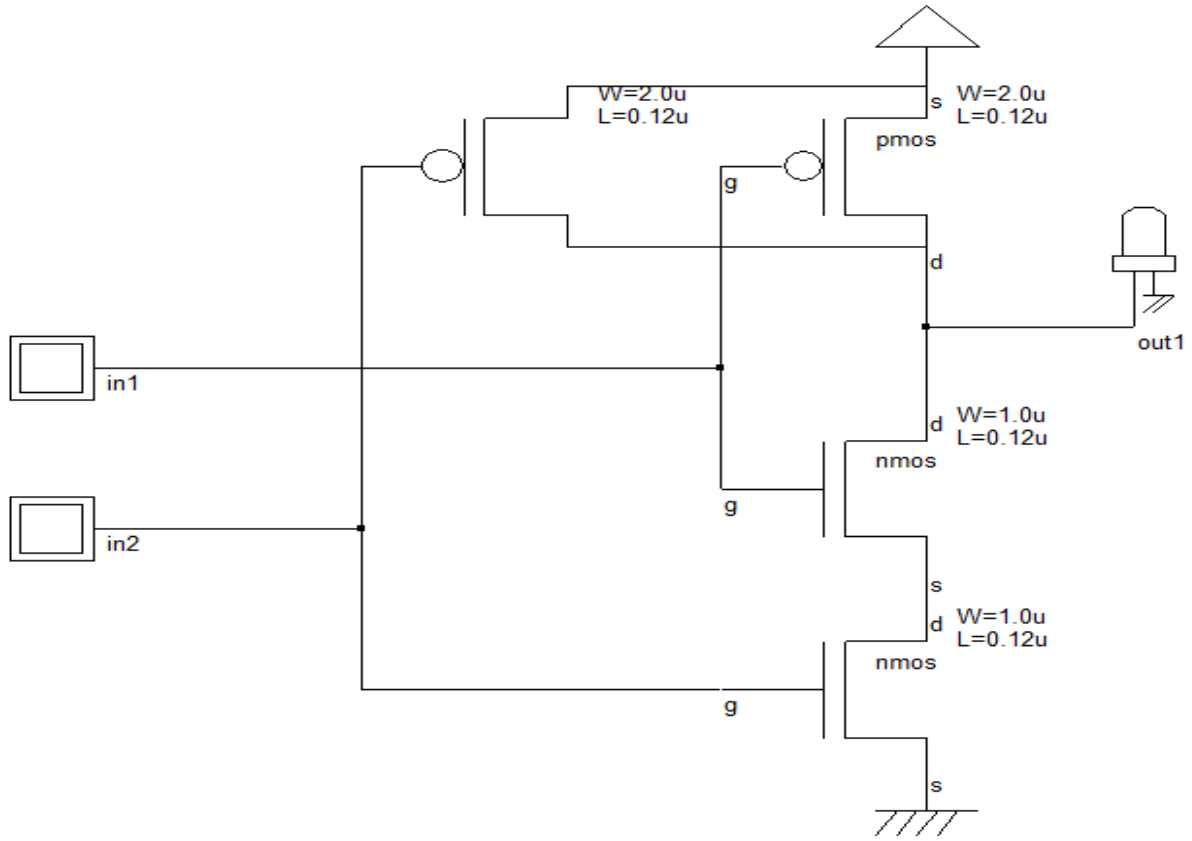
CMOS Inverter



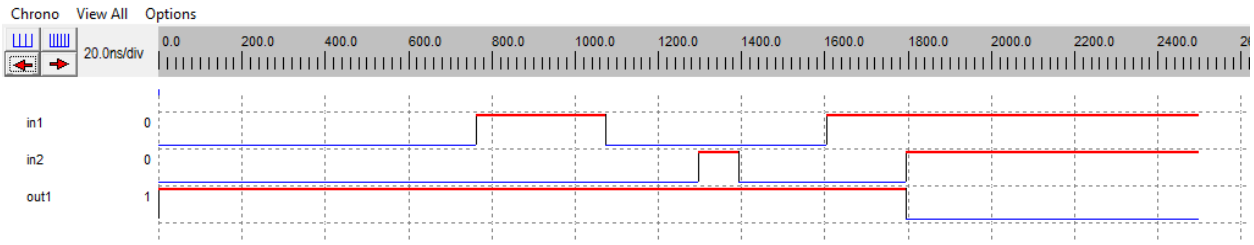
Simulation of CMOS Inverter:



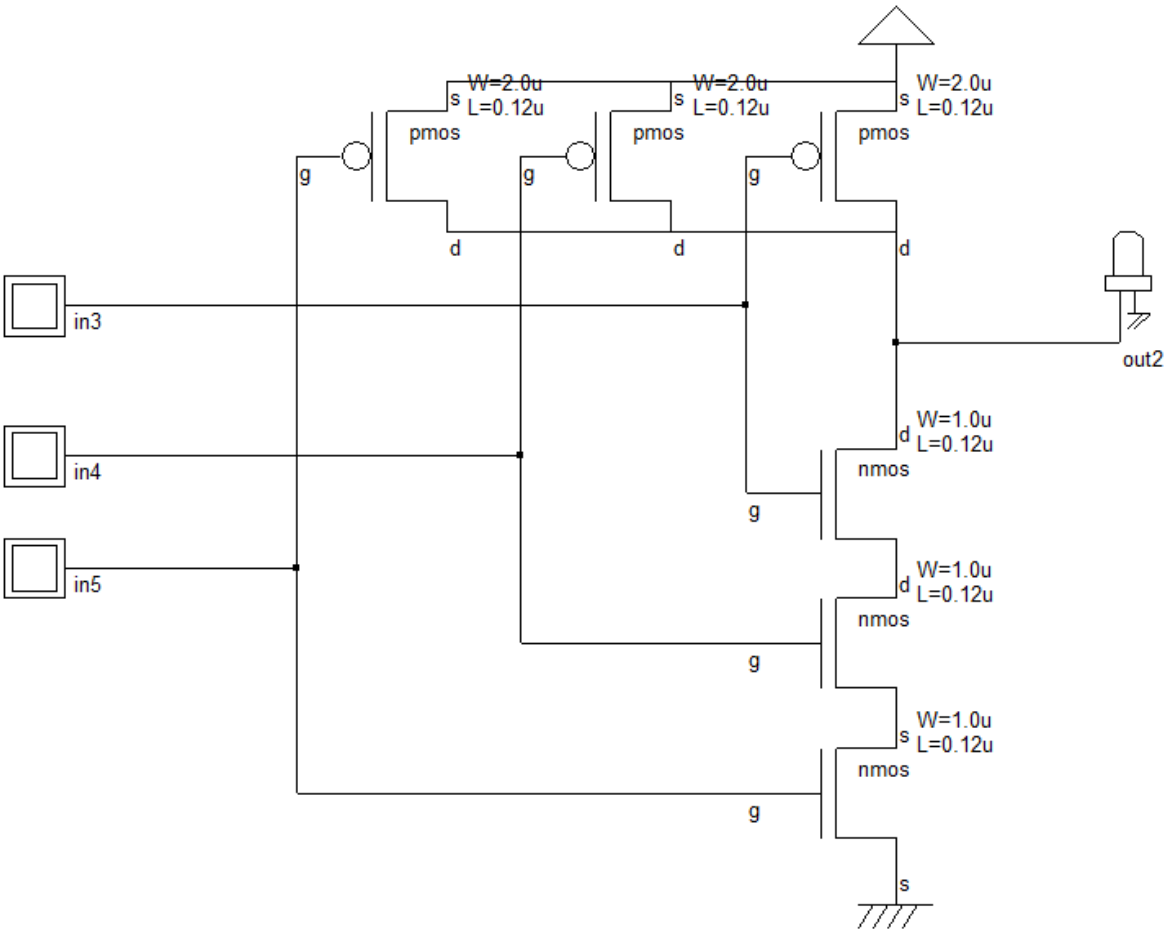
2 input CMOS NAND Gate:



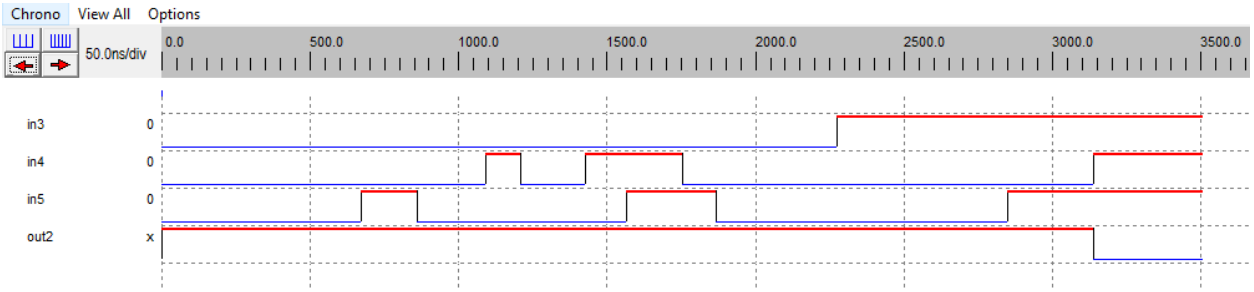
Simulation of 2 input CMOS NAND Gate:



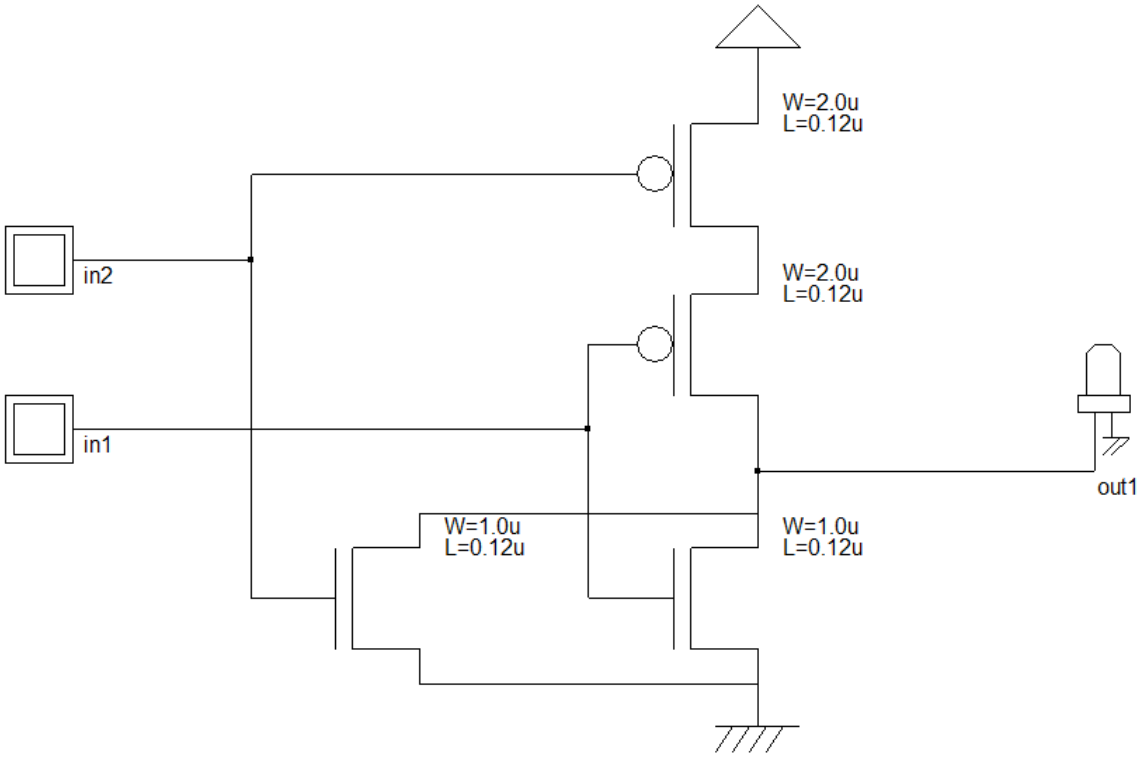
3 input CMOS NAND Gate:



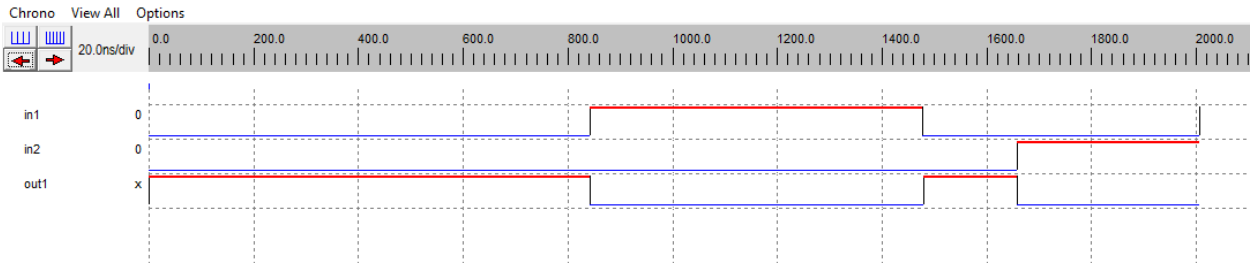
Simulation of 3 Input CMOS NAND Gate:



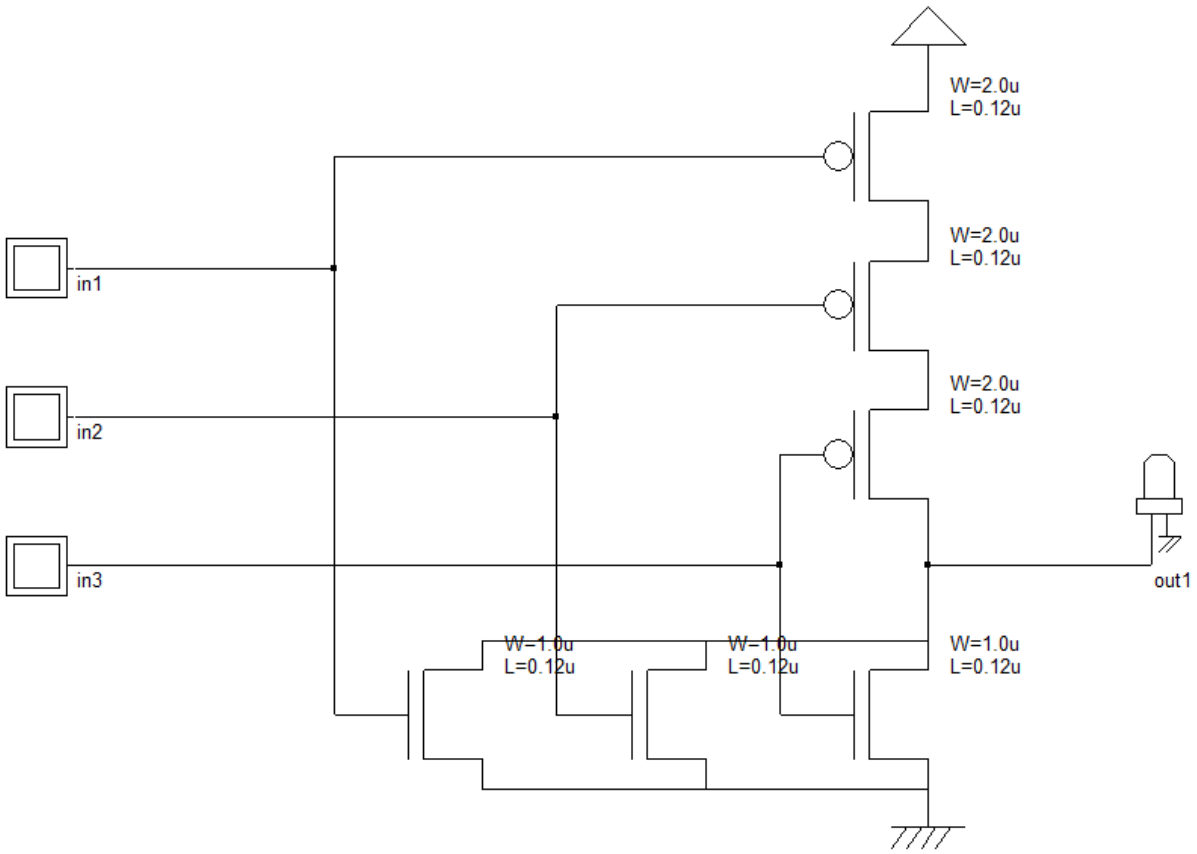
2 input CMOS NOR Gate:



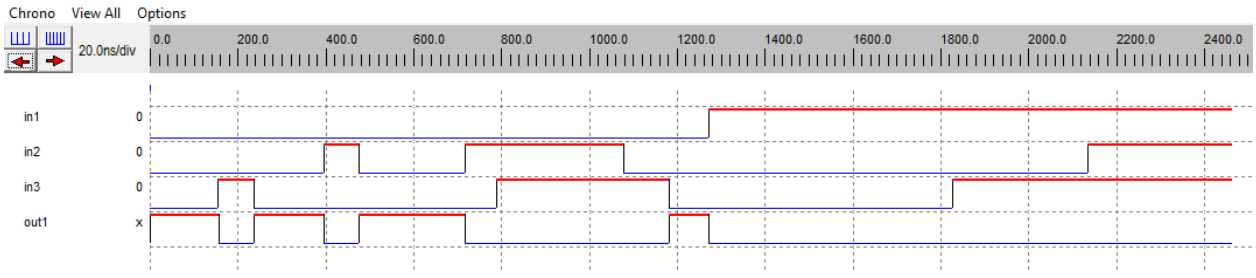
Simulation of 2 input CMOS NOR Gate



3 Input CMOS NOR Gate:



Simulation of 3 Input CMOS NOR Gate:



Discussion and Conclusion:

The provided circuit schematics and the output simulations have all been completed using the DSCH2 software. This software is very resourceful in the sense that it saves a lot of time when it comes to simulations such as these. The library is readily available at the right of the screen. The CMOS inverter circuit requires a pmos and an nmos transistor while the 2 input CMOS NAND gate requires 2 pmos and 2 nmos transistors and the 3 input require 3 pmos and 3 nmos transistors all the while keeping the pmos in the pull up configuration and the nmos in the pull down configuration. The circuit connections were provided in the software and then the output simulation was taken for various inputs. The software environment is very beginner friendly.