Leading University

Department of Electrical and Electronics Engineering

Course Code: EEE - 4128
Course Title: VLSI-1(Lab)

Lab Report: 05
Design of CMOS inverter, 2 and 3 inputs CMOS NAND and NOR Gates Combinational Logic Circuits using DSCH2 software

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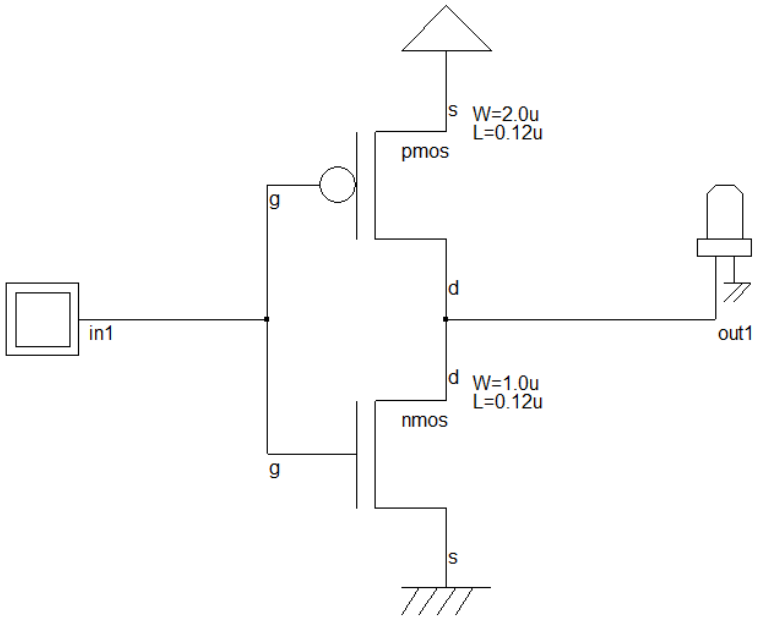
Experiment No.: 05

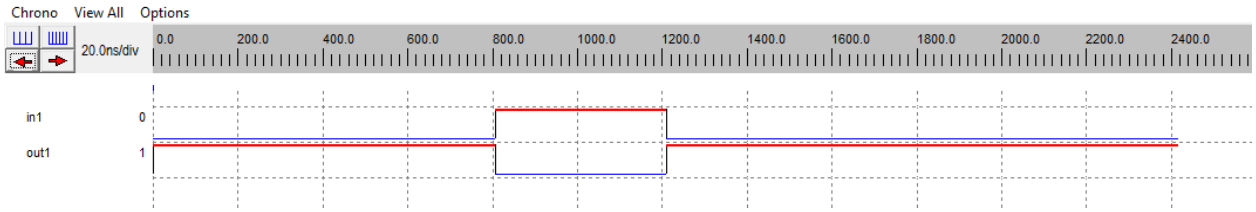
Title: Design of CMOS inverter, 2 and 3 inputs CMOS NAND and NOR Gates Combinational Logic Circuits using DSCH2 software.

Circuit Diagram and Simulations: All circuit diagrams and simulations have been completed in DSCH2 software.

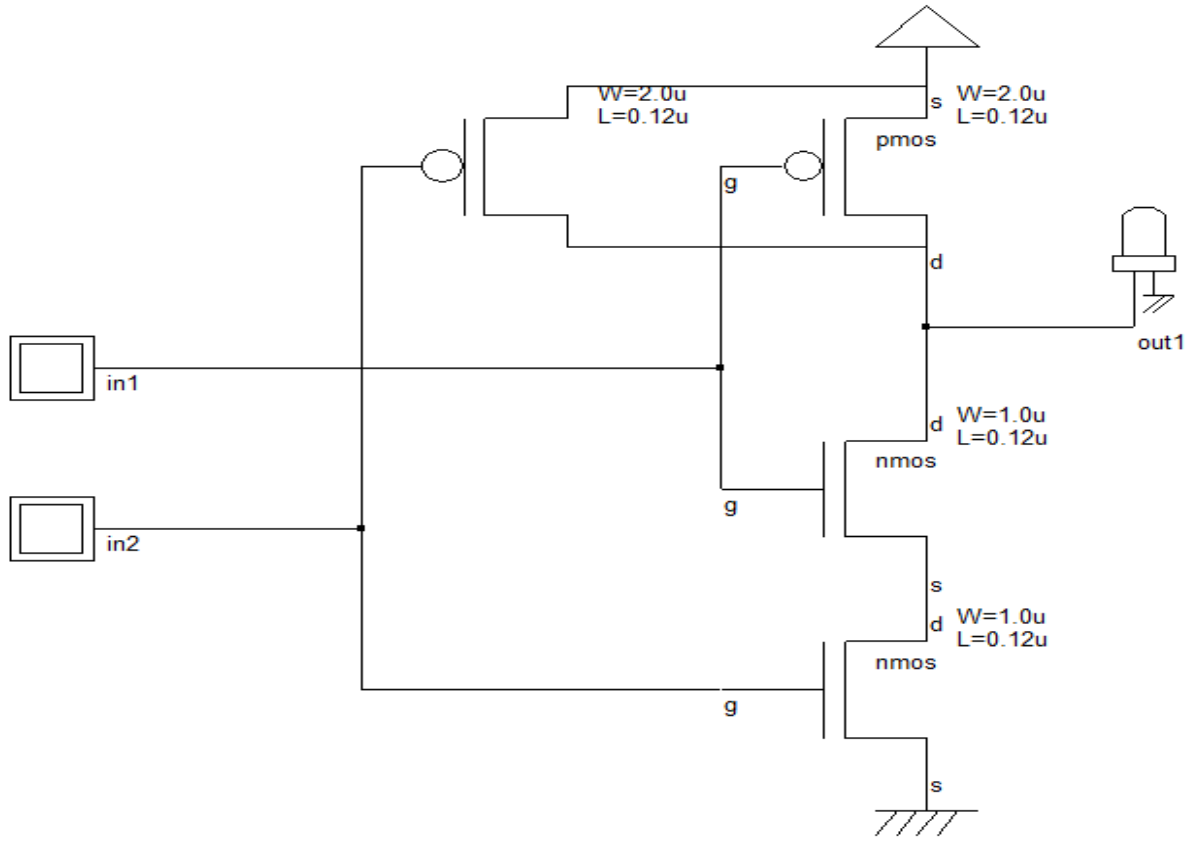
CMOS Inverter



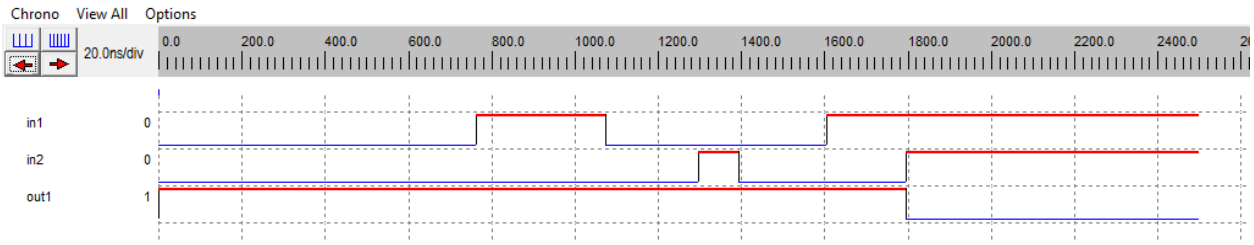
Simulation of CMOS Inverter:



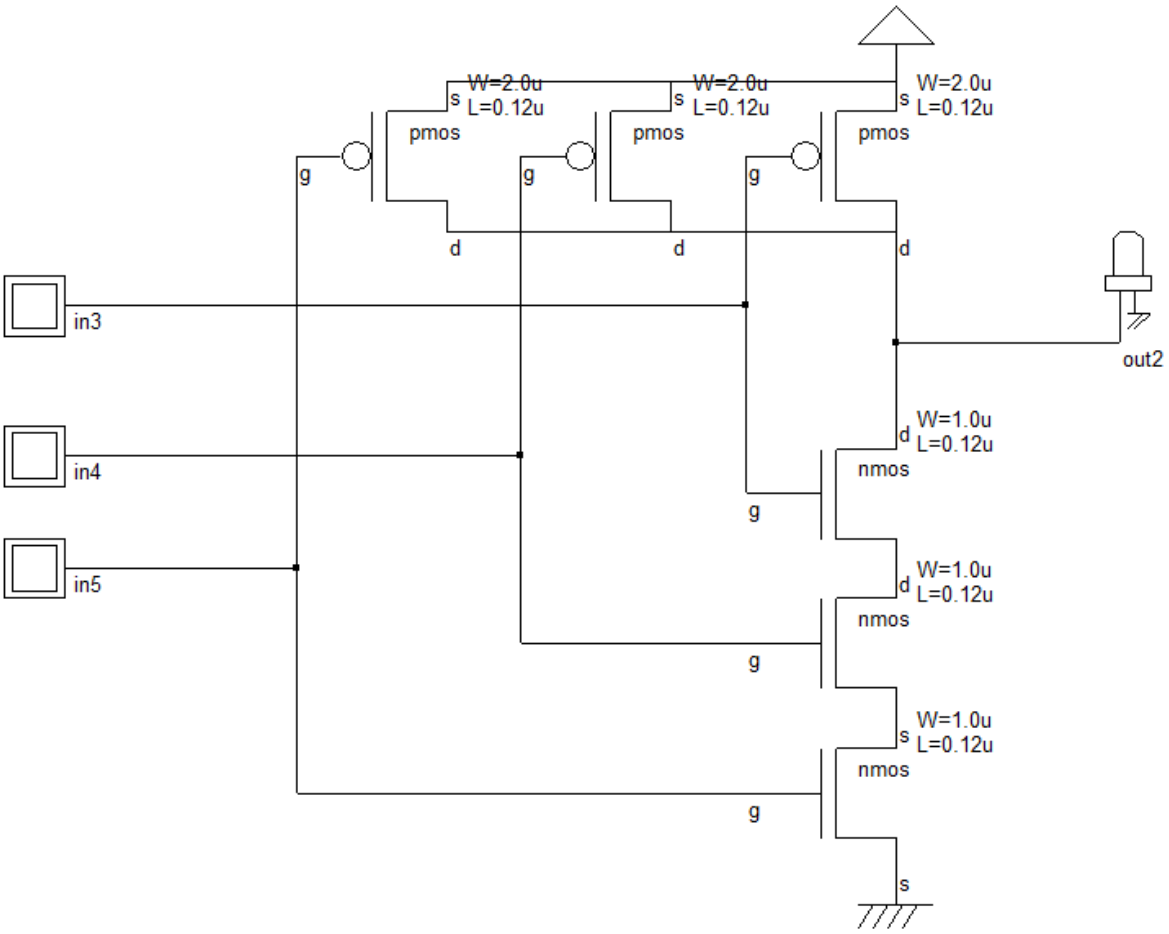
2 input CMOS NAND Gate:



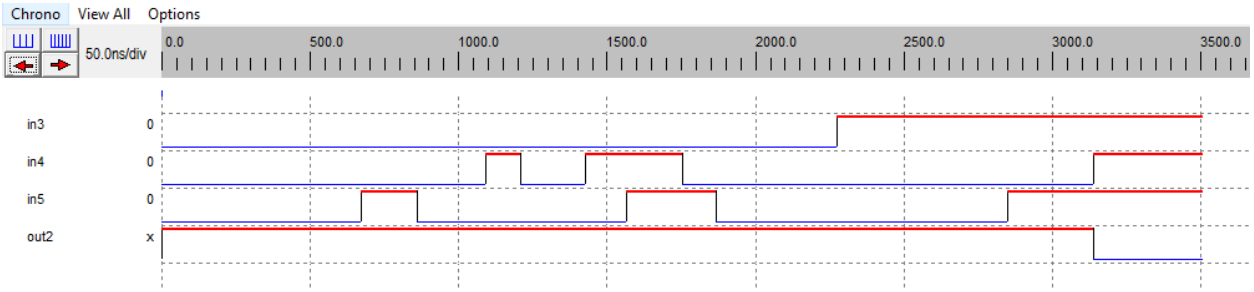
Simulation of 2 input CMOS NAND Gate:



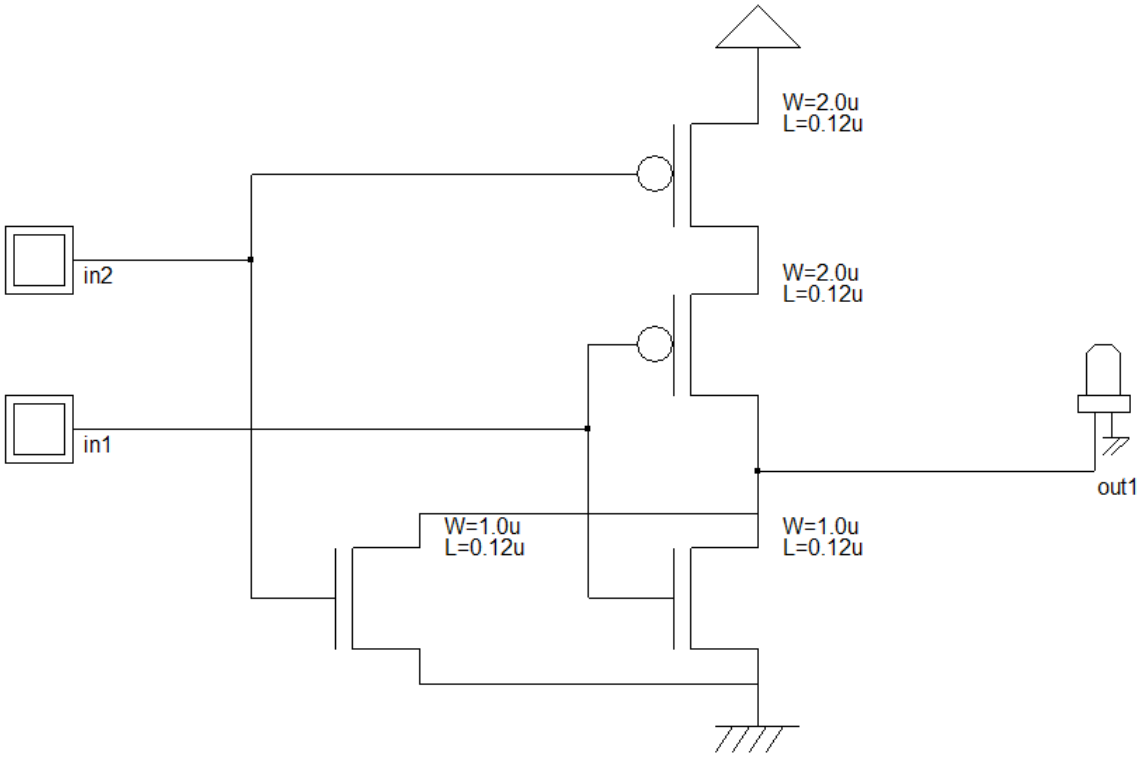
3 input CMOS NAND Gate:



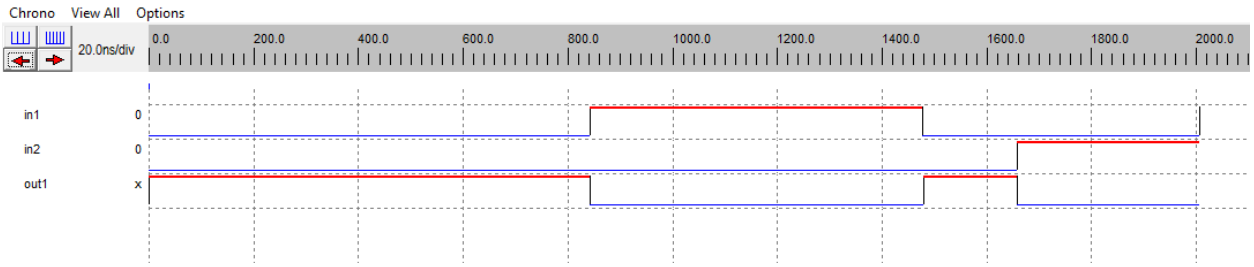
Simulation of 3 Input CMOS NAND Gate:



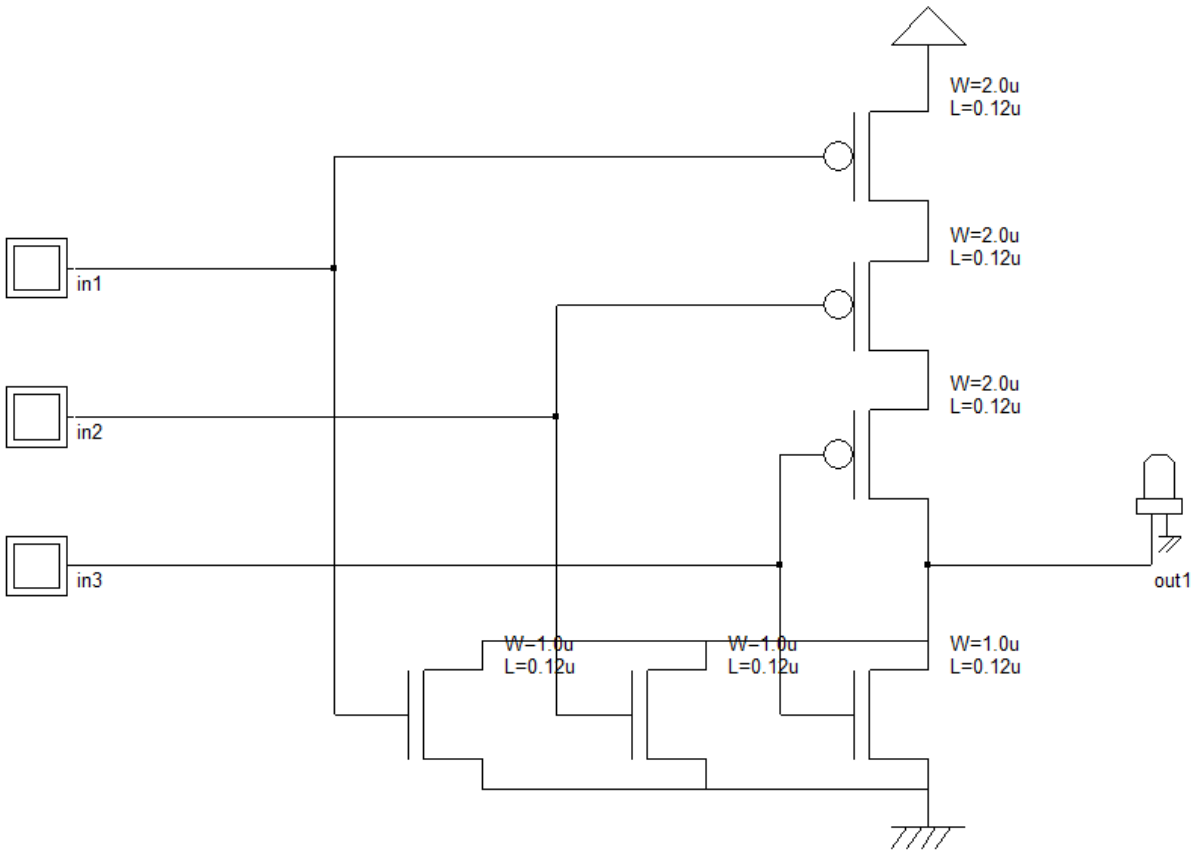
2 input CMOS NOR Gate:



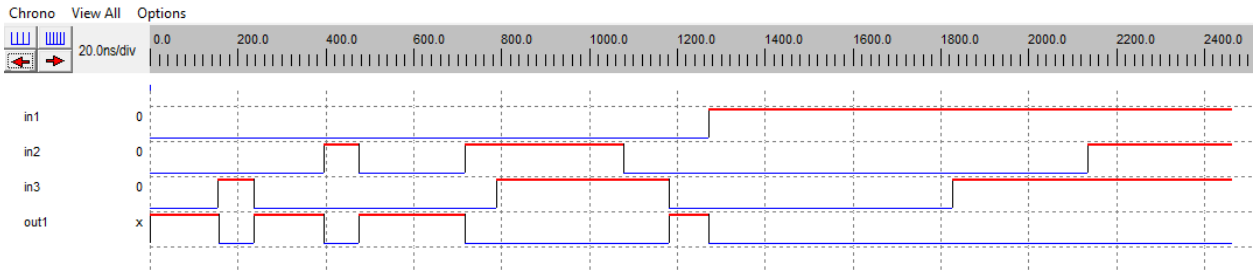
Simulation of 2 input CMOS NOR Gate



3 Input CMOS NOR Gate:



Simulation of 3 Input CMOS NOR Gate:



Discussion and Conclusion:

This lab experiment studies the circuit diagrams and simulations of a CMOS Inverter, 2 input CMOS NAND Gate, 3 input CMOS NAND Gate, 2 input CMOS NOR Gate and a 3 input CMOS NOR Gate along with their simulations using the software: DSCH2. The software enables the user to manipulate the input as he wishes and see the output in real time. This is one of the reasons for this software to be so preferred. The CMOS NAND gates have the pmos in the pull up configurations in parallel and the nmos in the pull down configurations in series. The CMOS NOR Gates however have the pmos in the pull up configuration in series and the nmos in the pull down configurations in parallel. The inverter is also a simple combination of the pmos and the nmos in the pull up and the pull down configurations respectively. The software DSCH2 used to complete these circuit schematics and simulations is very user friendly.