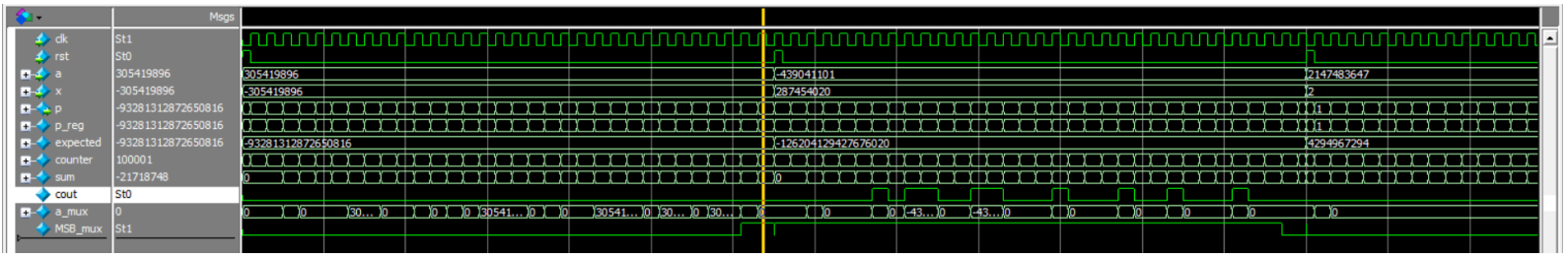
عبدالله عمر الازهري

Lab3

Question 1: Right shift multiplier

1- 32-bit

```
#   305419896 *  -305419896 =    -93281312872650816 (expected    -93281312872650816)
#  -439041101 *   287454020 =   -126204129427676020 (expected   -126204129427676020)
#  2147483647 *           2 =          4294967294 (expected          4294967294)
# -1073741824 *          -2 =          2147483648 (expected          2147483648)
#           0 * -1412567278 =                   0 (expected                   0)
# -2147483648 *          -1 =          2147483648 (expected          2147483648)
#  1985229328 *   305419896 =    606328534893909888 (expected    606328534893909888)
#           2 *           3 =                   6 (expected                   6)
#          -2 *          -3 =                   6 (expected                   6)
#           1 *  1985229328 =          1985229328 (expected          1985229328)
```



	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	73
2		
3	⌄ Combinational ALUT usage for logic	141
1	-- 7 input functions	0
2	-- 6 input functions	5
3	-- 5 input functions	4
4	-- 4 input functions	66
5	-- <=3 input functions	66
4		
5	Dedicated logic registers	70
6		
7	I/O pins	130
8	Total DSP Blocks	0
9	Maximum fan-out node	rst~input
10	Maximum fan-out	134
11	Total fan-out	976
12	Average fan-out	2.07

Multicorner Timing Analysis Summary

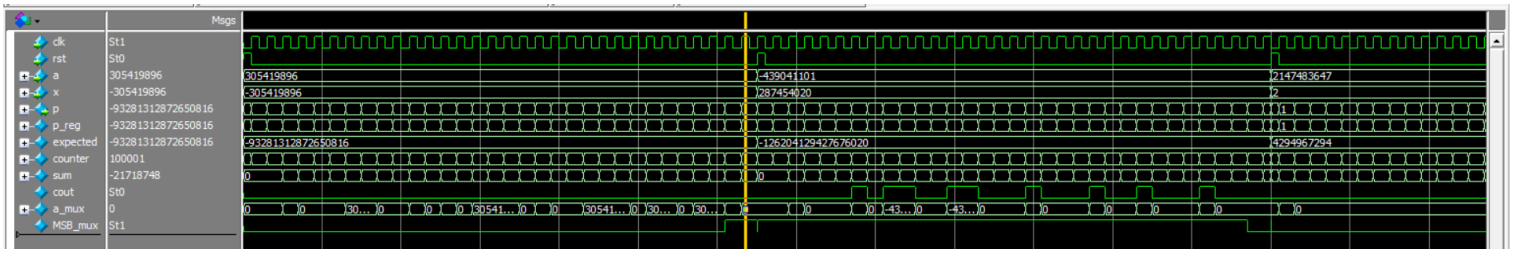
	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	⌄ Worst-case Slack	-3.667	-0.928	-0.371	-0.914	-0.394
1	clk	-3.667	-0.928	-0.371	-0.914	-0.394
2	rst	N/A	N/A	N/A	N/A	-0.105
2	⌄ Design-wide TNS	-191.975	-12.371	-16.755	-61.858	-40.431
1	clk	-191.975	-12.371	-16.755	-61.858	-40.431
2	rst	N/A	N/A	N/A	N/A	-3.803

Propagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	x[8]	p[8]	12.314			13.129
2	x[7]	p[7]	12.145			14.240
3	x[4]	p[4]	11.813			13.798
4	x[14]	p[14]	11.052			11.918
5	x[5]	p[5]	10.482			11.345
6	x[0]	p[0]	10.480			11.559
7	x[3]	p[3]	10.085			11.349
8	x[24]	p[24]	10.072			10.944
9	x[15]	p[15]	9.988			10.943
10	x[2]	p[2]	9.936			10.793
11	x[13]	p[13]	9.757			10.910
12	x[9]	p[9]	9.730			10.833
13	x[29]	p[29]	9.517			10.375
14	x[22]	p[22]	9.395			9.989
15	x[1]	p[1]	9.282			10.402
16	x[6]	p[6]	9.218			10.000
17	x[23]	p[23]	9.130			10.159
18	x[25]	p[25]	9.062			10.073
19	x[19]	p[19]	9.030			9.893
20	x[26]	p[26]	8.814			9.317
21	x[30]	p[30]	8.713			10.153
22	x[12]	p[12]	8.676			9.196
23	x[21]	p[21]	8.651			9.117
24	x[31]	p[31]	8.576			9.244
25	x[20]	p[20]	8.560			9.016
26	x[17]	p[17]	8.467			9.117
27	x[11]	p[11]	8.466			9.097

2- N-bit

```
#   305419896 *  -305419896 =    -93281312872650816 (expected    -93281312872650816)
#  -439041101 *   287454020 =   -126204129427676020 (expected   -126204129427676020)
#  2147483647 *           2 =           4294967294 (expected           4294967294)
# -1073741824 *          -2 =           2147483648 (expected           2147483648)
#           0 * -1412567278 =                    0 (expected                    0)
# -2147483648 *          -1 =           2147483648 (expected           2147483648)
#  1985229328 *   305419896 =    606328534893909888 (expected    606328534893909888)
#           2 *           3 =                    6 (expected                    6)
#          -2 *          -3 =                    6 (expected                    6)
#           1 *  1985229328 =           1985229328 (expected           1985229328)
```



Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	73
2		
3	⌄ Combinational ALUT usage for logic	141
1	-- 7 input functions	0
2	-- 6 input functions	5
3	-- 5 input functions	4
4	-- 4 input functions	66
5	-- <=3 input functions	66
4		
5	Dedicated logic registers	70
6		
7	I/O pins	130
8	Total DSP Blocks	0
9	Maximum fan-out node	rst~input
10	Maximum fan-out	134
11	Total fan-out	976
12	Average fan-out	2.07

Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-3.667	-0.928	-0.371	-0.914	-0.394
1	clk	-3.667	-0.928	-0.371	-0.914	-0.394
2	rst	N/A	N/A	N/A	N/A	-0.105
2	Design-wide TNS	-191.975	-12.371	-16.755	-61.858	-40.431
1	clk	-191.975	-12.371	-16.755	-61.858	-40.431
2	rst	N/A	N/A	N/A	N/A	-3.803

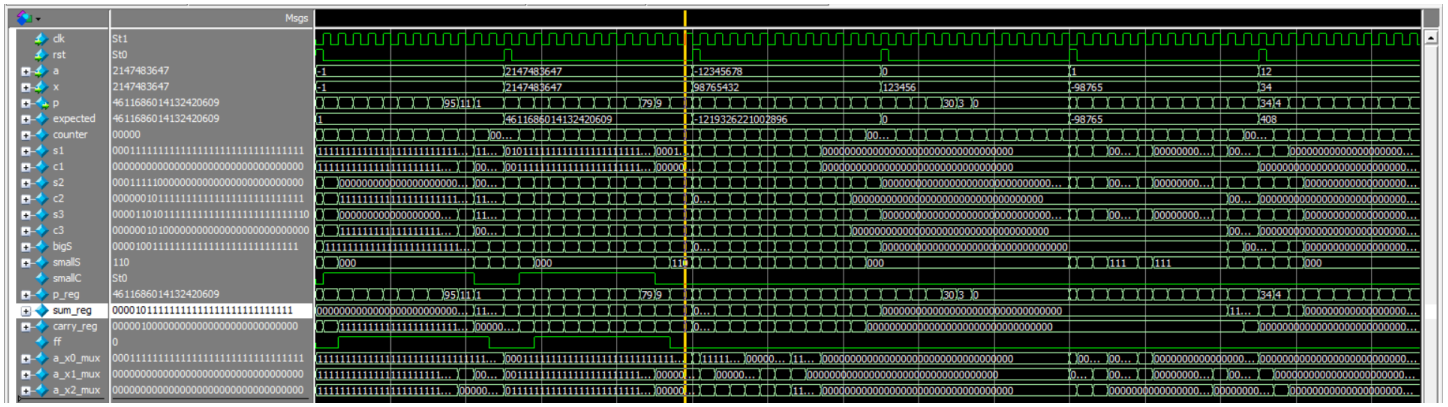
Propagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	x[8]	p[8]	12.314			13.129
2	x[7]	p[7]	12.145			14.240
3	x[4]	p[4]	11.813			13.798
4	x[14]	p[14]	11.052			11.918
5	x[5]	p[5]	10.482			11.345
6	x[0]	p[0]	10.480			11.559
7	x[3]	p[3]	10.085			11.349
8	x[24]	p[24]	10.072			10.944
9	x[15]	p[15]	9.988			10.943
10	x[2]	p[2]	9.936			10.793
11	x[13]	p[13]	9.757			10.910
12	x[9]	p[9]	9.730			10.833
13	x[29]	p[29]	9.517			10.375
14	x[22]	p[22]	9.395			9.989
15	x[1]	p[1]	9.282			10.402
16	x[6]	p[6]	9.218			10.000
17	x[23]	p[23]	9.130			10.159

Question 2: CSA radix-8 multiplier

1- 32-bit

```
#          -1 *          -1 =                    1 (expected                    1)
#  2147483647 *  2147483647 =    4611686014132420609 (expected    4611686014132420609)
#   -12345678 *    98765432 =      -1219326221002896 (expected      -1219326221002896)
#           0 *      123456 =                    0 (expected                    0)
#           1 *      -98765 =                -98765 (expected                -98765)
#          12 *          34 =                  408 (expected                  408)
# -2147483647 *           2 =           -4294967294 (expected           -4294967294)
#        1024 *        2048 =              2097152 (expected              2097152)
#          -3 *          -7 =                   21 (expected                   21)
#      987654 *      123456 =          121931812224 (expected          121931812224)
```



Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	218
2		
3	⌄ Combinational ALUT usage for logic	370
1	-- 7 input functions	0
2	-- 6 input functions	65
3	-- 5 input functions	58
4	-- 4 input functions	73
5	-- <=3 input functions	174
4		
5	Dedicated logic registers	134
6		
7	I/O pins	130
8	Total DSP Blocks	0
9	Maximum fan-out node	rst~input
10	Maximum fan-out	198
11	Total fan-out	2104
12	Average fan-out	2.75

Multicorner Timing Analysis Summary

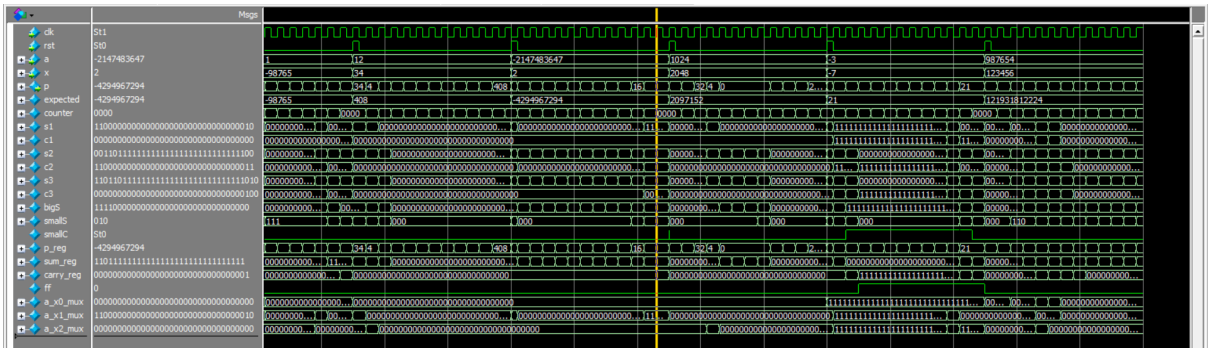
	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	⌄ Worst-case Slack	-4.241	-0.591	0.081	-0.303	-0.394
1	clk	-4.241	-0.591	0.081	-0.303	-0.394
2	rst	N/A	N/A	N/A	N/A	-0.031
2	⌄ Design-wide TNS	-380.923	-11.558	0.0	-38.091	-77.472
1	clk	-380.923	-11.558	0.000	-38.091	-77.472
2	rst	N/A	N/A	N/A	N/A	-0.082

Propagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	x[23]	p[23]	13.704			15.036
2	x[10]	p[10]	13.257			14.760
3	x[8]	p[8]	13.217			14.586
4	x[11]	p[11]	12.927			14.568
5	x[17]	p[17]	12.902			13.793
6	x[24]	p[24]	12.483			13.550
7	x[27]	p[27]	12.455			13.737
8	x[30]	p[30]	11.536			12.787
9	x[25]	p[25]	11.505			12.869
10	x[21]	p[21]	11.328			12.921
11	x[1]	p[1]	10.959			11.762
12	x[14]	p[14]	10.948			12.355
13	x[9]	p[9]	10.785			12.057
14	x[28]	p[28]	10.743			11.559

2- N-bit

```
#          -1 *          -1 =                    1 (expected                    1)
#  2147483647 *  2147483647 =    4611686014132420609 (expected    4611686014132420609)
#    -12345678 *    98765432 =   -1219326221002896 (expected   -1219326221002896)
#           0 *      123456 =                    0 (expected                    0)
#           1 *      -98765 =               -98765 (expected               -98765)
#          12 *          34 =                  408 (expected                  408)
# -2147483647 *           2 =           -4294967294 (expected           -4294967294)
#        1024 *        2048 =              2097152 (expected              2097152)
#          -3 *          -7 =                   21 (expected                   21)
#      987654 *      123456 =         121931812224 (expected         121931812224)
```



Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	218
2		
3	⌄ Combinational ALUT usage for logic	370
1	-- 7 input functions	0
2	-- 6 input functions	65
3	-- 5 input functions	58
4	-- 4 input functions	73
5	-- <=3 input functions	174
4		
5	Dedicated logic registers	134
6		
7	I/O pins	130
8	Total DSP Blocks	0
9	Maximum fan-out node	rst~input
10	Maximum fan-out	198
11	Total fan-out	2104
12	Average fan-out	2.75

Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	-4.241	-0.591	0.081	-0.303	-0.394
1	clk	-4.241	-0.591	0.081	-0.303	-0.394
2	rst	N/A	N/A	N/A	N/A	-0.031
2	Design-wide TNS	-380.923	-11.558	0.0	-38.091	-77.472
1	clk	-380.923	-11.558	0.000	-38.091	-77.472
2	rst	N/A	N/A	N/A	N/A	-0.082

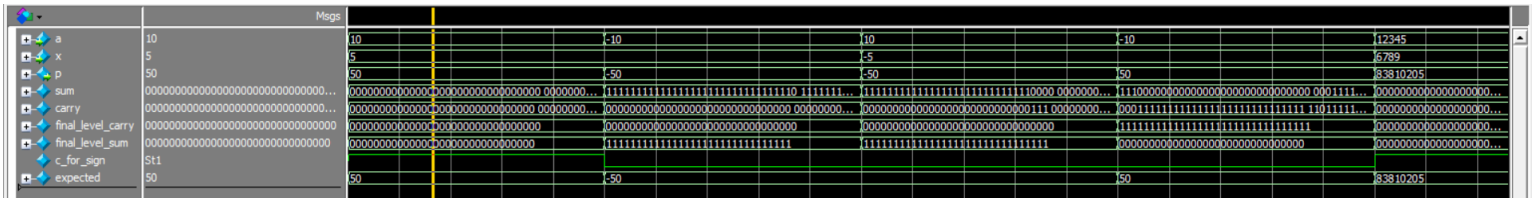
Propagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	x[23]	p[23]	13.704			15.036
2	x[10]	p[10]	13.257			14.760
3	x[8]	p[8]	13.217			14.586
4	x[11]	p[11]	12.927			14.568
5	x[17]	p[17]	12.902			13.793
6	x[24]	p[24]	12.483			13.550
7	x[27]	p[27]	12.455			13.737
8	x[30]	p[30]	11.536			12.787
9	x[25]	p[25]	11.505			12.869
10	x[21]	p[21]	11.328			12.921
11	x[1]	p[1]	10.959			11.762
12	x[14]	p[14]	10.948			12.355
13	x[9]	p[9]	10.785			12.057
14	x[28]	p[28]	10.743			11.550
15	x[2]	p[2]	10.637			11.613
16	x[16]	p[16]	10.632			11.723
17	x[20]	p[20]	10.492			11.413
18	x[13]	p[13]	10.491			11.717
19	x[22]	p[22]	9.896			10.612

Question 3: array multiplier

1- 32-bit

```
# Time = 0 | a =          10 | x =          5 | p =                50 | Expected =                50
# Time = 10000 | a =         -10 | x =          5 | p =               -50 | Expected =               -50
# Time = 20000 | a =          10 | x =         -5 | p =               -50 | Expected =               -50
# Time = 30000 | a =         -10 | x =         -5 | p =                50 | Expected =                50
# Time = 40000 | a =       12345 | x =       6789 | p =          83810205 | Expected =          83810205
# Time = 50000 | a =      -12345 | x =       6789 | p =         -83810205 | Expected =         -83810205
# Time = 60000 | a =           0 | x =       1234 | p =                 0 | Expected =                 0
# Time = 70000 | a =        5678 | x =          0 | p =                 0 | Expected =                 0
# Time = 80000 | a =  2147483647 | x =          2 | p =        4294967294 | Expected =        4294967294
# Time = 90000 | a = -2147483648 | x =         -1 | p =        2147483648 | Expected =        2147483648
```



Analysis & Synthesis Resource Usage Summary

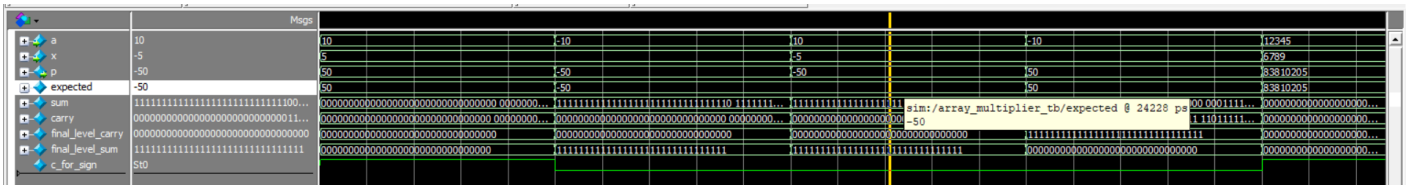
	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	1582
2		
3	Combinational ALUT usage for logic	2324
1	-- 7 input functions	0
2	-- 6 input functions	840
3	-- 5 input functions	24
4	-- 4 input functions	272
5	-- <=3 input functions	1188
4		
5	Dedicated logic registers	0
6		
7	I/O pins	128
8	Total DSP Blocks	0
9	Maximum fan-out node	x[2]~input
10	Maximum fan-out	67
11	Total fan-out	9319
12	Average fan-out	3.61

Propagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	a[21]	p[61]	51.623	53.527	52.817	54.721
2	x[3]	p[61]	51.243	53.147	52.741	54.645
3	a[11]	p[61]	50.351	52.255	51.456	53.360
4	a[15]	p[61]	50.302	52.206	50.659	52.563
5	x[2]	p[61]	49.974	51.878	50.643	52.547
6	a[23]	p[61]	49.956	51.860	50.854	52.758
7	x[0]	p[61]	49.831	51.735	50.851	52.755
8	a[21]	p[58]	49.748	51.228	50.942	52.422
9	x[1]	p[61]	49.696	51.600	50.432	52.336
10	a[12]	p[61]	49.626	51.530	50.639	52.543
11	a[25]	p[61]	49.615	51.519	50.400	52.304
12	a[21]	p[63]	49.609	48.247	50.803	49.441
13	x[4]	p[61]	49.585	51.489	50.551	52.455
14	a[22]	p[61]	49.536	51.440	49.985	51.889
15	a[21]	p[57]	49.507	49.739	50.701	50.933
16	a[24]	p[61]	49.481	51.385	50.155	52.059
17	a[20]	p[61]	49.392	51.296	50.325	52.229
18	a[28]	p[61]	49.377	51.281	50.302	52.206
19	x[3]	p[58]	49.368	50.848	50.866	52.346
20	a[21]	p[62]	49.267	49.524	50.461	50.718
21	x[3]	p[63]	49.229	47.867	50.727	49.365
22	a[21]	p[60]	49.163	49.858	50.357	51.052

2- N-bit

```
# Time = 0 | a =          10 | x =          5 | p =                50 | Expected =                50
# Time = 10000 | a =         -10 | x =          5 | p =               -50 | Expected =               -50
# Time = 20000 | a =          10 | x =         -5 | p =               -50 | Expected =               -50
# Time = 30000 | a =         -10 | x =         -5 | p =                50 | Expected =                50
# Time = 40000 | a =       12345 | x =       6789 | p =          83810205 | Expected =          83810205
# Time = 50000 | a =      -12345 | x =       6789 | p =         -83810205 | Expected =         -83810205
# Time = 60000 | a =           0 | x =       1234 | p =                 0 | Expected =                 0
# Time = 70000 | a =        5678 | x =          0 | p =                 0 | Expected =                 0
# Time = 80000 | a =  2147483647 | x =          2 | p =        4294967294 | Expected =        4294967294
# Time = 90000 | a = -2147483648 | x =         -1 | p =        2147483648 | Expected =        2147483648
```



Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	1582
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3	⌄ Combinational ALUT usage for logic	2324
1	-- 7 input functions	0
2	-- 6 input functions	840
3	-- 5 input functions	24
4	-- 4 input functions	272
5	-- <=3 input functions	1188
4		
5	Dedicated logic registers	0
6		
7	I/O pins	128
8	Total DSP Blocks	0
9	Maximum fan-out node	x[2]~input
10	Maximum fan-out	67
11	Total fan-out	9319
12	Average fan-out	3.61

Propagation Delay						
	Input Port	Output Port	RR	RF	FR	FF
1	a[21]	p[61]	51.623	53.527	52.817	54.721
2	x[3]	p[61]	51.243	53.147	52.741	54.645
3	a[11]	p[61]	50.351	52.255	51.456	53.360
4	a[15]	p[61]	50.302	52.206	50.659	52.563
5	x[2]	p[61]	49.974	51.878	50.643	52.547
6	a[23]	p[61]	49.956	51.860	50.854	52.758
7	x[0]	p[61]	49.831	51.735	50.851	52.755
8	a[21]	p[58]	49.748	51.228	50.942	52.422
9	x[1]	p[61]	49.696	51.600	50.432	52.336
10	a[12]	p[61]	49.626	51.530	50.639	52.543
11	a[25]	p[61]	49.615	51.519	50.400	52.304
12	a[21]	p[63]	49.609	48.247	50.803	49.441
13	x[4]	p[61]	49.585	51.489	50.551	52.455
14	a[22]	p[61]	49.536	51.440	49.985	51.889
15	a[21]	p[57]	49.507	49.739	50.701	50.933
16	a[24]	p[61]	49.481	51.385	50.155	52.059
17	a[20]	p[61]	49.392	51.296	50.325	52.229
18	a[28]	p[61]	49.377	51.281	50.302	52.206
19	x[3]	p[58]	49.368	50.848	50.866	52.346
20	a[21]	p[62]	49.267	49.524	50.461	50.718
21	x[3]	p[63]	49.229	47.867	50.727	49.365
22	a[21]	p[60]	49.163	49.858	50.357	51.052
23	a[26]	p[61]	49.150	51.054	49.803	51.707

Thank you