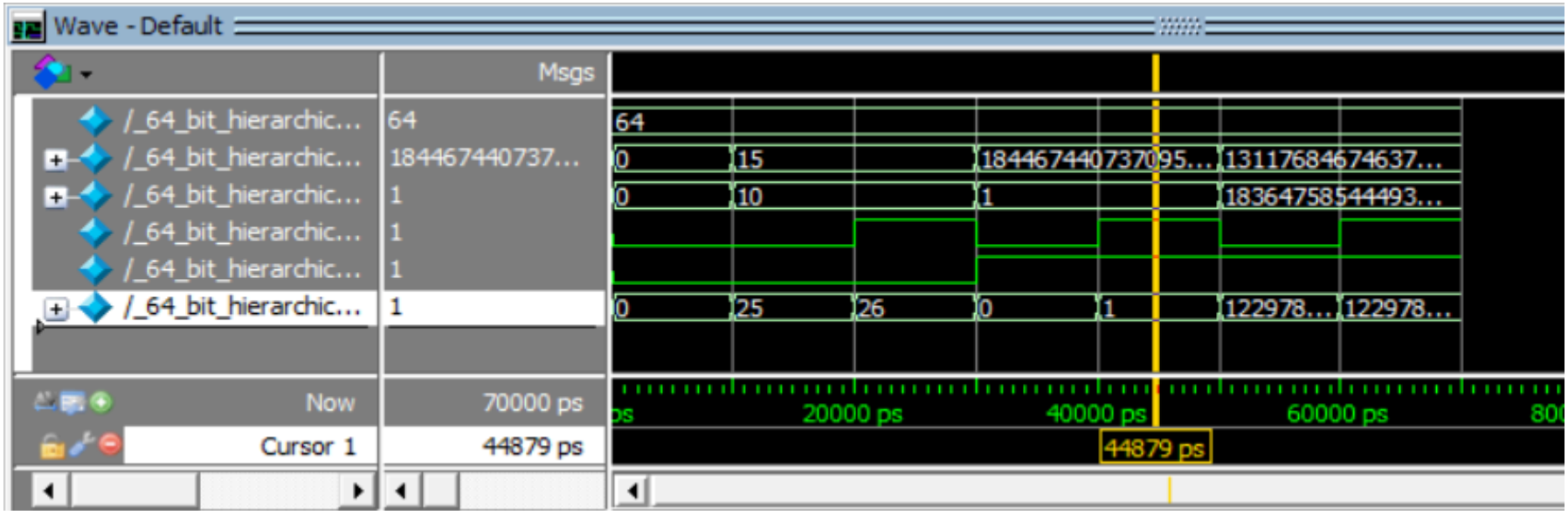
1- 64-bit CLA:

Output and wave simulation

```
# At time                 0, a =                  0, b =                  0, cin = 0, sum =                  0, cout = 0, {cout,sum} =                  0
# At time             10000, a =                 15, b =                 10, cin = 0, sum =                 25, cout = 0, {cout,sum} =                 25
# At time             20000, a =                 15, b =                 10, cin = 1, sum =                 26, cout = 0, {cout,sum} =                 26
# At time             30000, a = 18446744073709551615, b =                  1, cin = 0, sum =                  0, cout = 1, {cout,sum} = 18446744073709551616
# At time             40000, a = 18446744073709551615, b =                  1, cin = 1, sum =                  1, cout = 1, {cout,sum} = 18446744073709551617
# At time             50000, a =  1311768467463790320, b = 18364758544493064720, cin = 0, sum =  1229782938247303424, cout = 1, {cout,sum} = 19676527011956855040
# At time             60000, a =  1311768467463790320, b = 18364758544493064720, cin = 1, sum =  1229782938247303425, cout = 1, {cout,sum} = 19676527011956855041
# Break in Module _64_bit_hierarchical_Carry_look_ahead_adder_tb at C:/altera/13.1/modelsim_ase/examples/projects/p1/64-bit hierarchical Carry look ahead adder.v line 60
```



FPGA Utilization

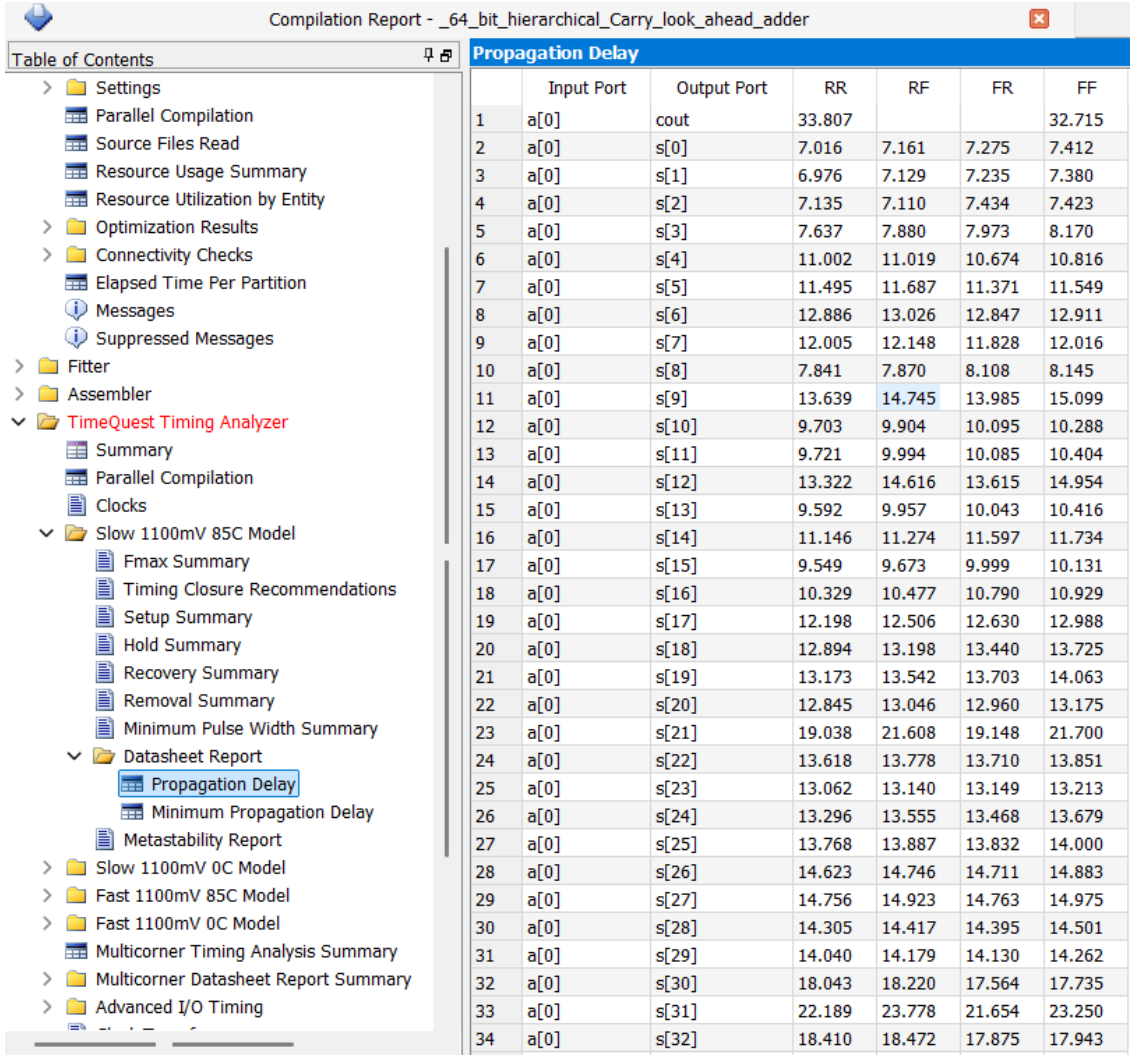
ALM contains two 4-input LUTs

ALUT can be 4,5,6 or 7-input LUT (flexible)

Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	102
2		
3	Combinational ALUT usage for logic	166
1	-- 7 input functions	0
2	-- 6 input functions	38
3	-- 5 input functions	31
4	-- 4 input functions	19
5	-- <=3 input functions	78
4		
5	Dedicated logic registers	0
6		
7	I/O pins	194
8	Total DSP Blocks	0
9	Maximum fan-out node	_64_bit_carry_look_ahead:cla|four_bit_carry_look_ahead:cla5|c[3]~1
10	Maximum fan-out	6
11	Total fan-out	920
12	Average fan-out	1.66

worst case delay is 33.807 ns



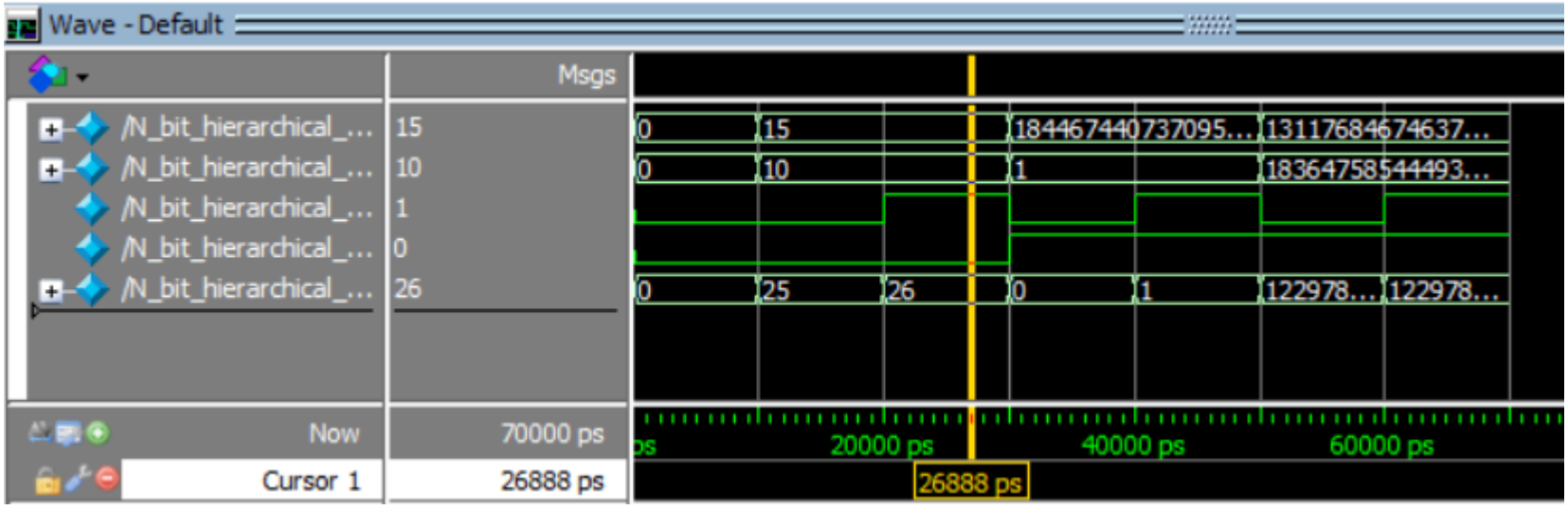
Propagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	a[0]	cout	33.807			32.715
2	a[0]	s[0]	7.016	7.161	7.275	7.412
3	a[0]	s[1]	6.976	7.129	7.235	7.380
4	a[0]	s[2]	7.135	7.110	7.434	7.423
5	a[0]	s[3]	7.637	7.880	7.973	8.170
6	a[0]	s[4]	11.002	11.019	10.674	10.816
7	a[0]	s[5]	11.495	11.687	11.371	11.549
8	a[0]	s[6]	12.886	13.026	12.847	12.911
9	a[0]	s[7]	12.005	12.148	11.828	12.016
10	a[0]	s[8]	7.841	7.870	8.108	8.145
11	a[0]	s[9]	13.639	14.745	13.985	15.099
12	a[0]	s[10]	9.703	9.904	10.095	10.288
13	a[0]	s[11]	9.721	9.994	10.085	10.404
14	a[0]	s[12]	13.322	14.616	13.615	14.954
15	a[0]	s[13]	9.592	9.957	10.043	10.416
16	a[0]	s[14]	11.146	11.274	11.597	11.734
17	a[0]	s[15]	9.549	9.673	9.999	10.131
18	a[0]	s[16]	10.329	10.477	10.790	10.929
19	a[0]	s[17]	12.198	12.506	12.630	12.988
20	a[0]	s[18]	12.894	13.198	13.440	13.725
21	a[0]	s[19]	13.173	13.542	13.703	14.063
22	a[0]	s[20]	12.845	13.046	12.960	13.175
23	a[0]	s[21]	19.038	21.608	19.148	21.700
24	a[0]	s[22]	13.618	13.778	13.710	13.851
25	a[0]	s[23]	13.062	13.140	13.149	13.213
26	a[0]	s[24]	13.296	13.555	13.468	13.679
27	a[0]	s[25]	13.768	13.887	13.832	14.000
28	a[0]	s[26]	14.623	14.746	14.711	14.883
29	a[0]	s[27]	14.756	14.923	14.763	14.975
30	a[0]	s[28]	14.305	14.417	14.395	14.501
31	a[0]	s[29]	14.040	14.179	14.130	14.262
32	a[0]	s[30]	18.043	18.220	17.564	17.735
33	a[0]	s[31]	22.189	23.778	21.654	23.250
34	a[0]	s[32]	18.410	18.472	17.875	17.943

2- N-bit CLA:

Output and wave simulation

```
# At time                 0, a =                 0, b =                 0, cin = 0, sum =                 0, cout = 0, {cout,sum} =                 0
# At time             10000, a =                15, b =                10, cin = 0, sum =                25, cout = 0, {cout,sum} =                25
# At time             20000, a =                15, b =                10, cin = 1, sum =                26, cout = 0, {cout,sum} =                26
# At time             30000, a = 18446744073709551615, b =                 1, cin = 0, sum =                 0, cout = 1, {cout,sum} = 18446744073709551616
# At time             40000, a = 18446744073709551615, b =                 1, cin = 1, sum =                 1, cout = 1, {cout,sum} = 18446744073709551617
# At time             50000, a =  1311768467463790320, b = 18364758544493064720, cin = 0, sum =  1229782938247303424, cout = 1, {cout,sum} = 19676527011956855040
# At time             60000, a =  1311768467463790320, b = 18364758544493064720, cin = 1, sum =  1229782938247303425, cout = 1, {cout,sum} = 19676527011956855041
# Break in Module N_bit_hierarchical_carry_look_ahead_adder_tb at C:/altera/13.1/modelsim_ase/examples/projects/p2/N-bit hierarchical carry look ahead adder.v line 61
```

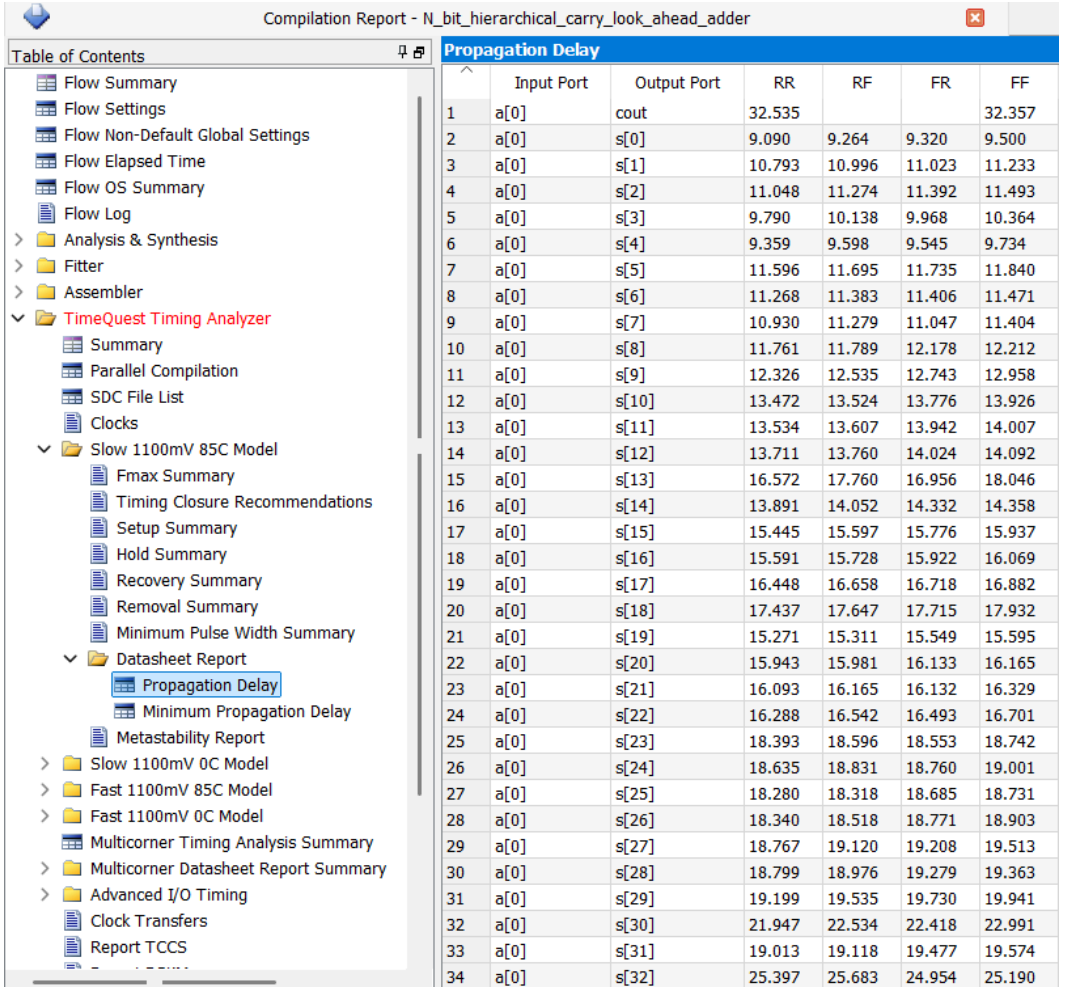


FPGA Utilization and Delay

Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	82
2		
3	Combinational ALUT usage for logic	129
1	-- 7 input functions	0
2	-- 6 input functions	35
3	-- 5 input functions	14
4	-- 4 input functions	14
5	-- <=3 input functions	66
4		
5	Dedicated logic registers	0
6		
7	I/O pins	194
8	Total DSP Blocks	0
9	Maximum fan-out node	N_bit_carry_look_ahead:cla|c[2]
10	Maximum fan-out	4
11	Total fan-out	762
12	Average fan-out	1.47

worst case delay is 32.535 ns



Propagation Delay

	Input Port	Output Port	RR	RF	FR	FF
1	a[0]	cout	32.535			32.357
2	a[0]	s[0]	9.090	9.264	9.320	9.500
3	a[0]	s[1]	10.793	10.996	11.023	11.233
4	a[0]	s[2]	11.048	11.274	11.392	11.493
5	a[0]	s[3]	9.790	10.138	9.968	10.364
6	a[0]	s[4]	9.359	9.598	9.545	9.734
7	a[0]	s[5]	11.596	11.695	11.735	11.840
8	a[0]	s[6]	11.268	11.383	11.406	11.471
9	a[0]	s[7]	10.930	11.279	11.047	11.404
10	a[0]	s[8]	11.761	11.789	12.178	12.212
11	a[0]	s[9]	12.326	12.535	12.743	12.958
12	a[0]	s[10]	13.472	13.524	13.776	13.926
13	a[0]	s[11]	13.534	13.607	13.942	14.007
14	a[0]	s[12]	13.711	13.760	14.024	14.092
15	a[0]	s[13]	16.572	17.760	16.956	18.046
16	a[0]	s[14]	13.891	14.052	14.332	14.358
17	a[0]	s[15]	15.445	15.597	15.776	15.937
18	a[0]	s[16]	15.591	15.728	15.922	16.069
19	a[0]	s[17]	16.448	16.658	16.718	16.882
20	a[0]	s[18]	17.437	17.647	17.715	17.932
21	a[0]	s[19]	15.271	15.311	15.549	15.595
22	a[0]	s[20]	15.943	15.981	16.133	16.165
23	a[0]	s[21]	16.093	16.165	16.132	16.329
24	a[0]	s[22]	16.288	16.542	16.493	16.701
25	a[0]	s[23]	18.393	18.596	18.553	18.742
26	a[0]	s[24]	18.635	18.831	18.760	19.001
27	a[0]	s[25]	18.280	18.318	18.685	18.731
28	a[0]	s[26]	18.340	18.518	18.771	18.903
29	a[0]	s[27]	18.767	19.120	19.208	19.513
30	a[0]	s[28]	18.799	18.976	19.279	19.363
31	a[0]	s[29]	19.199	19.535	19.730	19.941
32	a[0]	s[30]	21.947	22.534	22.418	22.991
33	a[0]	s[31]	19.013	19.118	19.477	19.574
34	a[0]	s[32]	25.397	25.683	24.954	25.190