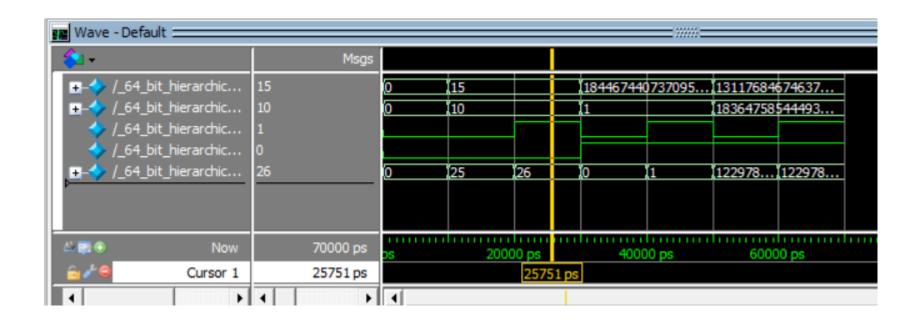
1- 64-bit Ling adder:

Output and wave simulation

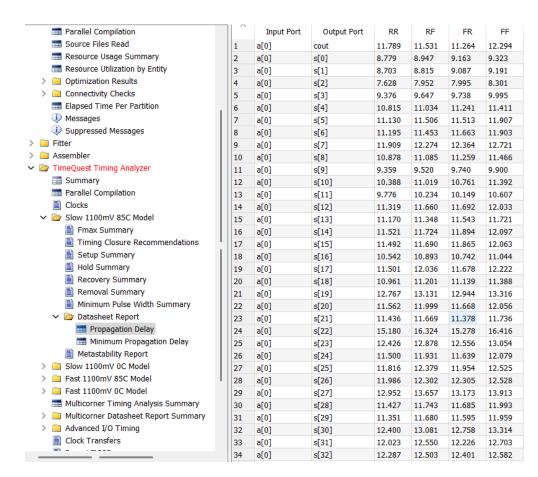
```
# At time
                           0, a =
                                                   0, b =
                                                                            0, cin = 0, sum =
                                                                                                                 0, cout = 0, {cout, sum} =
                                                                             10, cin = 0, sum =
# At time
                       10000, a =
                                                                                                                 25, cout = 0, {cout, sum} =
                                                                             10, cin = 1, sum =
# At time
                       20000, a =
                                                   15, b =
                                                                                                                 26, cout = 0, {cout, sum} =
# At time
                       30000, a = 18446744073709551615, b =
                                                                             1, cin = 0, sum =
                                                                                                                 0, cout = 1, {cout, sum} = 18446744073709551616
# At time
                       40000, a = 18446744073709551615, b =
                                                                              1, cin = 1, sum =
                                                                                                                  1, cout = 1, {cout, sum} = 18446744073709551617
# At time
                       50000, a = 1311768467463790320, b = 18364758544493064720, cin = 0, sum = 1229782938247303424, cout = 1, {cout, sum} = 19676527011956855040
                        60000, a = 1311768467463790320, b = 18364758544493064720, cin = 1, sum = 1229782938247303425, cout = 1, {cout, sum} = 19676527011956855041
```



FPGA Utilization and Delay

	Resource	Usage
1	Estimate of Logic utilization (ALMs needed)	119
2		
3		197
1	7 input functions	0
2	6 input functions	41
3	5 input functions	64
4	4 input functions	42
5	<=3 input functions	50
4		
5	Dedicated logic registers	0
6		
7	I/O pins	194
8	Total DSP Blocks	0
9	Maximum fan-out node	_64_bit_Ling_CLA:lcla _16_bit_Ling_CLA:lcla1 four_bit_Ling_CLA:lcla5 G~5
10	Maximum fan-out	11
11	Total fan-out	1113
12	Average fan-out	1.90

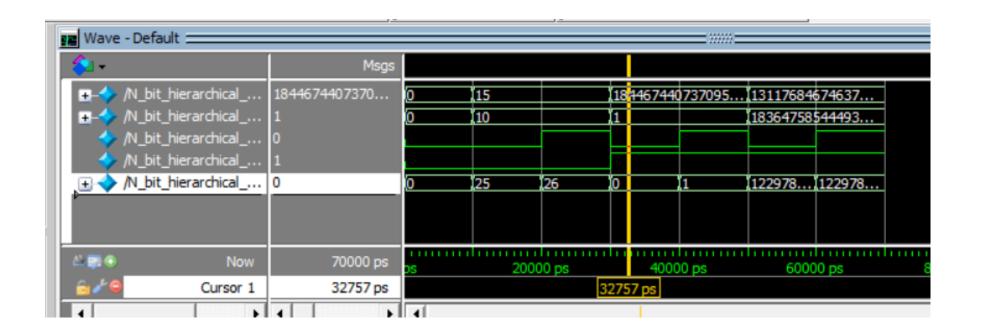
critical path delay is 11.789



1- N-bit Ling adder:

Output and wave simulation

```
# At time
                            0, a =
                                                                                0, cin = 0, sum =
                                                                                                                     0, cout = 0, {cout, sum} =
# At time
                        10000, a =
                                                     15, b =
                                                                               10, cin = 0, sum =
                                                                                                                                                                  25
                                                                                                                    25, cout = 0, {cout, sum} =
# At time
                        200000, a =
                                                                               10, cin = 1, sum =
                                                                                                                    26, cout = 0, {cout, sum} =
# At time
                        30000, a = 18446744073709551615, b =
                                                                               1, cin = 0, sum =
                                                                                                                     0, cout = 1, {cout, sum} = 18446744073709551616
# At time
                        40000, a = 18446744073709551615, b =
                                                                                1, cin = 1, sum =
# At time
                        50000, a = 1311768467463790320, b = 18364758544493064720, cin = 0, sum = 1229782938247303424, cout = 1, {cout,sum} = 19676527011956855040
# At time
                        60000, a = 1311768467463790320, b = 18364758544493064720, cin = 1, sum = 1229782938247303425, cout = 1, {cout,sum} = 19676527011956855041
```



FPGA Utilization and Delay

Ana	lysis & Synthesis Resource Usage Summary		
	Resource	Usage	
1	Estimate of Logic utilization (ALMs needed)	84	
2			
3	 Combinational ALUT usage for logic 	133	
1	7 input functions	0	
2	6 input functions	34	
3	5 input functions	23	
4	4 input functions	6	
5	<=3 input functions	70	
4			
5	Dedicated logic registers	0	
6			
7	I/O pins	194	
8	Total DSP Blocks	0	
9	Maximum fan-out node	N_bit_SUMgenerator:sg s[2]~0	
10	Maximum fan-out	4	
11	Total fan-out	778	
12	Average fan-out	1.49	

critical path delay is 37.125 مش عارف لي ضرب كده

Table of Contents 무 중			Propagation Delay						
Flow Summary		^	Input Port	Output Port	RR	RF	FR	FF	
		1	a[0]	cout	37.125			37.577	
		2	a[0]	s[0]	12.870	14.032	13.105	14.273	
➡ Flow Elapsed Time		3	a[0]	s[1]	10.471	10.597	10.706	10.839	
		4	a[0]	s[2]	10.898	11.036	11.079	11.263	
Flow Log		5	a[0]	s[3]	11.326	11.478	11.537	11.681	
🖊 🗁 Analysis & Synthesis		6	a[0]	s[4]	11.633	11.775	11.780	11.968	
		7	a[0]	s[5]	11.883	12.171	12.205	12.368	
> 🦲 Settings		8	a[0]	s[6]	11.483	11.615	11.647	11.729	
== Parallel Compilation		9	a[0]	s[7]	14.520	14.660	14.080	14.228	
source Files Read		10	a[0]	s[8]	15.229	15.370	14.745	14.892	
Resource Usage Summary		11	a[0]	s[9]	15.639	15.903	15.155	15.425	
Resource Utilization by Entity	111	12	a[0]	s[10]	16.120	16.391	15.628	15.913	
Optimization Results		13	a[0]	s[11]	14.194	14.222	13.712	13.748	
Parameter Settings by Entity Instance		14	a[0]	s[12]	16.176	16.455	15.733	15.967	
Elapsed Time Per Partition		15	a[0]	s[13]	15.292	15.521	14.776	15.01	
Messages		16	a[0]	s[14]	15.083	15.244	14.558	14.768	
Fitter		17	a[0]	s[15]	15.935	16.253	15.421	15.690	
Assembler		18	a[0]	s[16]	17.732	17.929	17.051	17.373	
🖒 🚞 TimeQuest Timing Analyzer		19	a[0]	s[17]	17.344	17.434	16.470	16.568	
		20	a[0]	s[18]	18.443	18.690	17.525	17.778	
=== Parallel Compilation		21	a[0]	s[19]	18.207	18.332	17.289	17.42	
Clocks		22	a[0]	s[20]	18.276	18.485	17.417	17.577	
✓ Image: Slow 1100mV 85C Model	. 1	23	a[0]	s[21]	18.445	18.588	17.574	17.711	
Fmax Summary		24	a[0]	s[22]	22.354	23.318	21.495	22.414	
Timing Closure Recommendations		25	a[0]	s[23]	19.344	19.637	18.408	18.747	
Setup Summary		26	a[0]	s[24]	18.646	18.754	17.746	17.840	
Hold Summary		27	a[0]	s[25]	27.902	29.710	27.812	29.755	
Recovery Summary		28	a[0]	s[26]	24.503	24.644	24.473	24.712	
Removal Summary		29	a[0]	s[27]	23.880	24.022	24.006	24.172	
Minimum Pulse Width Summary		30	a[0]	s[28]	23.721	24.215	23.833	24.318	
✓ Image: Value of the point of the poin		31	a[0]	s[29]	24.732	24.885	24.844	24.987	
Propagation Delay		32	a[0]	s[30]	24.988	25.116	25.166	25.284	
Minimum Propagation Delay		33	a[0]	s[31]	24.996	25.217	25.175	25.386	
		34	a[0]	s[32]	26.823	27.036	26.961	27.167	